

A Sub-10 mV Power Converter With Fully Integrated Self-Start, MPPT, and ZCS Control for Thermoelectric Energy Harvesting

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Abstract—An inductive power converter for thermoelectric generator (TEG) is presented in this paper. A novel redundant inverter ring oscillator is proposed to self-oscillate in a very low supply voltage down to 45 mV. An additional self-start assist circuit with a differential clock booster and an exponential charge pump is implemented in the power converter to achieve lower self-start voltage. Boundary continuous-conduction mode, zero current switch (ZCS), and maximum power point tracking (MPPT) features have been incorporated into the power converter. Selective turn-ON dynamical-comparators have been used in ZCS and MPPT circuits to save power and achieve minimum operating supply voltage. Fabricated in 65-nm CMOS process, the chip can self-start at 210 mV. After self-start, only 7-mV input voltage is needed to sustain the power converter operation. With a TEG open circuit voltage of 80 mV and internal resistance of 5 Ω, the chip can provide a maximum output power of 229 μW with end-to-end efficiency of 71.5%.

Index Terms—Charge pump, clock booster, energy harvesting, IoT, MPPT, redundant inverter, self-start, TEG, ZCS.

I. INTRODUCTION

INTERNET of things (IoT) has been perceived by semiconductor industry as the next potential growth area after the cellphone. However, its pervasive and widespread usage pose stringent requirement on the form factor of the resulting electronics and their power consumption. Although low power electronics can prolong the battery life, self-powered design through energy harvesting is still desirable as it eliminates the need of battery replacement or recharging.

For energy harvesting, many different sources have been investigated [1], [2], including RF, piezo, tribo and thermoelectric generator (TEG). Wireless energy harvesting requires

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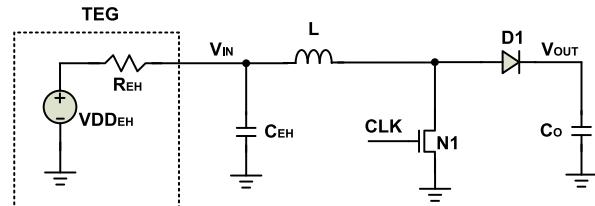


Fig. 1. Booster converter for TEG.

strong RF sources and antenna nearby. Piezoelectric or triboelectric needs constant mechanical movements and the resulting high output voltage may cause reliability issue for the subsequent circuits. Solar cell depends on the direct access of light source, which might not always be available. TEG operates based on temperature difference, which can be too small to produce significant output voltage to kick-start the circuit.

In this paper, we propose a power converter targeted at TEG source. As the TEG source is envisioned to rely on body-to-surrounding temperature difference to power the subsequent circuit, small temperature difference is expected. Hence, the proposed TEG should be able to self-start and continue its energy harvesting at low TEG output voltage. A self-start assist circuit is added to the conventional self-start structure to achieve our objectives. The power converter also includes maximum power point tracking (MPPT) feature to extract the maximum power from the TEG, providing a regulated output voltage to the subsequent electronics.

The rest of this paper is structured as follows: Section II examines the existing reported solutions for the self-start, MPPT and efficiency improvement; Section III elaborates the proposed power converter for TEG; Section IV describes silicon measurement result and the analysis; the last Section gives the conclusion.

II. PRIOR ARTS

A. Self-Start

Boost converter is a commonly used technique to boost the low TEG output voltage, as shown in Fig. 1. However, the CLK signal in Fig. 1 still needs to be sufficiently large to kick-start the converter, which is usually not available during the initial start-up stage. In [3], an external battery is used to kick start the converter by charging up the output capacitor (Co), which subsequently enables the ring oscillator powered by

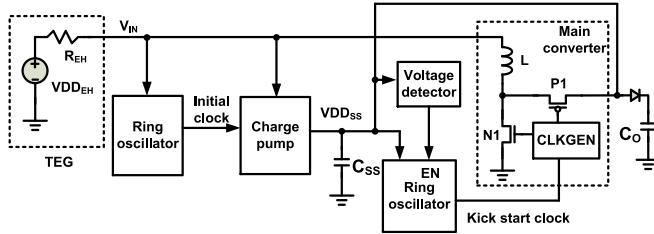


Fig. 2. Conventional self-start for TEG booster converter.

C_O to generate CLK with sufficiently large voltage swing to turn on/off the booster NFET (N1). In [4], mechanical energy is employed to kick start the booster circuit. Nevertheless, the need of alternative energy sources makes the solution less attractive.

In [5] and [6], external transformer and off-chip inductor are used to enable self-start with TEG output voltage as small as 40 mV. However, the bulkiness of these components limits the achievable form factor.

Ring oscillator coupled with charge pump circuit has gained its popularity as a potential candidate for low self-start voltage [7]–[11]. The principle is to use low voltage ring oscillator and charge pump circuits to charge a capacitor to higher voltage, which will power up another ring oscillator with larger output voltage to eventually kick start the main power converter, as shown in Fig. 2. The various reported works differ in the proposed ring oscillator and the arrangement of charge pump, with self-start voltage ranging from 70 mV to 330 mV.

B. MPPT

For all energy harvester sources, it is critical to have the power converter presenting matched impedance to the source to extract the maximum power. This will eliminate the possibility of using over-designed energy source, which can incur cost and area penalty. In this situation, power converter with built-in MPPT would be more desirable.

In [12], the MPPT functions by fixing the converter clock period while adjusting the clock pulse width to change the switch-on time of the converter NFET transistor. Zero current switch (ZCS) circuit is used to detect the PFET transistor zero current point and also to measure the total PFET transistor switch on time during each clock cycle. This provides a way to measure the extracted power. By varying the converter NFET clock pulse width to get the optimal PFET switch on time, the maximum power point can be attained. It is shown in [13] that the maximum power point is reached if the ratio of the converter input voltage to the open circuit voltage of TEG source is 0.5. The converter clock frequency is adjusted to vary the power converter impedance. However, careful selection of the output capacitance is needed to balance between short open circuit time and small output voltage fluctuation. Various MPPT circuits are also introduced in [14]–[16].

C. Efficiency Improvement

Efficiency is also important for power converter. In [17], a controller is proposed to adjust the charge pump stage.

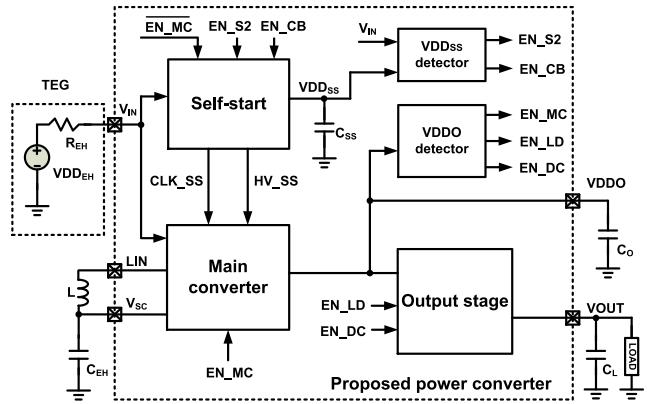


Fig. 3. Proposed power converter for TEG.

This is based on the observation that there exists dependency between efficiency, desired output voltage and the charge pump stage. MOS switches are also commonly used instead of diode for better efficiency consideration due to its lower voltage drop [5], [18]. Adaptive gate biasing technique is used to ensure high conversion efficiency for both heavy and light loads [19].

III. PROPOSED POWER CONVERTER STRUCTURE

The proposed power converter for TEG is shown in Fig. 3. It is composed of self-start, main converter, output stage and two voltage detectors for VDD_{SS} and $VDDO$ respectively. A self-start circuit is used to achieve low start-up voltage without any external components. The output of the self-start block is a high voltage swing clock CLK_{SS} and a high voltage node HV_{SS} . CLK_{SS} and HV_{SS} are then used to trigger the main converter. After self-start, the main converter will continuously extract power from TEG and charge the capacitor C_O to increase the output $VDDO$. The output stage is used to regulate the varying main converter output $VDDO$ to a stable output $VOUT$ for different load, and also to clamp the $VDDO$ for self-protection.

A. Self-Start

Generally inductor-based boost circuit needs around 600 mV clock output swing to kick-start the main converter [4]. Conventional self-start circuit uses a ring oscillator and a charge pump to boost the capacitor voltage to a value higher than 600 mV to kick start the main converter. However, directly charging VDD_{SS} to 600 mV in low supply voltage is quite difficult and slow.

In our proposed architecture, we achieve the low self-start voltage through 3 steps. By employing 1st ring oscillator and 1st charge pump which can operate at low supply voltage as indicated by the unshaded region in Fig. 4, a low self-start voltage down to 60 mV can be obtained during step 1. However, due to these two optimized blocks for low supply voltage operation, their driving capabilities are limited under V_{IN} of 60mV, which constrained the 1st charge pump output at C_{SS} to around 105 mV. To fill in the gap between the 1st charge pump output of 105 mV and the desired 600 mV, the blocks

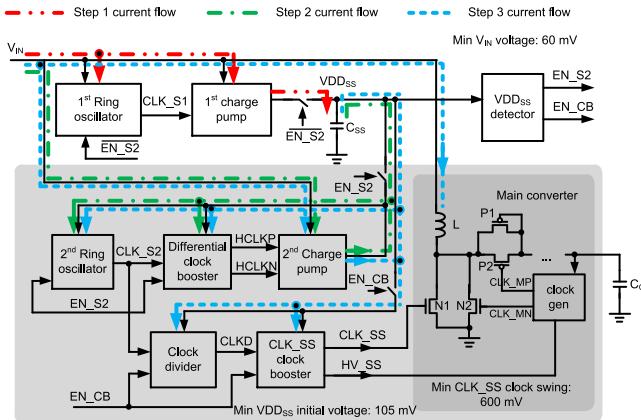


Fig. 4. Self-start block.

within the light grey region is employed to further boost up the C_{SS} voltage. With VDD_{SS} voltage of 105 mV, 2nd ring oscillator and differential clock booster are now optimized with larger clock swing to drive the 2nd charge pump in step 2. This allows 2nd charge pump to deliver more power to C_{SS} after offsetting the power consumed by the 2nd ring oscillator and differential clock booster. The voltage of VDD_{SS} can thus be further increased beyond 300 mV, and the self-start circuit enters step 3. During this step, the clock divider and the CLK_{SS} clock booster are turned on. Their power consumption can now be sustained by the 2nd charge pump at $VDD_{SS} > 300$ mV. With this value of VDD_{SS} , the output clock CLK_{SS} can attain 700 mV swing, which is now sufficiently large to trigger the main converter. The current flow for the three steps are indicated as the red dash dot dot line, green dash-dot line and blue dotted line in Fig. 4 respectively. Three power gates are implemented to further reduce the unwanted leakage during step 1, step 2 and step 3.

1) *Self-Start Step 1:* To enable the 1st charge pump to function in such a low supply voltage of 60 mV, the critical thing is to ensure self-oscillation of 1st ring oscillator at such low voltage. The fundamental building block for ring oscillator is an inverter. For normal inverter employing transistors with low threshold voltage (LVT inverter) as shown in Fig. 5(a), it can function properly at high supply voltage as the on/off resistance ratio between NFET and PFET is significantly large to toggle the output to either ground or supply rail easily. However, at lower supply voltage, this resistance ratio is no longer significant. Hence, it is difficult for ring oscillator with LVT inverter to operate at low supply voltage.

In this paper, we propose a novel redundant inverter that achieves better on/off resistance ratio even at low supply voltage. As shown in Fig. 5(b), a 2-stage redundant inverter which consists of three inverters is used as the fundamental building block. The power and ground of the 3rd inverter is from the output of the 1st and 2nd inverters, respectively. The 1st and 2nd inverters have asymmetric NFET/PFET sizing as illustrated. The main concept is to let 1st/2nd inverter have stronger pull-up/pull-down path through larger PFET/NFET sizing, respectively. When input A is '1', both the 1st and

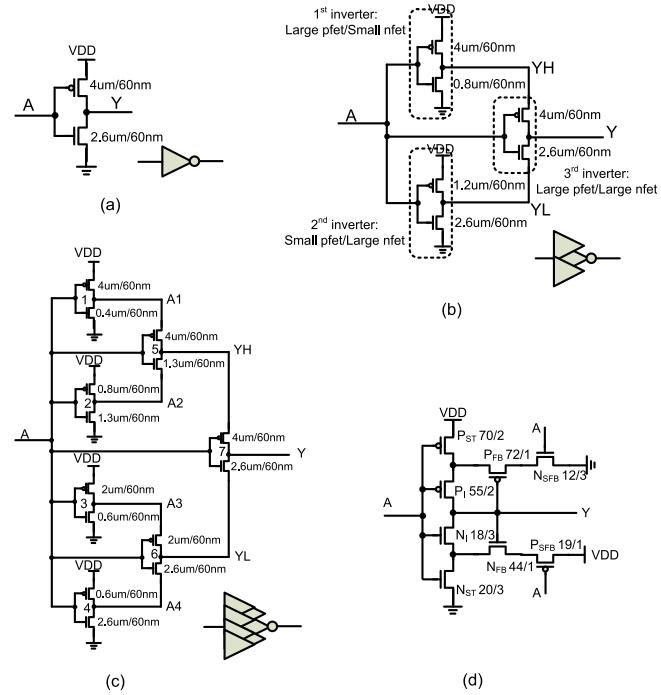


Fig. 5. Circuit of inverters (a) normal inverter (b) 2-stage redundant inverter (c) 3-stage redundant inverter (d) Selective Schmitt-trigger inverter [10].

2nd inverters will have '0' output. However, the 1st and 2nd inverters will have weak and strong '0' respectively. The 3rd inverter will present a large resistance ratio to ensure strong '0' propagate to the output Y even with low supply voltage. When input A is '0', both the 1st and 2nd inverters will have '1' output now. However, in this round, the 1st and 2nd inverters will have strong and weak '1' respectively. Through the 3rd inverter, similar large resistance ratio is observed in the opposite manner to ensure strong '1' propagate to the output Y under low supply voltage. In this way, we can still get large output swing with this redundant inverter under low supply voltage at the expense of lower switching speed.

The same concept can be extended to a 3-stage redundant inverter as shown in Fig. 5(c), which is composed of 7 inverters. It works in the similar way as the 2-stage redundant inverter, but can get even larger output swing. The concept can be easily extended to N -stage redundant inverter.

Fig. 6 shows the simulated ring oscillator output clock waveform with normal inverter, selective Schmitt-trigger inverter (as shown in Fig. 5 (d), its unit size is set to 60 nm), 2-stage redundant inverter and 3-stage redundant inverter under the supply voltage of 45 mV, 50 mV, 60 mV and 70 mV. It is observed that the oscillator with 3-stage redundant inverter can output clock with lowest self-start voltage and largest voltage swing. Fig. 7 shows the output swing histogram of these oscillators based on Monte-Carlo simulation under the supply voltage of 70 mV. The oscillator with 3-stage redundant inverter attained the largest output swing of 63.5 mV and the smallest standard deviation of 6.6 mV, which proves the robustness of the proposed 3-stage redundant inverter design.

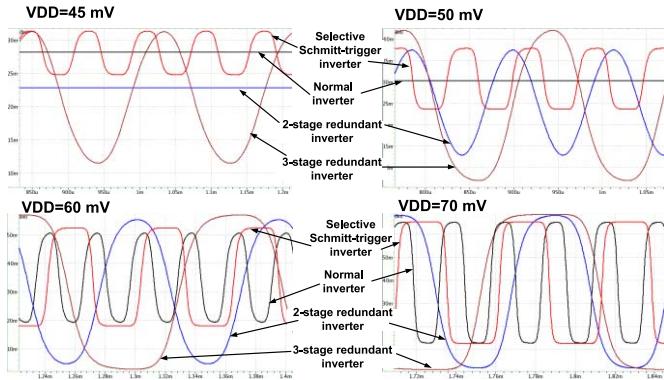


Fig. 6. Simulated ring oscillator waveform with normal inverter, selective Schmitt-trigger inverter, 2-stage redundant inverter, 3-stage redundant inverter @ $VDD=45$ mV/50 mV/60 mV/70 mV.

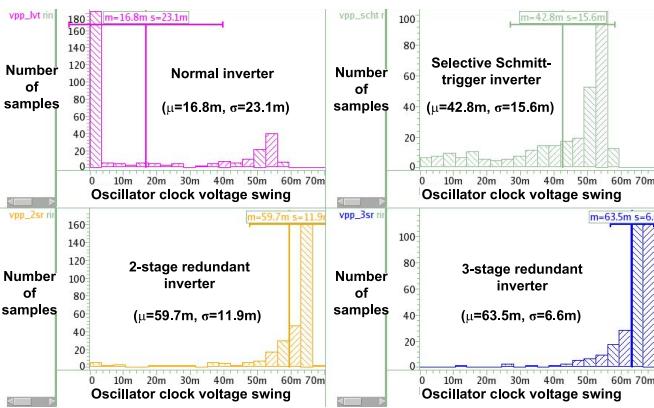


Fig. 7. Oscillator output swing histogram based on Monte-Carlo simulation with normal inverter, selective Schmitt-trigger inverter, 2-stage redundant inverter, 3-stage redundant inverter (VDD is 70 mV and temperature is 25 °C).

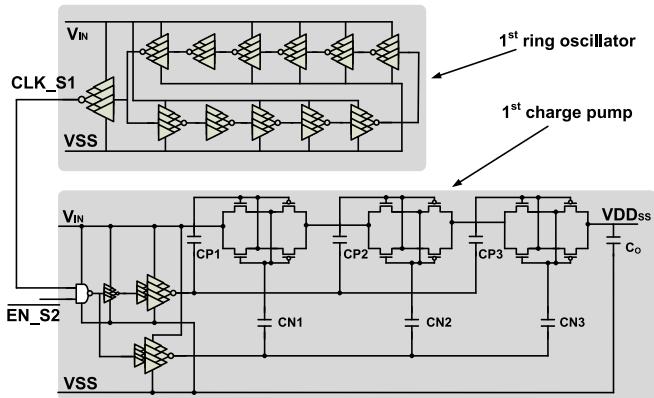


Fig. 8. Circuit of 1st ring oscillator and 1st charge pump.

In this work, a 3-stage redundant inverter is used for the 1st ring oscillator as shown in Fig. 8. From the measurement result shown in Fig. 9, the ring oscillator can oscillate with supply voltage as low as 45 mV, which is very close to the MOSFET oscillator's limitation of 36 mV [20], proving the feasibility of the proposed redundant inverter based ring oscillator. The simulated (post-layout) and measured oscillator clock frequency with respect to V_{IN} are shown in Fig. 10.

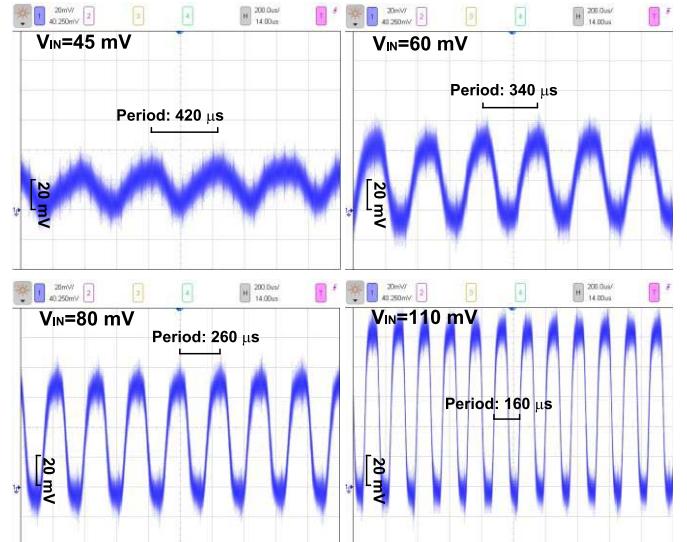


Fig. 9. Measured 1st ring oscillator output clock waveform @ $V_{IN} = 45$ mV, 60 mV, 80 mV and 110 mV.

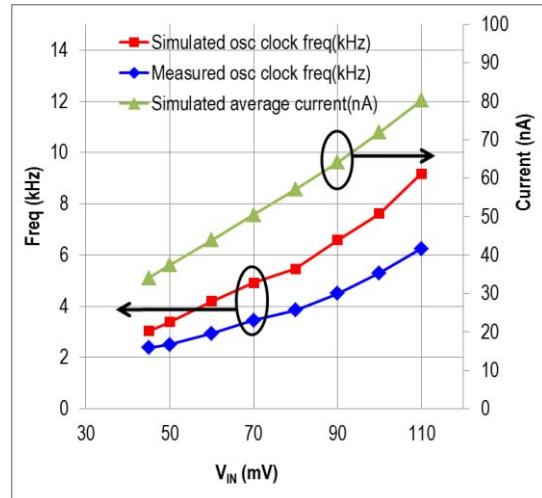


Fig. 10. Measured and simulated clock frequency and average current of 1st ring oscillator with respect to V_{IN} .

As shown, higher supply voltage will result in higher output clock frequency. The measured clock frequency is about 30% lower than the simulation result, which may be due to the inaccuracy of the device model in sub-threshold region. The simulated supply current of 1st ring oscillator is also shown to linearly increase with V_{IN} in Fig. 10. The power consumption of 1st ring oscillator is around 1~10 nW.

A 3-stage Pelliconi charge pump [21] is used for the 1st charge pump as shown in Fig. 8. The charge pump is powered by TEG source output V_{IN} and driven by the clock CLK_S1 from the 1st ring oscillator. Each of the clock signal and its complement will need to drive three large capacitors. A large buffer chain with 3-stage redundant inverters is thus provided for each clock path. The NAND cell used in 1st charge pump is also specially designed for ultra-low supply voltage [22]. Theoretically, if the clocks have the same voltage level as the

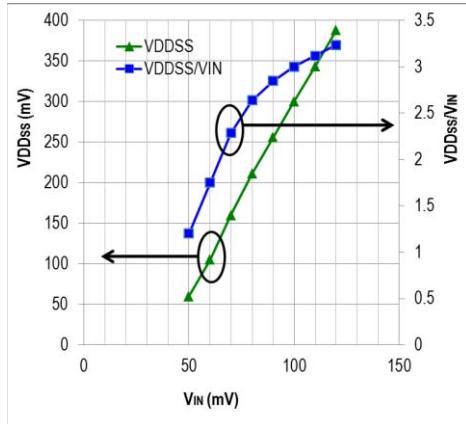


Fig. 11. Simulated dependence of achievable V_{DDSS} on V_{IN} for 1st ring oscillator and 1st charge pump.

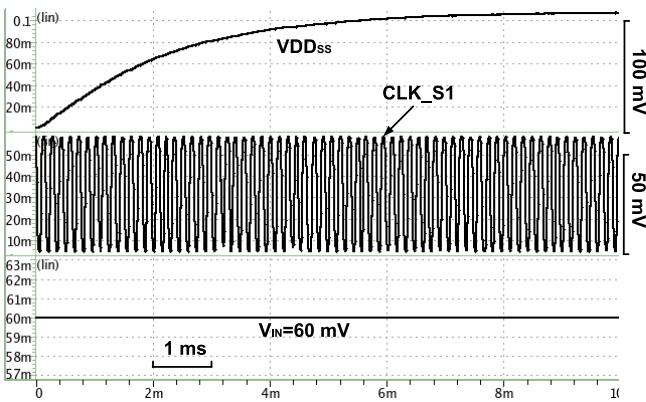


Fig. 12. Simulation waveform of 1st ring oscillator and 1st charge pump when $V_{IN} = 60$ mV.

supply and the load is zero, this 1st charge pump could produce output voltage at 4 times of V_{IN} . However, at lower supply voltage, for the reason of poorer clock driving capability and weaker reverse leakage cut off, the charge pump performance suffers and produces lower V_{DDSS}/V_{IN} ratio. Fig. 11 shows the simulated result of the maximum achievable V_{DDSS} and V_{DDSS}/V_{IN} ratio for different V_{IN} with loading of $50\text{ M}\Omega$. Fig. 12 shows the simulation waveform for V_{IN} of 60 mV. The ratio of V_{DDSS}/V_{IN} is limited to 1.75 at this V_{IN} voltage.

2) Self-Start Step 2: Exponential charge pump [3] is used for the 2nd charge pump as shown in Fig. 13. It can directly pump the charge from supply to output by subtly controlling the switching clock. The input clocks of the exponential charge pump are used for switching the NFETs instead of power delivery, which is unlike the traditional Dickson or Pelliconi charge pump. As these NFETs have smaller size, the input clocks are not required to have large driving strength. This leads to smaller power consumption for the clock generator.

As the exponential charge pump is composed of pure NFETs, signals pass through these NFETs will be clamped at the clock voltage level. If normal clock generator is used, the clock output swing will be limited which in turns constrain the achievable output voltage of the charge pump. To solve this problem, a differential clock booster is proposed to generate

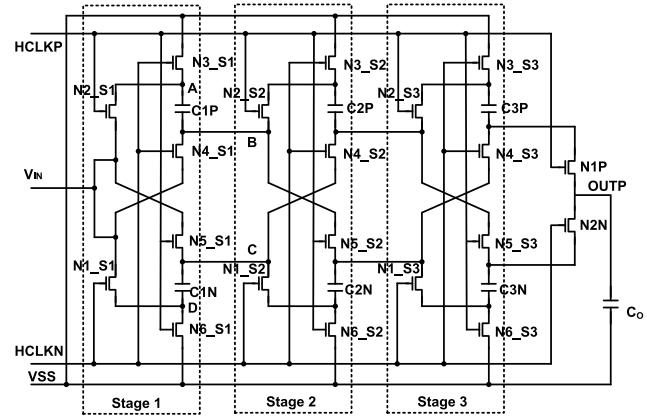


Fig. 13. 2nd charge pump circuit.

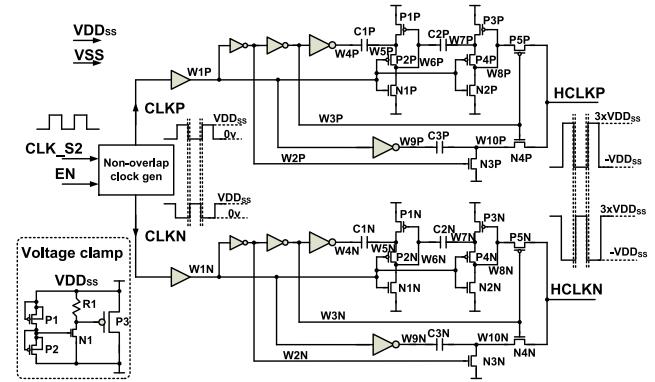


Fig. 14. Circuit of differential clock booster.

clock signal for the exponential charge pump. Although the differential clock booster is powered by the exponential charge pump's output, its clock output swing can be much higher than the charge pump's output. Despite the higher voltage swing, the power consumption of the differential clock booster is still limited, thanks to the small clock driving strength required by exponential charge pump. This enables the 2nd charge pump to continue increasing V_{DDSS} during step 2 once 105 mV is reached in step 1.

The circuit of this differential clock booster is shown in Fig. 14. It is powered by V_{DDSS} , and is driven by the clock CLK_S2 from the 2nd ring oscillator. The output signals $HCLKP/HCLKN$ are used as the input of the 2nd charge pump. Ideally, the high voltage level of $HCLKP/HCLKN$ for clock '1' can reach $3 \times V_{DDSS}$, and the low voltage level of $HCLKP/HCLKN$ for clock '0' can reach $-V_{DDSS}$. Due to the consideration of the device reliability, the voltage of V_{DDSS} should not exceed 0.45 V. A voltage clamp is thus implemented to clamp V_{DDSS} to 0.45 V, as shown in the bottom left of Fig. 14. Due to the clock high voltage level of $3 \times V_{DDSS}$, the current flows through the NFET will not be constrained by V_{DDSS} . Similarly, due to the clock low voltage level of $-V_{DDSS}$, the NFETs' off-resistance is increased which help reducing the reverse current. This helps improving the charge pump efficiency.

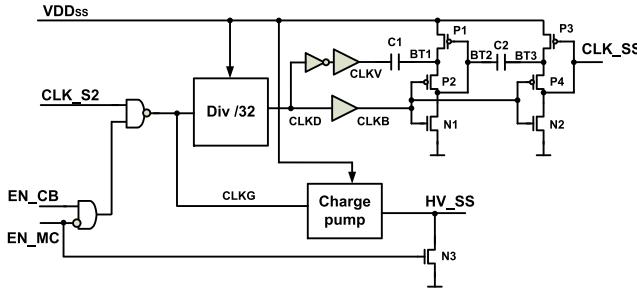


Fig. 15. CLK_SS clock booster.

3) *Self-Start Step 3*: Limited by the available TEG input voltage source, the resulting VDD_{SS} might not be sufficient to directly drive the NFET switch within the main converter. Hence, another clock booster is employed to generate clock with higher voltage swing (>700 mV) for the main converter. Once the voltage of the VDD_{SS} exceeds 300 mV during step 2, there is now sufficient power for the CLK_{SS} clock booster. EN_{CB} will now turn high to enable the CLK_{SS} clock booster, and self-start step 3 begins. The circuit of this CLK_{SS} clock booster is shown in Fig. 15. It is powered by VDD_{SS} , and its input clock CLK_{S2} is directly drawn from the 2nd ring oscillator output. To allow sufficient time for the voltage to rise up and reduce the dynamic power for high voltage circuit, the input clock is firstly divided down by 32 before it is boosted. In addition, HV_{SS} is generated to ensure proper switch operation within the main converter during self-start period, which will be explained in next section.

4) *Self-Start Simulation*: Fig. 16 shows the self-start simulation waveform when V_{IN} is 68 mV. Due to the leakage current and the additional power consumed by the VDD_{SS} detector, the simulated self-start voltage of the top level schematic is a little larger than the previous simulated standalone self-start voltage of 60 mV. As described earlier, the 1st ring oscillator generates the CLK_{S1} clock signal, which drives the 1st charge pump to charge up VDD_{SS} from 0 to around 110 mV in step 1. Then EN_{S2} is toggled, and step 2 initiates. The 2nd ring oscillator and the differential clock booster are activated. The resulting clock signals ($HCLKP/HCLKN$) with its higher voltage level, further drive the 2nd charge pump and continue to charge up VDD_{SS} at faster rate to 330 mV. At this instant, EN_{CB} is turned high and step 3 starts. CLK_{SS} clock booster is now activated to output high voltage clock CLK_{SS} and the high voltage node HV_{SS} to trigger the main converter. In the simulation, it takes around 10 ms to achieve a stable high voltage swing clock and a high voltage node.

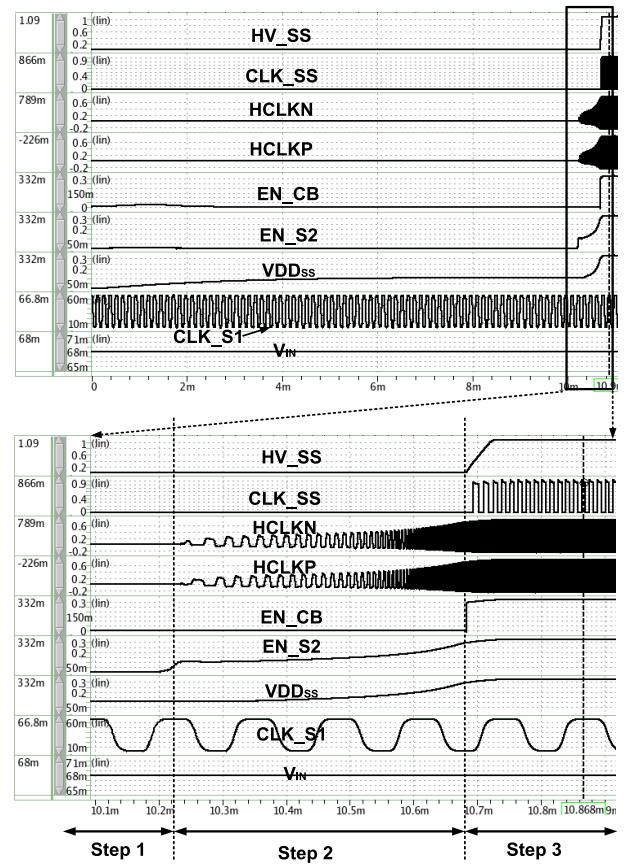
The simulated power consumption for each self-start step is listed in Table I. The maximum power consumed by the self-start block is $55.88 \mu\text{W}$ when V_{IN} is at 210 mV. This is well within the power that can be supplied by TEG source at this V_{IN} .

B. Main Converter

The main converter is shown in Fig. 17. Once CLK_{SS} is available, N1 and the diode connected P1 will form a simple booster converter to charge up C_0 until the voltage of $VDDO$

TABLE I
SIMULATED SELF-START POWER CONSUMPTION

V_{IN}	Start-up Phase	Average current	Average power consumption
80 mV	Step 1	$12.7 \mu\text{A}$	$1.02 \mu\text{W}$
	Step 2	$24.5 \mu\text{A}$	$1.96 \mu\text{W}$
	Step 3	$55.1 \mu\text{A}$	$4.41 \mu\text{W}$
120 mV	Step 1	$19.4 \mu\text{A}$	$2.33 \mu\text{W}$
	Step 2	$72.3 \mu\text{A}$	$8.67 \mu\text{W}$
	Step 3	$116.8 \mu\text{A}$	$14.0 \mu\text{W}$
210 mV	Step 1	$67.2 \mu\text{A}$	$14.11 \mu\text{W}$
	Step 2	$156.2 \mu\text{A}$	$32.88 \mu\text{W}$
	Step 3	$266.1 \mu\text{A}$	$55.88 \mu\text{W}$

Fig. 16. Self-start simulation waveform($V_{IN} = 68 \text{ mV}$).

reaches 1 V. Given that the driving strength of CLK_{SS} is limited, smaller NFET sizing of N1 is used. N2 gate input is fixed at '0' during this transition period. The gate of N4 and P2 are connected to HV_{SS} , which is from the self-start block. This ensures that N4 is fully turned on with small on-resistance and P2 is fully turned off with large off-resistance to prevent the current flow back during this transition mode when $VDDO$ is still lower than 1 V. Once $VDDO$ exceeds 1 V, EN_{MC} turns high and the main converter circuits supplied by $VDDO$ will start to work in normal operation mode.

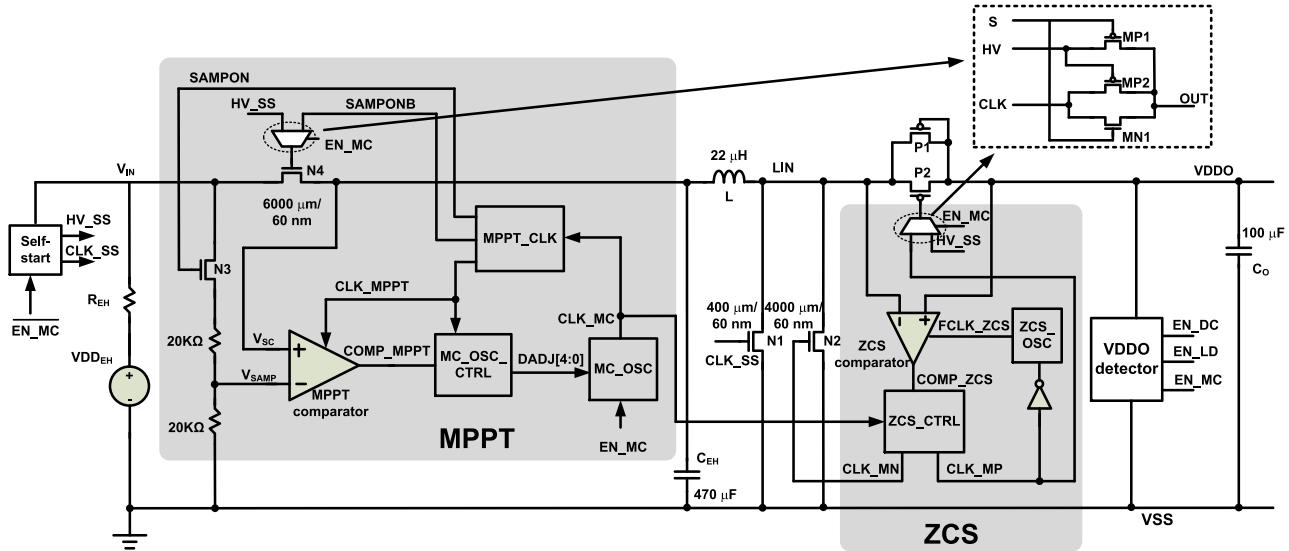


Fig. 17. Block diagram of main converter.

During normal operation mode, high efficiency, maximum extracted power and minimum operating voltage are the main considerations for energy harvesting power converter, which warrants further discussion.

1) *Efficiency Improvement*: During normal operation mode, the newly generated clock *CLK_MC* with higher voltage and optimized period time is used to trigger the larger size NFET N2 in main converter. *CLK_SS* is fixed at 0 V to fully turn off the NFET N1 to avoid unnecessary leakage current. Self-start block is fully switched off to avoid unnecessary power consumption.

Boundary continuous-conduction mode (CCM) is implemented for this main converter to avoid unnecessary leakage from *VDDO* to *LIN* when inductor current reduced to zero in conventional discontinuous conduction mode (DCM), so as to improve the conversion efficiency.

ZCS is also implemented to avoid the voltage drop across the diode to improve conversion efficiency. In normal operation mode, the NFET N2 and PFET P2 in Fig. 17 work in complementary manner to direct the inductor current through different paths. When N2 is switched off and P2 is switched on, the voltage drop on P2 is much smaller than the voltage drop on P1 in self-start step 3. The current flowing through P2 will keep reducing and eventually reaching zero or negative. Negative current will result in current flow back situation and discharge the capacitor *C_O*, which decrease the conversion efficiency. Hence, a ZCS block is employed here to detect the zero current point in P2. Upon detection, P2 will be switched off immediately, and at the same time N2 will be turned on to continuously charge the inductor.

As the voltage drop across P2 is proportional to the current flowing through it, a dynamic comparator is employed to sense the zero current point by comparing the differential voltage at the drain and source terminal of P2. In general, both the *V_{IN}* voltage and the voltage drop on P2 are much smaller than *VDDO*, so the inductor discharging speed can be

estimated as:

$$\frac{di}{dt} = VDDO/L, \quad (1)$$

where *L* is the inductor value. The desired pulse width (*T_{PW}*) of negative cycle of *CLK_MP* can be calculated as:

$$T_{PW} = L \times (I_{PEAK}/VDDO), \quad (2)$$

where *I_{PEAK}* is the inductor peak current, it can be estimated as:

$$I_{PEAK} = V_{IN} \times T_{CLK_MC} / L, \quad (3)$$

where *T_{CLK_MC}* is the *CLK_MC* cycle time. By approximating the input current with a triangular waveform, the extracted power can be estimated as:

$$P_{EXT} = 0.5 \times V_{IN}^2 \times T_{CLK_MC} / L. \quad (4)$$

Selecting a proper value of inductor *L* is very important for this power converter. Large inductor value *L* will require large *CLK_MC* cycle time, while too large *CLK_MC* cycle time will result in undesirably large fluctuation on *VDDO*. On the other hand, small *L* will require high frequency of *CLK_MC*, which will increase the intrinsic power consumption of the main converter. According to (2), small *L* will also result in small *CLK_MP* pulse width *T_{PW}*, which will affect the ZCS detection accuracy. Hence, using the above guidelines, we tried out different inductor through simulation to ensure that other parameters such as *CLK_MC* cycle time, *VDDO* fluctuation, *T_{PW}*, and intrinsic power consumption can still meet the requirements. A 22 μH inductor is finally chosen for this power converter.

For low supply voltage operation, the cycle time of ZCS comparator clock *FCLK_ZCS* should be smaller than half of the inductor discharging time.

$$FCLK_ZCS < 0.5 \times V_{IN} \times T_{CLK_MC} / VDDO. \quad (5)$$

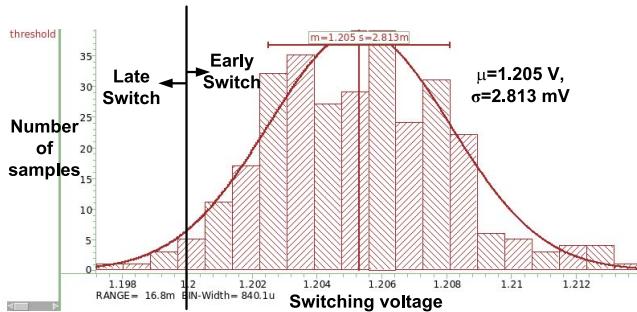


Fig. 18. ZCS comparator switching voltage histogram based on Monte-Carlo simulation (1.2 V reference voltage, 25 °C).

Assume the target minimum operating voltage is 10 mV, $VDDO$ of 1.0 V and the CLK_MC cycle time is 10 μs , T_{FCLK_ZCS} need to be smaller than 0.05 μs . The frequency of $FCLK_ZCS$ is finally designed to be around 40 MHz. The choice of CLK_MC cycle time will be explained in next section.

In reality, exact zero current point detection is impossible. Compared to late zero current point detection, slightly early zero current point detection is desirable as it will reduce the possibility of current flowing back, which will seriously degrade the efficiency. So the dynamic comparator is purposely designed with a fixed offset to let P2 have high possibility of turning off early after process variation consideration. It should be noted that the offset introduced should not be too big as well to allow the converter to function at very low voltage of V_{IN} . Fig. 18 shows the ZCS comparator switching voltage histogram based on Monte-Carlo simulation. As illustrated, the average switching threshold (V_{MEAN}) of 1.205 V, and the standard deviation (σ) of 2.813 mV are obtained. Given that $VDDO$ of 1.2 V is used as the reference voltage for the comparator, more than 95% of the samples will incur the desired early zero current detection and early switch-off. It should be noted that $VDDO$ may vary from 0.9 V to 1.4 V in the actual operation. Fig. 19 illustrates the timing diagram of this ZCS block. To save power, $FCLK_ZCS$ is only generated when P2 turns on.

2) MPPT: MPPT block is implemented in the main converter to maximize the extracted power. For TEG source, the maximum extraction power point occurs when the short circuit TEG output voltage V_{IN} (V_{IN} equals to V_{SC} , when N4 is on) is reduced to half of its open circuit voltage VDD_{EH} . In conventional design, C_{EH} appears across the TEG directly and before the main converter. During normal operation, voltage across C_{EH} will depend on the effective impedance presented by the main converter. Open circuit voltage is then sampled by totally disabling the main converter and allowing C_{EH} to charge up.

In this paper, we propose alternative MPPT solution. C_{EH} is put within the main converter, right after N4 switch as shown in Fig. 17. $SAMPON$ and $SAMPONB$ are the MPPT sampling clock signals, with reduced frequency, which is 1/64 of CLK_MC . During normal operation, the short circuit voltage V_{SC} is captured by C_{EH} . C_{EH} of 470 μF is chosen to minimize

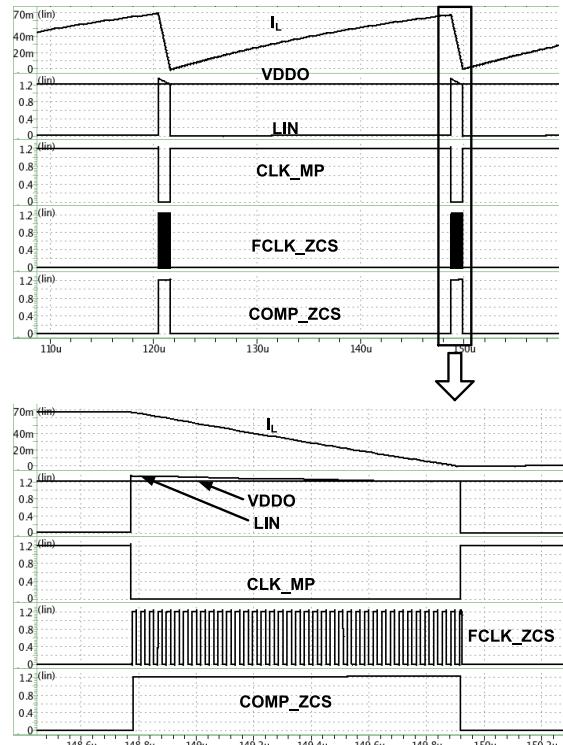


Fig. 19. Simulated timing diagram of ZCS.

the voltage fluctuation during open circuit mode. When $SAMPON$ is high and $SAMPONB$ is low, N3 will be switched on and N4 will be switched off. As the TEG internal resistance is much smaller than the two serial resistors of 20 K Ω , V_{SAMP} is nearly 50% of the TEG open circuit voltage. Due to the different placement of C_{EH} , large capacitor is not involved to sample the open circuit voltage. Hence, shorter charging time can be obtained. A dynamic comparator is then used here to compare the V_{SC} and V_{SAMP} . Based on the comparison result $COMP_MPPT$, the block MC_OSC_CTRL will adjust its digital output $DADJ[4:0]$ accordingly. $DADJ[4:0]$ will vary the oscillator frequency of MC_OSC . This in turn adjusts the equivalent input resistance of the main converter and modifies the V_{SC} .

Assume $VDDO \gg V_{SC}$, and V_{SC} equals to V_{IN} , the effective input resistance of this power converter can be calculated as:

$$REFF = V_{SC} / (0.5 \times I_{PEAK}) = 2 \times L / T_{CLK_MC}. \quad (6)$$

The short circuit voltage V_{SC} can be calculated as:

$$V_{SC} = VDD_{EH} \times REFF / (REH + REFF). \quad (7)$$

So the input power of this power converter is:

$$P_{IN} = VDD_{EH}^2 \times REFF / (REH + REFF)^2, \quad (8)$$

where VDD_{EH} is the TEG open circuit voltage, REH is the TEG internal resistance. When $REFF$ equals to REH , the maximum power extacted from TEG is:

$$P_{MEX} = VDD_{EH}^2 / (4 \times REH). \quad (9)$$

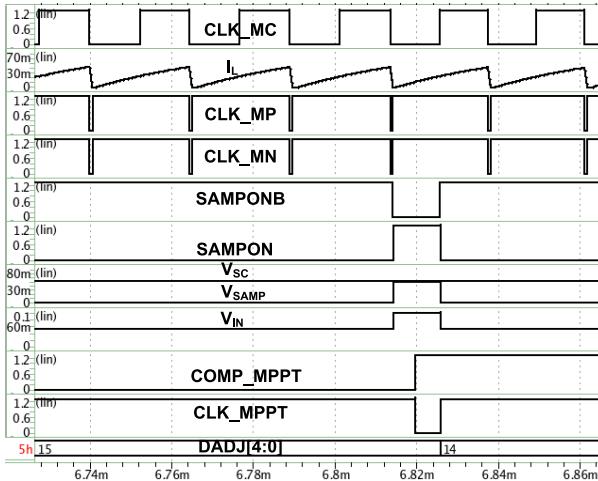


Fig. 20. Simulated timing diagram of MPPT.

As noted in (6), reducing T_{CLK_MC} (increasing the oscillator frequency) will increase the effective input resistance. Hence larger V_{SC} will appear. By comparing V_{SC} and V_{SAMP} and adjusting T_{CLK_MC} accordingly, MPPT can be achieved. The simulated MPPT waveform is shown in Fig. 20.

Given the selected inductor and the TEG internal resistance, the adjustable range of CLK_MC period time need to be designed properly so that the best matched R_{EFF} which equals to R_{EH} , can be searched by adjusting the period of CLK_MC .

$$0.5 \times R_{EH} \leq 2 \times L/T_{CLK_MC} \leq 2 \times R_{EH}. \quad (10)$$

As discussed earlier, L of 22 μH is chosen, assuming a TEG source with internal resistance R_{EH} in the range of 2 Ω to 5 Ω . Then the CLK_MC clock cycle time is designed with the adjustable range of 5 ~ 40 μs to meet the requirement of (10).

3) *Minimum Operating Voltage*: Due to the small temperature difference of body-to-surrounding, it is also very important to sustain the power converter operation with a very small input voltage. To ensure sustained operation at a certain low TEG input voltage after self-start, the power converter input power should be larger than the sum of the resistive power loss and intrinsic power consumption of the main converter at this input voltage.

By approximating the input current with a triangular waveform, the average input power can be calculated as:

$$P_{AIN} = 0.5 \times V_{IN}^2 / (R_O + R_{EFF}), \quad (11)$$

where V_{IN} is the power converter input voltage, R_O is the resistance along the inductor charging path, and R_{EFF} is the ideal power converter effective input resistance.

$$R_O = R_{N4} + R_{N2} + R_L + R_{PA}, \quad (12)$$

where R_{N4} and R_{N2} are the on-resistance of the 2 NFETs, N4 and N2, respectively, R_L is the internal resistance of the inductor, and R_{PA} is the routing parasitic resistance along the inductor charging path.

To reduce R_O , large N2 and N4 are used. In addition, wide and short multi-layer metal are layout for the critical

TABLE II
RESISTANCE IN THE INDUCTOR CHARGING PATH

	Transistor size (Width/Length)	Simulated resistance
N4	6 mm/60 nm	0.1 Ω
N2	4 mm/60 nm	0.15 Ω
L (Inductor)	-	0.073 Ω (Spec)
Parasitic (Chip/PCB/Cable)	-	1.0 Ω (Estimated)
Total	-	1.32 Ω

TABLE III
SIMULATED POWER CONSUMPTION FOR EACH MAIN CONVERTER BLOCK (UNDER SUSTAINED CONDITION WHEN $VDDO$ is 1.0 V)

	Simulated working current ($VDDO$)	Enabled Duty cycle	Simulated average current ($VDDO$)
MPPT comparator	0.81 μA	1.56%	0.013 μA
ZCS comparator	8.15 μA	$(V_{IN}/1.0) \times 100\%$	$(8.51 \times V_{IN}) \mu\text{A}$
ZCS OSC	8.36 μA	$(V_{IN}/1.0) \times 100\%$	$(8.36 \times V_{IN}) \mu\text{A}$
ZCS_CTRL	0.770 μA	100%	0.770 μA
VDDO detector	0.018 μA	100%	0.018 μA
MC_OSC	2.14 μA	100%	2.14 μA
MC_OSC_CTRL and MPPT CLK	0.08 μA	100%	0.08 μA
P1 and P2 leakage	0.638 μA	~100%	0.638 μA
Total	-	-	$(16.87 \times V_{IN} + 3.66) \mu\text{A}$

charging path. Inductor with small internal resistance is also chosen. Table II lists the resistance of all components along the inductor charging path, which gives rise to R_O of around 1.32 Ω . When R_{EH} is 0, the CLK_MC cycle time will be adjusted to the high boundary of 40 μs to extract as much power as possible, when the value of R_{EFF} is 1.1 Ω based on (6).

The intrinsic power consumption P_{INT} of the proposed power converter includes that of ZCS ring oscillator, ZCS comparator, MPPT comparator, P1 and P2 leakage, and etc. To minimize P_{INT} , dynamic comparator is adopted for both ZCS and MPPT. It should also be noted that ZCS ring oscillator and ZCS comparator are only activated when CLK_MP is ‘0’. The low duty cycling ratio reduces P_{INT} significantly when V_{IN} is small. Ideally, through ZCS, the duty cycle will be maintained at

$$D_{ZCS} = V_{IN} / VDDO. \quad (13)$$

Similar idea of power saving is applied to MPPT. As MPPT clock frequency is 1/64 of the main converter clock CLK_MC , its average power consumption is also kept small.

Table III lists the simulated working current and average current for each main converter block under the sustained condition when $VDDO$ is 1.0 V. The total P_{INT} is $(16.87 \times V_{IN} + 3.66) \mu\text{W}$.

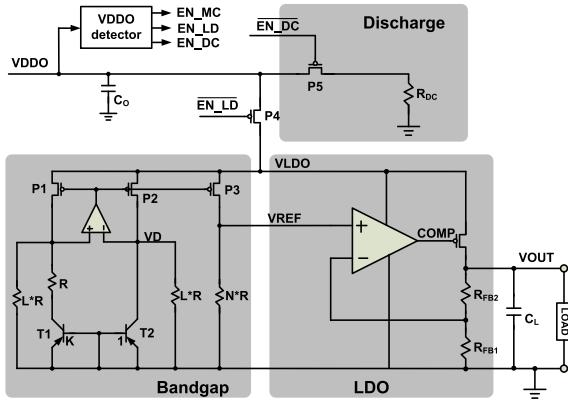


Fig. 21. Output stage.

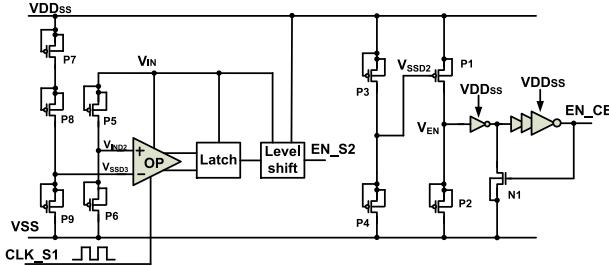


Fig. 22. VDDSS detector circuit.

Based on the value of R_{EFF} and R_O shown earlier, only $R_{EFF}/(R_{EFF}+R_O) = 45\%$ of the extracted power can be migrated to $VDDO$ and supplied to the main converter blocks. By equating this migrated power to the total P_{INT} ,

$$\frac{0.45 \times 0.5 \times V_{IN}^2}{1.32 + 1.1} = (16.87 \times V_{IN} + 3.66) \times 10^{-6}, \quad (14)$$

a minimum operating voltage of 6.4 mV can be obtained.

C. Output Stage

To get stable output voltage, conventional bandgap and LDO are implemented in the output stage as shown in Fig. 21. When $VDDO$ voltage is detected to be higher than 1.2 V, the Bandgap and LDO will then be switched on. With the Bandgap output reference voltage of exactly 0.65 V, the LDO will output regulated voltage at 1 V. When the $VDDO$ voltage is higher than 1.4 V, the discharge circuit will be turned on to clamp the $VDDO$ and protect the circuit.

D. VDDSS Detector and VDDO Detector

$VDDSS$ detector, as shown in Fig. 22, is designed to sense the achievable $VDDSS$ output voltage and generate two corresponding toggle signals, EN_S2 and EN_CB . To get better flexibility, we use the ratio of $VDDSS$ and V_{IN} as the criterion for EN_S2 . When $VDDSS$ is higher than 1.5 times of V_{IN} , EN_S2 will be toggled high. For EN_CB , absolute voltage of $VDDSS$ is used as the criterion. Once $VDDSS$ exceeds 300 mV, EN_CB will be toggled high.

To save silicon area and also to reduce the DC current of the $VDDSS$ detector, series of PFET based pseudo resistors

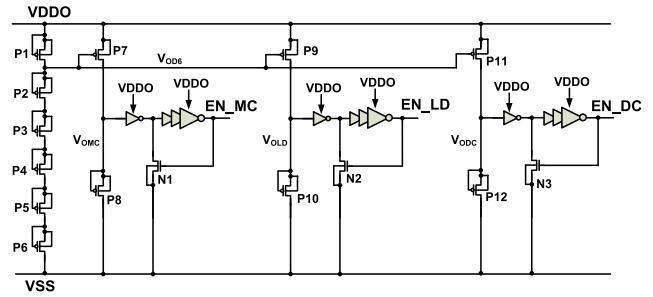


Fig. 23. VDDO detector circuit.

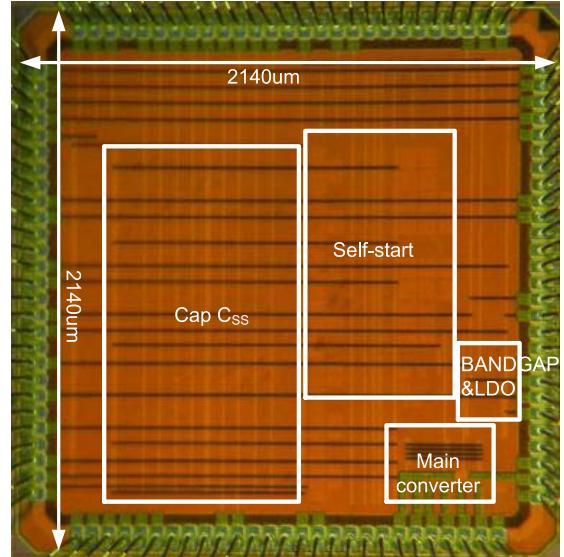


Fig. 24. Chip micrograph.

are used to generate voltage reference of half V_{IN} , half $VDDSS$ and one third of $VDDSS$. To obtain 300 mV threshold, one PFET (P1) with its gate connected to the half divided $VDDSS$ voltage is serially connected a PFET based pseudo resistor (P2) [23]. The threshold point of 300 mV can be achieved by selecting proper transistor sizing for P1 and P2.

$VDDO$ detector, as shown in Fig. 23, is designed to sense the achievable $VDDO$ voltage and generate three corresponding toggle signals, EN_MC , EN_LD and EN_DC . When $VDDO$ exceeds 1.0 V/1.2 V/1.4 V, $EN_MC/EN_LD/EN_DC$ will be toggled high respectively. Its structure is similar to that of the EN_CB in $VDDSS$ detector. As $VDDO$ voltage is much higher than $VDDSS$, the voltage divider is designed to output 5/6 of $VDDO$ to match with the PFET threshold voltage range.

IV. MEASUREMENT RESULT AND ANALYSIS

The proposed power converter has been fabricated in GLOBALFOUNDRIES 65LPe process. Fig. 24 shows the chip micrograph. The design occupies an active die area of $2140\mu\text{m} \times 2140\mu\text{m}$. An on-chip Metal-Oxide-Metal (MOM) capacitor of 1nF is implemented for C_{ss} to reduce external component count.

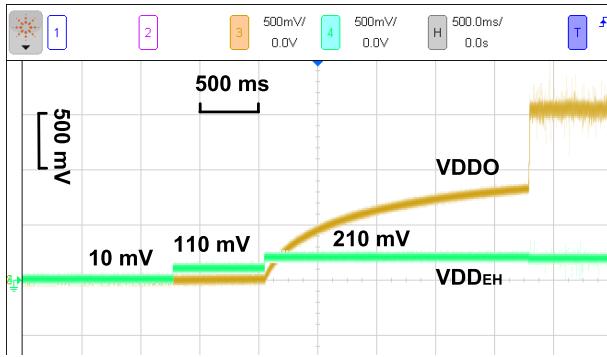
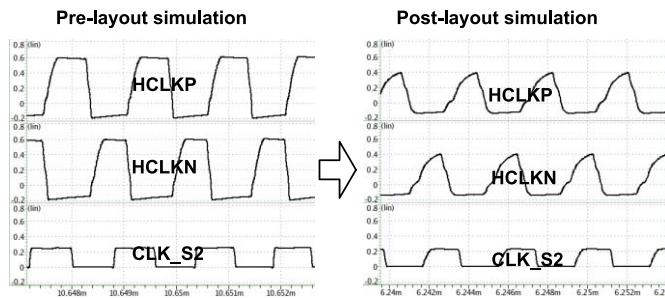


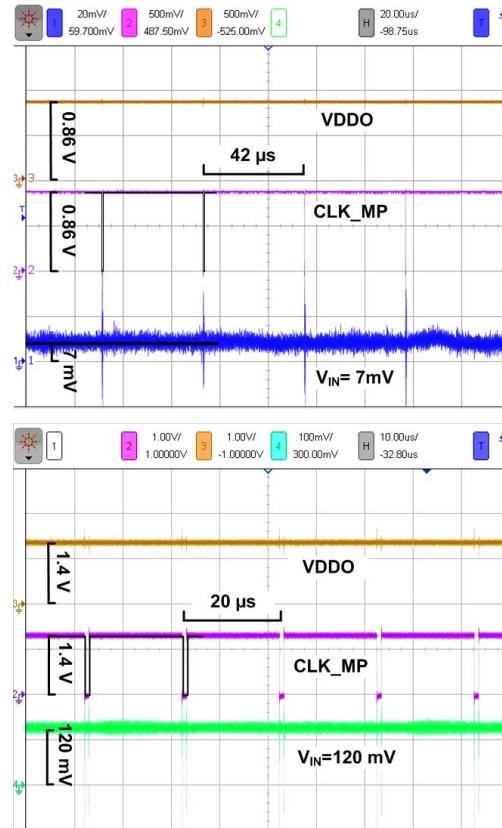
Fig. 25. Measured self-start waveform.

Fig. 26. Pre-layout and post-layout simulation waveform comparison for differential clock booster with large parasitic cap on *HCLKP/HCLKN*.

A. Self-Start Measurement

The measured waveform during self-start mode is shown in Fig. 25. When $VDEEH$ is increased to 210 mV, $VDDO$ voltage starts to rise until it reaches around 0.8 V. Beyond 0.8 V, the main converter enters normal operation mode, and the $VDDO$ voltage jump up to around 1.5 V within a very short interval. In total, it takes about 2.5 s for $VDDO$ to charge up from 0 to 0.8V due to the large C_O of $100\mu F$. It should be pointed out that this number is not the same as the earlier simulated 10 ms which is only related to $VDDSS$.

The measured self-start voltage is much higher than the pre-layout simulation result. From the measurement, we deduced that it is due to the large routing parasitic capacitors along the critical paths of *HCLKP* and *HCLKN* (output clock of the differential clock booster). As *HCLKP* and *HCLKN* are connected through stacked capacitors as shown in Fig. 14, capacitor sharing will limit the achievable output voltage level at *HCLKP/HCLKN*. The clock rising/falling time will also be increased due to the large parasitic capacitance on *HCLKP/HCLKN*. Both factors will limit the achievable clock output swing. This in turn limits the achievable minimum self-start voltage despite the fact that the 1st ring oscillator and 1st charge pump are able to function properly at low voltage. This is confirmed by the post-layout simulation waveform shown in Fig. 26. Due to the clock path parasitic, the post-layout simulation can only achieve 150 mV self-start voltage. By reducing this clock path parasitic for *HCLKP/HCLKN*, the post-layout simulation self-start voltage will be significantly reduced to 77 mV. Nevertheless, there is still discrepancy between the simulated self-start voltage

Fig. 27. Measured normal mode waveform when V_{IN} is 7 mV and 120 mV.

of 150 mV with clock path parasitic, and the measured self-start voltage of 210 mV. We suspect that inaccurate foundry model at subthreshold region or unmodelled leakage current could be the reason. As shown in Fig. 10 earlier, oscillator frequency discrepancy of 30% has been observed between the simulation and measurement, which indirectly prove the inaccuracy of the foundry model at sub-threshold region.

B. Minimum Operating Voltage Measurement

The operation voltage test result shows that this proposed power converter can continue to function with input voltage as low as 7 mV once it successfully starts up. The measured waveform is shown in Fig. 27 with V_{IN} of 7 mV and 120 mV respectively. As illustrated, with V_{IN} at 7 mV, the measured duty cycle of *CLK_MP* is around 0.6%, which is quite close to the calculated value of 0.8% based on (13); when V_{IN} is 120 mV, the measured duty cycle of *CLK_MP* is around 6.4%, which is also close to the calculated value of 9.1% based on (13).

The measured minimum operating voltage of 7 mV is quite close to the earlier estimated minimum operating voltage of 6.4 mV.

C. Power Converter Efficiency Measurement

In general, conversion efficiency of a power converter is defined as:

$$\eta_{COV} = P_{OUT} / P_{IN}, \quad (15)$$

TABLE IV
PERFORMANCE COMPARISON

	JSSC '15 [13]	JSSC '16 [10]	TCAS '15 [24]	TCAS '16 [25]	TCAS '17 [11]	TCAS '17 [26]	This work
Process	130 nm	130 nm	0.5 μ m	130 nm	65 nm	65 nm	65 nm
Energy source	TEG/Solar	TEG	TEG	TEG/Solar/ Piezo/fuel	TEG	TEG/Solar	TEG
Self-start Mechanism	PoR ring osc + Clock doubler	Schmitt trigger ring osc + CP	NA	Transformer + CP	PoR + CP	LC osc with on-chip L	redundant inverter based ring osc + CP + self-start assist
Self-start voltage	220 mV	70 mV	NA	36 mV	220 mV	100 mV	210 mV *
Min operating voltage	10 mV	-	50 mV	36 mV	85 mV	100 mV	7 mV
Conversion Efficiency	83%	58%	-	39%	75.9%	33%	74.5% (without LDO, measured at VDDO)
End-to-end Efficiency	-	58%	57.57%	-	-	-	71.5% (without LDO, measured at VDDO) 41.0% (with LDO, measured at VOUT)
MPPT	Yes	No	Yes	No	No	No	Yes
With LDO and Bandgap	No	No	Yes	No	No	No	Yes

* The measured self-start voltage is 210 mV. The pre-layout simulation result is 68 mV. The post-layout simulation result is 150 mV. If manually deduct the unexpected routing parasitic capacitance on the critical node of HCLKP/HCLKN, this value could be further reduced.

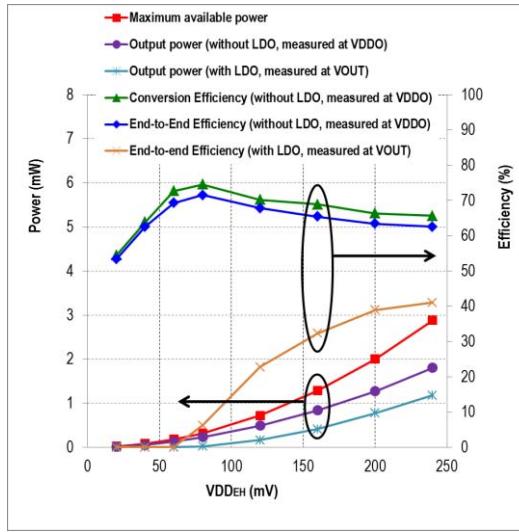


Fig. 28. Measured dependence of Output power and efficiency on V_{DDEH} .

where P_{OUT} is the power converter output power, and P_{IN} is the power converter input power from supply source. However, the definition of conversion efficiency might not reflect the effectiveness of the converter in extracting power from the energy source. This could directly impact the design of the energy source. Hence, another generally used end-to-end efficiency is applied here:

$$\eta_{ETE} = P_{OUT} / P_{MEX}, \quad (16)$$

where P_{MEX} is the maximum available power which can be extracted from energy harvester.

A 5 Ω resistor is connected in series with the power source to emulate the TEG internal resistance R_{EH} . The maximum available power, output power, conversion efficiency and end-to-end efficiency with and without LDO at different open circuit voltage V_{DDEH} are measured as shown in Fig. 28.

From the measurement, 10.6 μ W output power at VDDO is produced with the open circuit voltage of only 20 mV. At higher open circuit voltage of 240 mV, the output power at VDDO is increased to 1.8 mW. Maximum end-to-end efficiency (without LDO, measured at VDDO) of 71.5% is achieved when the open circuit voltage is 80 mV as shown in Fig. 28.

As mentioned earlier, P_{INT} and resistive loss along inductor charging path and discharging path are the main power losses. At low V_{DDEH} , resistive loss is insignificant due to the low current, and P_{INT} dominates. As the available power is small at low V_{DDEH} , this results in poor efficiency. Although higher power is available at higher V_{DDEH} , the higher current also leads to larger IR drop on the PFET P2 in Fig. 17, which result in higher percentage resistive power loss and thus worsens the efficiency. Hence, optimum efficiency (without LDO, measured at VDDO) is observed at V_{DDEH} of 80 mV, where the available power is large enough, while the resistive loss and P_{INT} are still relatively small.

The output power and the end-to-end efficiency of the whole system with cascaded bandgap and LDO (measured at VOUT) are also measured as shown in Fig. 28. The LDO can only function properly when the voltage of V_{IN} is higher than 60 mV. It should be noted that both the bandgap and LDO are not optimized in this design. Their high quiescent power and the LDO dropout voltage result in reduction of the end-to-end efficiency to 41.0% with output at VOUT, when V_{IN} is at voltage of 240 mV.

D. Performance Comparison

Table IV benchmarks the performance of the proposed TEG power converter with other reported results. As illustrated, our proposed power converter achieves the lowest operating voltage of 7 mV after self-start. It also achieves 210 mV

self-start voltage, which is comparable to others. It does not require alternative sources and external components. As mentioned earlier, lower self-start voltage can be expected once the routing parasitic of the clock path is minimized. MPPT has been incorporated into this proposed TEG power converter and achieved an end-to-end efficiency (without LDO, measured at VDDO) of 71.5%, which is amongst the highest across other reported TEG power converters. Similar to [24], our work provides complete solution including MPPT, LDO and bandgap, at much lower minimum operating voltage.

V. CONCLUSION

In this paper, a TEG power converter is presented. It uses redundant inverter based ring oscillator, Pelliconi charge pump and a self-start assist circuit with differential clock booster and exponential charge pump to obtain lower self-start voltage. MPPT and ZCS are included to obtain maximum power extraction, high end-to-end efficiency, and minimum operating voltage. The power converter achieves 210 mV self-start voltage and 7 mV operating voltage. With a $5\ \Omega$ TEG internal resistor, this power converter can output $229\ \mu\text{W}$ with 71.5% end-to-end efficiency (without LDO, measured at VDDO) when TEG open circuit is 80 mV. The end-to-end efficiency of the whole system with cascaded bandgap and LDO can achieve 41.0% when V_{IN} is at voltage of 240 mV.

REFERENCES

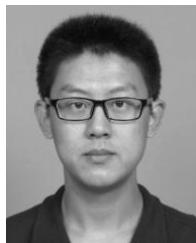
- [1] P. Fiorini, I. Doms, C. Van Hoof, and R. Vullers, "Micropower energy scavenging," in *Proc. IEEE ESSDERC*, Sep. 2008, pp. 4–9.
- [2] S. Kim *et al.*, "Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms," *Proc. IEEE*, vol. 102, no. 11, pp. 1649–1666, Nov. 2014.
- [3] C.-Y. Tsui, H. Shao, W.-H. Ki, and F. Su, "Ultra-low voltage power management circuit and computation methodology for energy harvesting applications," in *Proc. IEEE Asia South Pacific Conf. Design Autom.*, Jan. 2006, pp. 96–97.
- [4] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2011.
- [5] J.-P. Im *et al.*, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 104–105.
- [6] P.-S. Weng, H.-Y. Tang, P.-C. Ku, and L.-H. Lu, "50 mV-input batteryless boost converter for thermal energy harvesting," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1031–1041, Apr. 2013.
- [7] K. Kadirvel *et al.*, "A 330 nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 106–107.
- [8] P.-H. Chen *et al.*, "0.18-V input charge pump with forward body biasing in startup circuit using 65 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–4.
- [9] P.-H. Chen *et al.*, "An 80 mV startup dual-mode boost converter by charge-pumped pulse generator and threshold voltage tuned oscillator with hot carrier injection," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2554–2562, Nov. 2012.
- [10] J. Goeppert and Y. Manoli, "Fully integrated startup at 70 mV of boost converters for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1716–1726, Jul. 2016.
- [11] A. Das, Y. Gao, and T. T.-H. Kim, "A 220-mV power-on-reset based self-starter with 2-nW quiescent power for thermoelectric energy harvesting systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 1, pp. 217–226, Jan. 2017.
- [12] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.
- [13] A. Shrivastava, N. E. Roberts, O. U. Khan, D. D. Wentzloff, and B. H. Calhoun, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and $-14.5\ \text{dBm}$, 915 MHz RF kick-start," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1820–1832, Aug. 2015.
- [14] C.-Y. Yang, C.-Y. Hsieh, F.-K. Feng, and K.-H. Chen, "Highly efficient analog maximum power point tracking (AMPPT) in a photovoltaic system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1546–1556, Jul. 2012.
- [15] A. A. Abdelmoaty, M. Al-Shyoukh, Y.-C. Hsu, and A. A. Fayed, "A MPPT circuit with $25\ \mu\text{W}$ power consumption and 99.7% tracking efficiency for PV systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 272–282, Feb. 2017.
- [16] G. Chowdary and S. Chatterjee, "A 300-nW sensitive, 50-nA DC-DC converter for energy harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2674–2684, Nov. 2015.
- [17] I. Doms, P. Merken, C. Van Hoof, and R. P. Mertens, "Capacitive power management circuit for micropower thermoelectric generators with a $1.4\ \mu\text{A}$ controller," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2824–2833, Oct. 2009.
- [18] I. M. Darmayuda *et al.*, "A self-powered power conditioning IC for piezoelectric energy harvesting from short-duration vibrations," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 9, pp. 578–582, Sep. 2012.
- [19] P. H. Chen and P. M. Y. Fan, "An 83.4% peak efficiency single-inductor multiple-output based adaptive gate biasing DC-DC converter for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 405–412, Feb. 2015.
- [20] M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "On the minimum supply voltage for MOSFET oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 347–357, Feb. 2014.
- [21] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1068–1071, Jun. 2003.
- [22] N. Lotze and Y. Manoli, "A 62 mV $0.13\ \mu\text{m}$ CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan. 2012.
- [23] P.-H. Chen *et al.*, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and V_{TH} -tuned oscillator with fixed charge programming," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1252–1260, May 2012.
- [24] J. Zarate-Roldan, S. Carreon-Bautista, A. Costilla-Reyes, and E. Sánchez-Sinencio, "A power management unit with 40 dB switching-noise-suppression for a thermal harvesting array," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 1918–1928, Aug. 2015.
- [25] Y.-K. Teh and P. K. T. Mok, "DTMOS-based pulse transformer boost converter with complementary charge pump for multisource energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 5, pp. 508–512, May 2016.
- [26] H. Fuketa, S.-I. O'uchi, and T. Matsukawa, "Fully integrated, 100-mV minimum input voltage converter with gate-boosted charge pump kick-started by LC oscillator for energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 4, pp. 392–396, Apr. 2017.



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