A Low-Power High-Speed Comparator for Precise Applications

Ata Khorami and Mohammad Sharifkhani

***Abstract*— A low-power comparator is presented. pMOS transistors are used at the input of the preamplifier of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough preamplification gain and avoid excess power consumption. Meanwhile, small cross-coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the pMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for preamplification and avoid excess power consumption. The speed and the power benefits of the comparator were verified using solid analytical derivations, process–VDD–temperature corners, and Monte Carlo simulations along with silicon measurements in 0.18 μm. The tests confirm that the proposed circuit reduces the power consumption by 50% and provides 30% better comparison speed at the same offset and almost the same noise budgets. Moreover, the comparator provides a rail-to-rail input V_{cm} range in $f_{clk} = 500$ MHz.**

***Index Terms*— Dynamic comparator, high speed, low-offset comparator, low power, two-stage comparator.**

I. Introduction

NOWADAYS, low-power high-speed ADCs are integral parts of a variety of applications such as handheld devices. Comparators are the key building blocks of different types of ADCs, such as SAR, pipeline, and flash ADCs [1]–[4]. Several years ago, CMOS amplifiers were used as static comparators, although they suffer from very high power consumption (since they are always on) and inherent limited speed (since they have no positive feedback) [1]. Dynamic comparators improve the speed and reduce the total power consumption of the static comparators, since they employ positive feedback and save static power consumption [5]. One-stage dynamic comparators were proposed which used a latch circuit cascaded with a preamplifier. The kickback noise which is caused through the capacitive path from the output to input nodes makes the one-stage dynamic comparators inferior choices compared to their two-stage counterparts [6]. In the two-stage dynamic comparators, the problem of kickback noise is improved by weakening the capacitive path. In fact, in the two-stage dynamic comparators, the capacitive path is comprised of the series connection of gate–drain (C_{GD}) capacitors [6]. In the two-stage dynamic comparators, the first stage amplifies the input differential signal and is called the preamplifier stage while the second stage, the latch stage, amplifies its input differential signal up to VDD at one side and GND at the other side [1]–[7].

Examples of the two-stage dynamic comparators can be widely found in the literature. In the comparator reported in [8], the connection of the first stage to the second stage improves the speed and area, although a high-speed criterion causes offset and significant power consumption. In addition, the direct connection of the output nodes of the first and second stages (which endure a large voltage swing) deteriorates the kickback noise [6]. Two-stage comparators need both clock and its inverted signal to perform a comparison, which ask for a stricter timing design. To cover this problem, the comparator of [9] is proposed in which the activation of the latch is made by the common-mode voltage of the output nodes of the preamplifier, so it works with only one clock signal. Besides, the pMOS transistors are used at the input of the comparator to use their bulk pins for offset cancellation. Using this technique, the offset voltage is reduced at the cost of speed reduction. In that work, considering a low offset voltage, small sizing can be used for the input transistors of the preamplifier to reduce the power; however, the power is still high due to the additional components. In [10], a comparator with nMOS input transistors is reported to improve the speed; however, it increases the power consumption by a factor of four, since the preamplifier stage is always on to enhance the speed [10]. The comparator presented in [11] uses combined preamplifier and latch stages. The latch is activated with a delay to reduce the power consumption, achieving an acceptable offset voltage. However, it suffers from larger kickback noise and higher transistor count compared to the conventional method. In [12], a two-stage comparator is proposed which uses a simple latch with a direct connection to the output nodes of the preamplifier. This comparator is also working with a delayed clock to improve the offset voltage; however, it degrades the speed. Moreover, it suffers from kickback noise which is originated from the direct connection of the output nodes of the first and second stages. Moreover, using large input transistors for a low offset voltage results in large parasitic capacitors at the output nodes of the preamplifier stage. These capacitors must be charged using the latch stage; therefore, higher power consumption is required. The methods reported in [21]–[27] are some of the recent innovations on the dynamic comparators. For example, in [27], a low-power comparator with cross-coupled circuit is proposed which exacerbates the offset voltage, area. Also, the kickback noise increases since the preamplifier suffers a fast rail–rail voltage swing.

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In all mentioned research, the offset voltage or power consumption is improved using two methods which are described intuitively as follows. First, bulk-tuned calibration is used to have a lower offset voltage which results in smaller transistors and lower power, however, the calibration procedure takes time and increases complexity and area. Second, delayed comparators with larger input transistor sizing is used which sometimes increases the power consumption (for a low offset voltage) and reduces the speed of the comparator.

In this paper, a special controller (local clock generator) for the comparator and pMOS latch with pMOS preamplifier (latch and preamplifier with input pMOS transistors) are presented to achieve low-power and high-speed benefits. It is shown that the proposed comparator reduces the power consumption by half while increasing the speed. Moreover, it operates at large input common-mode voltages close to VDD, although pMOS transistors are used at the input of the comparator. As another benefit, the preamplification delay can be set to its optimum value to have a better comparison speed and reduce excess power consumption. However, in the conventional and other comparators, this delay is fixed to a value which is far from its optimum point. As a result, the proposed comparator is a good candidate for precise low-power high-speed applications.

This paper is organized as follows. Section II presents the conventional and proposed circuits. In Section III, the analytical derivations of the speed and the offset voltage are presented. Section IV discusses the noise behavior. In Section V, the controller behavior is verified using corner simulations. Section VI elaborates the simulations and compares different structures, and then in Section VII, silicon measurements are presented. Section VIII provides the conclusion.

II. Dynamic Comparators

A. Conventional Comparator

Fig. 1 presents the two-stage version of the conventional dynamic comparator [5], [13]. This comparator is comprised of a preamplifier and a latch. At the first phase which is called reset phase, clk is set to "1" and $\overline{clk}$ is set to "0" to reset the first and second stages of the comparator to GND and VDD, respectively (avoiding hysteresis). Then, clk changes to "0" and $\overline{clk}$ changes to "1" to begin the evaluation phase. In this phase, the parasitic capacitors of the output nodes of the preamplifier begin to being charged differentially based on the input differential signal ($V_{in+} - V_{in-}$). When the common voltage at the output of the preamplifier becomes higher than the threshold voltage of an nMOS transistor ($M_{10,11}$ in Fig. 1), the latch is turned on and amplifies its input differential voltage until it provides a rail-to-rail differential signal. In fact, the latch employs a positive feedback circuit to provide a fast amplification. Simultaneously, the output voltages of the preamplifier are charged to VDD.

Conventionally, for high-precision applications the size of the input transistors ($M_{3,4}$) are chosen large enough to achieve a high preamplifier gain and a better transistor matching. In this case, the effect of the latch on the input referred offset voltage is negligible. As discussed earlier, during the evaluation phase the output voltages of the preamplifier are charged to VDD gradually. As a result, considering the large sizing of M_3 and M_4 which causes large parasitic capacitors

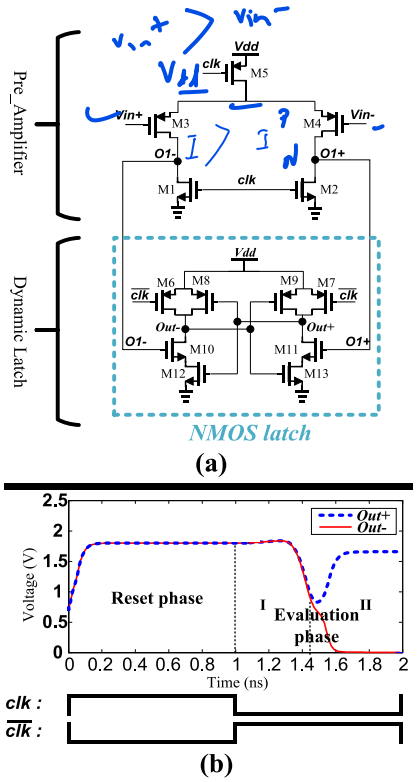

Fig. 1. (a) Conventional two-stage dynamic comparator. (b) Its typical output waveform and clock signal.

at O1+ and O1− nodes, a low-offset comparator demands a high power consumption. In addition, the speed is limited to the speed of the latch. In addition, a longer time is required to charge the output voltages of the preamplifier stage to a level higher than an nMOS threshold voltage. In fact, during the evaluation phase the latch stage is not activated until the output voltages of the first stage are large enough to turn on the input nMOS transistors of the latch. Unfortunately, this delay is uncontrollable and varies with the input V_{cm} of the comparator. Moreover, when the latch starts working the speed is low, since the overdrive voltage of $M_{10,11}$ is almost zero and takes time to increase.

In the conventional comparator, after a delay from the beginning of the evaluation phase, a differential voltage appears at the inputs of the latch (at O1− and O1+ nodes.). This differential voltage must be large enough to eliminate the effect of the latch on the input referred offset voltage and strongly activate the latch stage. Let us name this delay as the optimum delay. Unfortunately, in the conventional circuit the delay must be large enough to trigger the latch stage. After the optimum delay, the input common-mode voltage of the latch ($V_{cml} = 0.5 \times [V_{O1+} + V_{O1-}]$) is lower than the threshold voltage of an nMOS transistor (input transistors of the latch $M_{10,11}$). As a result, despite the fact that the preamplifier has produced adequate gain, the latch must wait until its input V_{cml} becomes large enough to activate it. Simulations reveal that the difference between the optimum and actual delays in the conventional comparator is at least 200 ps and is dependent on the input common-mode voltage of the comparator. The additional delay reduces the speed and causes more power consumption and is fixed to a value which is determined by the current of M_5 and parasitic capacitors of O1− and O1+

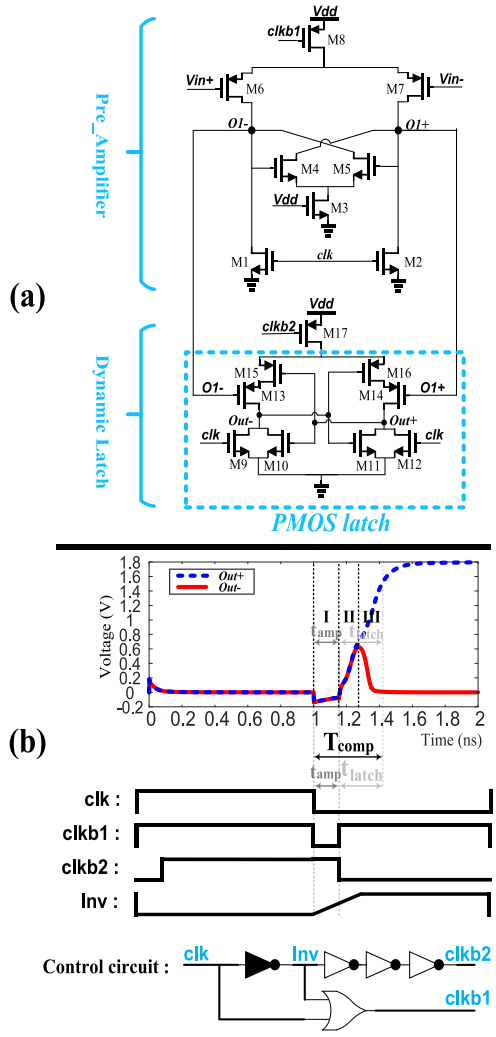

Fig. 2. (a) Proposed two-stage dynamic. (b) Its typical output waveform and clock signal.

nodes. Also, the latch starts to work weakly with a small overdrive voltage (which further cause speed reduction). The current of M_5 is determined by the power consumption and speed criteria. The parasitic capacitors at O1+ and O1− are mostly the parasitic capacitors of $M_{3,4}$ which are determined by the offset criterion. Consequently, the delay of latch stage activation is controlled by other parameters, such as offset or power, and is far away from the optimum value. With an efficient design methodology, this problem may be alleviated; however, this fundamental problem still exists.

The proposed comparator eliminates the problem inherently and efficiently makes it possible to have the optimum delay in the two-stage dynamic comparators. Therefore, it reduces the power consumption and improves the speed.

B. Proposed Comparator

The proposed comparator is shown in Fig. 2. In contrast to the conventional comparator, a pMOS latch (a latch with input pMOS transistors) is used in the latch which is activated with a predetermined delay during the evaluation phase [t_{amp}, as shown in Fig. 2(b)]. This delay is supposed to be the optimum delay. At the reset phase, the clk, clkb1, and clkb2 hold a logic "1" to discharge the output voltages of both preamplifier and latch to GND. At the evaluation phase, first the clk and clkb1 are toggled to logic "0" to start preamplification (charging the parasitic capacitors of O1+ and O1− nodes differentially). During this phase, the cross-coupled circuit increases the differential voltage ($V_{\text{idl}} = [V_{\text{O1+}} - V_{\text{O1-}}]$) slowly (since $M_{4,5}$ are mostly in subthreshold region) and reduces the common-mode voltage ($V_{\text{cml}} = 0.5 \times [V_{\text{O1+}} + V_{\text{O1-}}]$) to provide a strong drive for the input pMOS latch stage. Increasing V_{idl} (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage. Also, larger V_{idl} results in a smaller latch delay. Decreasing V_{cml} enhances the speed of the comparator, since pMOS transistors are used at the input of the latch ($M_{13,14}$). Finally, clkb2 is toggled to logic "0" to activate the latch. Simultaneously, clkb1 is changed to logic "1" to turn off the current source of the preamplifier in order to avoid excess power consumption. Amplification of V_{id} is kept going during this phase because the cross-coupled circuit is still working independently of the current source (M_8). Meanwhile, V_{cml} is kept reducing by M_{3-5}.

The control signals are implemented using a local clock generator as shown in Fig. 2(b), which consumes a small amount of power. The black inverter is designed carefully to adjust the delay. Instructively, the proposed comparator is robust against overlapped control signals, since overlapped signals only slightly affect the power consumption and have no effect on the precision.

In the proposed circuit, the delay of the evaluation-phase is long enough to achieve the minimum required preamplification gain for a given speed and latch offset elimination. Thanks to the cross-coupled circuit (M_{3-5}), during the first step of the evaluation phase, the differential voltage at O1+ and O1-nodes increases; however, the common-mode voltage of those nodes is kept low. Therefore, for a sufficient evaluation-phase delay, t_{amp}, V_{cml} ($= 0.5 \times [V_{\text{O1+}} + V_{\text{O1-}}]$) is pulled down to activate the pMOS latch strongly. Also, the larger V_{idl} boosts the latching process (speed). Consequently, the delay of the comparator will be small and almost flat over a wide range of the input V_{cm}. Transition of clkb1 to logic "1" limits the power consumption of the preamplifier which is the main part of the total power consumption. In the meanwhile, the cross-coupled circuit continues preamplification at no cost of power consumption.

As another benefit, the delay time from beginning of the evaluation phase to beginning of the latching process is simply controllable and can be tuned at its optimum value. However, in the conventional comparator, delay is inevitably fixed to the required time to charge the output parasitic capacitors of the preamplifier to the level of an nMOS voltage threshold.

The proposed structure can also be implemented using nMOS transistors, i.e., latch and preamplifier with input nMOS transistors. This will result in a higher speed because of the inherent superiority of nMOS transistors over pMOS ones. The size of $M_{4,5}$ is chosen large enough to keep the output common-mode voltage of the preamplifier small enough and increase the preamplifier differential gain.

In this paragraph, the core concept of the proposed comparator is briefly described. In the conventional comparator, if the preamplifier and the latch work in different time slots, the power consumption is improved. To do this efficiently, one way is to change the structure of the conventional comparator

from "pMOS preamp|| nMOS latch" to "pMOS preamp|| pMOS latch" (or "nMOS preamp|| nMOS latch" for a better speed). In fact, the type of both the input transistors of the preamplifier and latch must be the same in contrast to general structure of the dynamic comparators [1]–[22]. The proposed pMOS–pMOS (nMOS–nMOS) structure requires a special clocking pattern to work correctly and efficiently. We develop a low-power small-area delay-line-based controller which in addition to controlling the comparator, it makes the comparator robust against process–VDD–temperature (PVT) variations since the delay of the controller and the delay of the comparator components varies in the same direction in different PVT corners. The preamplification delay can be set to achieve the optimum delay and this delay is almost optimum in all PVT corners. In the achieved structure, Fig. 1 without the cross-coupled circuit, the optimum delay could not be realized since a larger preamplification time reduces the V_{GS} voltage of the following input pMOS transistors of the latch (worsening the speed and power). Therefore, a circuit which reduces the input common-mode voltage of the pMOS latch is needed while (at least) it keeps the differential gain untouched. The cross-coupled circuit can do this. The size of the transistors is much smaller than the size of the input transistors of the preamplifier (about 7–10 times). Therefore, the power, area, and offset contribution of the cross-coupled circuit is negligible. The cross-coupled circuit increases the differential voltage mainly when the preamplifier is turned off and enhances the speed; however, its main purpose is to reduce the input common-mode voltage of the latch.

III. Analytical Derivations

A. Delay

In this part, the speed of the proposed comparator is calculated. Also, it is proven analytically why the proposed comparator improves the speed. The comparison delay of the proposed comparator T_{comp} is a summation of two parts. The first one is t_{amp} as shown in Fig. 2(b) and is determined by the designer. The second part t_{latch} (II and III in Fig. 2) is the time that a latch needs to reach the full swing at output which depends on the input signals and transistors sizing both of the latch stage. The latch delay is defined as follows based on the analytical calculations presented in [14]:

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{\mathrm{VDD} - \mathrm{GND}}{V_{idl}}\right) \tag{1}$$

in which $\tau_{inv} = C_L/(G_{M_{pMOS}} + G_{M_{nMOS}})$ and V_{idl} is the input differential signal of the latch. As shown in Appendix I, (1) can be modified as follows to predict the delay more precisely:

$$t_{latch} = \tau_{inv} \times \ln\left(\frac{\mathrm{VDD} - \mathrm{GND}}{V_{idl}}\right) + \frac{K_{latch}}{(\mathrm{VDD} - V_{cml} - V_{thp})^2} \tag{2}$$

where V_{cml} and V_{idl} are the input common-mode and differential voltages of the latch ($V_{cml} = 0.5 \times [V_{O1+} + V_{O1-}]$, $V_{idl} = V_{O1+} - V_{O1-}$) coming from the preamplifier stage. K_{latch} is a constant depending on $M_{13,14}$ sizing and technology parameters. Equation (2) verifies that a higher V_{idl} or a lower V_{cml} results in a lower delay, since a higher V_{idl} reduces the first term and a lower V_{cml} reduces the second term. In the following parts, it is shown that higher V_{idl} and lower V_{cml} are achieved in the proposed comparator.

In the proposed circuit, the differential and common modes of V_{O1+} and V_{O1-} are dependent on the input common-mode voltage (V_{cm}) of the comparator. For example, a large input V_{cm} reduces the current of $M_{6,7}$ resulting a lower V_{cml} because of a lower charging current. To calculate the delay, V_{idl} and V_{cml} should be calculated based on the input differential voltage, common-mode voltage, and the circuit parameters. The input common-mode voltage and differential voltage of the comparator are defined as follows:

$$\begin{cases} V_{cm} = \dfrac{V_{in+} + V_{in-}}{2} \\ V_{id} = V_{in+} - V_{in-}. \end{cases} \tag{3}$$

Based on the value of V_{cm}, three different scenarios of the delay take place. First, for low values of V_{cm}, M_{6-8} work in the saturation region and the current of M_8 is partly controlled by V_{cm} because of the channel length modulation of M_8. Second, for large values of V_{cm} close to VDD, $M_{6,7}$ work in the subthreshold region and M_8 works in the deep triode region. Third, V_{cm} has a level between the two previous boundaries, $M_{6,7}$ work at the edge of saturation or subthreshold region, and M_8 works at the edge of triode or deep triode region. It is noteworthy that in all scenarios, $M_{6,7}$ do not work in the triode region (Linear region), since the nMOS cross-coupled transistors ($M_{4,5}$), keep the output voltages (V_{O1+}, V_{O1-}) well below the voltage threshold of a pMOS transistor.

Based on Appendix II, the cross-coupled circuit is modeled with two dependent current sources as shown in Fig. 3(a). M_3 works in the deep triode region and $M_{4,5}$ work in the subthreshold region. At the first scenario, the current of $M_{6,7}$ is

$$\begin{cases} I_1 = k_1(V_p - V_{in+} - V_{th})^2 \\ I_2 = k_2(V_p - V_{in-} - V_{th})^2 \end{cases} \tag{4}$$

where $k_i = 0.5\mu C_{ox}(W/L)_i$ and V_p is the drain voltage of M_8 as shown in Fig. 3(b). By subtracting the previous equations, the differential current ΔI is calculated as follows:

$$\begin{aligned} \Delta I &= I_2 - I_1 = kV_{id}(2V_p - V_{in+} - V_{in-} - 2V_{th}) \\ \Delta I &= 2kV_{id}(V_p - V_{cm} - V_{th}), \quad V_{id} = V_{in+} - V_{in-}. \end{aligned} \tag{5}$$

KCL equations at node O1+ and O− yields in the following set of equalities:

$$\begin{cases} V_{O1+} = (I_1 - \alpha V_{O1-}) \times \dfrac{t_{amp}}{C} \\ V_{O1-} = (I_2 - \alpha V_{O1+}) \times \dfrac{t_{amp}}{C}. \end{cases} \tag{6}$$

By solving this linear set of equations, V_{O1+} and V_{O1-} at the end of t_{amp} are calculated as the following equations:

$$\begin{cases} V_{O1+} = \dfrac{\left(I_1 - \alpha I_2 \frac{t_{amp}}{C}\right) \times \frac{t_{amp}}{C}}{1 - \alpha^2 \left(\frac{t_{amp}}{C}\right)^2} \\ V_{O1-} = \dfrac{\left(I_2 - \alpha I_1 \frac{t_{amp}}{C}\right) \times \frac{t_{amp}}{C}}{1 - \alpha^2 \left(\frac{t_{amp}}{C}\right)^2}. \end{cases} \tag{7}$$

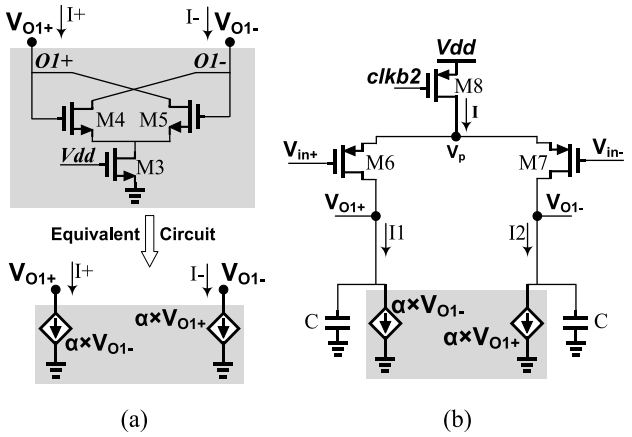

Fig. 3. (a) Equivalent circuit of the cross-coupled part. (b) Simplified circuit diagram of the preamplifier.

Consequently, V_{idl} and V_{cml} are calculated in the following equation to be used in the delay equation, i.e., (2)

$$\begin{cases} V_{\text{cml}} = \dfrac{V_{\text{O1+}} + V_{\text{O1-}}}{2} = \dfrac{I \times \frac{t_{\text{amp}}}{C}}{1 + \alpha\left(\frac{t_{\text{amp}}}{C}\right)}, \quad I = I_1 + I_2 \\ V_{\text{idl}} = V_{\text{O1+}} - V_{\text{O1-}} = \dfrac{\Delta I \times \frac{t_{\text{amp}}}{C}}{1 - \alpha\left(\frac{t_{\text{amp}}}{C}\right)}, \quad \Delta I = I_2 - I_1. \end{cases} \tag{8}$$

Let us assume that in the conventional comparator a pMOS latch (similar to Fig. 2) is used (to make an apple-to-apple comparison). It is noteworthy that the equivalent equations for such a comparator are as follows; in fact, there is no α term in the denominator:

$$\begin{cases} V_{\text{cml}} = \dfrac{V_{\text{O1+}} + V_{\text{O1-}}}{2} = \dfrac{I \times \frac{t_{\text{amp}}}{C}}{1 + 0} = \dfrac{I \times \frac{t_{\text{amp}}}{C}}{1} \\ V_{\text{idl}} = V_{\text{O1+}} - V_{\text{O1-}} = \dfrac{\Delta I \times \frac{t_{\text{amp}}}{C}}{1 - 0} = \dfrac{\Delta I \times \frac{t_{\text{amp}}}{C}}{1} \end{cases} \tag{9}$$

Compared to the proposed comparator, in that comparator, when the latch is activated, the value of V_{cml} is higher and the value of V_{idl} is lower, so the delay is worse than the proposed comparator.

In the conventional comparator, nMOS latch is used (Fig. 1) so the latch is gradually turned on (which means more delay). In fact, when the latch is turned on, the overdrive voltage of the input nMOS transistors [$M_{10,11}$ Fig. 1(a)] is low that exacerbates the delay.

As discussed earlier, in the proposed comparator thanks to the cross-coupled circuit [α term in (8)], a higher V_{idl} and a lower V_{cml} are achieved. Therefore, considering (2), the speed is improved. The amount of improvement is considerable, since both terms in (2) are reduced. As another reason for the speed improvement, in the proposed comparator, the latch starts its function strongly because of the large overdrive voltage for $M_{13,14}$ in Fig. 2 [$V_{\text{cml}} \sim 0 \Longrightarrow V_{\text{od}} \sim (\text{VDD} - V_{\text{thp}})$]. However, in the conventional comparator, at the beginning of the latching process $V_{\text{od}} \sim 0$.

At the second and third scenarios, the same procedure is used to calculate the delay. The equations will be tedious in this part; therefore, the results are presented in Appendix III.

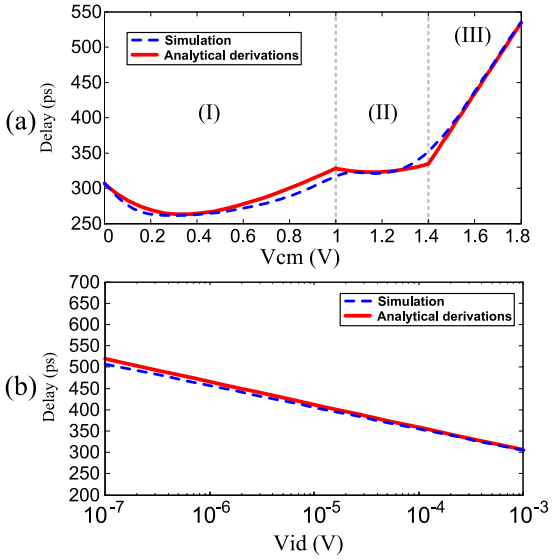

Fig. 4. (a) Delay of the proposed comparator versus input V_{cm}. (b) Delay of the proposed comparator versus input V_{id}.

In order to verify the derivations, a sample of the proposed comparator is designed in 0.18-μm CMOS technology to achieve a typical offset voltage of 2 mV. Then, the comparator delay is approximated using the delay derivations presented in (2), (3), and Appendix III. Fig. 4 presents the schematic simulation results along with the analytical derivations for all scenarios. To calculate the analytical results, first V_{idl} and V_{cml} are determined by the proposed equations [e.g., (8)], then equation (2) is used. In Fig. 4(a), the delay of the comparator with respect to the input V_{cm} is presented. Fig. 4(a) confirms the analytical derivations that predict the delay precisely. At the boundaries, the error between simulation results and analytical derivations is growing because the working region of $M_{6,7,8}$ changes smoothly in addition to α variations and increasing the effect of channel length modulation of $M_{6,7}$. Fig. 4(b) shows the delay versus V_{id} considering $V_{\text{cm}} = 1.1$ V.

B. Offset Voltage

The offset voltage is dependent on V_{cm}, since the working region of the transistors changes and the nonideal effects such as channel length modulation alters the effect of mismatch of each component on the differential gain. The offset voltage of the comparator is calculated analytically for V_{cm} less than VDD/2, where $M_{6,7,8}$ work in the saturation region and the channel length modulation of $M_{6,7}$ is negligible. In order to propose a closed-form equation, we neglect the effect of the latch on the offset voltage (which is satisfied in a good design). As discussed earlier, in a good design the sizing of the input transistors ($M_{6,7}$) for high-resolution applications are chosen large enough to eliminate the effect of the latch stage on the input referred offset voltage.

Technically, the input referred dynamic offset is the input differential voltage ($V_{\text{in+}} - V_{\text{in-}}$) that establishes equal voltage at the O1+ and O1− nodes at the end of the preamplification phase (t_{amp}). The current of $M_{6,7}$ [Fig. 3(b)] and the difference between them are calculated as follows by taking into account

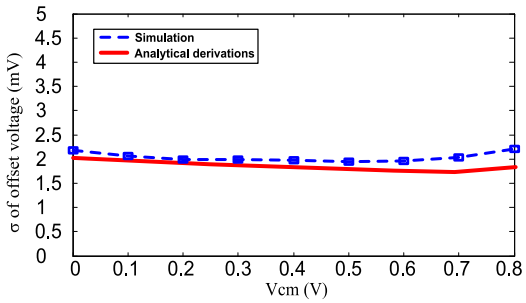

Fig. 5. Schematic and analytical simulation results of offset voltage versus $V_{\rm cm}$.

the effect of mismatch:

$$\begin{cases} I_1 = k(V_p - V_{\rm in+} - V_{\rm th})^2 \\ I_2 = (k+\Delta k)(V_p - V_{\rm in-} - V_{\rm th} - \Delta V_{\rm th})^2 \end{cases} \tag{10}$$

$$\begin{aligned} \Delta I &= (I_2 - I_1) = 2k(V_{\rm in+} - V_{\rm in-} - \Delta V_{\rm th})(V_p - V_{\rm th} - V_{\rm cm} - \Delta V_{\rm th}) \\ &\quad + \Delta k(V_p - V_{\rm in-} - V_{\rm th} - \Delta V_{\rm th})^2 \\ &\Rightarrow \Delta I \cong V_{\rm os}(g_m - 2k\Delta V_{\rm th}) - g_m \Delta V_{\rm th} \\ &\quad + \Delta k(V_p - V_{\rm th} - \Delta V_{\rm th} + 0.5 \times V_{\rm os} - V_{\rm cm}).^2 \end{aligned} \tag{11}$$

Employing KCL at O1+ and O1− nodes yields the following equations for $V_{\rm O1+}$ and $V_{\rm O1-}$:

$$\begin{cases} V_{\rm O1+} = \dfrac{\left(I_1 - \alpha I_2 \left(\frac{t_{\rm amp}}{C}\right)\right)\left(\frac{t_{\rm amp}}{C}\right)}{1 - \alpha\,(\alpha+\Delta\alpha)\left(\frac{t_{\rm amp}}{C}\right)^2} \\ V_{\rm O1-} = \dfrac{\left(I_2 - (\alpha+\Delta\alpha) I_1 \left(\frac{t_{\rm amp}}{C}\right)\right)\left(\frac{t_{\rm amp}}{C}\right)}{1 - \alpha\,(\alpha+\Delta\alpha)\left(\frac{t_{\rm amp}}{C}\right)^2}. \end{cases} \tag{12}$$

Based on the definition of the offset voltage, if an input differential voltage as large as $V_{\rm os}$ is applied to the comparator, $V_{\rm O1+}$ will be equal to $V_{\rm O1-}$ after the amplification time ($t_{\rm amp}$). Therefore, by solving the equation $V_{\rm O1+} = V_{\rm O1-}$ and substituting (11), the offset voltage is calculated in (13), shown at the bottom of this page.

Fig. 5 presents the simulation results of the offset voltage for the proposed comparator. In Fig. 5, the offset voltage versus $V_{\rm cm}$ is shown considering 1 k-points Spectre Monte Carlo simulations (using 0.18-μm technology) and 100 k-points MATLAB Monte Carlo simulations using (13).

IV. Noise

In two-stage dynamic comparators, the offset voltage and similarly the input referred noise is mainly dominated by the preamplifier stage. Using the proposed technique, both input nMOS and input pMOS preamplifiers can be used; their structures are similar to the conventional counterparts [neglecting the cross-coupled circuit Fig. 3(a)]. As a result, we expect an almost equal input referred noise. In the proposed comparator, the cross-coupled circuit increases both the noise and the preamplification gain. On the other hand, the cross-coupled circuit keeps the output voltages of the preamplifier stage low so it keeps the preamplifier input transistors in the saturation region. This is in contrast to the conventional comparator where the input transistors go to the triode region during preamplification exacerbating the input noise (gain $\downarrow \Rightarrow V_{\rm noise\text{-}in} \uparrow$). Assuming all above, the first effect increases the input noise while the second one reduces the input noise. Therefore, totally, it is expected that the input noise of the proposed comparator will be almost the same as the conventional comparator. In Section VI, multiple transient noise simulations prove this inspection.

TABLE I
Parameters of the Controller in Different Corners

VDD = 1.6V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	Ss	tt	ff	ss	tt	ff
Delay (ps)	230	175	133	246	185	140	270	201	152
Power (uW)	15	16	19	16	17	20	16	17	21
VDD = 1.8V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	186	146	148	198	155	121	179	170	132
Power (uW)	20	22	26	21	23	27	22	24	27
VDD = 2V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	156	126	102	166	134	108	183	146	117
Power (uW)	26	29	33	27	30	34	28	31	35

V. Delay-Line-Based Controller

Fig. 2(b) presents the controller and the voltage waveforms. The circuit was designed to produce 150-ps delay for the proposed comparator. The circuit consumes about 20 μw which is negligible compared to the total power consumption. To be sure about the behavior of this circuit, different PVT corners was considered. Table 1 presents the results. As can be seen, the power consumption remains acceptable for different corners compared to the total power consumption of about 210 μW. Naturally, the delay varies in different corners which is favorable for the comparator, since it is consistent with the delay variations of the comparator (which is toward the same direction in different corners). In fact, the proposed controller employs an inherent self-adjusting mechanism. The 10 k-points Monte Carlo simulations reveal that the σ of $t_{\rm amp}$ variations due to transistors mismatch is 5 ps, which is only 3% of the total 150-ps delay. The PVT and Monte Carlo simulations confirm the validity and efficiency of the controller.

$$V_{\rm OS} = \frac{[g_m \Delta V_{\rm th} + \Delta k(V_p - V_{\rm th} - \Delta V_{\rm th})^2 + 2V_{\rm cm}\Delta k(V_p - V_{\rm th} - \Delta V_{\rm th})^2 - V_{\rm cm}^2]}{(g_m - 2k\Delta V_{\rm th} + \Delta k(V_p - V_{\rm th} - \Delta V_{\rm th})^2 - V_{\rm cm})} + \frac{-\frac{\Delta\alpha}{2}\left(\frac{t_{\rm amp}}{C}\right) I}{(g_m - 2k\Delta V_{\rm th} + \Delta k\left(V_p - V_{\rm th} - \Delta V_{\rm th}\right)^2 - V_{\rm cm})\left(1 + \left(\alpha + \frac{\Delta\alpha}{2}\right)\left(\frac{t_{\rm amp}}{C}\right)\right)} \tag{13}$$

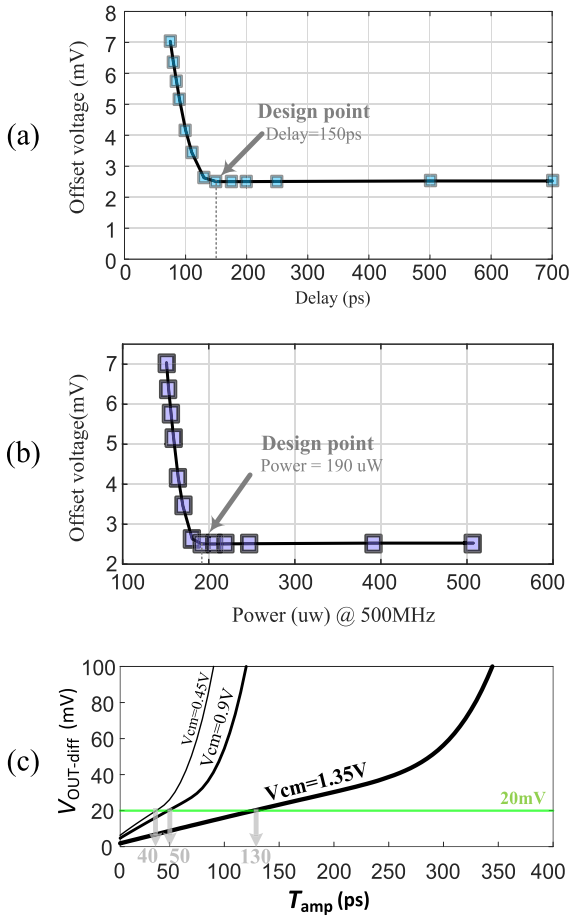

Fig. 6. Offset voltage of the proposed comparator versus (a) delay and (b) power (at 500 MHz) originated from different delay values. (c) Output differential voltage of the preamplifier at $t = t_{amp}$.

VI. Simulation Results and Comparison

Dynamic comparators are technology dependent since they suffer from both analog and digital nonidealities. Therefore, to make a fair comparison, the proposed and some previously published comparators were carefully designed using the same 0.18-μm CMOS technology. The comparators were designed for a typical offset voltage of 2 mV. The offset voltage of the proposed comparator is dependent on t_{amp}. Fig. 6(a) and (b) presents the offset voltage of the proposed comparator versus t_{amp} and versus power consumption originated from different values of t_{amp}. Obviously, $t_{amp} = 150$ ps is the optimum design point. Usually, in charge redistribution DACs, the output common-mode voltage of the DAC is in the range of 0.25–0.75 VDD [18]–[20]. Fig. 6(c) presents the output differential voltage of the preamplifier for the mentioned V_{cm} range. The σ of offset voltage of the latch is about 7 mV. Therefore, 20 mV ($\sim 3\sigma$) differential voltage is large enough to eliminate the effect of the latch on the input referred offset voltage. As can be seen, for the mentioned V_{cm} range (0.25–0.75 VDD) 130 ps preamplification time is the minimum required t_{amp}. The worst case happens for larger values of V_{cm}. In fact, the upper bound of input V_{cm} determines the minimum t_{amp}. This is consistent with the 150-ps delay originated form Fig. 6(a). Both Fig. 6(a) and (c) can be used to determine the optimum delay, i.e., t_{amp}. Based on Fig. 6(a) and (c), it is guaranteed that the offset voltage of the proposed comparator

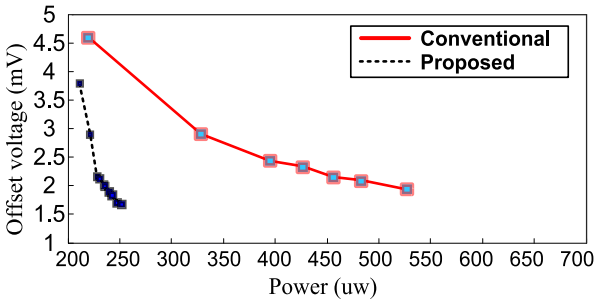

Fig. 7. Offset voltage versus power consumption for the proposed and the conventional comparators.

for the V_{cm} range of 0.25–0.75 VDD is less than 2 mV. However, the proposed comparator operates in the whole range of V_{cm} (0–VDD) with smaller offset for lower V_{cm}s and larger offset for higher V_{cm}s, although pMOS transistors are used at the input.

To design the proposed comparator, first, a two-stage dynamic comparator (e.g., the conventional or the ones reported in [8]–[10]) is designed using its own design procedure. Then, the latch of the designed comparator is replaced with its inverted type (n-type $\rightarrow$ p-type or *vice versa*) and one pMOS (or nMOS for n-type latch) transistor is added in series to the latch [similar to M_{17} in Fig. 2(a)]. The cross-coupled circuit with the size of 5%–15% of the input transistors is added to the preamplifier. At this step, the optimum preamplification delay is obtained using the methods of Fig. 6. Next, the controller of Fig. 2(b) is designed to produce the optimum delay and finalize the design procedure. One efficient method to design this controller is to use minimum size transistors for all the gates except the black one; the W and the L of the black inverter is set to achieve the optimum delay.

Testing different transistors sizing and measuring the offset voltage yield in Fig. 7. Based on Fig. 7, the proposed comparator offers a lower power compared to the conventional comparator for the same offset voltage.

The preamplifier gain increases with an increase in t_{amp} and the effect of the latch stage on the input referred offset voltage reduces. A 150-ps preamplification time is large enough to eliminate the effect of the latch stage significantly.

Fig. 8(a) presents the delay of proposed, conventional, and some recently reported comparators versus V_{id}. For those methods in which nMOS and pMOS transistors are used as the input transistors of the preamplifier stage, V_{cm} was considered to be 0.7 and 1.1 V, respectively. The proposed comparator is faster than the other ones by more than 150 ps. Assuming the delay equation of (2) ($T_d = \tau \times \ln(\text{VDD}/V_{id}) + t_0)\tau$ is almost equal in all comparators for mentioned V_{cm} [equal slopes in Fig. 8(a)] since all of the comparators employ the same latch structure (back-to-back inverter). However, t_0 is better in the proposed comparator due to its special structure.

Fig. 8(b) presents the delay versus V_{cm} assuming that $V_{id} = 1$ mV. The proposed circuit provides the lowest delay among the comparators in addition to a rail-to-rail input common-mode range for the clock frequency of 500 MHz. Moreover, it proposes an almost constant delay for a large V_{cm} range of 0–1 V. Fig. 9 presents the output voltage of the latch stage for the comparators. Obviously, the proposed circuit is faster than other methods.

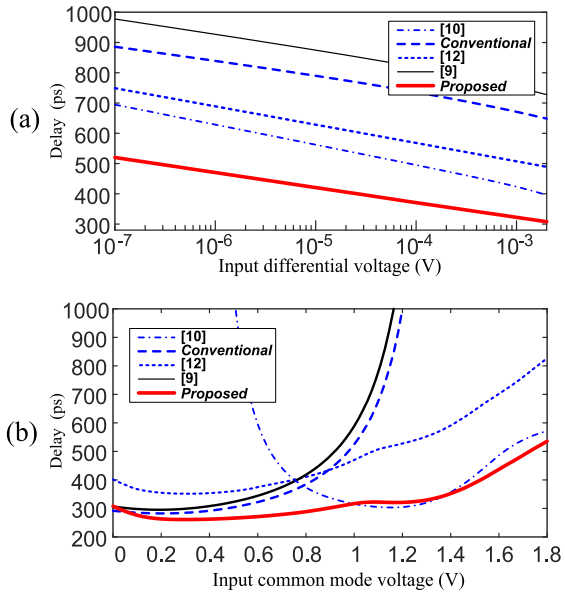

Fig. 8. (a) Delay versus V_{id} considering $V_{cm} = 0.7, 1.1$ for nMOS input and pMOS input comparators. (b) Delay versus V_{cm} considering $V_{id} = 1$ mV.

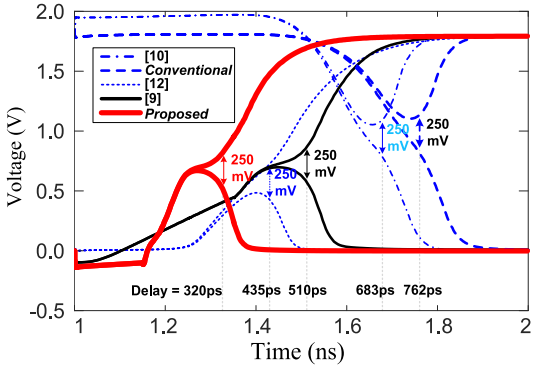

Fig. 9. Output waveforms of the proposed, conventional, and some other comparators.

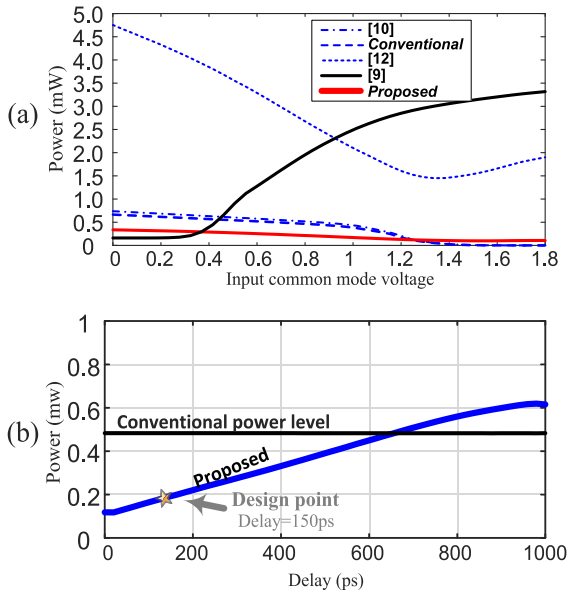

Fig. 10. (a) Power consumption of comparators versus input V_{cm}. (b) Power consumption of the proposed comparator versus t_{amp}, $V_{cm} = 1.1$ V.

TABLE II

COMPARISON BETWEEN THE COMPARATORS BASED ON THE AUTHOR SIMULATIONS ($\sigma_{offset} = 2$ mV)

	Conventional	[9]	[10]	[12]	Proposed
Average power at 500MHz	0.48 mW	0.44 mW	2.3 mW	2.75 mW	0.20 mW
Estimated area (μm^2)	440	370	580	1100	490
Delay	301 ps	303 ps	313 ps	370 ps	263 ps
V_{cm} range at 500MHz	64% VDD	66% VDD	71% VDD	100% VDD	100% VDD
$\sigma V_{noise-in}$	24.6uV	28.4uV	34.2uV	65.5uV	28.6uV

Fig. 10(a) presents the power consumption versus V_{cm} at the clock frequency of 500 MHz. The output voltage swing of the preamplifier at the end of t_{amp} is larger for a lower input V_{cm}; as a result, the power consumption is higher for a lower V_{cm} Neglecting the power consumption of the latch, the total power consumption is calculated as

$$\text{Power} = \frac{1}{T}\int_0^{T=T_{clk}/2} v(t)\cdot i(t)dt + P_{latch} = \frac{1}{T}\int_0^{t_{amp}} \text{VDD}\cdot(I_1+I_2)dt + P_{latch} \cong \frac{t_{amp}}{T}\text{VDD}\times I_{M8}. \quad (14)$$

$T_{clk}/2$ is replaced with t_{amp}, since only during t_{amp} the preamplifier draws power from the supply voltage. By increasing t_{amp}, the power consumption increases linearly. Fig. 10(b) presents the power consumption versus delay for $V_{cm} = 1.1$ V. The conventional power level is fixed, since in the conventional comparator, the preamplification delay is fixed to $T_{clk}/2$. As expected, in the proposed comparator, the power consumption has a linear relationship with t_{amp}. In the sample designed comparator, t_{amp} is chosen 150 ps which offers very low power consumption while it is large enough to eliminate the effect of the latch stage on the offset voltage. If the delay is chosen 600 ps, the power of the proposed comparator is the same as that in the conventional one. Thus, here, the difference between the actual and ideal delay is about 450 ps. In the conventional comparator, for about 450 ps, time and preamplifier power are wasted.

Table II compares the proposed and some comparators which are designed using the same technology (0.18 μm) and offset voltage (~2 mV). The maximum frequency is calculated using Fig. 8, and the power consumption is the average power over the input V_{cm} range of each comparator. The proposed comparator presents a higher speed and a higher input V_{cm} range with lower power consumption. The area overhead is negligible. The last row of Table II presents the input noise of the comparators. As discussed in the noise section, the input referred noise of the proposed comparator is almost the same as the other ones. The dynamic noise is negligible compared to the offset voltage. Totally, the proposed comparator is a good candidate for low-power high-speed high-resolution ADCs.

A. Corner Simulations

In order to confirm the benefits of the proposed comparator, the designed comparator was tested under different process

TABLE III

PARAMETERS OF THE COMPARATOR IN DIFFERENT CORNERS CONSIDERING THE IDEAL AND PROPOSED CONTROLLERS ($V_{cm} = V_{ref}/2$)

VDD = 1.6V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	Ss	tt	ff
Delay (ps)	524 636	435 458	342 344	537 652	437 478	338 361	551 665	438 512	335 387
σV_{offset} (mV)	2.07 2.29	2.06 2.04	2.05 2.06	2.04 2.17	2.05 2.08	2.06 2.06	2.04 2.10	2.04 2.15	2.06 2.09
Power @500MHz (uW)	108 126	128 136	168 151	113 134	135 143	173 158	120 144	143 153	180 170
$\sigma V_{noise\text{-}in}$ (uV)	23 27	26 27	24 24	24 26	28 26	25 25	25 30	29 30	27 28
VDD = 1.8V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	Ss	tt	ff
Delay (ps)	394 492	332 360	303 297	400 519	324 381	299 309	408 562	319 402	307 326
σV_{offset} (mV)	2.07 2.06	2.04 2.04	2.15 2.12	2.06 2.05	2.05 2.05	2.14 2.13	2.06 2.06	2.08 2.10	2.14 2.09
Power @500MHz (uW)	194 190	237 202	298 220	199 200	240 211	299 228	204 214	244 224	301 240
$\sigma V_{noise\text{-}in}$ (uV)	23 27	25 27	23 24	23 28	26 28	22 26	29 27	29 27	25 26
VDD = 2V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	317 416	307 328	296 253	322 440	302 340	293 262	332 468	299 259	292 278
σV_{offset} (mV)	2.06 2.08	2.06 2.11	2.17 2.19	2.07 2.10	2.07 2.10	2.18 2.18	2.07 2.10	2.14 2.12	2.18 2.17
Power @500MHz (uW)	314 261	374 277	457 296	314 272	377 287	463 305	315 289	378 303	468 320
$\sigma V_{noise\text{-}in}$ (uV)	25 26	23 26	25 23	26 28	22 28	25 23	30 27	26 27	24 22

(ss, tt, and ff), voltage (1.6, 1.8, and 2 V), and temperature (0°, 27°, and 70 °C) corners (PVT corners). Table III presents the results for 27 different corners ($3^3 = 27$). In each cell of Table III, the top numbers represent the results considering an ideal controller (fixed 150-ps delay), while the down number is for the proposed controller [Fig. 2(b)]. As can be seen, the offset voltage remains about 2 mV in different corners, since the proposed controller somehow self-adjust the comparator. In fact, whenever the delay is low (e.g., VDD = 2 V, *ff* in 0 °C) the delay-line-based controller is fast forcing the comparator to work correctly. On the contrary, if the delay is high (e.g., VDD = 1.6 V, *ss* in 70 °C) the delay-line-based controller is slow letting the comparator work correctly. As a result, the delay-line-based controller serves the comparator as a self-adjusting clock generator. The delay naturally reduces or increases in different corners. The power consumption for the case of the proposed controller (the down numbers) varies only with VDD variations. In fact, in different process and temperature corners the power consumption almost remains constant. In the case of an ideal controller, however, the power changes significantly (due to the current variation of the preamplifier and a fix t_{amp}).

Consequently, the simulation results in different PVT corners prove the efficiency of the proposed comparator and the delay-line-based controller. Moreover, Table III shows that employing the proposed delay-line-based controller is more efficient than using a fixed-delay (process-independent) controller.

VII. MEASUREMENT

In order to verify the low-power benefit of the proposed comparator, the sample comparator (discussed in Section VI)

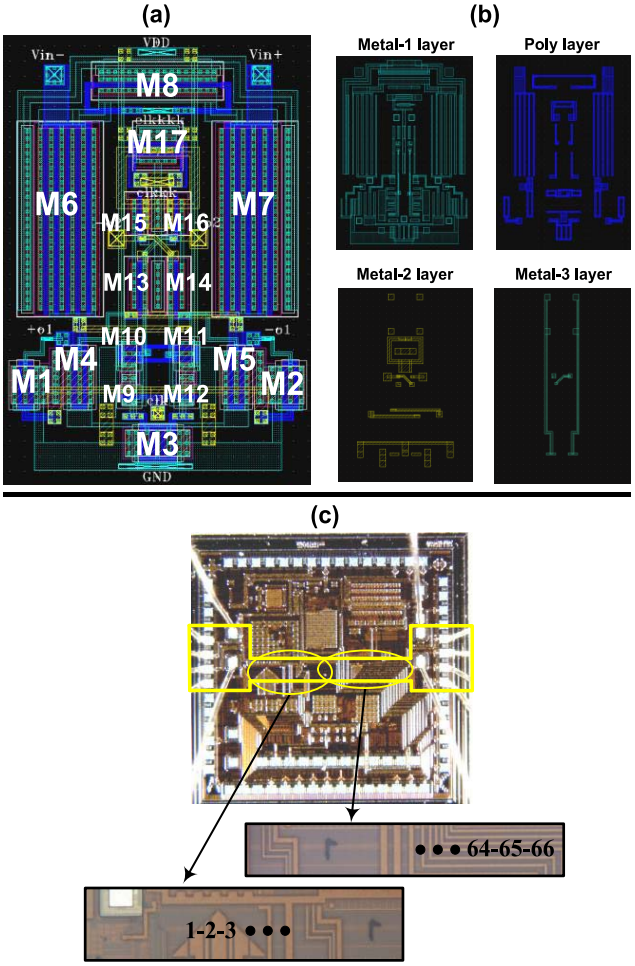

Fig. 11. (a) Symmetric layout of the proposed comparator. (b) Different layers of the layout. (c) Die micrograph.

TABLE IV

COMPARISON BETWEEN THE PROPOSED AND OTHER COMPARATORS

	[11]	[9]	[10]	[12]	Proposed
Operating frequency	-	33 MHz	1 GHz	0.9 GHz *	0.5 GHz
Offset voltage	7.78mV*	56 uV	5.62mV*	16.5 mV*	2 mV*
Area (μm^2)	-	64000	-	260*	530
Power in operating frequency	600 uW*	766 uW	-	51 uW*	230 uW
$V_{cm\text{-}in}$ range ($\times VDD$)	63 %*	66 %	71 %	100 %*	100 %
Technology	130 nm	0.5 um	90 nm	90 nm	0.18 um

* These values are from simulations.

was fabricated using CMOS 0.18-μm technology. Fig. 11(a) shows the layout of the circuit. In order to avoid the static offset voltage caused by the load capacitors mismatch, the circuit was laid out in a fully symmetric fashion. In Fig. 11(a), all transistors are labeled with their name as depicted in Fig. 2. Fig. 11(b) presents the wiring of the layers. Fig. 11(c) depicts the die micrograph. To calculate the power consumption accurately, 66 comparators were fabricated. Fig. 12(a) presents the power consumption versus input V_{cm}. The average power consumption is less than 250 μW for 500-MHz clock frequency. In Fig. 12(a), power consumption versus input frequency is presented. The proposed comparators offer a

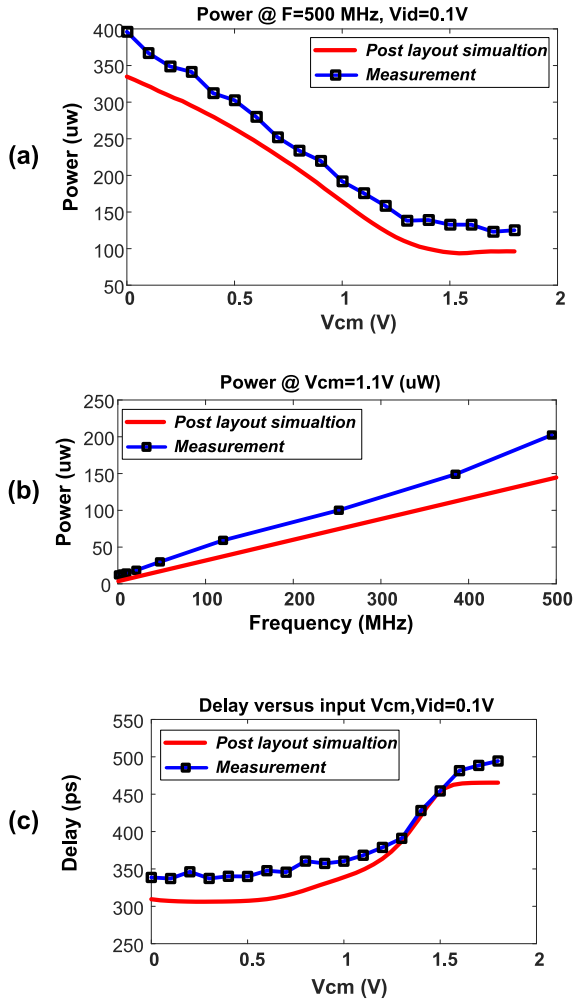

Fig. 12. (a) Power versus input V_{cm}. (b) Power versus clock frequency. (c) Delay versus input V_{cm}.

low power consumption in different frequencies. Fig. 12(c) presents the delay versus input V_{cm}. The delay is less than 500 ps for the whole range of V_{cm}. Table IV presents the comparison between the proposed and other comparators. The proposed comparator offers a low power behavior with a low offset voltage while having an input V_{cm} range of 0–VDD. This feature enables the comparator to be used followed by low-power components with a rail-to-rail output V_{cm} range such as the ultralow-power capacitive DACs reported in [16] and [17].

VIII. Conclusion

In the proposed comparator, pMOS latch and pMOS preamplifier in addition to a small cross-coupled circuit are used with a special clocking pattern to adjust the preamplifier gain. The clocking pattern provides enough preamplifier gain; since pMOS transistors are used at the input of the latch, and the cross-coupled circuit is employed to keep the common-mode voltage of the preamplifier outputs at a low level. As a result, the speed of the comparator is increased and is constantly high for a wide input V_{cm} range [Fig. 12(c)]. Deactivating the preamplifier after the optimum delay reduces the power consumption significantly. Therefore, the proposed

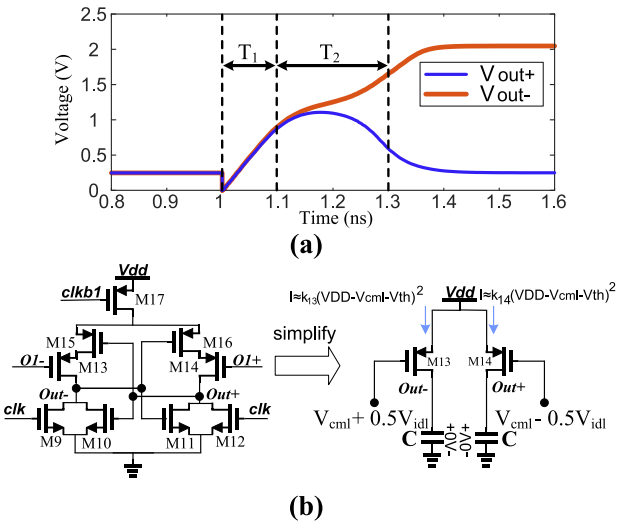

Fig. 13. (a) Typical output waveform of the pMOS latch. (b) Simplified circuit diagram of the latch right after beginning the latching process.

circuit is a low-offset low-power high-speed comparator which works at a wide input common-mode voltage range. Analytical modeling, PVT corner, and post layout simulations along with silicon measurements prove the benefits of the proposed comparator.

Appendix I

Fig. 13(a) presents a typical output waveform of a pMOS latch. As shown in Fig. 13(a), the delay of the latch can be divided into two parts. First, the voltage of the output nodes is charged from Gnd to V_{thn} with almost the same rate considering a small differential voltage at the input (since V_{idl} at the output of the preamplifier is small). Then the nMOS transistors are turned on and the back-to-back inverter starts to lock based on its input differential signal. Equation (1) presents an approximation of the second delay. The first delay is calculated as follows. When the latch is in a comparator circuit, the signal at the both outputs of the preamplifier is assumed to be V_{cml} neglecting the differential voltage. In this case, when the latch is activated M_{15-17} are deeply triode, M_{9-12} are OFF and $M_{13,14}$ work in the saturated region. Therefore, the equivalent circuit of Fig. 13(b) is obtained. If a capacitor is charged using a dc current source, the voltage of the capacitor is calculated as follows:

$$V_c(t) = \frac{I}{C}t \tag{15}$$

$$T_1 = \frac{C}{I} \times \Delta V = \frac{C}{k_{13,14}\left(\mathrm{VDD} - V_{cml} - V_{thp}\right)^2} \times V_{thn}. \tag{16}$$

T_2 is a constant delay and is referred to as the regeneration time of the back-to-back inverter.

Appendix II

Considering Fig. 3(a), the gate of $M_3$is connected to VDD and the common-mode voltage of O1+ and O1− nodes during comparison are typically less than 0.4 V for different values of input V_{cm} of the comparator. Therefore, M_3 is deeply triode

and the voltage of the source pins of $M_{4,5}$ is almost GND. $M_{4,5}$ works in the subthreshold region. Then, we have

$$I_+ = I_{D0}e^{\left(\frac{V_{\mathrm{O1}-}-V_{\mathrm{th}}}{\eta V_T}\right)}\left(1-e^{\left(\frac{-V_{\mathrm{O1}+}}{V_T}\right)}\right) \times e^{\left(\frac{-V_{\mathrm{O1}+}}{V_T}\right)} < 0.1 \text{ for } V_{\mathrm{O1}+} > 50 \text{ mV} \quad (17)$$

$$\rightarrow I_+ \cong I_{D0}e^{\left(\frac{V_{\mathrm{O1}-}+V_{\mathrm{th}}}{\eta V_T}\right)} = I_{D0}e^{\left(\frac{V_{\mathrm{th}}}{\eta V_T}\right)}e^{\left(\frac{V_{\mathrm{O1}-}}{\eta V_T}\right)} = I'_{D0}e^{\left(\frac{V_{\mathrm{O1}-}}{\eta V_T}\right)} = I'_{D0}\left(1+\frac{V_{\mathrm{O1}-}}{\eta V_T}\right) \quad (18)$$

$$\rightarrow I_+ \cong I'_{D0}\left(1+\frac{V_{\mathrm{O1}-}}{\eta V_T}\right) = I'_{D0}+\frac{V_{\mathrm{O1}-}}{\eta V_T} = I_0+\frac{I_0}{\eta V_T}V_{\mathrm{O1}-}. \quad (19)$$

For I_- on the other side of the comparator, we have the same derivations

$$I_- \cong I'_{D0}\left(1+\frac{V_{\mathrm{O1}+}}{\eta V_T}\right) = I'_{D0}+\frac{V_{\mathrm{O1}+}}{\eta V_T} = I_0+\frac{I_0}{\eta V_T}V_{\mathrm{O1}+}. \quad (20)$$

I_0 has a common-mode effect in lowering $V_{\mathrm{O1}+}$ and $V_{\mathrm{O1}-}$; therefore, it has no effect on the input differential voltage of the latch (V_{idl}). On the other hand, the effect of I_0 on the input common-mode voltage of the latch (V_{cml}) is negligible compared to $(I_0/\eta V_T)V_{\mathrm{O1}+}$, since $(1/\eta V_T) \cong 32$ (for typical parameters in room temperature). Moreover, the current coming from the input pMOS transistors of the preamplifier stage dominates I_0. Consequently, I_- and I_+ are approximated by

$$\begin{cases} \mathrm{I}_+ \cong \dfrac{I_0}{\eta V_T}V_{\mathrm{O1}-} = \alpha V_{\mathrm{O1}-} \\ \mathrm{I}_- \cong \dfrac{I_0}{\eta V_T}V_{\mathrm{O1}+} = \alpha V_{\mathrm{O1}+}. \end{cases} \quad (21)$$

Appendix III

At the second scenario, $M_{6,7}$ are in the subthreshold region and M_8 is completely triode. Therefore, V_p is almost VDD and the current of $M_{6,7}$ is calculated as follows for the subthreshold region, considering a first-order approximation of the effect of drain–source voltage $(1-e^{(-V_{\mathrm{DS}}/V_T)} = (V_{DS}/V_T))$ [15]:

$$\begin{cases} I_1 = I_0e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}+}}{\eta V_T}\right)}\left(\dfrac{1}{V_T}[\mathrm{VDD}-V_{\mathrm{O1}+}]\right) \\ \quad = \dfrac{I_0}{V_T}e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}+}}{\eta V_T}\right)}(\mathrm{VDD}-V_{\mathrm{O1}+}) \\ I_2 = I_0e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}-}}{\eta V_T}\right)}\left(\dfrac{1}{V_T}[\mathrm{VDD}-V_{\mathrm{O1}-}]\right) \\ \quad = \dfrac{I_0}{V_T}e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}-}}{\eta V_T}\right)}(\mathrm{VDD}-V_{\mathrm{O1}-}). \end{cases} \quad (22)$$

Equation (22) is simplified to

$$\begin{cases} I_1 = A_1(\mathrm{VDD}-V_{\mathrm{O1}+}), \quad A_1 = \dfrac{I_0}{V_T}e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}+}}{\eta V_T}\right)} \\ I_2 = A_2(\mathrm{VDD}-V_{\mathrm{O1}-}), \quad A_2 = \dfrac{I_0}{V_T}e^{\left(\frac{\mathrm{VDD}-V_{\mathrm{in}-}}{\eta V_T}\right)}. \end{cases} \quad (23)$$

O1+ and O1− nodes are being charged with I_1 and I_2 then the following equations hold:

$$\begin{cases} I_1 = C\dfrac{dV_{\mathrm{O1}+}}{dt}+\alpha V_{\mathrm{O1}-} \\ I_2 = C\dfrac{dV_{\mathrm{O1}-}}{dt}+\alpha V_{\mathrm{O1}+} \end{cases} \Rightarrow \begin{cases} C\dfrac{dV_{\mathrm{O1}+}}{dt}+\alpha V_{\mathrm{O1}-} = A_1\mathrm{VDD}-A_1V_{\mathrm{O1}+} \\ C\dfrac{dV_{\mathrm{O1}-}}{dt}+\alpha V_{\mathrm{O1}+} = A_2\mathrm{VDD}-A_2V_{\mathrm{O1}-}. \end{cases} \quad (24)$$

The solution of the above set of linear differential equations for $t \geq 0$ is

$$\begin{cases} V_{\mathrm{O1}+}(t) \\ = \dfrac{m_{2,1}}{C^2m_4}\left(-1+\cosh(m_1t)-\dfrac{C}{m_1}\sinh\left(\dfrac{m_1t}{C}\right)\left(m_3-\dfrac{m_{5,1}}{m_{2,1}}\right)\right) \\ V_{\mathrm{O1}+}(t) \\ = \dfrac{m_{2,2}}{C^2m_4}\left(-1+\cosh(m_1t)-\dfrac{C}{m_1}\sinh\left(\dfrac{m_1t}{C}\right)\left(m_3-\dfrac{m_{5,2}}{m_{2,2}}\right)\right) \end{cases} \quad (25)$$

where m_{1-4} coefficients are defined as follows:

$$\begin{cases} m_1 = \dfrac{1}{C}\sqrt{\dfrac{1}{4}(A_1-A_2)^2+a^2} \\ m_{2,1} = A_2C^2\times\mathrm{VDD}(A_1-\alpha) \\ m_{2,2} = A_1C^2\times\mathrm{VDD}(A_2-\alpha) \\ m_3 = \dfrac{1}{2C}(A_1+A_2) \\ m_4 = \alpha^2-A_1A_2 \end{cases} \quad (26)$$

$m_{5,1}$, and $m_{5,2}$ are defined as follows:

$$\begin{cases} m_{5,1} = C\times\mathrm{VDD}\left(-A_2^2\alpha+A_1A_2^2-A_1A_2\alpha+A_1\alpha^2\right) \\ m_{5,2} = C\times\mathrm{VDD}\left(-A_1^2\alpha+A_2A_1^2-A_2A_1\alpha+A_2\alpha^2\right). \end{cases} \quad (27)$$

As excepted, $V_{\mathrm{O1}+}(0^+) = V_{\mathrm{O1}-}(0^+) = 0$, since the following equations hold:

$$\mathrm{const}\times(-1+\cosh(0^+)-\mathrm{const}\times\sinh(0^+)) = \mathrm{const}\times(-1+1) = \mathrm{const}\times 0 = 0. \quad (28)$$

Equation (25) derivations are evaluated at $t = t_{\mathrm{amp}}$, then $V_{\mathrm{O1}+}$ and $V_{\mathrm{O1}-}$ are used in the following equation to predict the delay using (2):

$$\begin{cases} V_{\mathrm{cml}} = \dfrac{V_{\mathrm{O1}+}(t_{\mathrm{amp}})+V_{\mathrm{O1}-}(t_{\mathrm{amp}})}{2} \\ V_{\mathrm{idl}} = V_{\mathrm{O1}+}(t_{\mathrm{amp}})-V_{\mathrm{O1}-}(t_{\mathrm{amp}}). \end{cases} \quad (29)$$

At the third scenario, $M_{6,7}$ working region is between saturation and subthreshold region and M_8 almost operates in the triode region. V_p is highly dependent on V_{cm} and the channel length modulation effect of $M_{6,7}$ becomes important. The analytical calculations of this scenario lead to an extensive, yet straightforward derivations which is beyond the length of

this paper. Therefore, just the results are reported

$$\begin{cases} V_{\text{cml}} = \dfrac{V_{\text{O1+}} + V_{\text{O1-}}}{2} \\ \qquad = \dfrac{B\left(2A\frac{1}{V_T}D - \alpha D - A\alpha\right)\left(\frac{t_{\text{amp}}}{C}\right)^2 + B\,(A+D)\left(\frac{t_{\text{amp}}}{C}\right)}{2\left[\left(A\left(\frac{1}{V_T}\right)^2 D - \alpha^2\right)\left(\frac{t_{\text{amp}}}{C}\right)^2 + \frac{1}{V_T}\,(A+D)\left(\frac{t_{\text{amp}}}{C}\right) + 1\right]} \\ V_{\text{idl}} = V_{\text{O1+}} - V_{\text{O1-}} \\ \qquad = \dfrac{B\,(A-D)\left(\frac{t_{\text{amp}}}{C}\right)\left(\alpha\left(\frac{t_{\text{amp}}}{C}\right) + 1\right)}{\left(A\left(\frac{1}{V_T}\right)^2 D - \alpha^2\right)\left(\frac{t_{\text{amp}}}{C}\right)^2 + \frac{1}{V_T}\,(A+D)\left(\frac{t_{\text{amp}}}{C}\right) + 1} \end{cases} \tag{30}$$

where A, B, and D are defined as

$$\begin{cases} A = I_0 e^{\left(\frac{\text{VDD}-V_{\text{in+}}}{\eta V_T}\right)} \\ B = \dfrac{1}{V_T} \times \text{VDD} \\ D = I_0 e^{\left(\frac{\text{VDD}-V_{\text{in-}}}{\eta V_T}\right)} \end{cases} \tag{31}$$

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