An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor

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***Abstract*—Harvesting ambient vibration energy through piezoelectric means is a popular energy harvesting technique which can potentially supply 10–100's of μW of available power. One of the main limitations of existing piezoelectric harvesters is in their interface circuitry. In this paper, a bias-flip rectifier circuit that can improve the power extraction capability from piezoelectric harvesters over conventional full-bridge rectifiers and voltage doublers by greater than 4X is implemented in a 0.35 μm CMOS process. An efficient control circuit to regulate the output voltage of the rectifier and recharge a storage capacitor is presented. The inductor used within the bias-flip rectifier is shared efficiently with a multitude of switching DC-DC converters within the system reducing the overall component count.**

***Index Terms*—Bias-flip rectifier, DC-DC converter, full-bridge rectifier, inductor sharing, micropower, piezoelectric harvester.**

I. Introduction

With the need for portable and lightweight electronic devices on the rise, highly efficient power generation approaches are a necessity. The dependence on the battery as the only power source is putting an enormous burden in applications where either due to size, weight, safety or lifetime constraints, doing away with the battery is the only choice. Emerging applications like wireless micro-sensor networks [1], implantable medical electronics and tire-pressure sensor systems [2] are examples of such a class. It is often impractical to operate these systems on a fixed energy source like a battery owing to the difficulty in replacing the battery. The ability to harvest ambient energy through energy scavenging technologies is necessary for battery-less operation. A 1 cm^3 primary lithium battery has a typical energy storage capacity of 2800J [3]. This can potentially supply an average electrical load of 100 μW for close to a year but is insufficient for systems where battery replacement is not an easy option. The most common harvesters transduce solar, vibrational or thermal energy into electrical energy. The vibrational harvesters use one of three methods: electromagnetic (inductive), electrostatic (capacitive) or piezoelectric. The thermoelectric harvesters exploit temperature gradients to generate power. Most harvesters in practically usable forms can provide an output power of 10–100 μW [4], setting a constraint on the average power that can be consumed by the load circuitry for self-powered operation.

For the applications mentioned above, the presence of ambient vibrations makes it possible to scavenge mechanical energy. Harvesting ambient vibration energy through piezoelectric (PE) means is a popular energy harvesting technique which can potentially supply 10–100's of μW of available power [3]. This low power output necessitates not only the design of ultra-low power logic circuits but also efficient power delivery interface circuits that can extract the maximum power available out of the energy harvesters. One of the limitations of existing PE harvesters is in their interface circuitry. Commonly used full-bridge rectifiers and voltage doublers [5] severely limit the electrical power extractable from a PE harvesting element. Further, the power consumed in the control circuits of these harvesters reduces the amount of usable electrical power. In this paper, a bias-flip rectifier that can improve upon the power extraction capability of existing full-bridge rectifiers by greater than 4X is presented. An efficient control circuit with embedded DC-DC converters that can share their filter inductor with the bias-flip rectifier thereby reducing the volume and component count of the overall solution is demonstrated.

II. Equivalent Circuit of a Piezoelectric Energy Harvester

Using piezoelectric elements is a popular way to harvest ambient mechanical energy. An input vibration applied on to a piezoelectric material as shown in Fig. 1 causes mechanical strain to develop in the device which is converted to electrical charge. Lead-zirconate-titanate (PZT) is a commonly used piezoelectric material for power generation. The equivalent circuit of the piezoelectric harvester [3], [6] can be represented as a mechanical spring mass system coupled to an electrical domain as shown in Fig. 1. Here, L_M represents the mechanical mass, C_M the mechanical stiffness and R_M takes into account the mechanical losses. The mechanical domain is coupled to the electrical domain through a transformer that converts strain to current. On the electrical side, C_P represents the plate capacitance of the piezoelectric material. At or close to resonance, the whole circuit can be transformed to the electrical domain, where the piezoelectric element when excited by sinusoidal vibrations can be modeled as a sinusoidal current source in parallel with a capacitance C_P and resistance R_P. One of the challenges in a power generator of this type is the design and construction of an efficient power conversion circuit to harvest

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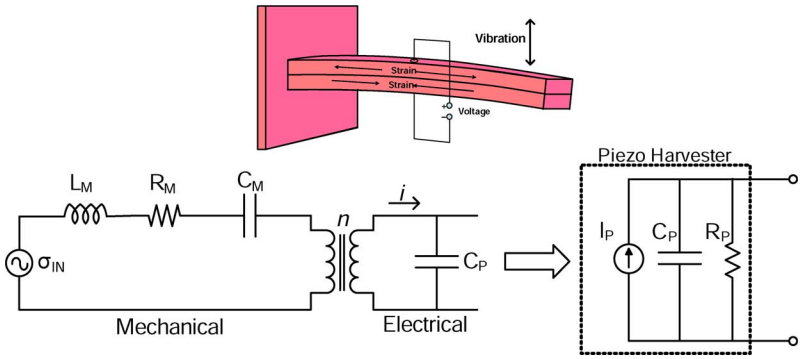

Fig. 1. Equivalent circuit of a piezoelectric energy harvester showing the mechanical and electrical sides of the device [3].

the energy from the PZT membrane. Unlike conventional power supplies and batteries, which typically have very low internal impedance, the piezoelectric generators internal impedance is relatively high. This high internal impedance restricts the amount of output current that can be driven by the PZT source to the micro-amp range. Another unique characteristic of this power source is that it outputs relatively low output voltages for the low levels of input vibration typically encountered in ambient conditions. This low output voltage makes it challenging to develop rectifier circuits that are efficient since many diode rectifiers require nonzero turn-on voltages to operate.

III. Commonly Used Interface Circuits to Piezoelectric Harvesters

A piezoelectric harvester is usually represented electrically as a current source in parallel with a capacitor and resistor [3], [5], [7]. The current source provides current proportional to the input vibration amplitude. For the sake of the following analysis, the input vibrations are assumed to be sinusoidal in nature and hence the current is represented as $i_P = I_P \sin \omega_P t$, where $\omega_P = 2\pi f_P$ and f_P is the frequency with which the piezoelectric harvester is excited. The power output by the piezoelectric harvester is not in a form which is directly usable by load circuits such as micro-controllers, radios etc. which the harvester powers. The voltage and current output by the harvester needs to be conditioned and converted to a form usable by the load circuits. The power conditioning and converting circuits should also be able to extract the maximum power available out of the piezoelectric energy harvester. Commonly used analog and digital circuits require a regulated supply voltage to operate from. Since the piezoelectric harvester outputs a sinusoidal current, it first needs to be rectified before it can be used to power circuits. Some of the commonly used rectifier circuits are discussed below.

A. Full-Bridge Rectifiers and Voltage Doublers

Full-bridge rectifiers [7], [8] and voltage doublers [5], [9] are commonly used as rectifier circuits to convert the AC output of a piezoelectric harvester into a DC voltage. Typical implementation of these rectifier circuits is shown in Fig. 2. The capacitor C_{RECT} at the output of the rectifier is assumed to be large compared to C_P and hence holds the voltage at the output of the rectifier (V_{RECT}) essentially constant on a cycle-to-cycle basis. With this assumption, the voltage and current waveforms associated with these circuits are shown in Fig. 2.

The non-idealities of the diodes is represented using a single parameter V_D which is the voltage drop across the diode when current from the piezoelectric harvester flows through it. Every half-cycle of the input current waveform can be split into 2 regions. For the full-bridge rectifier, in the interval between $t = t_0$ and $t = t_{\mathrm{OFF}}$, the piezoelectric current i_P flows into C_P to charge or discharge it. In this interval, all the diodes are reverse-biased and no current flows into the output capacitor C_{RECT}. This condition continues till the voltage across the capacitor C_P which is labeled as V_{BR} in Fig. 2(a) is equal to $V_{\mathrm{RECT}} + 2V_D$ in magnitude. When this happens, one set of diodes turn ON and the current starts flowing into the output. This is the interval between $t = t_{\mathrm{OFF}}$ and $t = t_\pi$ in Fig. 2(a). This interval lasts till the current i_P changes direction. The shaded portion of the current waveform shows the amount of charge not delivered to the output every half-cycle. At low values of V_{RECT}, most of the charge available from the harvester flows into the output but the output voltage is low. At high values of V_{RECT}, very little charge flows into the output. These opposing trends causes the full-bridge rectifier's output power to vary with V_{RECT}. The output power obtained by the full-bridge rectifier in the presence of diode non-idealities can be given by

$$P_{\mathrm{RECT,FB}} = 4C_P V_{\mathrm{RECT}} f_P (V_P - V_{\mathrm{RECT}} - 2V_D) \qquad (1)$$

where the term V_P is the open-circuit voltage amplitude at the output of the piezoelectric harvester which can be represented as $V_P = I_P/\omega_P C_P$. The maximum power [10] that can be obtained using the full-bridge rectifier is given by

$$P_{\mathrm{RECT,FB}}(\max) = C_P (V_P - 2V_D)^2 f_P \qquad (2)$$

and this is achieved at $V_{\mathrm{RECT}} = V_P/2 - V_D$. Appendix B in [11] provides the derivation of the output power equations presented in this paper. In the case of the voltage doubler, the current flow into the output does not occur every half-cycle. During the negative half-cycle of the input current, the diode in parallel with the harvester turns ON and it essentially keeps the voltage across the harvester (V_{VD}) at $-V_D$. There is no current flow into the output during this period. As the current becomes positive, i_P flows into the capacitor C_P first to charge it up to $V_{\mathrm{RECT}} + V_D$ before the series diode can turn ON for the current to flow to the

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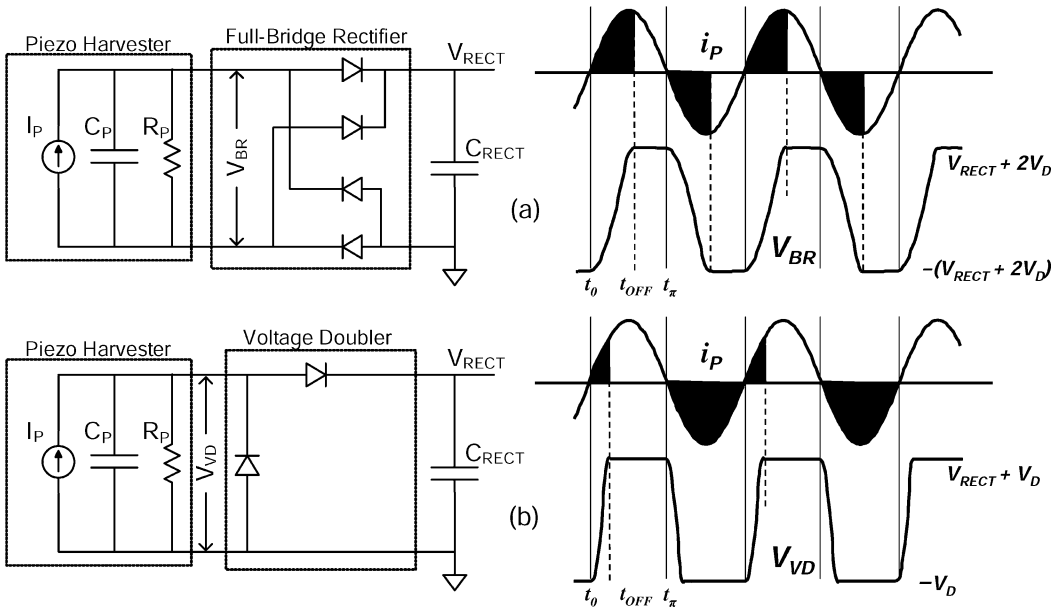

Fig. 2. (a) A full-bridge rectifier and (b) voltage doubler used to extract power from a piezoelectric energy harvester and their associated simulated voltage and current waveforms.

output. The output power obtained by the voltage doubler in the presence of diode non-idealities can be given by

$$P_{\mathrm{RECT},VD} = C_P V_{\mathrm{RECT}} f_P (2V_P - V_{\mathrm{RECT}} - 2V_D) \quad (3)$$

which reaches a maximum at $V_{\mathrm{RECT}} = V_P - V_D$. The maximum power that can be obtained using the voltage doubler can be given by

$$P_{\mathrm{RECT},VD}(\max) = C_P (V_P - V_D)^2 f_P. \quad (4)$$

In the presence of ideal diodes $(V_D = 0)$, the maximum power obtained by using a voltage doubler is the same as that obtained using a full-bridge rectifier as shown in Fig. 3. The voltage doubler however helps in pushing the voltage at which the maximum is obtained up by 2X. In the presence of diode non-idealities, the voltage doubler gives an improvement in the overall power obtained.

Using a single parameter (V_D) to take into account the diode non-idealities helps in keeping the mathematical expressions simple. It also gives good insight into the effect the non-ideal diode has in introducing losses into the system. A simple way to determine V_D is to average the voltage across the diode when current flows through it over a half-cycle of the input current. Fig. 3 shows a comparison between the simulated and theoretical power obtained at the output of the rectifier for both the full-bridge and voltage doubler cases. The plots show the power output with ideal and CMOS diodes. For the CMOS diode, a value of 0.38 V was used for V_D when calculating the output power. It can be seen from the figure that the diode non-idealities affect the full-bridge rectifier more than the voltage doubler. The close match between the theoretical prediction and simulated results validates using a single parameter to describe diode non-idealities. The analysis till now has ignored the presence of the damping resistance R_P. Appendix B in [11] presents an

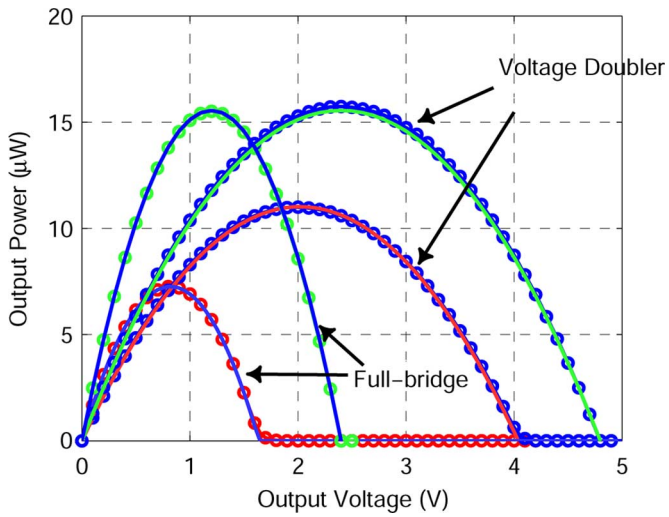

Fig. 3. Theoretical and simulated power obtained at the output of the full-bridge rectifier and voltage doubler with and without ideal diodes as V_{RECT} is changed. The power obtained reduces with non-ideal diodes. Circular markers show simulated values.

analysis of the power obtained at the output of the full-bridge rectifier and voltage doubler taking into account the effect of resistance R_P.

The diode used in the simulation was obtained using a pMOS transistor with its source as the anode and the gate, drain and bulk connected together as the cathode of the diode. Considerable work [5], [12]–[14] has been done on using synchronous rectifiers that use MOS transistors to replace the diodes. These have much lower forward voltage loss compared to p-n junction diodes or transistor-based diodes.

The theoretical maximum power, $P_{\mathrm{RECT,THE}}(\max)$, that can be extracted from the piezoelectric equivalent circuit shown in

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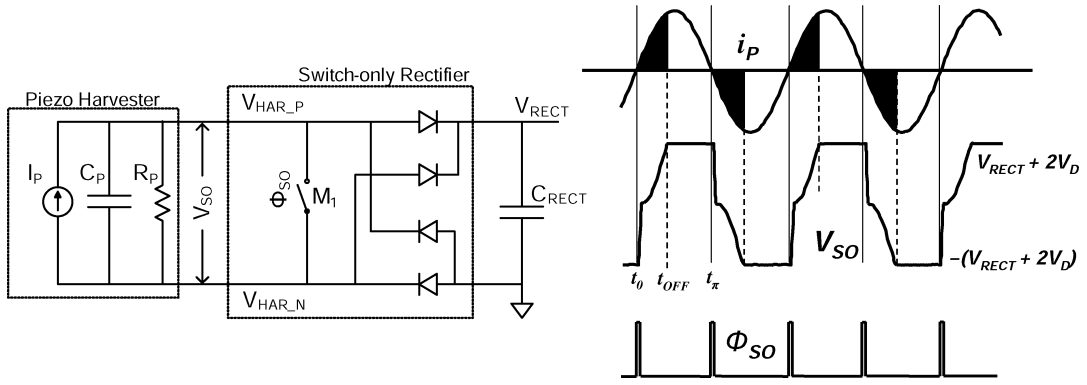

Fig. 4. A switch-only rectifier circuit and its associated current and voltage waveforms.

Fig. 1 can be obtained from maximum power point theory by presenting a conjugate impedance match as

$$P_{\mathrm{RECT,THE}}(\max) = \frac{I_p^2 R_P}{8} = \frac{Q_P^2 V_P^2}{8R_P} \tag{5}$$

where $Q_P = \omega_P C_P R_P$. Compared to the maximum theoretical power available from the piezoelectric equivalent circuit, the ratio of the maximum power obtained using a full-bridge rectifier or voltage doubler with ideal diodes, $P_{\mathrm{RECT}}(\max)$, is given by

$$\frac{P_{\mathrm{RECT}}(\max)}{P_{\mathrm{RECT,THE}}(\max)} = \frac{4}{\pi Q_P} \tag{6}$$

For a commercial piezoelectric harvester from Mide (V22W), the internal impedance of the device can be modeled as $C_P = 12$ nF and $R_P = 600$ k Ω. When this device is excited at close to its resonance frequency of 225 Hz, the full-bridge rectifier or the voltage doubler output only 12.5% of the actual maximum power available even when ideal diodes are considered. The output power extracted is even smaller when non-ideal diodes are taken into account.

IV. Proposed Rectifier Schemes

The main limitation of the full-bridge rectifier and voltage doubler is that, most of the charge available from the harvester does not go into the output at high voltages. The loss in charge due to charging and discharging of C_P limits the maximum power that can be extracted using these rectifier circuits. This section presents the design of advanced rectifier circuits that can improve the power extraction capabilities from piezoelectric harvesters thereby trying to reach the theoretical maximum power output possible.

A. Switch-Only Rectifier

The full-bridge rectifier and voltage doubler circuits both provide the same amount of maximum output power when ideal diodes are considered. However, the voltage doubler provides current to the output only during the positive half-cycle of i_P. During the negative half-cycle, its parallel diode helps in pre-discharging C_P to ground. This way during the positive half-cycle, i_P only needs to do half the work to charge up C_P to V_{RECT} before it can flow into the output. This observation leads to the design of the switch-only rectifier.

Fig. 4 shows the design of the switch-only rectifier where a simple switch M_1 is connected across the piezoelectric harvester driving a full-bridge rectifier. For the moment, assume that the switch is turned ON for a brief time at every zero-crossing of the piezoelectric current i_P. When the switch is ON, it discharges the capacitor C_P immediately to ground. Once C_P has been discharged, M_1 is turned OFF. This frees up the rectifier to conduct during both the half-cycles of the input current. The voltage and current waveforms associated with the switch-only rectifier is shown in Fig. 4. At every half-cycle, when i_P changes direction, the switch M_1 is turned ON briefly to discharge the voltage across C_P. Now, the piezoelectric current only has to charge up C_P from 0 to $\pm(V_{\mathrm{RECT}} + 2V_D)$ before it can flow into the output. The switch-only rectifier combines the advantages of the full-bridge rectifier and the voltage doubler by conducting current in both the half-cycles as in a full-bridge rectifier while charging C_P up from only 0 to $\pm(V_{\mathrm{RECT}} + 2V_D)$ every half-cycle similar to that in a voltage doubler. The power delivered to the output by the switch-only rectifier can be given by

$$P_{\mathrm{RECT,SO}} = 2C_P V_{\mathrm{RECT}} f_P (2V_P - V_{\mathrm{RECT}} - 2V_D) \tag{7}$$

which reaches a maximum at $V_{\mathrm{RECT}} = V_P - V_D$. The maximum power that can be obtained using the switch-only rectifier is given by

$$P_{\mathrm{RECT,SO}}(\max) = 2C_P (V_P - V_D)^2 f_P \tag{8}$$

The power output by the switch-only rectifier is exactly twice that obtained by using the voltage doubler and also reaches a maximum at the same voltage as that of the voltage doubler. Fig. 5 shows a comparison between the simulated and theoretical power obtained at the output of the rectifier for the full-bridge rectifier, voltage doubler and switch-only rectifier cases. A value of 0.38 V was used for V_D. It can be seen from the figure that the power versus voltage profile for the switch-only rectifier is very similar to that obtained using the voltage doubler. The switch-only rectifier in effect works similar to two voltage doublers of opposite phase working in tandem. With the addition of a simple switch, the switch-only rectifier is able to provide 2X the amount of electrical power that was provided

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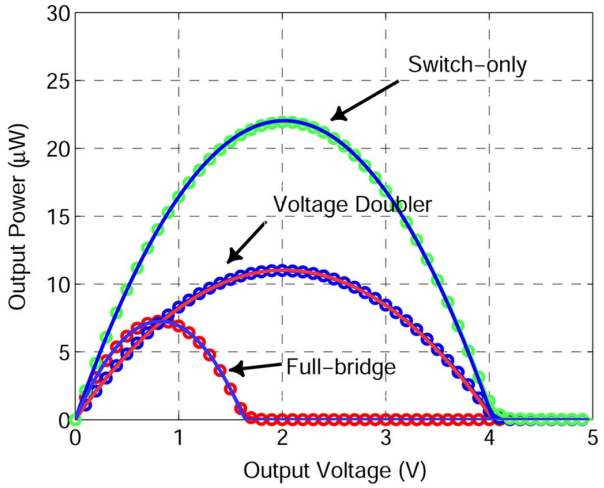

Fig. 5. Theoretical and simulated power obtained at the output of the full-bridge rectifier, voltage doubler and switch-only rectifier employing CMOS diodes with change in $V_{\rm RECT}$. Circular markers show simulated values.

by the voltage doubler. Appendix B in [11] presents an analysis of the power obtained at the output of the switch-only rectifier taking into account the effect of resistance R_P. The implementation of the switch M_1 and its gate-drive circuitry is explained in Section VI.

B. Bias-Flip Rectifier

The switch-only rectifier is able to utilize both half-cycles of the input current. However, there is still significant amount of charge lost in the rectifier due to charging C_P up from 0 to $\pm(V_{\rm RECT}+2V_D)$ every half-cycle. Any further increase in output power can only be obtained if this charge lost is reduced further. The bias-flip rectifier achieves this with the help of an inductor.

Fig. 6 shows the circuit implementation of the bias-flip rectifier. Compared to the switch-only rectifier, an additional inductor $(L_{\rm BF})$ has been added in series with the switch M_1. An inductor can passively flip the voltage across a capacitor. So instead of just using a switch, the bias-flip rectifier utilizes an inductor to flip the voltage across C_P. The voltage and current waveforms associated with this circuit is shown in Fig. 6. At every half-cycle, when i_P changes direction, the switch M_1 is turned ON briefly to allow the inductor to flip the voltage across C_P. The switch is turned OFF when the current in the inductor reaches zero. If the current flow path in the $L_{\rm BF}$, C_P network were ideal, the voltage flipping would be perfect. However, the resistances along this path limits the magnitude of the voltage inversion as shown in Fig. 6. Now, the piezoelectric current only has to charge up C_P from the flipped voltage to $\pm(V_{\rm RECT}+2V_D)$ before it can flow into the output. This significantly reduces the amount of charge lost. This way the majority of the charge available from the harvester can go into the output capacitor without having to charge or discharge C_P. To derive the amount of output power extractable using a bias-flip rectifier, it is assumed that the resistance along the $L_{\rm BF}$, C_P path is $R_{\rm BF}$. This resistance includes the parasitic resistance of the inductor, the switches in series with the inductor and the series resistance along the piezoelectric harvester.

Fig. 7 shows the $L_{\rm BF}$, C_P path when the switch M_1 is turned ON. When the switch is ON, the inductor helps in flipping in an efficient manner, the voltage $(V_{\rm BF})$ across C_P. The resistance $R_{\rm BF}$ limits the magnitude of this voltage inversion. Ideally, the switch needs to be turned OFF exactly when the inductor current reaches zero to achieve maximal flipping of the voltage across C_P. For the moment, assume that this is the case. Section VI explains how this issue is tackled in the actual implementation of the bias-flip rectifier. Assuming the voltage across C_P starts at $V_{\rm RECT}+2V_D$ when the switch is turned ON, the final voltage across C_P after bias-flipping can be derived to be

$$V_{\rm BF}({\rm final}) = -(V_{\rm RECT}+2V_D)e^{-\tau} \tag{9}$$

where $\tau = \pi\beta/\omega, \beta = R_{\rm BF}/2L_{\rm BF}, \omega = \sqrt{\omega_o^2-\beta^2}$, and $\omega_o = 1/\sqrt{L_{\rm BF}C_P}$.

Once the bias-flipping takes place, the piezoelectric current i_P has to only charge C_P from the voltage across it after the flipping to $\pm(V_{\rm RECT}+2V_D)$. The power delivered to the output by the bias-flip rectifier can be given by

$$P_{\rm RECT,BF} = 2C_PV_{\rm RECT}f_P(2V_P-(V_{\rm RECT}+2V_D)(1-e^{-\tau})). \tag{10}$$

Hypothetically, if the conditions were ideal and $R_{\rm BF}=0$, this equation suggests that increasing $V_{\rm RECT}$ leads to more output power. In the limit, infinite power can be obtained out of the harvester! This power output is however consistent with the simplistic model that has been assumed till now in deriving $P_{\rm RECT}$. The resistance R_P has not been taken into account till now. Without this resistance, the source should be capable of providing any amount of power without any limitation. The derivation for the output power extractable using a bias-flip rectifier in the presence of R_P is provided in Appendix B of [11]. From equation B.23 of [11], the power output by the bias-flip rectifier is given by

$$P_{\rm RECT,BF} = 2C_PV_{\rm RECT}f_P\left(2V_P-(V_{\rm RECT}+2V_D)\times(1-e^{-\tau})-\frac{\pi k_{\rm BF}(V_{\rm RECT}+2V_D)}{Q_P}\right) \tag{11}$$

where

$$k_{\rm BF} = \frac{(V_P+(V_{\rm RECT}+2V_D)e^{-\tau})\omega_Pt_1}{\pi(V_{\rm RECT}+2V_D)} - \frac{V_P\sin\omega_Pt_1}{\pi(V_{\rm RECT}+2V_D)}+\frac{\pi-\omega_Pt_1}{\pi} \tag{12}$$

and

$$\omega_Pt_1 = \cos^{-1}\left(1-\frac{(V_{\rm RECT}+2V_D)(1-e^{-\tau})}{V_P}\right). \tag{13}$$

From (11) it can be seen that the output power reaches a maximum at

$$V_{\rm RECT,BF}({\rm max}) = \frac{V_P}{1-e^{-\tau}+\dfrac{\pi k_{\rm BF}}{Q_P}} - V_D. \tag{14}$$

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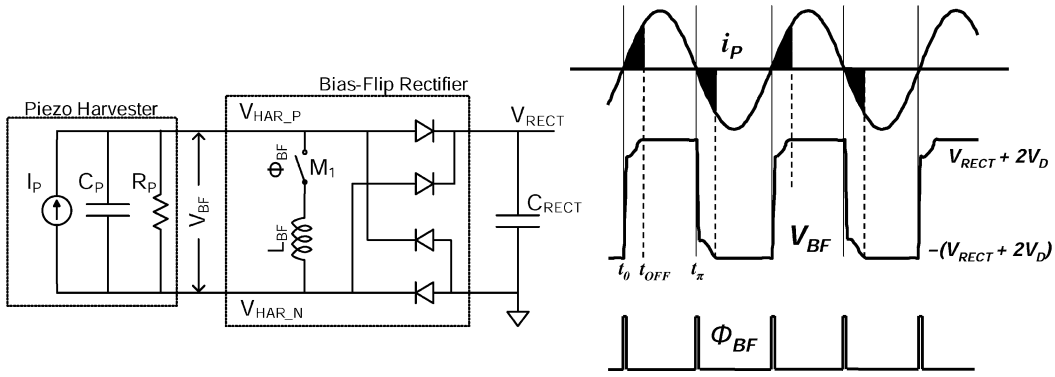

Fig. 6. A bias-flip rectifier circuit and its associated current and voltage waveforms.

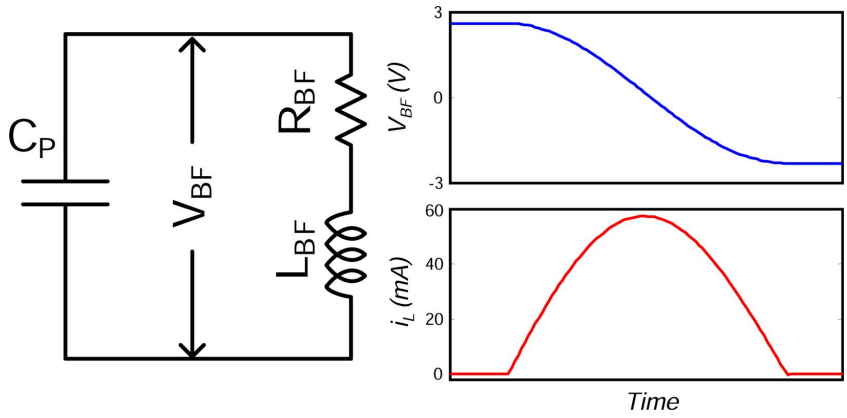

Fig. 7. Simulated voltage and current waveforms of the bias-flipping network when switch M_1 is ON.

We can introduce a new term $Q_{\rm BF}$ which can qualitatively be thought of as the parallel combination of the Q-factors of the piezoelectric harvester and that of the $L_{\rm BF}, C_P$ resonant path.

$$Q_{\rm BF} = \frac{1}{1 - e^{-\tau} + \dfrac{\pi k_{\rm BF}}{Q_P}}. \tag{15}$$

The maximum power output by the bias-flip rectifier can now be given by

$$P_{\rm RECT,BF}(\max) = 2C_P \left(V_P - \frac{V_D}{Q_{\rm BF}}\right)^2 Q_{\rm BF} f_P \tag{16}$$

Fig. 8 shows a comparison between the simulated and theoretical power obtained at the output of the bias-flip rectifier. The following values were used for the simulation and theoretical calculations: $C_P = 12$ nF, $R_P = 600$ k Ω, $V_P = 2.4$ V, $f_P = 225$ Hz, $R_{\rm BF} = 26\ \Omega$ and $V_D = 0.38$ V. It can be seen from the figure that there is a close match between the theoretical power calculated using (11) and the simulated value of output power. Increasing the value of $L_{\rm BF}$ decreases τ and hence helps in improving the bias-flip magnitude thereby providing more output power. The implementation of the bias-flip rectifier is discussed in more detail in Section VI.

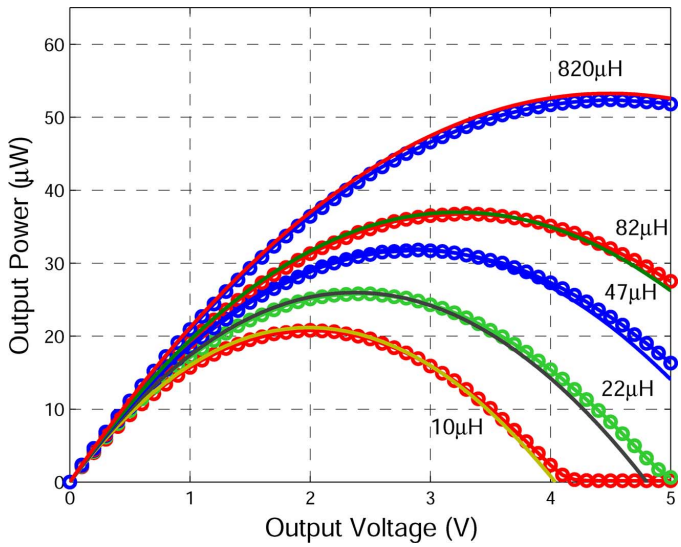

Fig. 8. Theoretical and simulated power obtained at the output of the bias-flip rectifier employing CMOS diodes with change in $V_{\rm RECT}$. Circular markers show simulated values.

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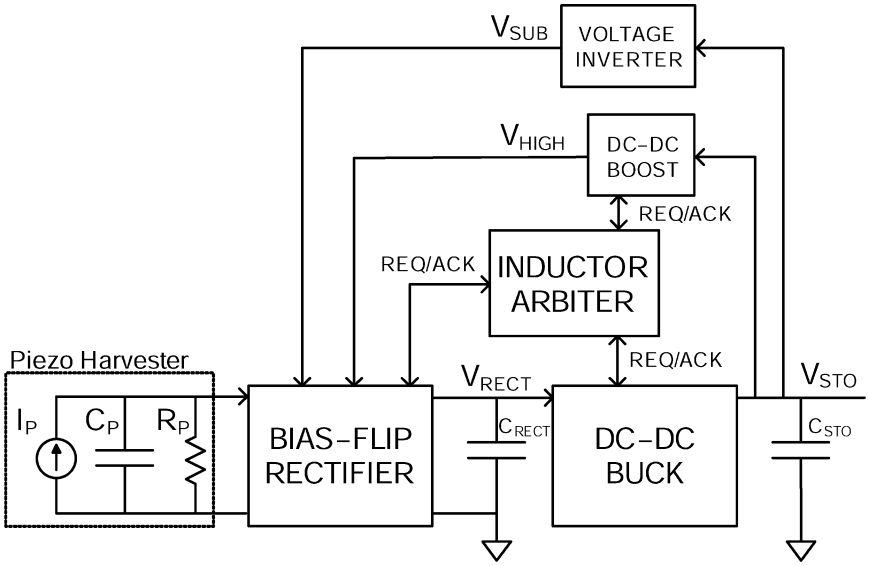

Fig. 9. Architecture of the bias-flip rectifier system. The inductor arbiter controls access to the shared inductor L_{SHARE}.

C. Comparison Between Power Extraction Capabilities of Full-Bridge Rectifier and Bias-Flip Rectifier

Compared to the maximum theoretical power available as shown in (5), the ratio of the power obtained using a full-bridge rectifier from (2) is given by

$$\frac{P_{\mathrm{RECT,FB}}(\max)}{P_{\mathrm{RECT,THE}}(\max)} = \frac{4(V_P - 2V_D)^2}{\pi Q_P V_P^2}. \tag{17}$$

For the bias-flip rectifier, the ratio of the maximum power obtained as given by (16) to the maximum theoretical power available can be given by

$$\frac{P_{\mathrm{RECT,BF}}(\max)}{P_{\mathrm{RECT,THE}}(\max)} = \frac{8Q_{\mathrm{BF}}\left(V_P - \dfrac{V_D}{Q_{\mathrm{BF}}}\right)^2}{\pi Q_P V_P^2}. \tag{18}$$

It can be thus seen that, the bias-flip rectifier improves upon the maximum power extractable by a factor of

$$\frac{P_{\mathrm{RECT,BF}}(\max)}{P_{\mathrm{RECT,FB}}(\max)} = \frac{2Q_{\mathrm{BF}}\left(V_P - \dfrac{V_D}{Q_{\mathrm{BF}}}\right)^2}{(V_P - 2V_D)^2}. \tag{19}$$

Assuming $C_P = 12$ nF, $R_P = 600$ k Ω, $V_P = 2.4$ V, $\tau = 0.36$ and a conservative estimate of $k_{\mathrm{BF}} = 1$ for the bias-flip rectifier, the improvement in power extraction of the bias-flip rectifier over the full-bridge rectifier is 3.29X when ideal diodes ($V_D = 0$ V) are considered. A further advantage of the bias-flip rectifier scheme is that it pushes the optimal voltage for power extraction to be higher than that obtained using only a full-bridge rectifier, thereby minimizing the losses which occur when diode non-idealities are introduced. In the presence of CMOS diodes ($V_D = 0.38$ V), the power improvement with moderate bias-flipping ($\tau = 0.36$) is 5.46X and the improvement with perfect bias-flipping ($\tau = 0$) is 12.55X. From (18), it can be seen that in the presence of ideal diodes and with perfect bias-flipping, the bias-flip rectifier can reach $8/\pi^2 = 81\%$ of the theoretical maximum possible. To obtain the maximum theoretical power possible through conjugate impedance matching, it is necessary to tune out the input capacitance C_P using an inductor which would require close to 41.7 H of inductance at 225 Hz vibration, which is impractical. The bias-flip rectifier tries to resonate with the input capacitance C_P at a frequency much higher than the frequency of the input vibrations. Hence, it can get close to the theoretical maximum with only a small amount of inductance.

The analysis above suggests that using an inductor and switching it suitably can lead to a significant increase in the output power obtained from piezoelectric energy harvesters. This conclusion was arrived at by analyzing the equivalent circuit of a piezoelectric energy harvester and by trying to increase the charge delivered to the output every cycle. A similar conclusion was arrived at by the authors of [15] who with the help of the synchronized switch harvesting (SSH) technique, were able to demonstrate a 2.6X improvement [16] in output power extracted compared to conventional full-bridge rectifiers. The authors were able to arrive at the SSH circuit by using the synchronized switch damping (SSD) method [17], which is a nonlinear technique developed to address the problem of vibration damping on mechanical structures. The solution the authors present is however on a macro scale with discrete board-level components. The work presented here targets integrated CMOS applications with embedded control for timing and gate-overdrive of the bias-flip rectifier.

V. Architecture of the Bias-Flip Rectifier System

Fig. 9 shows the architecture employed for the bias-flip rectifier system. The piezoelectric harvester is connected to the bias-flip rectifier block which contains the bias-flip switches and the control circuitry to determine the timing and gate-overdrive control of the switches. The power output by the rectifier goes into C_{RECT}. A buck DC-DC converter is used to regulate V_{RECT} and efficiently pass on the energy obtained from

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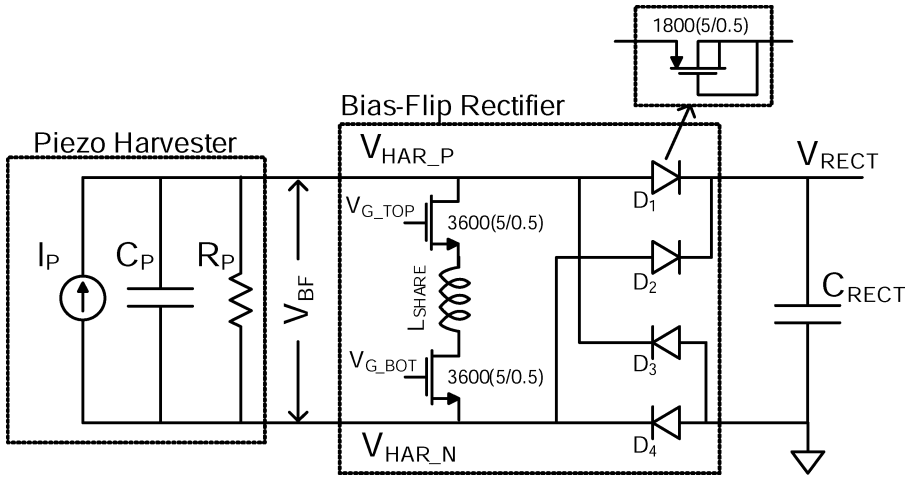

Fig. 10. The bias-flip rectifier circuit showing the shared inductor and bias-flip switches. The substrate of the nMOS switches is connected to $V_{\rm SUB}$.

the harvester on to a storage capacitor $C_{\rm STO}$. In this implementation, the storage capacitor is in the form of a rechargeable battery with a nominal voltage of 1.8 V. A boost DC-DC converter is used to generate a high voltage $V_{\rm HIGH}$ ($\sim$5 V) which is used to power the switches of the bias-flip rectifier. Driving the bias-flip switches with a high voltage helps to reduce their resistance thereby improving the bias-flip magnitude and power output by the rectifier. Both the buck and boost DC-DC converters employ an inductor-based architecture [18] for improved efficiency. The bias-flip rectifier also uses an inductor in the rectification process. The arbiter block shown in Fig. 9 is used to control access to a shared inductor $L_{\rm SHARE}$, which is shared between the bias-flip rectifier, buck and boost DC-DC converters. Section IX explains the need and feasibility of inductor sharing and how the arbiter is implemented. A voltage inverter block is used to generate a negative voltage to bias the substrate of the integrated circuit.

VI. Circuit Implementation of the Bias-Flip Rectifier

This section describes the implementation of the bias-flip rectifier as a CMOS circuit. The bias-flip rectifier is shown with the bias-flip switches and the shared inductor in Fig. 10. The switches are implemented using nMOS transistors. It was assumed in Section IV.B that the bias-flip switches are turned ON when the current i_P from the harvester crosses zero. Also, it is essential to keep the switches ON for just enough time to achieve zero-current switching of the inductor current. This timing control circuitry is described in Section VI.A. Let the maximum gate overdrive allowed by the technology in use be $V_{\rm HIGH}$. For most efficient charge transfer through the inductor, the gate overdrive of the bias-flip switches needs to be as high as possible. The gate-drive circuitry described in Section VI.B accomplishes this while maintaining the bias-flip switches within breakdown limits. The voltages at the nodes $V_{\rm HAR\_P}$ and $V_{\rm HAR\_N}$ shown in Fig. 10 can go as low as one diode drop below ground when in operation. Assuming a pessimistic value of $V_D = 0.7$ V, this can easily turn on the P-N junction diodes of the substrate-N+ interface in the bias-flip switches. Hence, it is essential to keep the substrate connection of the bias-flip switches at least as low as -0.6 V to prevent any unwanted diode leakage of the piezoelectric current. Since most CMOS processes including the one used for this implementation are twin-well processes, it becomes essential to keep the substrate potential of the entire chip at a negative voltage ($V_{\rm SUB}$). The voltage inverter block shown in Fig. 9 is used to generate this negative voltage. It makes use of a switched capacitor voltage inverter to generate a negative voltage for feeding the substrate voltage in the CMOS implementation of the bias-flip rectifier. The diodes used in the rectifier were obtained using a pMOS transistor with its source as the anode and the gate, drain and bulk connected together as the cathode of the diode as shown in Fig. 10.

A. Timing Control Circuit

Fig. 11 shows the block diagrammatic representation of the control circuitry that determines the timing and gate-overdrive control of the switches in the bias-flip rectifier. The switches need to be turned ON when i_P crosses zero. When i_P is close to zero, the diodes are just on the verge of turning OFF. At this point one of the voltages $V_{\rm HAR\_P}$ or $V_{\rm HAR\_N}$ is close to $V_{\rm RECT} + V_D$ and the other one is close to $-V_D$. The zero-crossing of i_P is detected by comparing (depending on the direction of current) either $V_{\rm HAR\_P}$ or $V_{\rm HAR\_N}$ with a reference voltage $V_{D\_\rm REF}$. This comparison is done using a continuous-time comparator shown in Fig. 12. The comparator is modeled based on the circuit described in [5]. The same bias current generation circuit is shared between the two arms of the comparator. The reference voltage $V_{D\_\rm REF}$ is set very close to the negative value of the voltage across a diode when a small amount of current (< 1 μA) is flowing through it. In this implementation of the bias-flip rectifier system, this reference voltage was set externally. The reference voltage can be obtained on-chip by forcing a current much smaller than 1 μA through a scaled version of the diode similar to the one used in the rectifier. When the current i_P is positive and diodes 1 and 4 of the bias-flip rectifier are ON, the voltage $V_{\rm HAR\_P}$ is close to $V_{\rm RECT} + V_D$. This keeps $\rm OUT_1$ low. At the same time, $V_{\rm HAR\_N}$ is close to $-V_D$ which is lower than the $V_{D\_\rm REF}$ set. Hence, $\rm OUT_2$ is high.

When i_P reaches close to zero, $V_{\rm HAR\_N}$ approaches $V_{D\_\rm REF}$ and this causes $\rm OUT_2$ to go low. This makes the output of the

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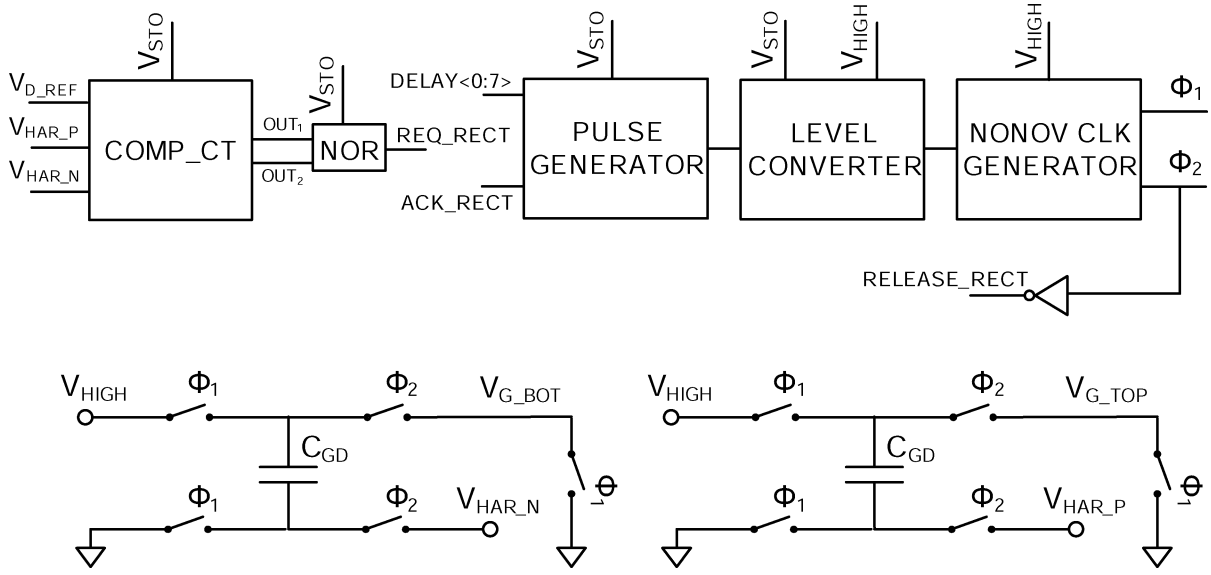

Fig. 11. Block diagrammatic representation of the circuit for timing and gate-overdrive control of the bias-flip rectifier.

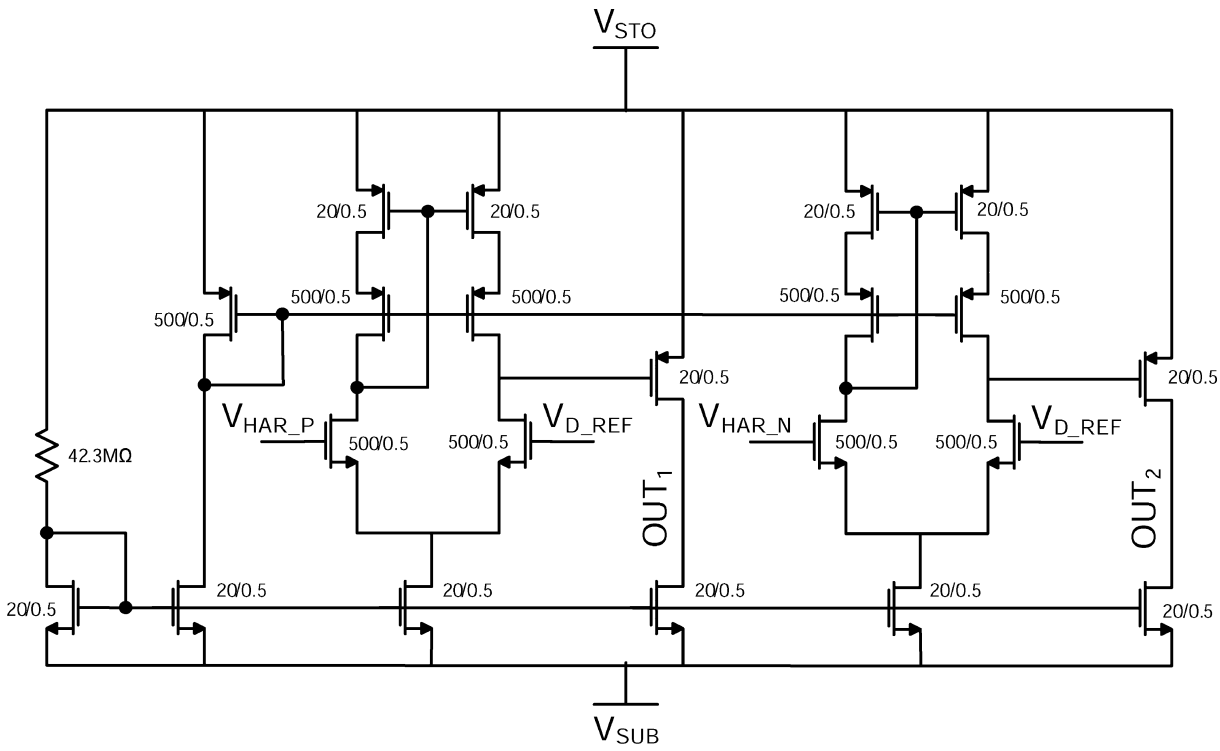

Fig. 12. Continuous time comparator to detect the zero-crossing of the piezoelectric current.

NOR gate REQ_RECT in Fig. 11 to go high. A similar process repeats when i_P is negative and approaches zero. This way the comparator is able to detect the zero-crossing of i_P in either direction. In simulations, the comparator consumes a constant current of 225 nA from the 1.8 V $V_{\rm STO}$ supply. The REQ_RECT signal going high signals that the bias-flipping is to begin soon. Since, the inductor used within the bias-flip rectifier is shared with the buck and boost DC-DC converters, before bias-flipping can begin, the access to the common inductor $L_{\rm SHARE}$ needs to be obtained. The REQ_RECT signal does this function by requesting the inductor arbiter to grant access to the inductor. The arbiter block is described in Section IX. The arbiter grants access through the ACK_RECT signal which triggers a pulse generator whose width can be controlled by the signal $\rm DELAY\langle 0:7\rangle$.

The pulse generator is a simple AND gate where the signal ACK_RECT is ANDed with a delayed inverted version of itself. The delay block shown in Fig. 13 is used for delaying the ACK_RECT signal. The delay block is controlled by an 8-bit signal out of which 4-bits $(C\langle 0:3\rangle)$ are used for coarse control and the other 4-bits $(F\langle 0:3\rangle)$ are used for fine control of the delay. The delays themselves are generated using weak

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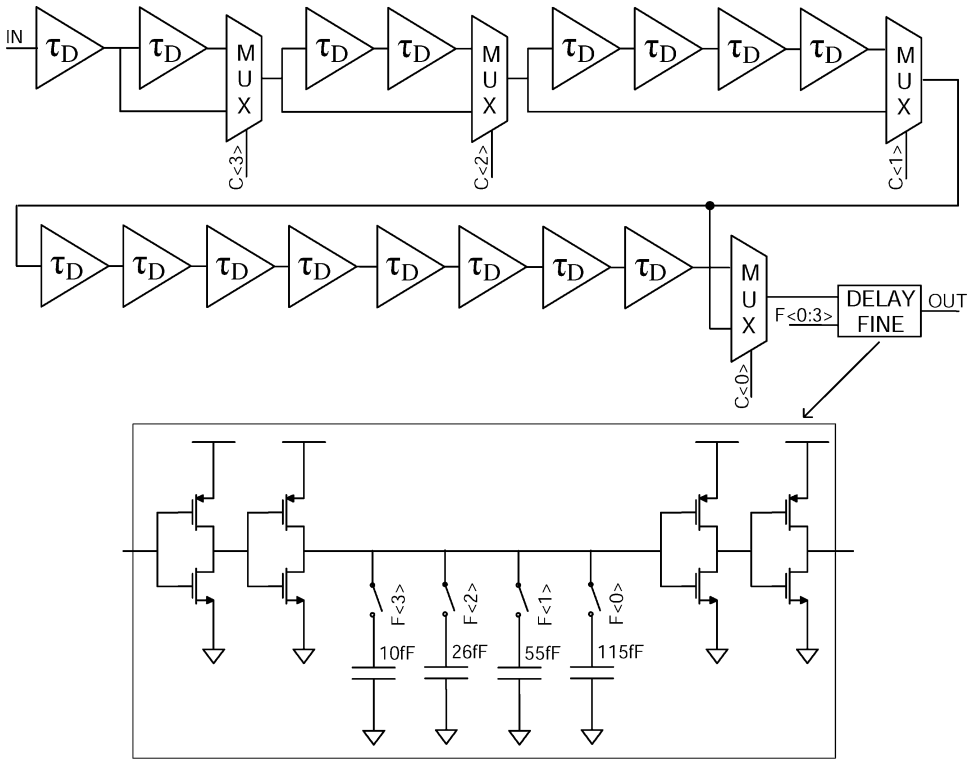

Fig. 13. Delay block to control the ON-time of the bias-flip switches.

inverters charging up capacitances. A look into the fine delay block is provided in Fig. 13. The coarse delay elements are obtained similar to the fine delay block with all capacitances activated. The partitioning of delay into a coarse and fine set allows a large range of delays to be achieved with fine granularity in the delay. The large delay range is necessary to accommodate a wide change in inductor values and CMOS process variations. The delay control signal $\mathrm{DELAY}\langle 0:7\rangle$ controls the duration for which the bias-flip switches are ON. It is adjusted to achieve zero-current switching of the current through the shared inductor when bias-flipping is taking place. In this implementation of the bias-flip rectifier system, the delay control signal was fed in externally. Once a suitable inductor value is chosen for L_{SHARE}, the amount of time the bias-flip switches need to be ON is fixed. So, it is possible to do a one-time calibration of the delay control signal. The pulse generated by the pulse-generator block is then level converted to get a pulse which transitions from 0 to V_{HIGH}.

B. Gate-Overdrive Control Circuit

The pulse obtained at the output of the level converter cannot be used directly to feed the gates of the bias-flip switches. The reason for this can be understood by observing Fig. 14. When bias-flipping takes place, the voltages $V_{\mathrm{HAR\_}P}$ and $V_{\mathrm{HAR\_}N}$ transition from close to $V_{\mathrm{RECT}}+V_D$ to $-V_D$ or vice-versa. Assume that V_{RECT} is 4 V and V_D is 0.4 V. If the switches are turned ON using V_{HIGH} which is close to 5 V, the gate-overdrive of one of the bias-flip switches will just be $(5-4.4=0.6\ \mathrm{V})$ initially. This is very close to the threshold voltage of the transistors used and the bias-flipping will not even start. It is essential

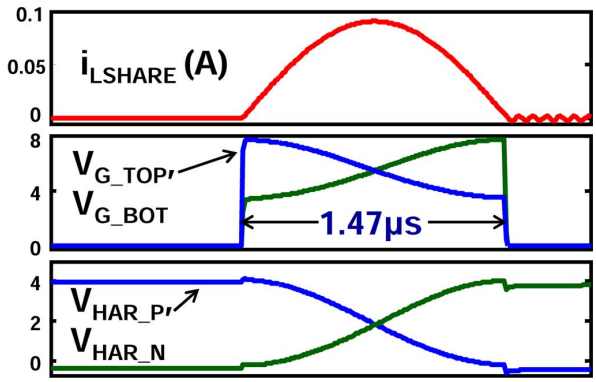

Fig. 14. Simulation plots of the voltage at the output nodes of the harvester and the gate-drive of the bias-flip switches.

to maintain a constant gate over-drive of V_{HIGH} when the voltages $V_{\mathrm{HAR\_}P}$ and $V_{\mathrm{HAR\_}N}$ are transitioning. The switched capacitor circuit shown in the bottom of Fig. 11 allows the bias-flip switches to have a gate-overdrive of V_{HIGH} when they are ON irrespective of the value of V_{RECT}. The gate-drive circuitry consists of switches and a capacitor C_{GD} which is implemented on-chip. During phase ϕ_1 when the bias-flip switches are OFF, the capacitor C_{GD} gets charged to V_{HIGH} and the gate voltages of both the bias-flip switches are brought to ground. When bias-flipping has to take place, phase ϕ_2 begins, where the voltage across C_{GD} remains almost the same, but the voltage referenced to ground at V_{G_TOP} and V_{G_BOT} becomes $(V_{\mathrm{HIGH}}+V_{\mathrm{HAR\_}P})$ and $(V_{\mathrm{HIGH}}+V_{\mathrm{HAR\_}N})$ respectively as shown in Fig. 14. This turns ON the bias-flip switches and keeps them ON till maximal possible flipping of voltage across C_P has taken place. After

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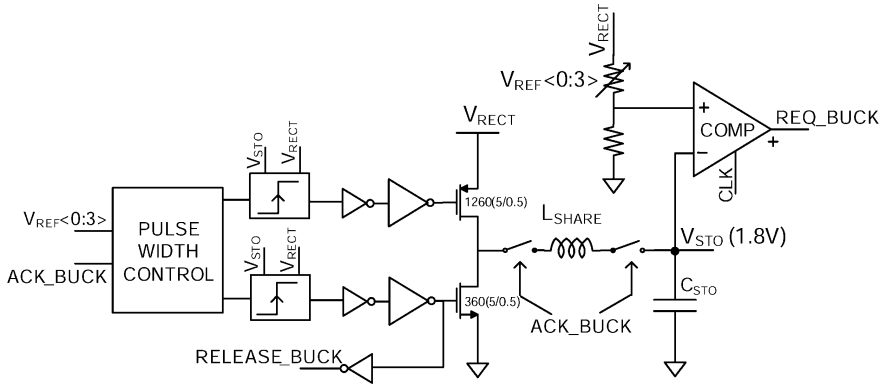

Fig. 15. Architecture of the buck DC-DC converter for regulating V_{RECT}.

this, phase ϕ_2 ends and the bias-flip switches are turned OFF. When ϕ_2 goes low, the RELEASE_RECT signal is sent to the inductor arbiter to free up the shared inductor. This signal signifies that the bias-flip rectifier has finished utilizing the inductor for now. The voltage V_{HIGH} is obtained using a boost DC-DC converter as described in Section VIII.

VII. DC-DC Buck Converter

This section talks about the design of the DC-DC buck converter that is used to efficiently transfer the energy obtained from the piezoelectric energy harvester on to the storage capacitor C_{STO} which is fixed at 1.8 V in this implementation. Fig. 15 shows the architecture of the buck converter. Most DC-DC converter designs are used to provide power to a regulated output voltage from a fixed input voltage. In this DC-DC converter, the power is provided to a storage capacitor which is fixed at 1.8 V. The regulation happens at the input side (V_{RECT}). The buck converter is designed to regulate V_{RECT} from 2.2 V to 5 V with 4 bits of precision $(V_{\mathrm{REF}}\langle 0:3\rangle)$. The power provided by the harvester and that handled by the DC-DC converter is in the order of 1–100 μW. This low power output demands extremely simple control circuitry design with minimal overhead power to get good efficiency.

The converter designed is a synchronous rectifier buck regulator and employs a pulse frequency modulation (PFM) mode of control [18]. PFM mode of control is essential to achieve high efficiencies at the micro-watt power levels handled by the converter. The control achieves regulation with the help of a clocked comparator. A divided version of V_{RECT} is compared with V_{STO} (1.8 V) and if it is found to be higher, the comparator sends the REQ_BUCK signal to the inductor arbiter to request access to the shared inductor. Once the arbiter grants access through the ACK_BUCK signal, the pulsewidth control block turns the pMOS and nMOS power transistors ON sequentially with suitable pulse widths to transfer energy from the rectifier to C_{STO}.

In order to keep the control circuitry simple and consume little overhead power, an all-digital open loop control as described in [19] is used to achieve zero-current switching of the inductor current. The control block fixes the ON-time of the pMOS transistor to a set number of delay units. For the nMOS ON-time, the pulsewidth control block then suitably multiplexes in the required number of delay units depending on the 4-bit reference voltage set to achieve approximate zero-current switching. Increasing the number of these delay units and the complexity of the multiplexer block gives a better approximation to zero-current switching. Since only the ratios of the nMOS and pMOS ON-time pulse widths need to match, this scheme is independent of absolute delay values and any tolerance in the inductor value.

VIII. DC-DC Boost Converter

This section talks about the design of the DC-DC boost converter that is used to generate the voltage V_{HIGH} which is close to 5 V. This voltage is used to drive the switches of the bias-flip rectifier helping to reduce their resistance. The boost converter is designed in a similar way to the buck converter. It also employs pulse frequency modulation mode of control to regulate V_{HIGH}. This is again because of the extremely low power ($< 10\ \mu$W) handled by the boost converter. The boost converter is designed to regulate V_{HIGH} to a fixed voltage of 5 V. Hence, there is no reference ladder employed in its design. The resistive divider shown in Fig. 16 has a fixed voltage division ratio of 0.36. This is used to bring down 5 V to 1.8 V for comparison with V_{STO}. When the voltage V_{HIGH} falls below 5 V, the comparator sends the REQ_BOOST pulse to the arbiter to request access to the shared inductor L_{SHARE}. The arbiter grants access to the inductor through the ACK_BOOST signal. Once, the request is granted the pulsewidth control block sequentially turns ON the nMOS and pMOS power transistors. Unlike the buck converter, the pulsewidth control block in the boost converter has no multiplexed delay elements. This is again because the boost converter is used to regulate V_{HIGH} to a fixed voltage. The nMOS and pMOS ON-time ratios can be pre-determined to be

$$\frac{\tau_P}{\tau_N} = \frac{V_{\mathrm{STO}}}{V_{\mathrm{HIGH}} - V_{\mathrm{STO}}} = \frac{1.8}{5 - 1.8} \approx \frac{5}{9} \tag{20}$$

Hence, the nMOS power transistor's ON-time is set to $9\tau_D$ while the pMOS power transistor's ON-time is set to $5\tau_D$. This helps to achieve approximate zero-current switching of the inductor current. After the pMOS power transistor turns OFF, the boost converter sends the RELEASE_BOOST signal to the arbiter to signify that the boost converter has finished utilizing the

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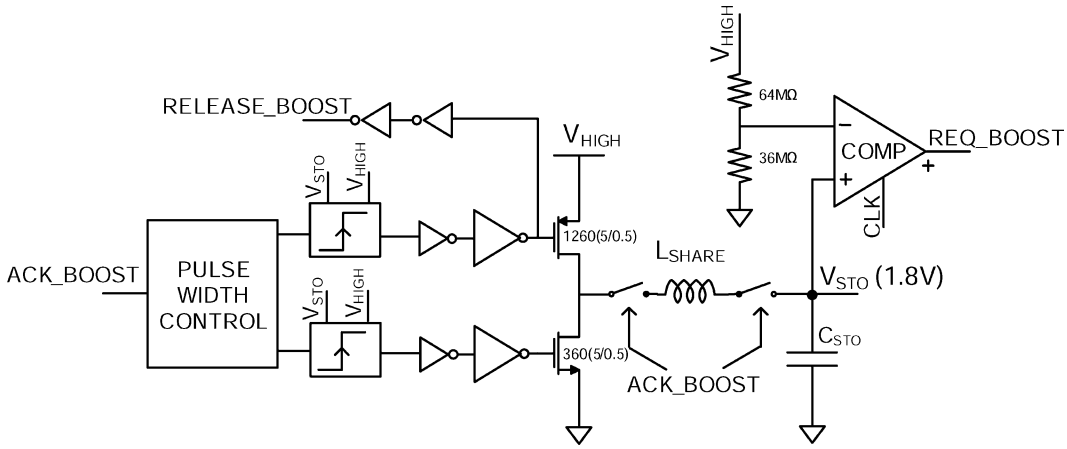

Fig. 16. Architecture of the boost DC-DC converter used to generate V_{HIGH}.

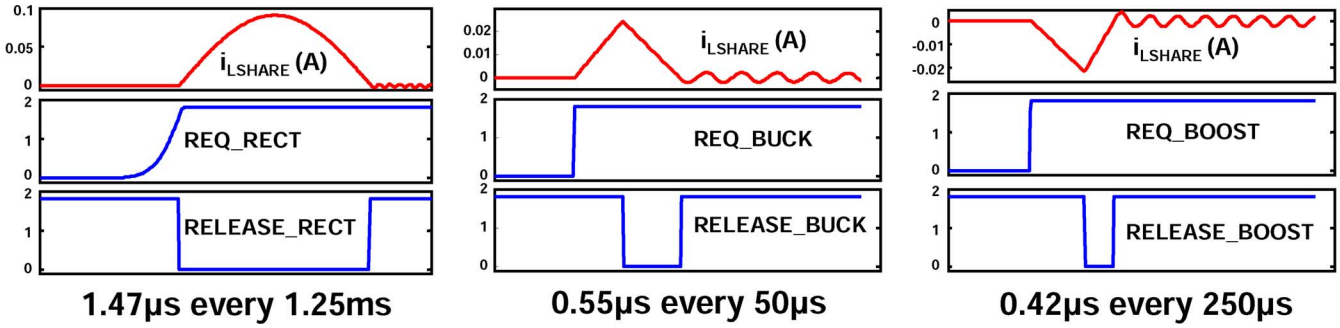

Fig. 17. Inductor utilization times of the bias-flip rectifier, buck and boost DC-DC converters.

inductor for this cycle. This frees up the inductor for use by other blocks.

IX. Inductor Sharing Using an Arbiter

The bias-flip rectifier described in this paper can help to significantly improve the power extracted from piezoelectric harvesters compared to conventionally used rectifier schemes. However, its one main disadvantage is that it requires an inductor which has to be off-chip owing to its size and quality factor requirements. On the plus side, the bias-flip rectifier needs to use the inductor only for brief fractions of time when the input current i_P crosses zero. The buck and boost DC-DC converters used in the system also employ an inductor-based architecture to provide high efficiencies. As was explained in Sections VII and VIII, these DC-DC converters work in discontinuous conduction mode. This means that even the DC-DC converters need to utilize the inductor only for fractions of the time based on the load power they deliver. Fig. 17 shows the typical inductor utilization times for the three blocks along with their respective inductor current, request and release waveforms. For the bias-flip rectifier, the inductor utilization is around 1.47 μs and it happens every 1.25 ms. These numbers are arrived at assuming a 400 Hz input vibration frequency and a 22 μH inductor. The current through the inductor is sinusoidal when bias-flipping is taking place and once the current reaches zero, the bias-flip switches are turned OFF and the inductor is free. For the buck converter with a clock frequency of 20 kHz, the utilization is 0.55 μs. In the worst case, this happens every 50 μs. The effect of discontinuous mode of conduction is evident from the inductor current waveform which ramps up when the pMOS power transistor is ON and ramps down to zero when the nMOS power transistor is ON. Here again after the inductor current reaches zero, the buck converter does not need the inductor anymore till the next clock cycle begins. The same is true for the boost converter where a typical utilization time is 0.42 μs every 250 μs. The boost converter supplies very little load power and hence its inductor utilization is infrequent. We can see from these numbers that the inductor utilization is very sparse. This makes it possible to share the inductor between the 3 blocks thereby saving the volume and cost of the final solution.

Since the clock for the DC-DC converters is not synchronous with the input vibration of the harvester, the DC-DC converter blocks and the bias-flip rectifier may require to use the inductor at the same time. To prevent any conflicts in the access to the shared inductor, an arbiter block is used to control the access. The arbiter block takes in the request and release signals from the three different blocks and it outputs the acknowledge signal which allows a specific block to access the inductor as shown in Fig. 18. The arbiter consists of simple register based digital logic where the request and release signals are edge triggered.

The arbiter is designed to perform the following functions.

1) If the inductor is free, allocate access of the inductor to the next block which requests it.

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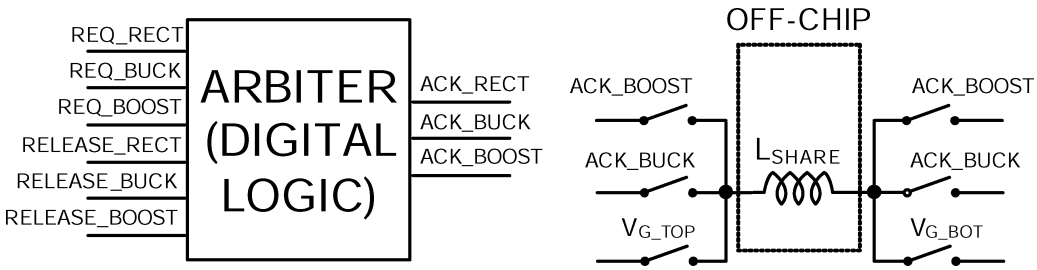

Fig. 18. Simple representation of the arbiter block.

2) If the inductor is occupied when a request comes in, put the request in a queue and acknowledge it once the inductor frees up based on a priority access scheme.
3) The inbuilt priority is given to the buck converter followed by the bias-flip rectifier followed by the boost converter.

The arbiter is designed to guarantee acknowledgment of any inductor request within 4 μs.

A. *Effect of Inductor Sharing on System Performance*

While inductor sharing helps to minimize the number of off-chip components and overall form factor and cost of the final power management solution, it comes at a penalty. The two main problems with inductor sharing is the delayed acknowledgment of request signals and the additional switches added in the path of current flow to accommodate sharing of the inductor. Its effect on the three main blocks are as follows:

1) **Bias-flip Rectifier:** The bias-flip rectifier requires the addition of one more switch in series with $L_{\rm SHARE}$ to enable inductor sharing. If the inductor was not shared, one of the bias-flip switches would not be necessary. This additional switch adds resistance in the $L_{\rm SHARE}$, C_P resonant path. This reduces the magnitude of the flipped voltage and hence reduces the overall power output. The amount of power reduction can be found by including this additional resistance to the value of $R_{\rm BF}$ in (9). The other issue with inductor sharing is that there may be a delay of up to 4 μs from the time the bias-flip rectifier requests the inductor till when it is granted access. Since the time scales of the input vibration is of the order of milli-seconds, this has a negligible effect on the performance of the bias-flip rectifier.
2) **DC-DC Converters:** Inductor sharing requires the addition of 2 switches on either side of $L_{\rm SHARE}$ in the buck and boost converters as shown in Figs. 15 and 16. This adds more resistance in the conductive path and also additional switching loss. The measurement results presented in Section X show that a 2–3% drop in efficiency is seen because of inductor sharing. This is an acceptable penalty to pay considering the benefits of inductor sharing. Further, once the inductor is shared between two blocks, the addition of further blocks to share the same inductor only results in more delays in accessing the inductor. It does not affect the additional resistance due to the multiplexer switches. Since the time delay is still very small, additional DC-DC converters can be allowed to access $L_{\rm SHARE}$ with little to no penalty.

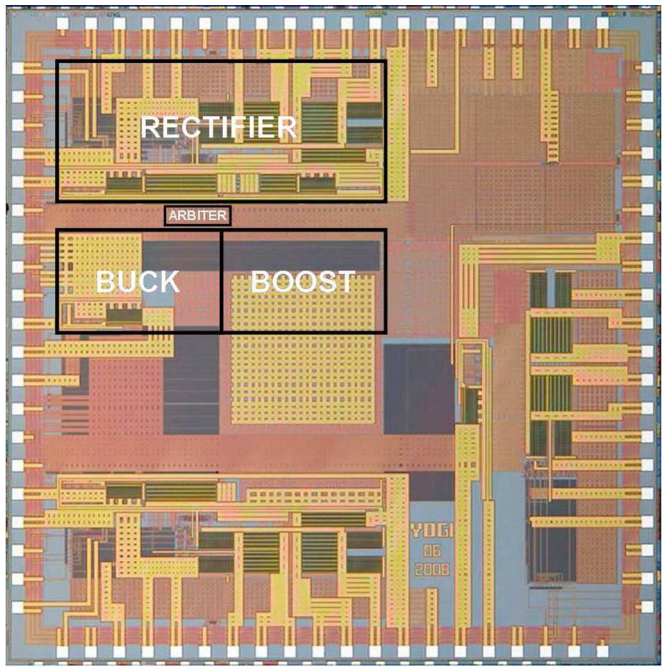

Fig. 19. Die photo of the piezoelectric energy harvesting chip.

X. Measurement Results

The piezoelectric energy harvester interface circuit [20] was implemented in a 0.35 μm CMOS process. Fig. 19 shows the die photo of the test chip. The active area of the interface circuitry together with the DC-DC converters is 4.25 mm^2. The majority of this area is occupied by passive elements like resistors and capacitors implemented as part of the resistive ladder, delay blocks and the continuous time comparator. The die photo identifies the areas occupied by the rectifier, buck and boost DC-DC converters and the inductor arbiter.

A commercially available piezoelectric device (model v22b) from Mide was used to perform all the measurements reported in this section. The piezoelectric device was mounted on a shaker table (Labworks ET-126-B1) which was excited using a sine wave from a signal generator amplified through a power amplifier (Labworks PA-138).

Fig. 20 shows oscilloscope waveforms of the output voltage of the piezoelectric harvester for the different rectifier scenarios. The amplitude of the open-circuit voltage (V_P) of the piezoelectric harvester was 2.4 V for this measurement. The waveforms obtained are consistent with the operation of the different rectifiers as described in Sections III and IV. The voltage $V_{\rm RECT}$ for the full-bridge rectifier case was set to 1.2 V. For the switch-

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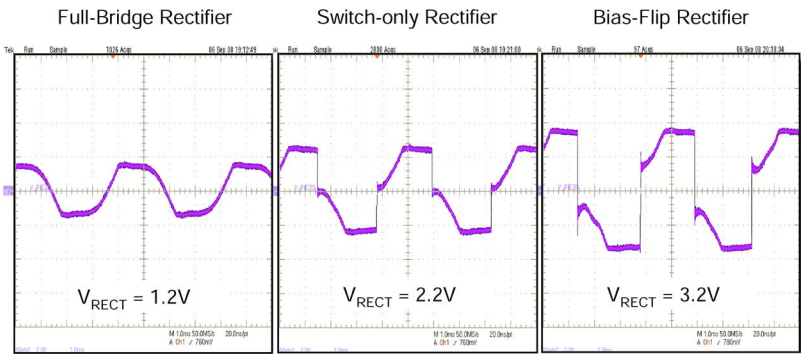

Fig. 20. Measured waveforms of the output voltage across the piezoelectric harvester for the full-bridge, switch-only and bias-flip rectifier cases.

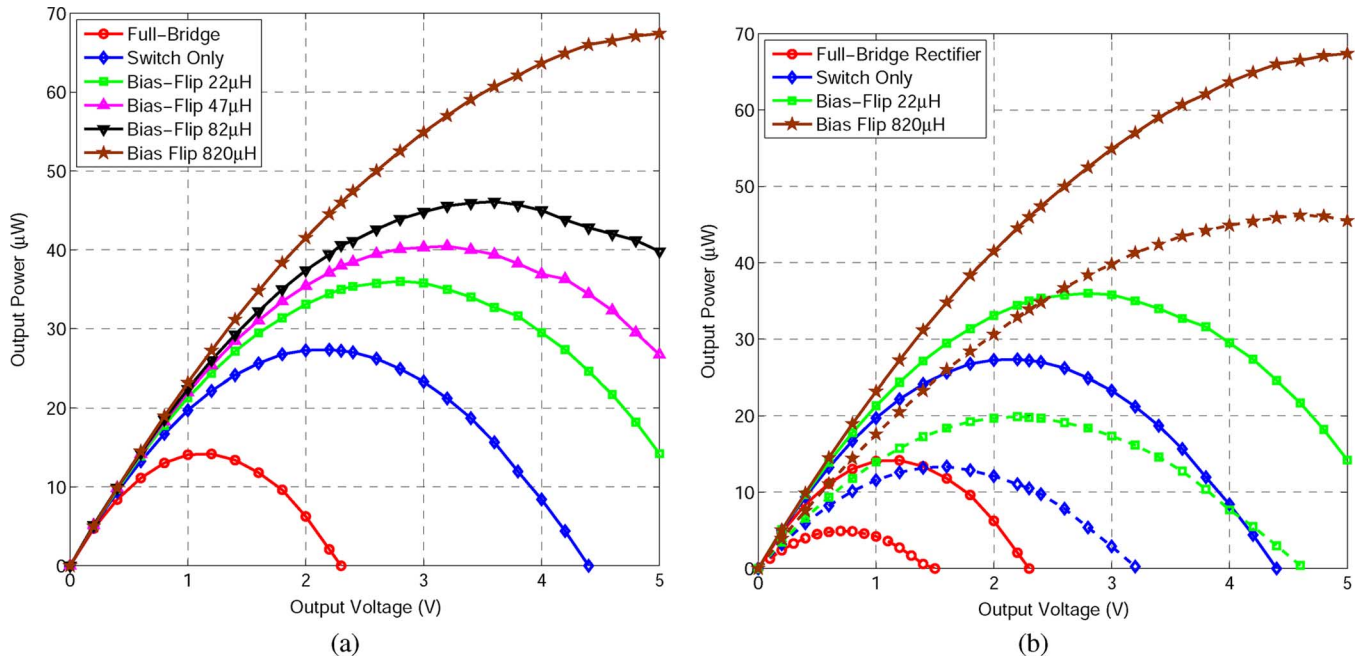

Fig. 21. (a) Measured electrical power output by the piezoelectric energy harvester with off-chip diodes ($V_D = 0.05$ V). (b) Effect of on-chip diodes ($V_D = 0.38$ V) in decreasing the electrical power output. Solid lines: Off-chip diodes; Dashed lines: On-chip diodes.

only rectifier, $V_{\rm RECT}$ was set to 2.2 V. The switch-only rectifier brings the voltage to ground almost instantly, thereby using the piezoelectric current i_P to only do half the job in inverting the voltage. The bias-flip rectifier with $V_{\rm RECT}$ set at 3.2 V, goes further and inverts the voltage across the piezoelectric harvester. A 47 μH inductor with a 4 Ω series resistance was used with the bias-flip rectifier.

Fig. 21(a) shows the measured power obtained at the output of the rectifier as the rectifier voltage is changed. The shaker was excited using a 225 Hz vibration with an acceleration of 3.35g for this measurement. The piezoelectric device output a sinusoidal open-circuit voltage with a frequency of 225 Hz and an amplitude of 2.4 V. The curve at the bottom with circular markers is the power output by a conventional full-bridge rectifier. The full-bridge rectifier was able to provide a maximum power output of 14 μW at an optimal rectifier voltage of 1.1 V which closely matches theoretical predictions. The switch-only rectifier shown in the curve with diamond markers improved upon the extractable power by 1.9X compared to the full-bridge rectifier. It was able to push the optimal voltage for maximal power transfer up by close to 2X. The top four curves show the power output by the bias-flip rectifier for different values of the inductor. The effectiveness of the bias-flip rectifier improves as the inductance is increased as this increases the Q of the resonant network. With an 820 μH inductor, the bias-flip rectifier was able to provide more than 4X improvement in power extracted compared to the full-bridge rectifier. These measurements were done with off-chip diodes which are close to ideal ($V_D = 0.05$ V). It was noted earlier that another big advantage of using the bias-flip rectifier scheme is that it pushes the optimal voltage for power extraction to be higher than that obtained using only a full-bridge rectifier as can be seen from Fig. 21. This helps in reducing the effect of the losses which occur when diode non-idealities are introduced. When these same measurements were done with on-chip diodes ($V_D = 0.38$ V) as shown in Fig. 21(b), the improvement in power extracted on using a bias-flip rectifier increases to above 8X compared to the full-bridge rectifier.

Fig. 22 shows measured waveforms of the voltage at one end of the shared inductor $L_{\rm SHARE}$ when accessed by the buck converter followed by the boost converter. When ACK_BUCK is high, the buck converter uses the inductor. It turns its pMOS power transistor ON first followed by its nMOS power transis-

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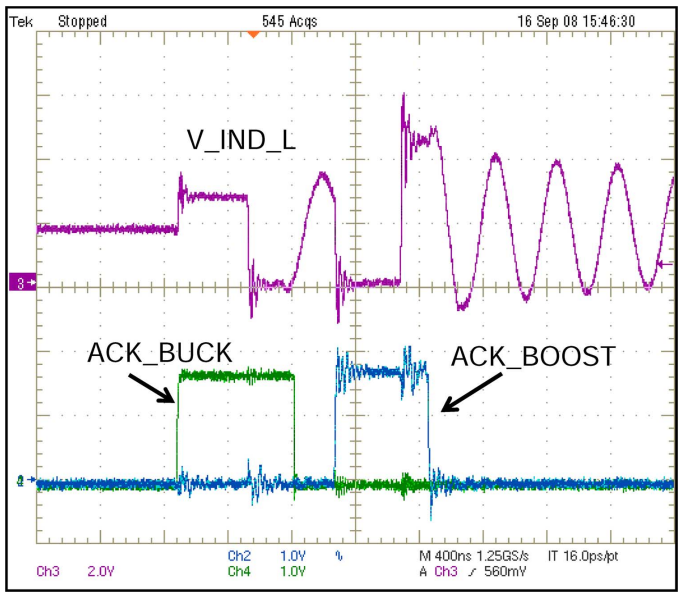

Fig. 22. Measured waveform of the voltage at one end of L_{SHARE} that demonstrates inductor sharing.

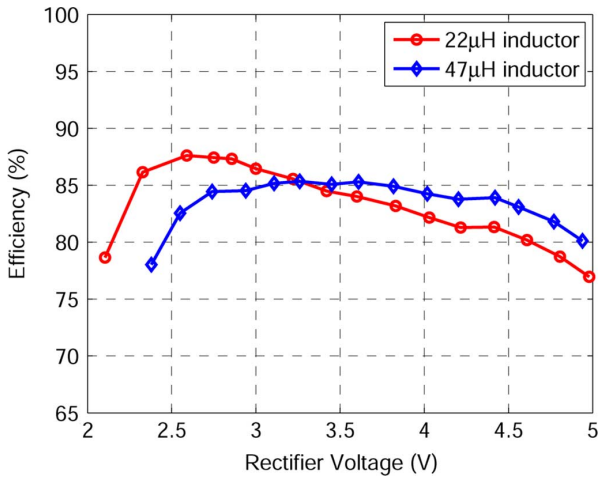

Fig. 23. Measured efficiency of the buck converter with the shared inductor.

tor. The node voltage at the left end of L_{SHARE} reflects this by going close to V_{RECT} when the pMOS is ON and being close to 0 when the nMOS is ON. Once both the power transistors are OFF, the buck converter releases the inductor which causes ACK_BUCK to go low. In this scenario, the boost converter requests the inductor at the same time the buck converter requests it. Due to the inbuilt priority in the arbiter, the buck converter is given access first. After ACK_BUCK goes low, the boost converter is given access. When the boost converter is active, it turns its nMOS power transistor ON first followed by its pMOS transistor. This can be seen from the node voltage which stays close to 0 when the nMOS is ON and close to V_{HIGH} ($\sim$5 V) when the pMOS transistor is ON. Once both transistors turn OFF, the boost converter releases the inductor. The ringing seen in the voltage V_IND_L is due to the parasitic capacitance at that node which resonates with L_{SHARE}. The voltage will eventually settle at V_{STO} due to the resistance along the path.

Fig. 23 shows the measured efficiency of the buck converter with change in the rectifier voltage with the shared inductor in use. The DC-DC converter achieves an efficiency of around 85% across the voltage range when handling a current of only 20 μA. At the lower values of V_{RECT}, the efficiency is primarily limited by switching losses and at the higher values, by conduction losses. The inductor sharing approach leads to a compact system with only a small drop of (2–3%) in efficiency. On connecting the rectifier to the buck DC-DC converter and using a 47 μH inductor, a total output power of 32.5 μW is obtained at the storage capacitor C_{STO}. This power output is after taking into account the efficiency of buck and boost regulators and the power consumed by the control circuitry which is less than 2 μW.

XI. Conclusion

This paper has identified problems that exist with the rectifier schemes that are commonly used to extract power out of piezoelectric energy harvesters. Mathematical expressions for the power extractable using different rectifier schemes were presented and they match well with simulated and experimental results. New rectifier designs were introduced that can improve the power extracted from piezoelectric harvesters by greater than 4X compared to commonly used full-bridge rectifiers and voltage doublers. In systems where it is prohibitive to use an inductor to improve power output, a switch-only rectifier scheme was proposed that could improve the extracted power by 2X with the help of a simple switch. The inductor used by the bias-flip rectifier was shared efficiently with a multitude of DC-DC converters used within the system leading to a compact and cost-efficient solution. A complete power management solution which includes the rectifiers and DC-DC converters was provided.

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