27.1 A Batteryless Thermoelectric Energy-Harvesting Interface Circuit with 35mV Startup Voltage

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Energy harvesting is an emerging technology with applications to handheld, portable and implantable electronics. Harvesting ambient heat energy using thermoelectric generators (TEG's) [1] is a convenient means to supply power to body-worn electronics and industrial sensors. Using TEG's for body-wearable applications limits the output voltage to 50mV for temperature differences of 1-2K usually found between the body and ambience. Several existing systems [2, 3] use a battery or an initial high voltage energy input to kick-start operation of the system from this low voltage. Further, changing external conditions cause the voltage and power generated by the TEG to vary, necessitating efficient control circuits that can adapt and extract the maximum possible power out of these systems. In this paper, a battery-less thermoelectric energy harvesting interface circuit which uses a mechanically assisted startup circuit to operate from 35mV input is presented. An efficient control circuit that performs maximal end-to-end transfer of the extracted energy to a storage capacitor and regulates the output voltage at 1.8V is demonstrated.

Figure 27.1.1 shows the startup circuitry that is used to kick-start the energy extraction process from the TEG. The TEG can be modeled as a voltage source (V_T) in series with a resistance (R_T) [1], where V_T is directly proportional to the temperature difference applied across the TEG. The TEG used in this paper has an R_T of 5Ω and provides a V_T of 25-50mV for small temperature differences of 1-2K. In the absence of other energy sources, the input voltage has to be boosted to above 1V to operate electronics in the CMOS process employed. Since the interface circuit designed is intended for body-wearable applications, small mechanical vibrations present in the movement of humans is put into use in a mechanically assisted startup circuit shown in Fig. 27.1.1. The switch S1 is a mechanical spring which turns ON and OFF on the application of very small amount of vibration caused by human motion. When S1 is ON, the voltage available from the TEG causes current to flow in the inductor L_{START}. When the switch turns OFF, the current in the inductor is cut off causing the diode M1 to turn ON and charge the on-chip capacitor C_{DD}. This mechanical switch can be miniaturized into a MEMS scale device to startup the circuit.

L_{START} and C_{DD} are suitably sized such that the closing and opening of S1 enables a 35mV input from the TEG to charge C_{DD} above 1V. This triggers internal clock and reference voltage generator blocks which deliver the *CLK* and V_{REF} (0.7V) signals respectively. The clocked comparator then activates the CMOS switch M2 to help pump in further charge into C_{DD} through the inductor L_{START}. The *CHG_VDD* signal is activated whenever V_{DD} is less than 1.8V and the comparator helps maintain V_{DD} close to 1.8V. The mechanical switch S1 is used only once initially to kick-start the system. No other external inputs are required.

Figure 27.1.2 shows the architecture of the thermal harvesting system. The storage block is necessary to act as a buffer to energy obtained from the TEG. When V_{DD} goes above 1.8V, power from the TEG is diverted towards the storage capacitor C_{STO}. The voltage V_{STO} varies depending on the power available from the TEG and the power consumed by the load. Hence, it cannot be used to directly power load circuits. A DC-DC converter is used after C_{STO} to transfer energy to the load at a constant voltage of 1.8V. The DC-DC converter block is activated only after V_{STO} goes above 2.4V for efficient energy transfer. V_{DD} is used as the control voltage for both the storage and DC-DC converter blocks.

The storage block shown in Fig. 27.1.3 is essentially a boost converter and acts as the energy buffer in the system. During the rising edge of a *CLK* signal, if the comparator in Fig. 27.1.1 senses that V_{DD} is greater than 1.8V, the *CHG_VSTO* signal goes high. This turns on M4 and causes current to flow in the inductor L_{STO}. Once *CHG_VSTO* goes low, M4 turns OFF and M3 is turned ON. Unlike the start block, the switch M3 in the storage block is used as a synchronous rectifier. Zero-current switching (ZCS) of the inductor current is obtained using a closed-loop control of the pulse width of signal *PG*. If M3 is turned OFF too early, the parasitic diode along M3 turns ON pushing the voltage at *VX_STO* to go above V_{STO}. This is sensed by the comparator COMP2 to suitably increase or decrease the ON-time of M3 in a closed loop fashion to achieve ZCS.

Fig. 27.1.4 shows the DC-DC converter that is used to regulate V_L at 1.8V. The converter is a synchronous rectifier buck regulator and employs PFM mode of control [5]. The buck converter is active only when V_{STO} goes above 2.4V. COMP3 takes care of this by gating the clock to COMP4. The comparator COMP4 helps to regulate V_L at 1.8V. For the buck regulator, the PMOS ON-time is fixed and the NMOS ON-time is controlled in a closed-loop fashion to achieve ZCS. Here, if the NMOS is OFF too early, the diode along M6 turns ON forcing *VX_DCDC* to go below ground. This is detected by COMP5 to suitably adjust the NMOS ON-time to achieve ZCS.

Once V_L reaches 1.8V, the capacitors C_{DD} and C_L are shorted and the signal *VDD_VL* shown in Fig. 27.1.1 goes low. Since C_{DD} is now charged through the buck converter (the L_{START}, M1/M2 path is disabled), the storage boost converter runs at a constant frequency f_{CLK} and presents an equivalent resistance R_{EQ} to the TEG. f_{CLK} is suitably set such that R_{EQ} is the same as R_T as shown in Eq. 1.

$$Power\,(P_{STO}) = \frac{V_{TH}^{\ 2}}{8L_{STO}f_{CLK}} \Rightarrow R_{EQ} = 8L_{STO}f_{CLK}$$
$$R_{EQ} = R_T \Rightarrow f_{CLK} = \frac{R_T}{8L_{STO}} \quad (1)$$

Thus, by just fixing f_{CLK} to a value that can be determined at design time, the interface circuit can achieve maximum transfer of the harvested power with varying thermal conditions.

Figure 27.1.5a shows measured waveforms of the startup sequence. This measurement was done with a 50mV input voltage in series with a 5Ω resistance. No external clocks or voltage references were used for the measurements. The mechanically assisted startup raises V_{DD} close to 1V which then turns ON the start block to boost V_{DD} to above 1.8V. Once V_{DD} goes above 1.8V, the storage block is enabled as seen by the rise in V_{STO}. The start block keeps V_{DD} close to 1.8V while powering up the storage block. Only after V_{STO} reaches 2.4V is the DC-DC buck converter enabled to power V_L. While V_L is getting powered, the voltage V_{STO} stays almost constant at 2.4V. Once V_L reaches 1.8V, the capacitors C_L and C_{DD} are shorted together. From this point on, both V_{DD} and V_L have overlapping waveforms. Figure 27.1.5b shows the measured power obtained at the output of the DC-DC converter for varying V_T's compared to the maximum power available from the TEG. The interface circuit provides a peak overall end-to-end efficiency of 58%. The TEG used provides 25mV/K of temperature difference and occupies an area of 10cm^2.

The performance of the presented circuit is compared to state-of-the-art circuits in Fig. 27.1.6. The proposed circuit can startup from 35mV and provides the best end-to-end efficiency through efficient control circuits and maximum power tracking. The circuit incorporates a storage block and provides a regulated 1.8V output to the load.

Figure 27.1.7 shows the die photo of the test chip fabricated in a 0.35µm CMOS process. The active area of the TEG interface circuitry together with the on-chip capacitor C_{DD} is 1.7mm^2.

Acknowledgements:
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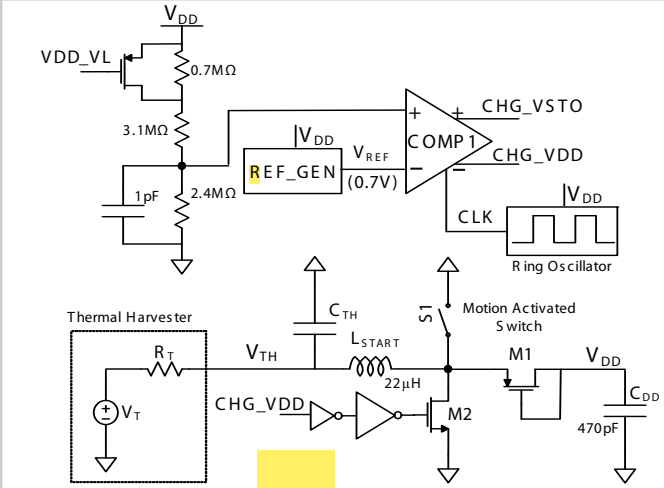

Figure 27.1.1: Low voltage startup circuit for energy extraction from the TEG. The switch S1 is a motion activated discrete mechanical switch which needs to toggle once to start the system. *VDD_VL* is at V_{DD} during the startup process.

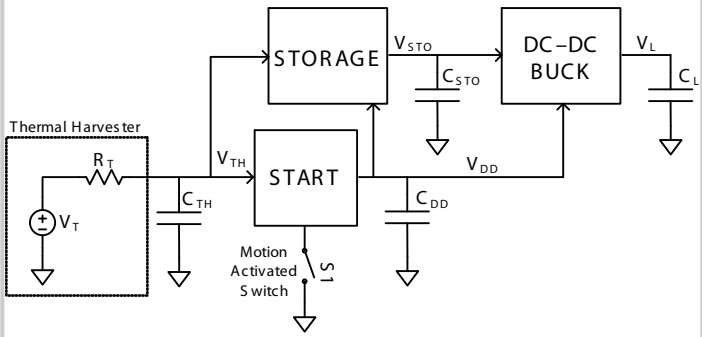

Figure 27.1.2: Architecture of the thermoelectric energy harvesting system. The START block is used to kick-start the energy extraction process. During steady state, energy flows through the STORAGE and DC-DC blocks, bypassing the START block.

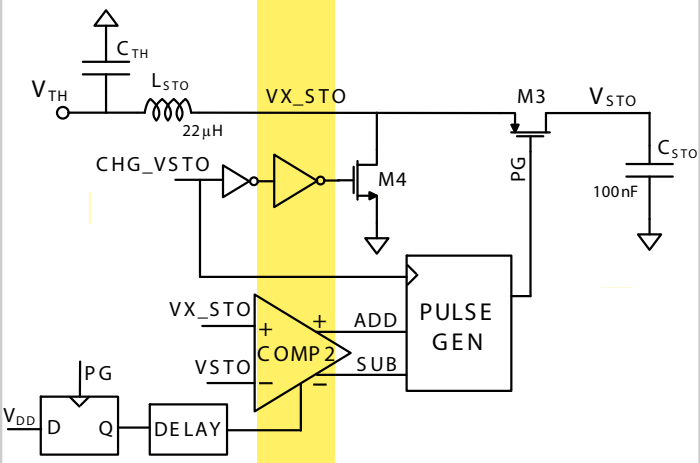

Figure 27.1.3: Storage circuit to transfer energy from the thermal harvester to the storage capacitor C_{STO}. The comparator and pulse generator help to achieve closed loop zero-current switching of the current through L_{STO}.

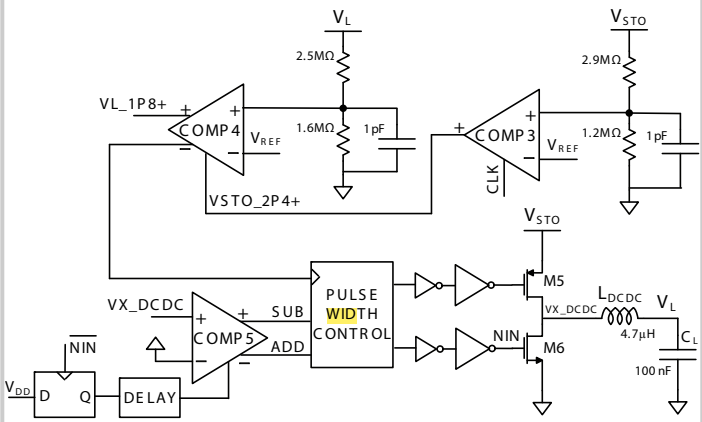

Figure 27.1.4: Architecture of the buck DC-DC converter to provide a regulated 1.8V output. The buck converter gets activated only after V_{STO} goes above 2.4V.

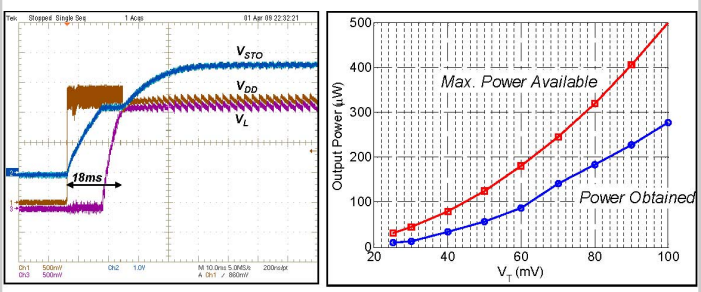

Figure 27.1.5: (a) Measured waveforms of the voltages within the thermal harvesting circuit during startup from a 50mV input voltage (b) Measured electrical power obtained at the output of the buck converter compared to the maximum power available from the TEG.

Parameter	Lhermet [1]	Doms [2]	Carlson [3]	EnOcean [4]	This work
Process	0.35µm	0.35µm	0.13µm	n/a	0.35µm
Min. input voltage	1V	0.6V	20mV	20mV	25mV (35mV to startup)
External voltage?	None	2V battery	Minimum of 650mV	None	None
Output Voltage	1.75V-4.3V	2V	1V regulated	4V-4.5V	1.8V regulated
Peak efficiency	50% (just boost converter)	70% (just boost converter)	52% (end-to-end)	20% (end-to-end)	58% (end-to-end)
Maximum Power Tracking?	No	Yes	No	No	Yes

Figure 27.1.6: Comparison of the state-of-the-art power management circuits for thermal energy harvesting. End-to-end efficiency is defined as the ratio of the power provided to the output to the maximum power available from the TEG.

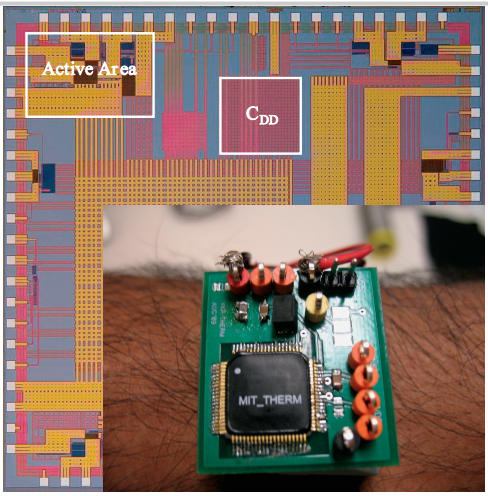

Figure 27.1.7: Die photo of the thermal energy harvesting interface circuit identifying the area consumed by the active blocks and C_{DD}. The inset shows the thermal harvesting chip worn on the arm of a person. The PCB occupies 7.5cm² in area.

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