Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module

Xunwei Zhou, *Member, IEEE*, Mauro Donati, Luca Amoroso, and Fred C. Lee, *Fellow, IEEE*

***Abstract*—A DC/DC converter with high efficiency over a wide load range is necessary for many low voltage applications, such as battery supplied systems and micro-processor power supplies—Voltage Regulator Module (VRM). In order to improve the efficiency of low voltage converters, synchronous rectifier technology is widely used. The disadvantage of this technology is low efficiency at light load. This paper proposes a new technology, which utilizes the duty cycle signal, to improve light load efficiency with simple implementation. Since current sensors are not required, high density and high efficiency can be achieved that makes the whole circuit suitable for integration. In the paper, two application examples are given. Experimental results verified that the proposed control schemas significantly improve the efficiency of synchronous rectifier buck converters at light load.**

***Index Terms*—Light load, high efficiency, duty cycle.**

I. Introduction

THE ever-present demands for faster and more efficient data processing have prompted a significant development effort in the area of low-voltage IC's. Currently, 3.3-V IC's are gradually replacing the standard 5-V IC's due to their better speed/power-consumption performance and higher integration densities. However, the 3.3 V is only a transitional stage to IC's with even lower voltages that will not only further improve the speed and reduce the power consumption of IC's but also will allow direct, single-cell battery operation. It is expected that next generations of the data processing IC's will require power supplies with a 1–3 V output voltage range [1].

At the same time, since more devices are packed on a single processor chip and the processors operate at higher operating frequencies, microprocessors need aggressive power management. Future generation processors' will draw current from 13 A to 30 A $\sim$ 50 A [2]. The load range may reach from 1% to full load. On the other hand, as the speed of the IC's increases, they are becoming more dynamic loads to their power supplies. Next generation microprocessors are expected to exhibit current slew rates of 5 A/ns. With all these requirements, voltage regulator modules (VRM's), which feed these loads, have to have high efficiency, fast transient response and high power density.

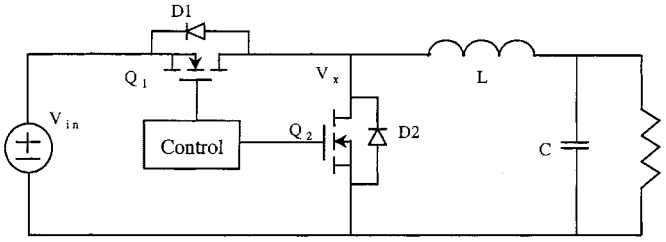


Fig. 1. Synchronous rectifier buck VRM.

Most VRM's use synchronous rectifier buck topology as shown in Fig. 1. This topology increases the efficiency of low-output-voltage DC-to-DC converters by replacing the freewheel diode in a conventional buck converter with a MOSFET. To achieve fast transient response and high power density, synchronous rectifier buck converter must have small filter inductance. The disadvantage of this topology is its low efficiency at light load, due to the higher conduction loss and gate drive loss. Actually, this is a common drawback to the synchronous rectifier type of converters. However, for many low-voltage applications, like mobile and portable and battery applications, VRM's are always expected to be implemented with advanced power management functions to further reduce the power consumption at light load, in order to extend the battery-operation time in portable systems or to facilitate the compliance with various "energy star" ("green" power) requirements in office systems. Therefore, it is very important that VRM's have high efficiency at light load.

This paper proposes a new technique that can improve light load efficiency by utilizing the duty cycle signal. Since current sensors are not required by this technique, high density and high efficiency can be achieved that makes the whole circuit suitable for integration. In this paper, four improved approaches are proposed and verified with experimental results. The first two is designed for the fixed frequency controlled VRM's. The left two is designed for the hybrid mode controlled VRM's [3] whose switching frequency changes proportionally to the load at light load and keeps constant at heavy load.

II. Challenge in Synchronous Rectifier Buck VRM

Today's VRM's have large output filter inductance. During the transient, this large inductance limits the energy transfer from the VRM input to the output and almost all the energy is provided by VRM output capacitors. For future application,

Manuscript received December 21, 1998; revised November 19, 1999. This work was supported by Intel, Texas Instruments, National Semiconductors, Inc., SGS Thomson, Delta Electronics Inc., ERC Shared Facilities, and the National Science Foundation under Award EEC-9731677. Recommended by Associate Editor N. Femia.

X. Zhou is with Volterra Company, Fremont, CA 94538 USA (e-mail: wzhou@volterra.com).

M. Donati and L. Amoroso are with Magnetek S.P.A, Rome, Italy.

F. C. Lee are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA.

Publisher Item Identifier S 0885-8993(00)07320-8.

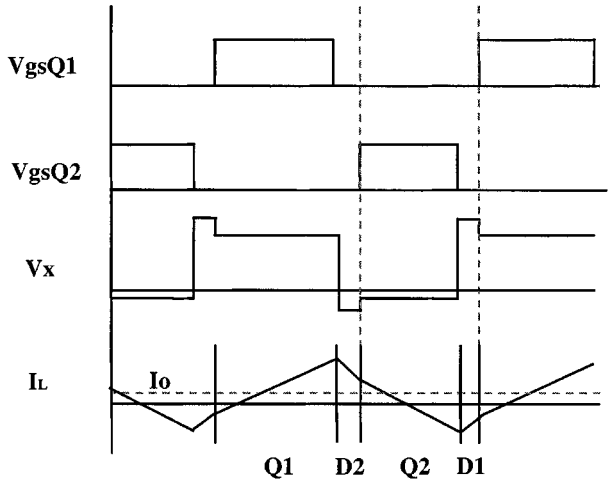


Fig. 2. Light load inductor current of a synchronous rectifier buck VRM with filter small inductance.

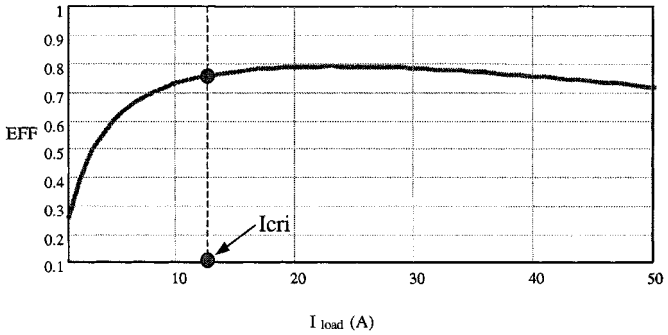


Fig. 3. Efficiency of 4-module interleave QSW VRM.

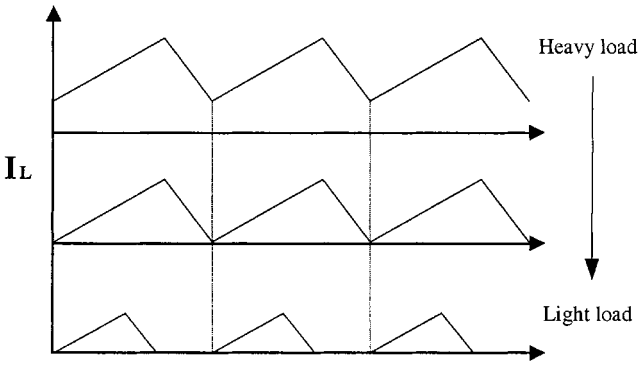


Fig. 4. Approach A: fixed frequency control.

with the higher load current and tighter voltage tolerance requirements, more decoupling capacitors (on board capacitors) and VRM output bulk capacitors will be needed to reduce the voltage spike. More capacitors are used to reduce ESR, ESL and to provide energy [4]. As a result, in order to meet future specifications, 23 times of the decoupling capacitors are needed and three times the bulk capacitors are needed. Since the computer motherboard real estate is relatively expensive, the future on-board VRM's have to have high-power densities as well as high efficiencies. The need for a large quantity of capacitors makes the VRM's impractical for future microprocessors.

To overcome the limitation occurring in the conventional VRM's, synchronous buck converter with smaller output filter inductance is more desirable in VRM applications to increase the energy transfer speed. The VRM's with small inductance (one-tenth inductance used in today's VRM), like quasisquare-wave (QSW) VRM, only needs very small filter capacitance to meet transient requirement and can realize very high power density [5]. The disadvantage of the small inductance VRM is its large current ripple, which in turn makes its light load efficiency very low. For synchronous rectifier buck VRM, since the main switch and the synchronous rectifier switch are always complementarily on. Its inductor current can go negative at light load. Fig. 2 shows the inductor current of a low-inductance synchronous rectifier buck VRM at light load. The negative current represents the circulating energy. The smaller the inductance, the larger the circulating energy, the larger the conduction loss, and the lower the efficiency at light load. Besides, with synchronous rectifier, the additional gate drive loss and switching loss make the synchronous rectifier buck VRM have very low light load efficiency. Fig. 3 shows the efficiency of a QSW VRM. It can be seen that light load efficiency is lower than 50%.

There are several approaches to improve VRM efficiency at light load. The first approach is fixed frequency control: prevent the inductor current from going negative and force the inductor current to go into discontinuous mode (DCM) operation after current lower than the critical current Icri shown in Fig. 3. This can reduce VRM conduction loss at light load. So as to improve the efficiency. The inductor current waveforms at different load are shown in Fig. 4.

The second approach is hybrid mode control: fixed frequency control is used at heavy load; when the load is lower than the critical current value, VRM switching frequency is reduced proportionally to the load. With hybrid mode approach, the inductor current is forced to operate in DCM mode. Its conduction loss is reduced at light load. Meanwhile, its gate drive loss is also minimized because of its lower switching frequency. As a result, VRM can have very high efficiency at light load. The inductor current waveform at different load operation and the predicted efficiency for different control schemes are shown in Figs. 5 and 6, respectively. The VRM light load efficiency is constant when variable frequency control is used [6], [7]. With variable frequency control, no matter what constant on or constant off control, the inductor current peak value is constant. In DCM mode, synchronous rectifier buck conduction loss is proportional to the switching frequency. Also, its gate drive loss and switching loss is proportional to the switching loss. As a result, its total loss is proportional to the switching frequency:

$$P_{\text{loss}} = k_1 \times f_s. \tag{1}$$

Where, k_1 is a constant and f_s is switching frequency. In hybrid mode control, at light load, the switching frequency is proportional to the load current. The output power is proportional to the switching frequency:

$$P_{\text{out}} = I_o \times V_o = (k_2 \times f_s) \times V_o. \tag{2}$$

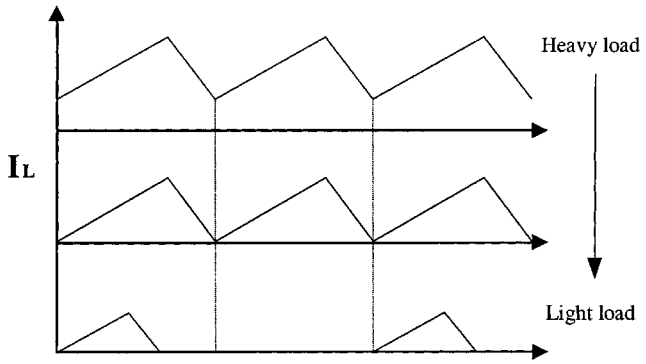


Fig. 5. Approach B: hybrid mode control.

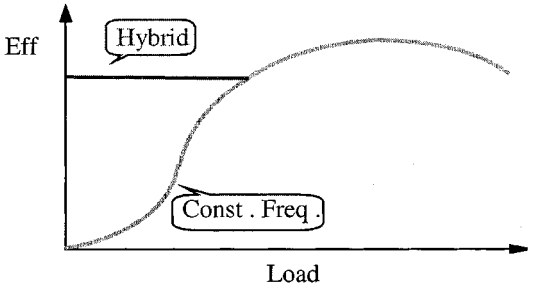


Fig. 6. VRM efficiencies under different control.

Where, k_2 is a constant. The synchronous rectifier buck converter efficiency is:

$$\eta = 1 - \frac{P_{\text{loss}}}{P_{\text{out}} + P_{\text{loss}}} = 1 - \frac{k_1}{k_2 \times V_o + k_1}. \tag{3}$$

Obviously, this efficiency is a constant.

The difficulty of these two approaches is how to turn off synchronous rectifier automatically when the inductor current goes negative at light load. The same question is how to predict inductor current when it changes from continuous current mode (CCM) mode to DCM mode. Actually, for the synchronous rectifier buck, the inductor can change from DCM mode to CCM mode automatically. When the load changes from heavy load to light load, it cannot detect the mode change automatically. It needs to sense the inductor current to tell the switches when the converters operate in DCM. With a conventional approach, current transformers are too bulky and expensive; sensing resistors reduce conversion efficiency significantly. So, the challenge is how to detect the critical point between CCM and DCM automatically without using current sensor.

III. Detect Inductor Current Mode Automatically

Many papers discuss the current detecting approach without current sensing. In [3], it forced the converter to operate in DCM periodically, which causes an output voltage spike when the inductor current changes from CCM to DCM. In [6], it took advantage of the inductor winding resistance and controlled the peak value of inductor current. In practice, low winding resistance is required for low-voltage high-current VRM's to achieve high efficiency, this approach is very complicated and noise sensitive. The simplest way to detect an inductor current is to use the

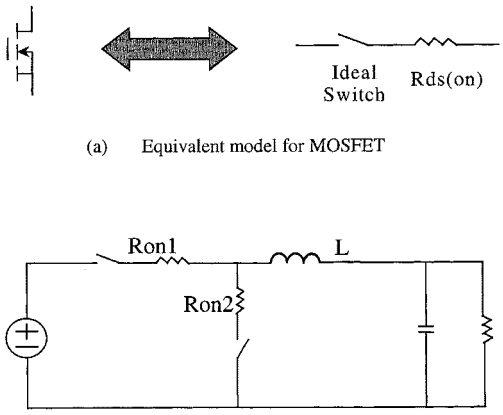


Fig. 7. Equivalent model. (a) Equivalent model for MOSFET. (b) Equivalent model for synchronous rectifier.

MOSFET on-resistance, $R_{ds,\text{on}}$, by measuring the voltage drop (V_{ds}) across the MOSFET when MOSFET is on. The measured peak voltage represents the inductor peak current.

$$V_{ds,\text{peak}} = I_{L,\text{peak}} \times R_{ds,\text{on}} \tag{4}$$

In fact, the V_{ds} waveform of low $R_{ds,\text{on}}$ MOSFET is very noisy. As a result, it is really difficult to utilize the peak signal of V_{ds}. To avoid the noise problem, the best way is to measure average inductor current. Now the question is how to measure average inductor current without traditional current sensing approach. If V_{ds} is used to estimate the average load current, the approach will be very complicated, because V_{ds} includes too much information, such as dead time, load current, duty cycle information, parasitic inductance and R_{ds}, on.

Normally, the duty cycle of a buck converter with CCM operation shown in Fig. 1 can be expressed as

$$D = \frac{V_o}{V_{\text{in}}}. \tag{5}$$

However, this is not precise in the low-voltage high-current application. The equivalent model of a synchronous rectifier is shown in Fig. 7. The duty cycle is given by

$$D = \frac{V_o + I_o \times R_{\text{on2}}}{V_{\text{in}} + I_o \times (R_{\text{on2}} - R_{\text{on1}})}. \tag{6}$$

where R_{on1} and R_{on2} are on-resistance of top and bottom switch, respectively. I_o is the average of inductor current and V_o is output voltage. For low-voltage high-current application, V_o is low; V_{in} is large; I_o is high. Compared with effect of $I_o * (R_{\text{on2}} - R_{\text{on1}})$, $I_o * R_{\text{on2}}$ is more significant. (6) can be simplified as

$$D = \frac{V_o + I_o \times R_{\text{on2}}}{V_{\text{in}}}. \tag{7}$$

Since the input voltage and the output voltage are fixed, the duty cycle changes with load. For example, when V_{in} 5 V, V_o 2 V, R_{on2} 14 mΩ and the load changes from 0 A to 30 A, the duty cycle will change from 0.4 to 0.48. By detecting the

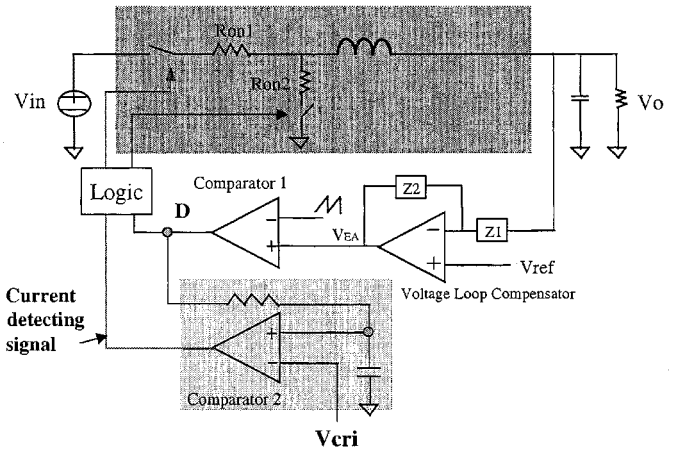


Fig. 8. Automatically detecting inductor current.

change of duty cycle, the average inductor current can be estimated. In fact, duty cycle signal can be expressed as a voltage signal in the control. This voltage signal can be used to tell the switches whether the inductor current is larger than the critical current. Fig. 8 shows the operation function block. Like a traditional control loop design, there is a voltage loop compensator. The error signal generated by voltage loop compensator is compared with the ramp signal in comparator 1. The output of comparator 1 is the duty cycle signal. The duty cycle signal is compared with $V_{\rm cri}$ to generate the current detecting signal that tells whether inductor current should be in CCM mode or DCM mode. The reference voltage of comparator 2, $V_{\rm cri}$, is proportional to $D_{\rm cri}$, which is the critical duty cycle when the inductor current reaches the critical point $I_{\rm cri}$. $D_{\rm cri}$ is

$$D_{\rm cri} = \frac{V_o + I_{\rm cri} \times R_{\rm on2}}{V_{\rm in}}. \tag{8}$$

Usually, the on-resistance of MOSFET has ±20% tolerance. It's impossible to define an accurate critical point for every individual converter. Practically, $D_{\rm cri}$ is selected as (9)

$$D_{\rm cri} = \frac{V_o + I_{o,\rm cri} \times R_{\rm on2,max}}{V_{\rm in}} \tag{9}$$

where $R_{\rm on,max}$ is the maximum on-resistance value given by manufacturer's data sheet. This ensures a synchronous rectifier buck operating in DCM when the load current lower than the critical current.

IV. Improve VRM Light Load Efficiency: Fixed Frequency Control

A. Disable Synchronous Rectifier at Light Load

The control function block is the same as that shown in Fig. 8. The idea is to shut down the synchronous rectifier when the load current is lower than the critical current. Fig. 9 explains the operation. At heavy load, the synchronous rectifier buck converter operates in CCM mode. At light load, when the average duty cycle signal is lower than $V_{\rm cri}$, a disable signal is generated from comparator 2 and the synchronous rectifier is shut down.

Fig. 10 shows schematic of the power stage. The input voltage is 5 V. The output voltage is 2 V. The switching frequency

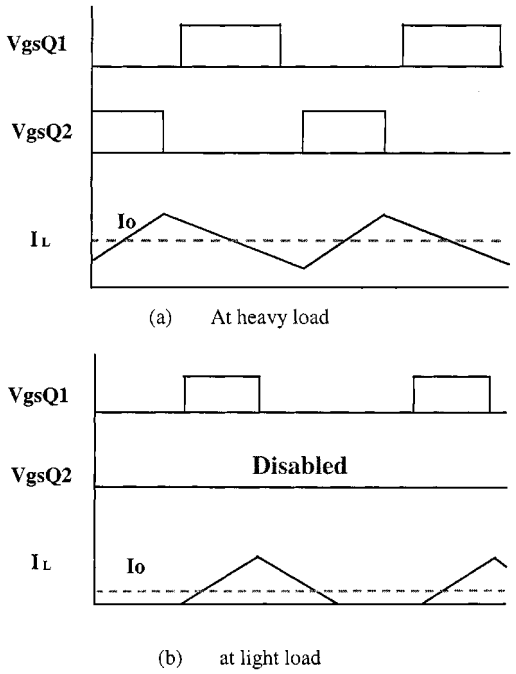


Fig. 9. Fixed frequency: disable synchronous rectifier at light load. (a) At heavy load. (b) At light load.

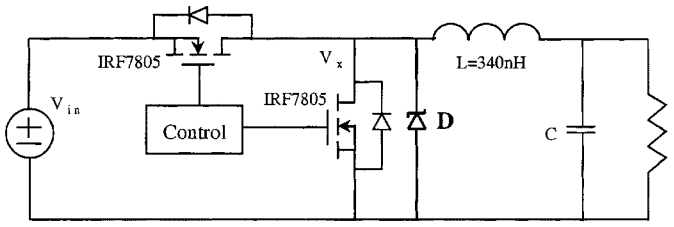


Fig. 10. Test circuit.

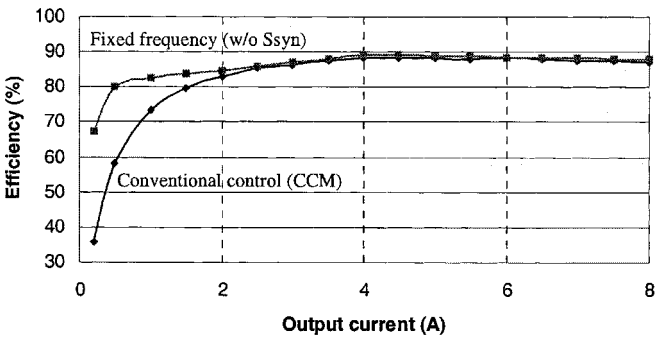


Fig. 11. Efficiency test results (including gate driver loss.

is 300 kHz. The output filter inductance is 340 nH. The load changes from 0.2 A to 8 A. The switches used here are IRF 7805. A schottky diode D, 95SQ015, is in anti-parallel with the synchronous rectifier $Q2$. At light load, $Q2$ is shut down, and the schottky diode D is used to continue the inductor current. Fig. 11 shows conversion efficiency at different load. It can be seen that it has higher efficiency for the proposed control approach than that for the conventional approach.

The results show that there is 30% improvement at light load, although the conduction loss at light load is high due to the

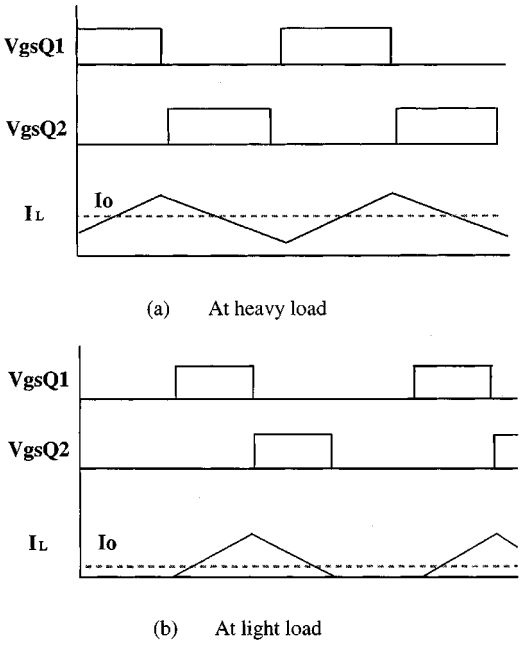


Fig. 12. Fixed frequency: with synchronous rectifier at light load.

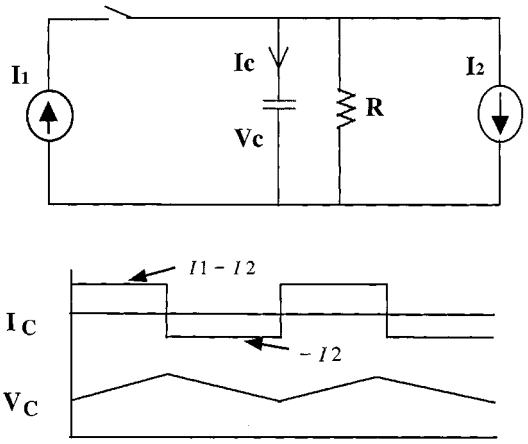


Fig. 13. The current emulating network.

schottky diode used. With this approach, the gate driver loss and switching loss of the synchronous rectifier is saved by 50%, because only one switch is operating at light load. The cost added is the anti-paralleled schottky diode.

B. With Synchronous Rectifier at Light Load

This approach is explained in Fig. 12. At heavy load, the synchronous rectifier VRM operates at CCM mode. At light load, the synchronous rectifier is turned off when the inductor current goes into negative and the VRM operates at DCM mode. In order to control the synchronous rectifier turn off timing, an inductor current emulating signal is required. Fig. 13 shows the inductor current emulating network. It is like a dual network of a synchronous rectifier buck converter. The two current sources, I_1 and I_2, is used to replace the two voltage sources, V_{in} and V_o. The resistor, R, is used to replace the inductor and is in parallel with the capacitor. In Fig. 13, $(I_1\text{-}I_2)$ is used to charge the capacitor, and the charge time is controlled by duty cycle. $-I_2$ is

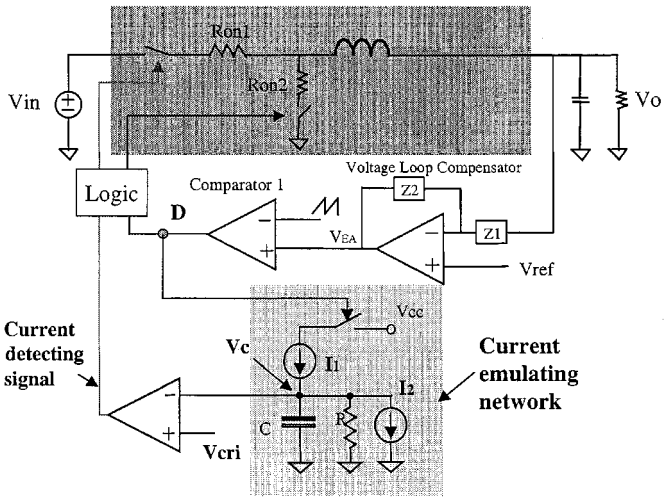


Fig. 14. Control function block for fixed frequency control.

used to discharge the capacitor. The duty cycle of the current emulating network is:

$$D = \frac{I_1 + V_{c(\text{avg})}/R}{I_2}. \tag{10}$$

Compared with (7), if I_1 and I_2 are proportional V_{in} and V_o respectively, V_c is proportional to the inductor current. For example, When V_{in} is 5 V and V_o is 2 V, if I_1 is 5 mA and I_2 is 2 mA, and if two duty cycles of the current emulating and the synchronous rectifier buck converter are the same, then V_c is

$$V_{c(\text{avg})} = \frac{I_o \times R_{\text{on}} \times R}{1000} \tag{11}$$

Therefore, the average value of V_c is proportional to the average inductor current I_o. From (11), at critical point, $V_{c(\text{avg}),\text{cri}}$ is:

$$V_{c(\text{avg}),\text{cri}} = \frac{I_{\text{cri}} \times R_{\text{on}} \times R}{1000}. \tag{12}$$

The capacitor ripple volatge is

$$\Delta V_c = \frac{(I_1 - I_2) \times D}{C \times f_s}. \tag{13}$$

At critical point, $\Delta V_{c,\text{cri}}$ is

$$\Delta V_{c,\text{cri}} = \frac{(I_1 - I_2) \times D_{\text{cri}}}{C \times f_s}. \tag{14}$$

The control function block is shown in Fig. 14. The selection of V_{cri} is according to 8. V_c signal is compared with V_{cri} to control synchronous rectifier buck DCM operation. Here, select C to meet

$$V_c = V_{c(\text{avg}),\text{cri}} + \Delta V_{c,\text{cri}} = V_{\text{cri}}. \tag{15}$$

With this control strategy, when the load changes, the inductor current of the synchronous rectifier can change the mode automatically from CCM mode to DCM mode, and vice versa. Fig. 15 shows the key control waveforms when the buck operates at heavy load. At heavy load, there is no intersection between load emulating signal V_c and V_{cri}, which means that its

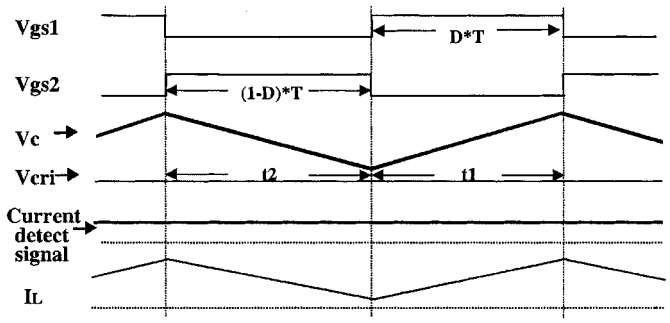


Fig. 15. Key waveforms at heavy load.

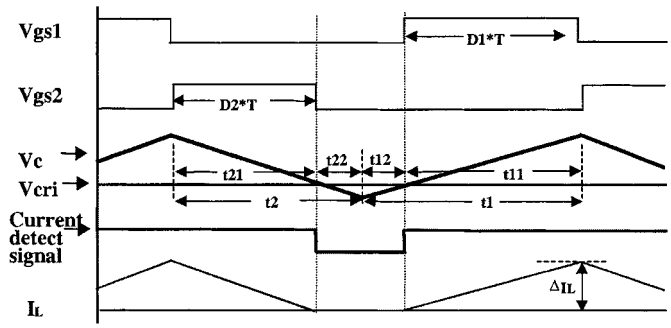


Fig. 16. Key waveforms at light load.

load current is higher than the critical current. The synchronous rectifier buck operates at CCM mode. At heavy load, in current emulating network, the capacitor C's charging time, t_1, is equal to duty cycle time, $D*T$. Its discharging time, t_2, is equal to $(1-D)*T$. There is

$$\frac{t_1}{t_2}=\frac{D\times T}{(1-D)\times T}=\frac{V_o}{(V_{\text{in}}-V_o)}. \tag{16}$$

Actually, at heavy load, the operation of this control is the same as conventional buck PWM control.

Fig. 16 shows the key control waveforms when synchronous rectifier buck operates at light load. Since the load is reduced, there is intersection between load emulating signal V_c and V_{cri}. The generated current-detect signal blocks the gate signal of the synchronous rectifier. As a result, the conduction period of the synchronous rectifier is reduced. The synchronous rectifier buck is forced to operate in DCM mode. The main switch is turned on after the current emulating signal V_c larger than V_{cri}. Then, the inductor current is charged up from zero. After duty cycle time, D_1*T, the inductor current is charged up to ΔI_L

$$\Delta I_L=\frac{(V_{\text{in}}-V_o)\times D_1\times T}{L}. \tag{17}$$

After the main switch turned off, the synchronous rectifier is turned on and the inductor current is discharged. The discharge time is D_2*T. If the inductor current is prevented from going into negative, D_2*T should be

$$D_2\times T=\frac{\Delta I_L\times L}{V_o}. \tag{18}$$

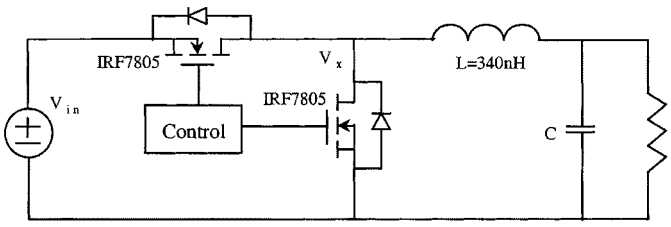


Fig. 17. Test circuit.

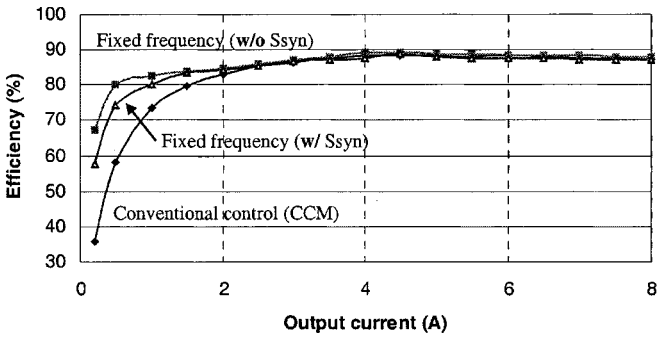


Fig. 18. Efficiency test results (including gate driver loss).

In other words, from (17) and (18), D_1*T and D_2*T should meet

$$\frac{D_1\times T}{D_2\times T}=\frac{V_o}{(V_{\text{in}}-V_o)}. \tag{19}$$

From Fig. 16, D_1*T is equal to t_{11} and D_2*T is equal to t_{21}. Therefore

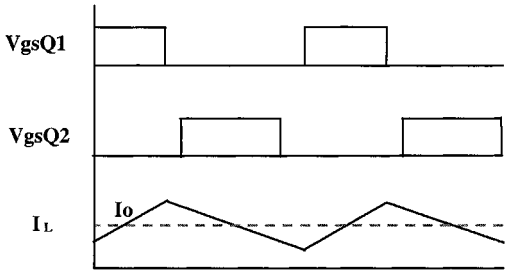
$$\frac{D_1\times T}{D_2\times T}=\frac{t_{11}}{t_{21}}=\frac{t_{12}}{t_{22}}=\frac{t_{11}+t_{12}}{t_{21}+t_{22}}=\frac{t_1}{t_2}. \tag{20}$$

From (16), there is

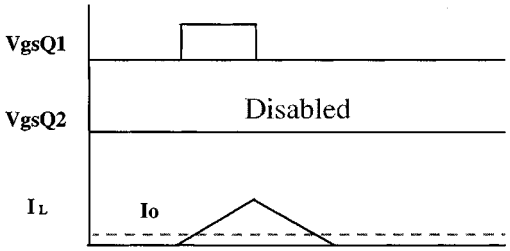
$$\frac{D_1\times T}{D_2\times T}=\frac{t_1}{t_2}=\frac{V_o}{(V_{\text{in}}-V_o)}. \tag{21}$$

With this control approach, at light load, the main switch on time and the synchronous rectifier switch on time are reduced proportional. As a result, at light load, the inductor does not go into negative and the converter conduction loss is reduced.

Fig. 17 shows the tested power stage. The switches used here are IRF 7805 and the output inductance is 340 nH. Input voltage is 5 V and the output voltage is 2 V. Switching frequency is 300 kHz. Compared with Fig. 10, there is no anti-paralleled schottky diode. In the design, the critical current is set to 4 A. The load variation range is from 0.2 A to 8 A. Fig. 18 shows the conversion efficiency with load variation. The bottom curve shows the results by using conventional control approach, which use two complementary signals to control main switch and synchronous rectifier respectively. With this control approach, because its conduction loss is reduced at light load, its light load efficiency is improved significantly. However, its light load power loss is dominated by gate drive loss of the two switches. Compared with the first approach, its light load efficiency is lower. The trade off here is the cost of the schottky diode and the light load efficiency.



(a) At heavy load: fixed frequency



(b) At light load: variable frequency

Fig. 19. Hybrid mode control: disable synchronous rectifier at light load. (a) At heavy load: fixed frequency. (b) At light load: variable frequency.

V. Improve VRM Light Load Efficiency: Hybrid Mode Control

Constant frequency control has high efficiency at heavy load when conduction loss dominates, but low efficiency at light load when switching loss dominates. The variable frequency control, proposed by Barry Arbetter in [7], results in almost uniform efficiency over the entire load range. However the efficiency is relatively low at heavy load due to high conduction loss. Hybrid mode control has fixed frequency at heavy load; after the current is lower than the critical value, the switching frequency is reduced proportionally to the load. By using hybrid mode control, the efficiency can be optimized at both heavy load and light load. [8].

A. Disable Synchronous Rectifier at Light Load

Fig. 19 shows one hybrid mode control approach. The synchronous rectifier is shut down at light load. When the load current is higher than the critical current, the converter operates in CCM mode with fixed frequency. When the load current is lower than the critical current, the converter operates in DCM mode with variable frequency. Fig. 20 shows the control function block, which is constant on time control. During the whole load range, the on time of the main switch is kept constant.

Its test circuit is the same as that shown in Fig. 10. A schottky diode is in anti-parallel with the synchronous rectifier. In the test, the load changes from 0.2 A to 8 A and the critical current is set to 4 A. Fig. 21 shows the measured efficiency curves. Compared with fixed frequency control, its light load efficiency

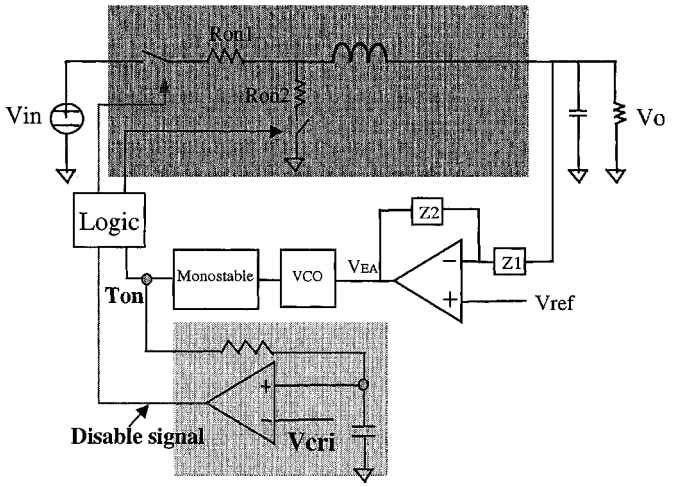


Fig. 20. Control function block for hybrid mode control: disable synchronous rectifier at light load.

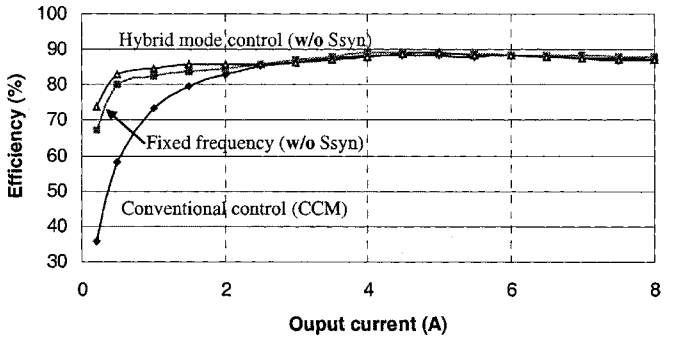


Fig. 21. Efficiency test results (including gate driver loss).

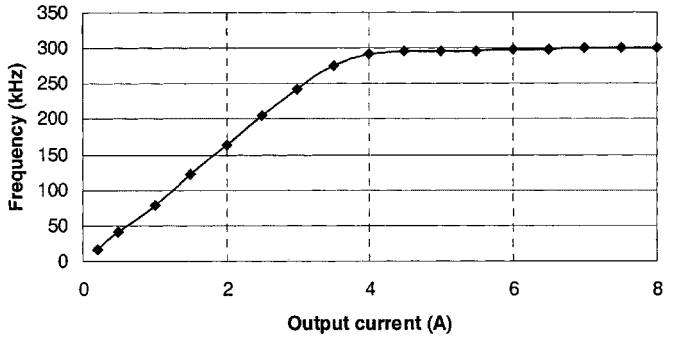
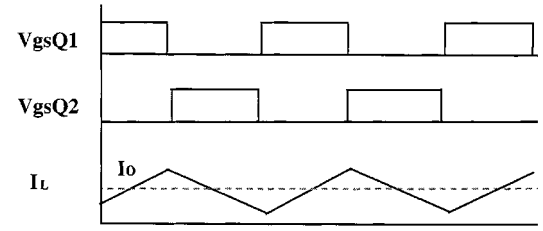


Fig. 22. The switching frequency versus the load.

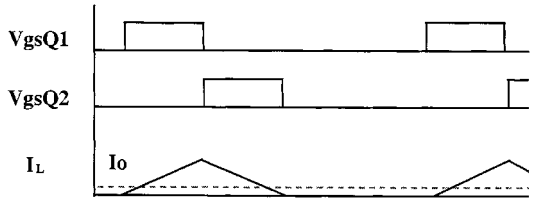
is higher. The reason is that at light load, switching frequency is reduced, as a result, the gate drive loss of the main switch is reduced. In this testing circuit, the maximum switching frequency is set to 300 kHz and the minimum switching frequency is about 15 kHz. Fig. 22 shows the switching frequency range. At heavy load, the switching frequency is fixed at 300 kHz. At light load, the switching frequency is proportional to the load.

B. With Synchronous Rectifier at Light Load

Fig. 23 explains the operation. At heavy load, the converter operates in CCM mode at fixed frequency. At light load, the synchronous rectifier is turned off when the inductor current



(a) At heavy load: fixed frequency control



(b) At light load: variable frequency control

Fig. 23. Hybrid mode control: with synchronous rectifier at light load. (a) At heavy load: fixed frequency. (b) At light load: variable frequency.

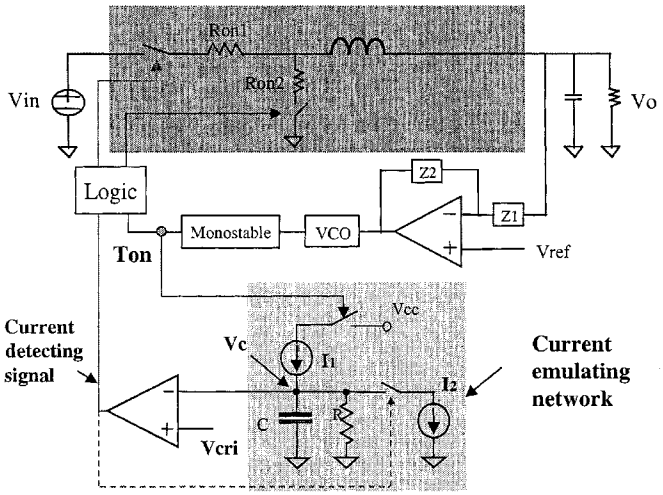


Fig. 24. Control function block for hybrid mode control: with synchronous rectifier at light load.

goes into negative and the VRM operates in DCM mode at variable frequency. Using the current emulating network shown in Fig. 13, the control function block is shown in Fig. 24. There is a little difference between Fig. 14 and Fig. 24. In Fig. 14, the control is fixed frequency control. In Fig. 24, the control is constant on time control. There is one more controlled switch in the current emulating network in Fig. 24. This switch is used to control the capacitor C in current emulating network to have constant charge time at variable frequency.

Fig. 25 shows the key waveforms at heavy load, where the converter operates in CCM mode. Since the load current is higher than the critical current, there is no intersection between current emulating signal V_c and $V_{\rm cri1}$. The synchronous rectifier buck converter operates at fixed frequency. The main switch on time is controlled by mono-stable function output. In this case,

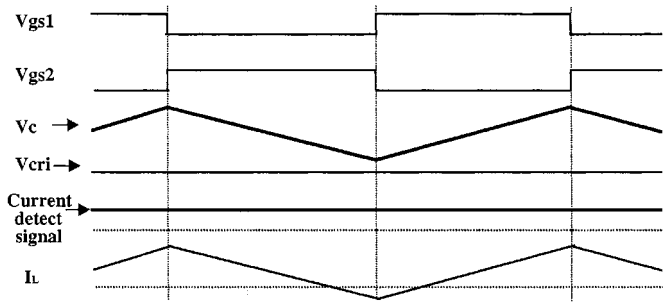


Fig. 25. Key waveforms at heavy load.

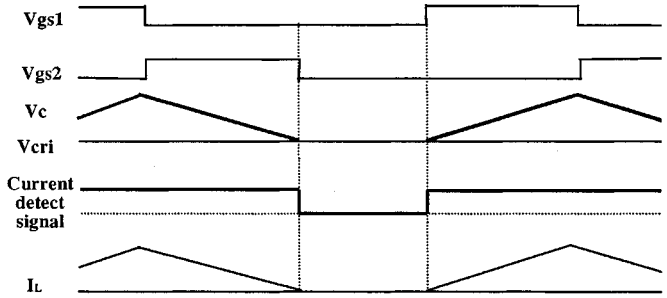


Fig. 26. Key waveforms at light load.

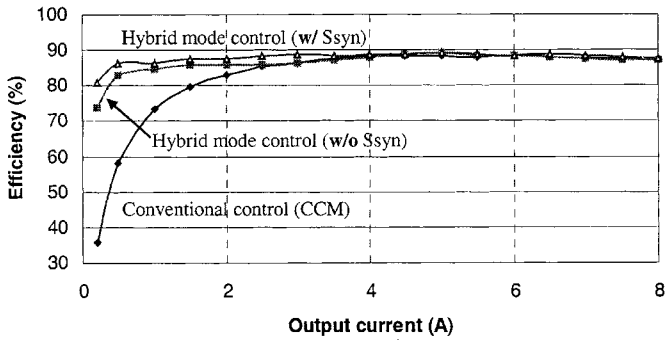


Fig. 27. Efficiency test results (including gate driver loss).

its operation is similar to the conventional approach, which uses two complementary signals to control the main switch and synchronous rectifier respectively.

Fig. 26 shows the key waveforms at light load. When the load changes from heavy load to light load, the current emulating signal Vc moves down. When the load is equal to the critical current, the current emulating signal V_c touches $V_{\rm cri1}$. Then stop discharging C. V_c is kept at $V_{\rm cri}$. At the same time, the current detecting signal is changed to low level and the synchronous rectifier is turned off. The converter is forced to operate in DCM mode. Since the on time of the main switch is constant, its switching frequency is reduced and its change is proportional to the load.

Its test circuit is the same as that shown in Fig. 17. In the test, the load changes from 0.2 A to 8 A. The maximum switching frequency is set to 300 kHz and 4 A of the critical current. Fig. 27 shows the measured efficiency. Compared with the previous approach, disable synchronous rectifier, its light load efficiency is higher. The reason is that with this approach, converter's light load conduction loss is reduced due to the use of

synchronous rectifier. It can be seen that, the converter has efficiency higher than 80% in the whole load variation range. With this approach, it is easy to optimize the converter efficiency at both light load and heavy load. Compared all other approaches, this approach has the highest light load efficiency.

VI. Conclusions

For low-voltage high-current applications, synchronous rectifier technologies are widely used. However, its light load efficiency is pretty low. To improve at light load, the converters have to operate in DCM mode to reduce its conduction loss and at lower switching frequency to reduce the gate drive loss. In this chapter, several new control approaches, which utilize the duty cycle signal to improve the efficiency at light load, are proposed. These approaches can detect inductor current mode automatically and do not need current sensors. Experimental results verify that these approaches are able to improve synchronous rectifier buck converter light-load efficiency significantly. And the hybrid mode control with synchronous rectifier at light load has the best result.

References

[1] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Design consign considerations for low-voltage on-board dc/dc modules for next generations of data processing circuits," *IEEE Trans. Power Electron.*, vol. 11, pp. 328–337, Mar. 1996.

[2] S. Goodfellow and D. Weiss, "Designing power systems around processor specifications," *Electron. Design*, pp. 53–57, Jan. 1997.

[3] T. Wang, X. Zhou, and F. C. Lee, "A low voltage high efficiency and high power density dc/dc converter," in *Proc. IEEE PESC Conf. Rec.*, 1997, pp. 240–245.

[4] P. Wong, F. C. Lee, X. Zhou, and J. Chen, "VRM transient study and output filter design for future processors," in *Proc. IEEE IECON Conf. Rec.*, 1998, pp. 410–415.

[5] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee, and D. Y. Chen, "Investigation of candidate VRM topologies for future microprocessors," in *Proc. IEEE APEC Conf. Rec.*, 1998, pp. 145–150.

[6] B. Arbetter and D. Maksimovic, "DC-DC converter with fast transient response and high efficiency for low-voltage microprocessor loads," in *Proc. IEEE APEC Conf. Rec.*, 1998, pp. 156–162.

[7] B. Arbetter, R. Erickson, and D. Maksimovic, "DC-DC converter design for battery-operated systems," in *Proc. IEEE PESC Conf. Rec.*, 1995, pp. 103–109.

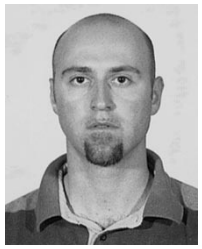
[8] X. Zhou, T. Wang, and F. C. Lee, "Optimizing design for low voltage dc-dc converters," in *Proc. IEEE APEC Conf. Rec.*, 1997, pp. 612–616.

[9] R. Redl and B. Erisman, "Designing minimum cost VRM8.2/8.3 complaint converters," in *Proc. PCIM HFPC Conf. Rec.*, 1998, pp. 172–181.

[10] J. O'Connor, "Converter optimization for power low voltage, high performance microprocessors," in *Proc. IEEE APEC Conf. Rec.*, 1996, pp. 984–989.

Xunwei Zhou (S'99) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1991 and 1994, respectively, and the Ph.D. degree from the Virginia Polytechnic Institute and State University, Blacksburg, in 1999.

He joined Volterra Semiconductor Company, Fremont, CA, in 1999. His research interest include design and control of distributed power system, high-frequency power conversion and magnetics, PFC techniques, and low-voltage power management techniques.



Mauro Donati received the B.S. degree in electrical engineering from University of Florence, Italy, in 1997.

In 1998, he joined the Virginia Power Electronics Center, Virginia Institute of Technology and State University, Blacksburg, as a Visiting Scholar. Since 1999, he has been a Research and Development Engineer with Magnetek S.P.A, Rome, Italy. His current activities are in the area of power electronics, including ac/dc PFC topologies and electronic ballast.

Luca Amoroso received the B.S. degree in electrical engineering from University of Padova, Italy, in 1995 and is currently pursuing the M.S. degree in control circuits of voltage regulator module for future generation microprocessors at the Virginia Polytechnic Institute and State University, Blacksburg.

His research activities include different areas of electronics: dc/dc converter, ac/dc converters, modeling, and control.

Fred C. Lee (S'72–M'74–SM'87–F'90) received the B.S. degree in electrical engineering from National Cheng Kung University, Taiwan, R.O.C., in 1968, and the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1971 and 1974, respectively.

He is a University Distinguished Professor at Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, and was the Lewis A. Hester Chair of Engineering at Virginia Tech and the James S. Tucker endowed professor in the Bradley Department of Electrical and Computer Engineering. He directs the Center for Power Electronics Systems (CPES), a National Science Foundation engineering research center whose participants include five universities and over 100 corporations. In addition to Virginia Tech, participating CPES universities are the University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, and the University of Puerto Rico-Mayaguez. He is also the founder and director of the Virginia Power Electronics Center (VPEC), one of the largest university-based power electronics research centers in the country. His research interests include high-frequency power conversion, distributed power systems, space power systems, power factor correction techniques, electronics packaging, high-frequency magnetics, device characterization, and modeling and control of converters.

Dr. Lee received the Society of Automotive Engineering's Ralph R. Teeter Education Award (1985), Virginia Tech's Alumni Award for Research Excellence (1990), and its College of Engineering Dean's Award for Excellence in Research (1997), the William E. Newell Power Electronics Award, the highest award presented by the IEEE Power Electronics Society for outstanding achievement in the power electronics discipline, in 1989, the Power Conversion and Intelligent Motion Award for Leadership in Power Electronics Education (1990), and the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology (1998). From 1993 to 1994, he served as President of the IEEE Power Electronics Society and, before that, as Program Chair and then Conference Chair of IEEE-sponsored power electronics specialists conferences.