50 mV-Input Batteryless Boost Converter for Thermal Energy Harvesting

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***Abstract*—A fully electrical startup boost converter for thermal energy harvesting is presented in this paper. The converter is implemented in a 65-nm bulk CMOS technology. With the proposed 3-stage stepping-up architecture, the minimum input voltage for startup is as low as 50 mV while the input voltage required for sustained power conversion is 30 mV. Due to the use of a zero-current-switching (ZCS) converter as the last stage and an automatic shutdown mechanism for the auxiliary converter, conversion efficiency up to 73% is achieved. By incorporating the boost converter and a thermoelectric generator (TEG), a miniaturized module is demonstrated for energy harvesting applications.**

***Index Terms*—Boost converter, conversion efficiency, energy harvesting, low input voltage, thermoelectric generator.**

I. Introduction

OMNIPRESENT thermal energy is one of the most eco-friendly energy sources. It is often presented as losses during other energy conversion processes and is applicable for energy harvesting in terms of a temperature gradient or a heat flow in our daily life. One important application with large-scale energy harvesting is automotive or industrial waste heat recovery. Recovering waste heat not only improves the overall efficiency but reduces the pollutions as well. Another emerging application with small-scale energy harvesting is the body heat which establishes a temperature gradient between the human body and the ambient. With recent advances in semiconductor fabrication technology, miniaturized thermoelectric generator (TEG) devices have been successfully fabricated for small-scale energy harvesting, promoting a promising application scenario of wearable electronics powered by body heat.

Limited by the physical dimension of the TEG device and the temperature difference between the human body and the ambient, the induced voltage from thermoelectric harvesting could be as low as tens of millivolts in a realistic case. Therefore, a boost converter with low input voltage is mandatory to provide a desirable output voltage as the power supply for electronic circuitry. In the past few years, efforts have been made to reduce the required input voltage of the boost converters by utilizing a pre-charge battery [1], off-chip transformers [2], mechanical switches [3] and off-chip antenna with auxiliary RF energy harvesting [4]. Due to the use of built-in batteries or bulky off-chip components, these techniques are not suitable for system integration or miniaturization. Alternatively, a boost converter with ultra-low input voltage has been reported in [5]. As a post process is needed for threshold tuning, the proposed technique is not applicable for standard CMOS technologies provided by the foundry. Recently, a miniaturized transformer has been adopted for the implementation of a low-voltage boost converter [6]. However, the conversion efficiency is generally low for an input voltage below 100 mV, making it less attractive for applications with small temperature differences. In this work, a batteryless boost converter with fully electrical startup is presented. Owing to the proposed 3-stage stepping-up architecture, the converter demonstrates a minimum input voltage of 50 mV and maximum efficiency of 73% for thermoelectric energy harvesting applications.

The paper is organized as follows. Section II introduces the architecture and operation principles of the proposed converter. Detailed circuit implementations for each building block and experimental results are presented in Sections III and IV, respectively. Finally, a concluding remark is given in Section V.

II. Proposed 3-Stage Stepping-Up Architecture

Among the energy conversion techniques, voltage multipliers are widely used to convert electric power from a lower AC voltage to a higher DC voltage. It is well suited for low-input-voltage application scenarios at the cost of conversion efficiency. On the other hand, charge pumps and switching power supplies are excellent candidates for high conversion efficiency. However, due to the need of control circuitry, such converters are not applicable when the available voltage is too low. It is obvious that none of these converter circuits mentioned above can achieve the requirements for low input voltage and high conversion efficiency simultaneously. Therefore, a hybrid-type architecture is adopted and a boost converter with three stepping-up stages is proposed for thermoelectric energy harvesting.

Fig. 1 shows the architecture of the proposed boost converter, which consists of four functional blocks: a low-voltage starter, an auxiliary step-up converter, a zero-current-switching (ZCS) controlled boost converter and peripheral controllers. As the input voltage V_{IN} exceeds the minimum value for startup, which

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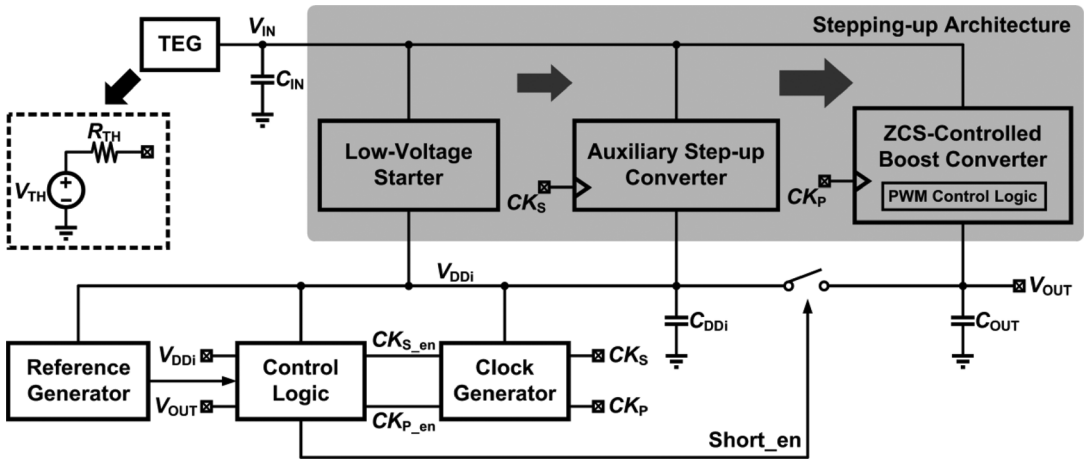


Fig. 1. Block diagram of the proposed 3-stage stepping-up architecture.

is approximately 50 mV in this particular case, the boost converter becomes operational. In order to facilitate startup at extremely low input voltage, all building blocks are initially off except for the starter, charging the internal voltage $V_{\rm DDi}$ at the cost of conversion efficiency. After $V_{\rm DDi}$ is charged up to approximately 300 mV, the logic circuits in the peripheral controllers start to work, providing a system clock $CK_{\rm s}$ with sufficient swing for the auxiliary boost converter. As the auxiliary converter stage becomes operational, the internal voltage $V_{\rm DDi}$ is boosted with an enhanced charging current into $C_{\rm DDi}$. Once $V_{\rm DDi}$ reaches a value in the vicinity of 800 mV, the high-efficiency ZCS-controlled boost converter is activated, charging the output node $V_{\rm OUT}$ by using $V_{\rm DDi}$ as the supply voltage for its control circuitry. When $V_{\rm OUT}$ increases up to 1 V, a short-enable signal goes high, shunt connecting the capacitors $C_{\rm DDi}$ and $C_{\rm OUT}$. At the same time, the auxiliary converter stage is turned off by disabling the clock signal $CK_{\rm s}$. Owing to the voltage drop at $V_{\rm IN}$ caused by a larger charging current under maximum power transfer operation with $V_{\rm IN} \approx V_{\rm TH}/2$, the low-voltage starter draws much less current at the same $V_{\rm TH}$, which is considered deactivated in this operating phase. It is noted that the automatic shutdown mechanism of the first two stages at this operating phase significantly improve the overall conversion efficiency. Finally, the ZCS-controlled boost converter is gated and regulated by the on-chip reference circuitry, providing a 1.2-V regulated voltage at the output.

III. Circuit Implementations

A. Low-Voltage Starter

The primary goal of the low-voltage starter is to perform energy conversion at an extremely low input voltage. Due to the use of the stepping-up architecture, the conversion efficiency and charging capability are considered secondary issues and can be traded for minimum input voltage. In order to achieve such design requirements, a low-voltage starter with an *LC*-tank oscillator followed by a voltage multiplier is adopted. By converting the input DC energy into an AC form via an oscillator then transforming it back to DC with a boosted level by a voltage multiplier, the minimum input voltage can be effectively reduced. A conceptual illustration is shown in Fig. 2.

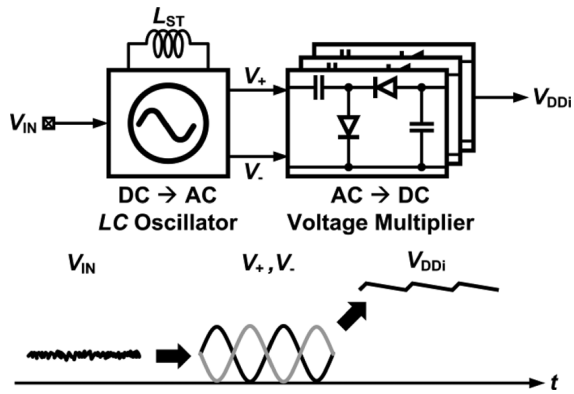


Fig. 2. Circuit architecture of the low-voltage starter.

Fig. 3(a) illustrates the circuit schematic of a simple voltage-limited *LC*-tank oscillator with NMOS cross-coupled transistors. Without transistor stacking in the oscillator topology, the entire input voltage is utilized as the gate bias for negative-$g_{\rm m}$ generation. In order to minimize the startup voltage of the oscillator, native NMOS devices with a threshold voltage close to 0 V are employed as the cross-coupled transistors. In the design of the oscillator, the first specification to be determined is the oscillation frequency. Theoretically, higher oscillation frequency enhances the conversion efficiency of the following voltage multiplier stages. However, high-frequency oscillator design encounters more challenges such as stringent startup conditions, loading effects and availability of the SMD inductor devices. In this particular starter design, an oscillation frequency of 20 to 30 MHz is chosen for circuit implementation.

The equivalent circuit of the unloaded *LC*-tank oscillator is shown in Fig. 3(b). For an inductor with a finite quality factor, the device is typically modeled by an ideal inductance $L_{\rm ST}$ and a series resistance $R_{\rm S}$. To simplify the analysis, high-Q approximation [7] is employed and the loss of the tank is represented by a shunt resistance $R_{\rm P}$ as

$$R_{\rm P} \approx \frac{L_{\rm ST}}{R_{\rm S} C_{\rm P}}, \tag{1}$$

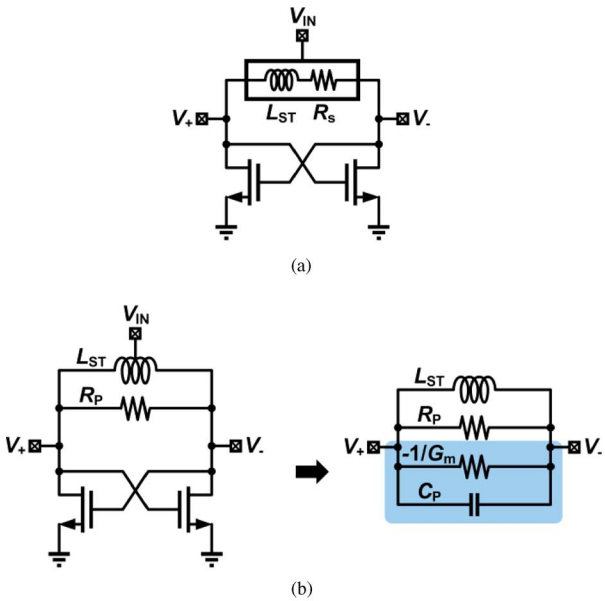


Fig. 3. Circuit schematics of (a) an unloaded *LC*-tank oscillator using high-Q approximation and (b) its small-signal equivalent circuit.

where $C_{\rm P}$ is the parasitic capacitance from the cross-coupled transistors. To ensure the oscillation startup, a transconductance four times larger than $1/R_{\rm P}$ is utilized as the design constraint based on the design consideration given in [8] for PVT variations, parasitic effects and losses from the interconnect. The startup condition is thus given by

$$G_{\rm m} > \frac{4R_{\rm S}C_{\rm P}}{L_{\rm ST}}. \tag{2}$$

Since both $G_{\rm m}$ and $C_{\rm P}$ are proportional to the width of the transistors, in an unloaded case, the oscillator design is independent of the device size as far as startup is concerned. Note that the cutoff frequency of the transistor and the quality factor ($Q_{\rm L}$) of the inductor are generally defined as $\omega_{\rm t} = G_{\rm m}/C_{\rm P}$ and $Q_{\rm L} = \omega L_{\rm ST}/R_{\rm S}$, respectively. Therefore, the startup condition in (2) can be expressed as

$$Q_{\rm L} > \frac{4\omega}{\omega_{\rm t}}. \tag{3}$$

As the cutoff frequency of the transistors is considered a process-dependent parameter, the required quality factor of the inductor versus the oscillation frequency can be easily identified as a design reference. Another important design issue is the minimum input voltage for startup which can be evaluated by

$$V_{\rm IN} > \frac{4R_{\rm S}C_{\rm P}}{k_{\rm n}L_{\rm ST}} + V_{\rm TN}, \tag{4}$$

where $k_{\rm n}$ and $V_{\rm TN}$ are the transconductance parameter and the threshold voltage of the native NMOS transistors. To further investigate the influence of the quality factor on the input voltage, circuit simulations were performed based on the device models of a 65-nm standard CMOS process. The results are shown in Fig. 4, indicating that the minimum input voltage increases from 22 to 33 mV as the inductor quality factor varies from infinity to 10 at 30 MHz.

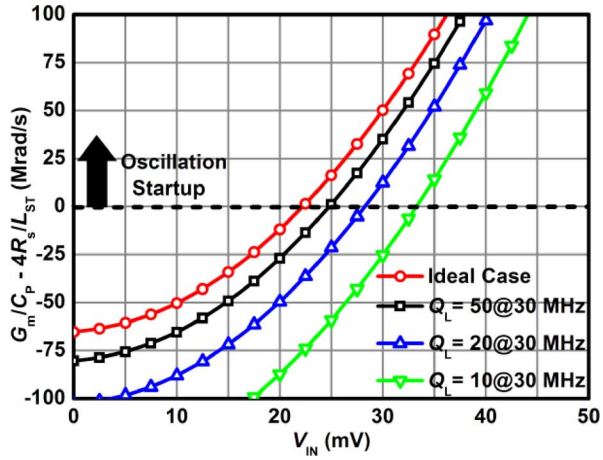


Fig. 4. Simulated startup constraint versus $V_{\rm IN}$ for various inductor quality factors.

In the low-voltage starter, the *LC*-tank oscillator is followed by a voltage multiplier to boost the voltage level. Considering the stringent power condition, a buffer stage is not applicable. As a result, the output node of the oscillator is directly loaded with the input capacitance of the voltage multiplier. By taking the loading effects into consideration, the startup conditions in (2) and (4) are modified as

$$G_{\rm m} > \frac{4R_{\rm S}(C_{\rm P} + C_{\rm VM})}{L_{\rm ST}} \tag{5}$$

and

$$V_{\rm IN} > \frac{4R_{\rm S}(C_{\rm P} + C_{\rm VM})}{k_{\rm n}L_{\rm ST}} + V_{\rm TN}, \tag{6}$$

where $C_{\rm VM}$ is the equivalent input capacitance of the voltage multiplier. It is noted that, in a loaded case, the aspect ratio of the cross-coupled transistors becomes an important design parameter in terms of startup and minimum input voltage. Besides, it is strongly influenced by the value of $C_{\rm VM}$ and has to be optimized in circuit implementation.

Fig. 5 shows the circuit schematic of the voltage multiplier adopted in this design. To simplify the analysis, a single-stage voltage multiplier presented in a single-ended manner is illustrated in Fig. 6(a). The rectified output voltage is given by

$$V_{\rm OUT\_i} = V_{\rm OUT\_i-1} + 2\left(V_{\rm A} - V_{\rm ON}\right), \tag{7}$$

where $V_{\rm A}$ is the AC voltage amplitude at the input V_+ and $V_{\rm ON}$ is the voltage drop by the native NMOS transistor. From the recursive equation, the overall output voltage by cascading N differential stages can be expressed as

$$V_{\rm OUT} = 4N\left(V_{\rm A} - V_{\rm ON}\right). \tag{8}$$

For an application scenario where $V_{\rm A} = 45$ mV and $V_{\rm ON} = 22$ mV, the simulation results indicate that the required stage number is 4 for 300-mV output voltage. In practical design cases, however, the effectiveness of the voltage multiplier decreases as the stage number increases due to non-ideal effects. For N cascaded stages, the output resistance of the multiplier can be approximated as

$$R_{\rm OUT} \approx \frac{2N}{g_{\rm m}}, \tag{9}$$

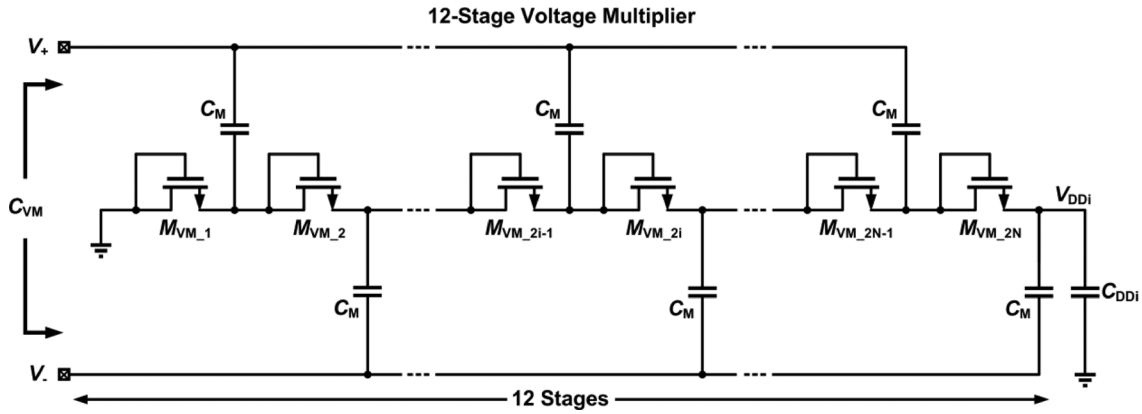


Fig. 5. Circuit schematic of the cascaded voltage multiplier.

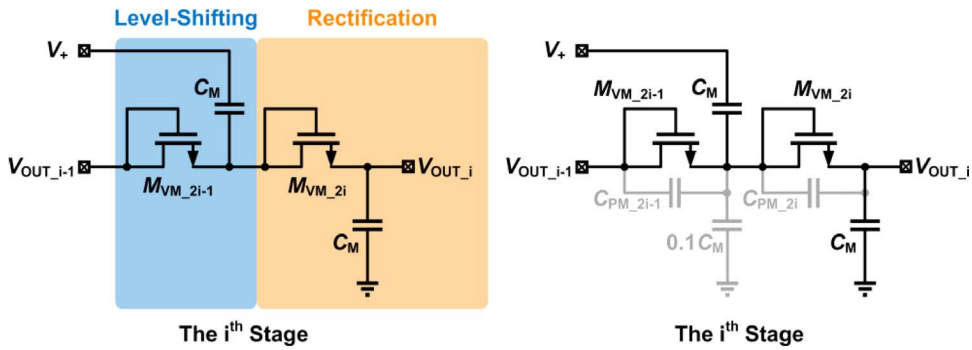


Fig. 6. (a) Circuit schematic of a single-ended voltage multiplier and (b) voltage division effect due to parasitic capacitances.

where $g_{\rm m}$ is the transconductance of the diode-connected MOS devices. In order not to increase the output resistance, the aspect ratio of the transistors has to be increased as the stage number increases. Nevertheless, the voltage-division effect, as shown in Fig. 6(b), manifests itself due to the excess parasitic capacitance, leading to a reduced voltage amplitude for rectification. By taking the non-ideal effects into account, the output voltage of the multiplier is given by

$$V_{\rm OUT\_loaded} = \frac{4N\left(\dfrac{C_{\rm M}}{1.1C_{\rm M}+2C_{\rm PM}}V_{\rm A}-V_{\rm ON}\right)}{1+\dfrac{2N}{g_{\rm m}R_{\rm L}}}, \quad (10)$$

where $C_{\rm PM}$ denotes the parasitic capacitance of the transistor with a specific output load of $R_{\rm L}$ and 10% parasitic of $C_{\rm M}$. The design goal of the voltage multiplier is to achieve an output DC voltage higher than 300 mV at a 500-nA loading current while minimizing the equivalent input capacitance $C_{\rm VM}$. Fig. 7(a) shows the simulated $C_{\rm VM}$ versus the stage number (N) and device size, while the boosted output voltage versus the stage number (N) is illustrated in Fig. 7(b). Based on (10) and the simulation results, the design parameters are determined in this particular design with a multiplier stage number of 12 and a capacitance $C_{\rm VM}$ of 11 pF.

Once the value of $C_{\rm VM}$ is determined, the required aspect ratio of the cross-coupled transistors in the oscillator can be obtained from (5) for a given inductance. Fig. 8 shows the estimated and simulated minimum startup voltage as well as corresponding power consumptions. Based on circuit simulations, a native NMOS transistor with a channel width of 5,000 μm and a channel length of 0.2 μm, which is the minimum allowable channel length for native NMOS devices in 65-nm CMOS technology, is adopted in the oscillator design, leading to a minimum input voltage of 40 mV and a power consumption of 16 μW at an input voltage of 50 mV. It is noted that the LC-tank oscillator is expected to operate in voltage-limited region, indicating an output voltage swing twice of the input voltage [9]. However, with the design parameters given above, the oscillator starts to oscillate at $V_{\rm IN} = 40$ mV, but it does not reach the voltage-limited region until the input voltage is higher than 55 mV. In practice, the minimum input voltage for startup falls in the vicinity of 50 mV. The design parameters of the low-voltage starter are tabulated in Table I along with the required off-chip inductance and specified load conditions of the following converter stage.

B. Auxiliary Step-Up Boost Converter

The auxiliary boost converter mainly serves as an intermediate buffer stage between the low-voltage starter and the high-efficiency converter to prevent undesirable loading effects on the low-voltage starter. A conventional asynchronous boost converter, as shown in Fig. 9(a), is thus used not only to boost the input voltage to a higher level but to provide a better driving capability as well. Since the NMOS transistor $M_{\rm N\_ASC}$ performs as a switch, low-$V_{\rm T}$ device rather than native one is utilized to minimize the leakage current when the switch is off. As the loading of this converter is simply digital controllers, the load current ($I_{\rm O}$) is relatively low (< 500 nA), allowing the

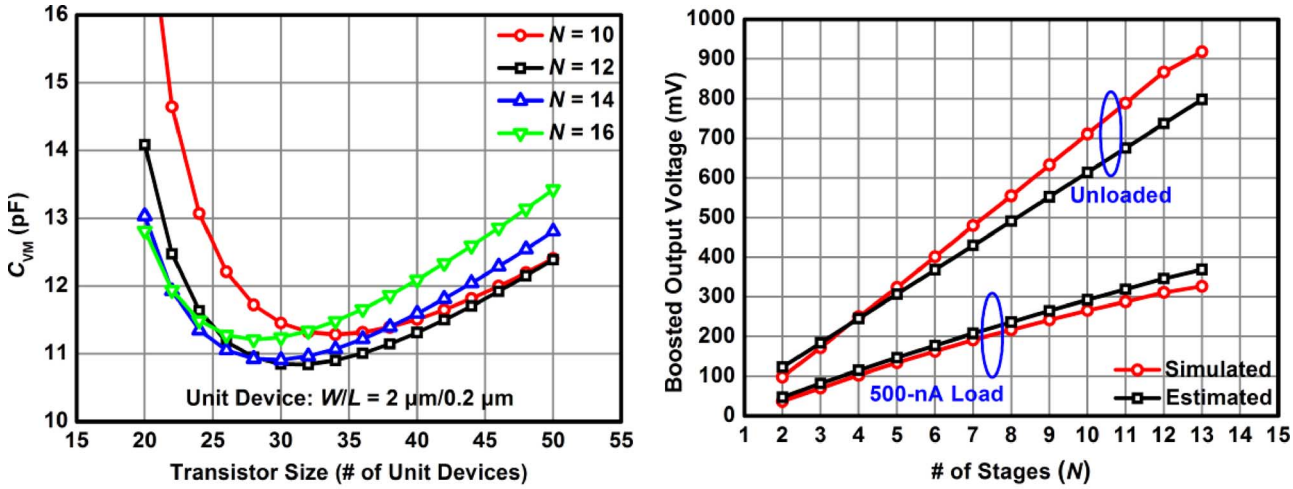


Fig. 7. (a) Equivalent capacitive loading ($C_{\rm VM}$) for *LC*-tank oscillator versus N and device sizes and (b) the boosted output voltage of the multiplier with an input voltage amplitude (V_+, V_-) of 45 mV at 30 MHz.

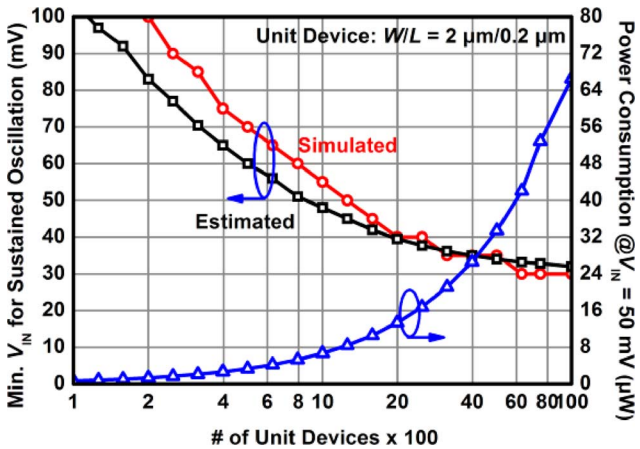


Fig. 8. Simulated minimum startup voltage and power consumption of the low-voltage oscillator.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED BOOST CONVERTER

Parameter	Unit	Value
Low-Voltage Starter		
L_{ST}	µH	2.0
$(W/L)_{OSC.}$	(µm/µm)	5000/0.2
$(W/L)_{VM}$	(µm/µm)	60/0.2
C_{VM}	pF	11
N	-	12
Auxiliary Boost Converter		
L_{ASC}	µH	100
$(W/L)_{N\_ASC}$	(µm/µm)	100/0.06
C_{DDi}	nF	4.7
ZCS-Controlled Boost Converter		
L_{ZCS}	µH	27
$(W/L)_P$,$(W/L)_N$	(µm/µm)	3000/0.26, 10000/0.26
C_{OUT}	µF	1.0

converter operation in discontinuous conduction mode (DCM). Fig. 9(b) illustrates the timing waveforms of the converter operation. The corresponding boost ratio (*BR*) can be expressed as [10]

$$BR = \frac{V_{\rm DDi}}{V_{\rm IN}} = 1 + \frac{V_{\rm IN} D^2 T_{\rm S}}{2 L_{\rm ASC} I_{\rm O}}, \tag{11}$$

where $T_{\rm S}$ is the period, D is the duty cycle and $I_{\rm O}$ is the output loading current.

From (11), it is clear that large boost ratio can be achieved in low loading current cases even if the duty cycle is close to 50%. As the main purpose of this auxiliary stage is to activate the final converter stage, the required output voltage is an intermediate value. In addition to the duty-cycle-controlled method, the inductance value $L_{\rm ASC}$ also provides another degree-of-freedom to accomplish the required *BR* with sufficient design margin. In this particular case, given that $V_{\rm DDi} = 800\ {\rm mV}$, $T_{\rm S} = 31.25\ \mu{\rm s}$, $D = 50\%$, $I_{\rm O} = 500\ {\rm nA}$ and $V_{\rm IN} = 50\ {\rm mV}$, the upper bound for the value of $L_{\rm ASC}$ is 26 mH. On the other hand, for operations with ultra-low supply voltage during the startup transient, the switch losses may cause startup failure if the inductor is not chosen properly. Fig. 10(a) shows the equivalent circuit during the inductor charging and discharging phases by modeling the switch as a resistance $R_{\rm N\_ASC}$ in series with an ideal switch and the forward-biased diode as a constant voltage drop $V_{\rm DF}$. The timing waveforms are shown in Fig. 10(b), where the corresponding free-wheeling time ($T_{\rm F}$) can be expressed as

$$T_{\rm F} = \frac{V_{\rm IN}}{R_{\rm N\_ASC}} \frac{L_{\rm ASC}}{V_{\rm DDi} + V_{\rm DF} - V_{\rm IN}}. \tag{12}$$

Note that extra energy is required during initialization ($V_{\rm DDi} \approx 0.3\ {\rm V}$) to successfully activate the self-regeneration loop, which can be written as

$$\frac{1}{2} L_{\rm ASC} \left(\frac{V_{\rm IN}}{R_{\rm N\_ASC}|_{V_{\rm DDi}=0.3\ {\rm V}}} \right)^2 + \frac{1}{2} \frac{{V_{\rm IN}}^2 T_{\rm F}|_{V_{\rm DDi}=0.3\ {\rm V}}}{R_{\rm N\_ASC}|_{V_{\rm DDi}=0.3\ {\rm V}}} > \frac{1}{2} \frac{V_{\rm DF} V_{\rm IN} T_{\rm F}|_{V_{\rm DDi}=0.3\ {\rm V}}}{R_{\rm N\_ASC}|_{V_{\rm DDi}=0.3\ {\rm V}}} + V_{\rm DDi} I_{\rm O} T_{\rm S}|_{V_{\rm DDi}=0.3\ {\rm V}}. \tag{13}$$

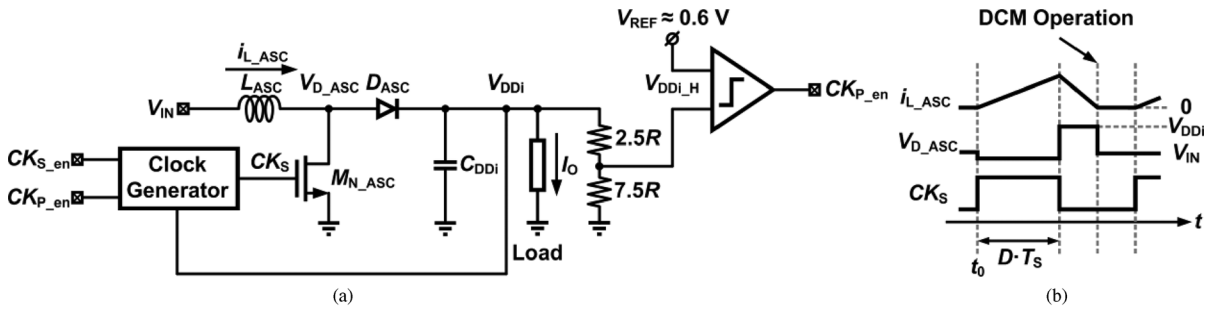


Fig. 9. (a) Circuit schematic of the auxiliary boost converter and (b) the corresponding waveforms in DCM operation.

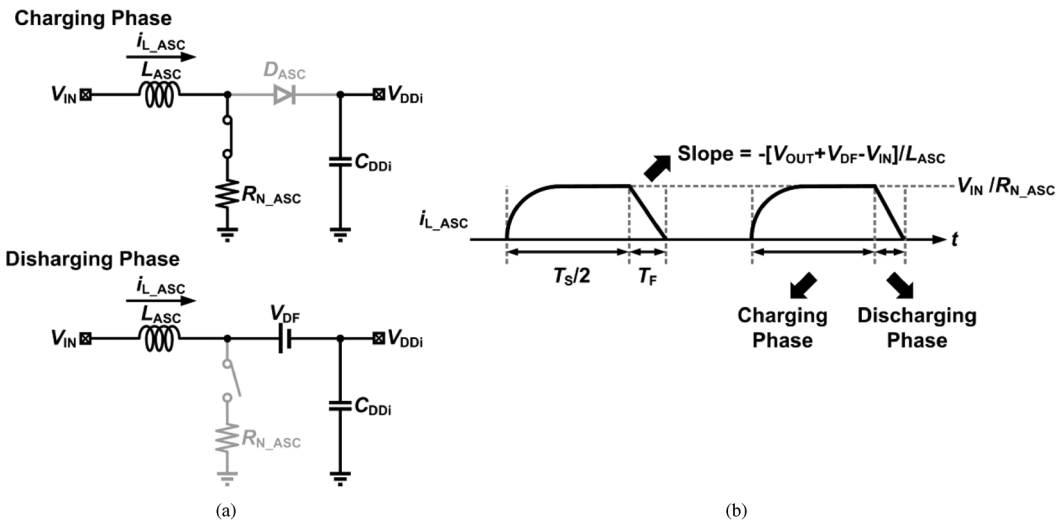


Fig. 10. (a) Equivalent circuit of the auxiliary boost converter and (b) the corresponding waveforms of $i_{\mathrm{L\_ASC}}$ for $L_{\mathrm{ASC}}/R_{\mathrm{N\_ASC}} \ll T_{\mathrm{S}}/2$.

The expression in (13) indicates that the energy from the generator ($E_{\mathrm{generator}}$) is larger than the energy dissipated ($E_{\mathrm{dissipated}}$) during the conversion, where $E_{\mathrm{generator}}$ accounts for the energy stored in the inductor when the switch is on and the energy transferred to the output at the free-wheeling period, while $E_{\mathrm{dissipated}}$ includes the energy dissipated on the diode during T_{F} and on the load during the entire period. Consequently, the lower bound of the inductance value is given by

$$L_{\mathrm{ASC}} > \left.\frac{2I_{\mathrm{O}}{R_{\mathrm{N\_ASC}}}^2 T_{\mathrm{S}}\left(V_{\mathrm{DDi}}+V_{\mathrm{DF}}-V_{\mathrm{IN}}\right)}{{V_{\mathrm{IN}}}^2}\right|_{V_{\mathrm{DDi}}=0.3\ \mathrm{V}}. \tag{14}$$

Based on the above derivations, an inductance value of 100 μH is employed for L_{ASC} with a transistor size of 100 μm/0.06 μm and $T_{\mathrm{S}} = 100$ μs. Simulation results indicate an available load current of 635 nA, which is sufficient to drive the digital controller for the final converter stage. The detailed design parameters are tabulated in Table I.

C. ZCS-Controlled Boost Converter

The circuit schematic of the ZCS-controlled boost converter is shown in Fig. 11(a), where a PMOS switch M_{P} is utilized to replace the diode such that the voltage drop can be avoided. It is noted that an extra pulse-width-modulation (PWM) controller is also employed to control the turn-on time of M_{P} and the timing waveforms for ZCS condition are depicted in Fig. 11(b). For ZCS operation, the current in the inductor becomes zero at the end of the timing window T_{ON}, which can be expressed as

$$T_{\mathrm{ON}} = \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}-V_{\mathrm{IN}}}\frac{T_{\mathrm{P}}}{2}. \tag{15}$$

In order to satisfy such requirement, either T_{ON} or T_{P} should be dynamically controlled by the regulated V_{OUT} to compensate for the variation of V_{IN} [1], [3]. However, since T_{P} is preserved to achieve the maximum power transfer during charging transient, a digital self-PWM control is implemented in this design to ensure ZCS operation within a specified input range. As a result, unnecessary charging or discharging the inductor via lossy MOS switches can be generally prevented.

In addition to the ZCS technique employed in this converter stage, similar self-regeneration on the supply voltage is also included once V_{OUT} is boosted to 1.0 V and finally regulated to 1.2 V, as depicted in Fig. 12. Although V_{DDi} has been boosted up to 800 mV when the ZCS converter is activated, the self-regeneration loop is not built up simultaneously and an optimization procedure similar to the auxiliary stage is still indispensable. Following the same optimization procedures, design parameters of this converter stage are summarized in Table I. Note that, in order to minimize the undesirable gate leakage, thick-oxide transistors in 65-nm CMOS are utilized for circuit implementation.

To sustain the ZCS operations under different loading conditions, a gated regulation scheme is applied to provide the re-

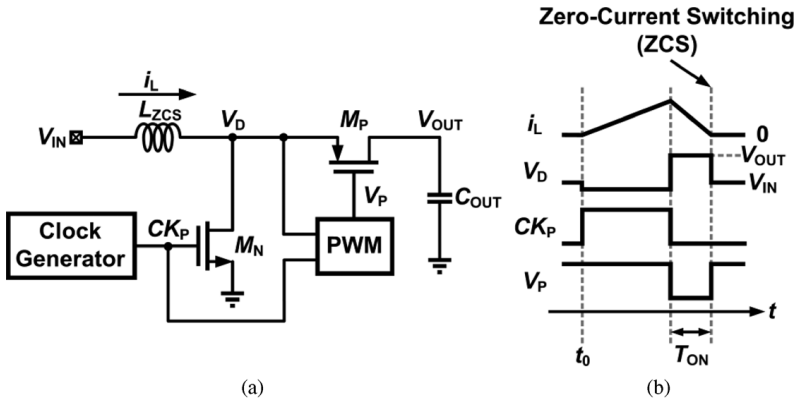


Fig. 11. (a) Architecture of the ZCS-controlled boost converter and (b) the corresponding ZCS waveforms.

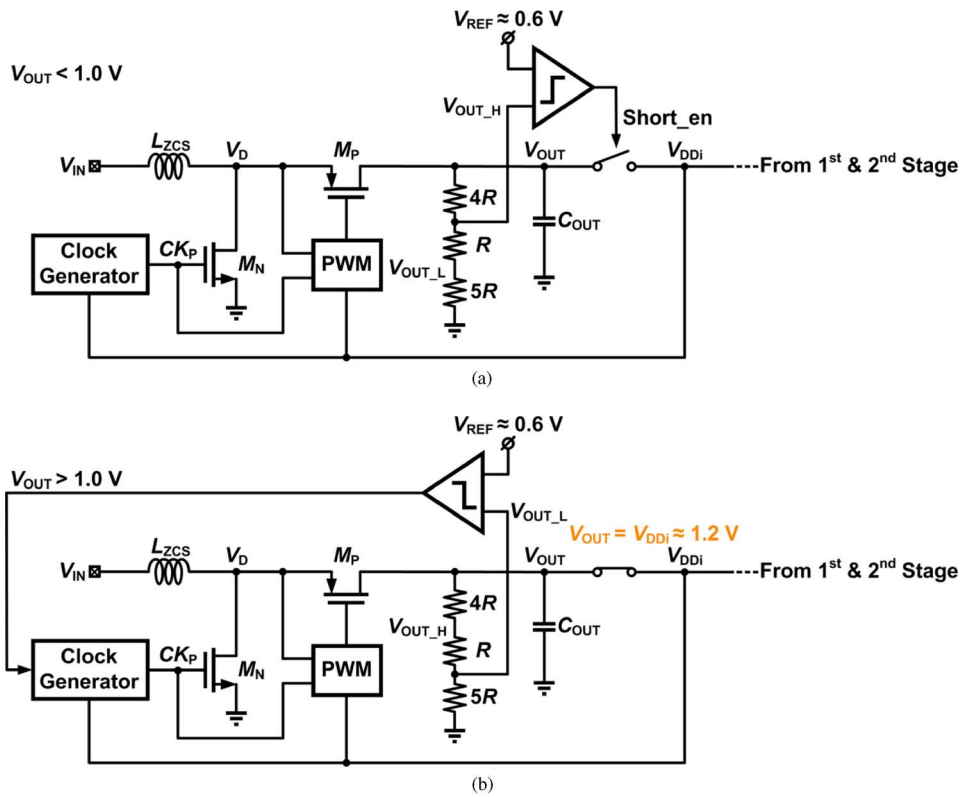


Fig. 12. Operations of the ZCS-controlled boost converter (a) before and (b) after V_{OUT} reaches 1.0 V.

quired load current while maintaining the ZCS condition for each charging period. As shown in Fig. 12, a comparator is used to sense the output voltage; once the output voltage is charged up to be higher than 1.2 V by one positive comparator threshold ($V_{\mathrm{TC+}}$), the converter is turned off and the load current is supplied by the output capacitor till the output voltage is discharged to be smaller than 1.2 V by one negative comparator threshold ($V_{\mathrm{TC-}}$). A conceptually illustration is illustrated in Fig. 13. With such regulation scheme, the available load current can be approximated as

$$I_{\mathrm{L,avg.}} \approx \alpha \cdot \frac{V_{\mathrm{IN}}}{4L_{\mathrm{ZCS}}}\left(T_{\mathrm{ON}} + \frac{T_{\mathrm{P}}}{2}\right)\Bigg|_{V_{\mathrm{OUT}}=1.2\ \mathrm{V}}, \tag{16}$$

where α represents the percentage of the ZCS charging duration within one gated regulation period, $T_{\mathrm{REG.}}$. From (16), the maximum available output power at $\alpha = 1$ with $V_{\mathrm{OUT}} = 1.2$ V and $T_{\mathrm{P}} = 40$ μs is 13.6 mW, which is much higher than the maximum available power from the TEG at small temperature difference, implying that this gated scheme works well within the predetermined input range.

D. Self-PWM Control and Peripheral Circuits

As the ZCS operation provides efficiency optimization at steady state, it is preferred that such optimization can also compensate for variations in the input voltage and the oscillation frequency. Detailed waveforms for the converter under various T_{ON} conditions are shown in Fig. 14. In cases where M_{P} turns off late, a negative voltage jump on V_{D} occurs. On the other hand, if M_{P} turns off early, a positive voltage jump on V_{D} is observed. Accordingly, automatic control mechanism for the

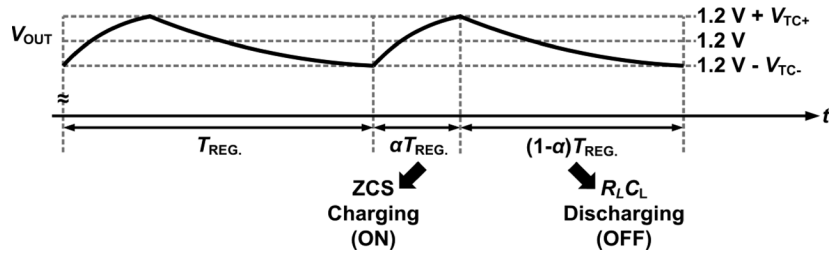


Fig. 13. Conceptual illustrations of the gated regulation scheme.

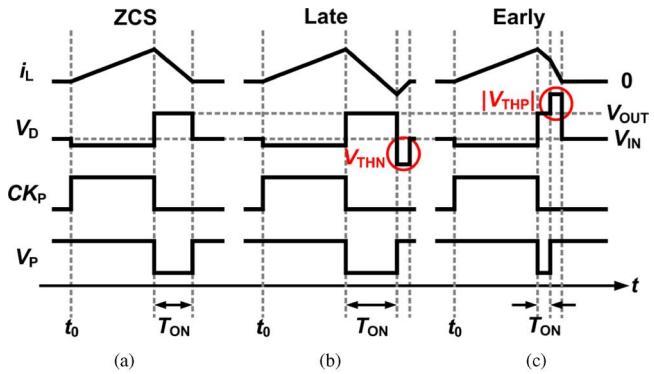


Fig. 14. Detailed waveforms of the ZCS-controlled boost converter with (a) exact ZCS operation, (b) M_P turning off late and (c) M_P turning off early.

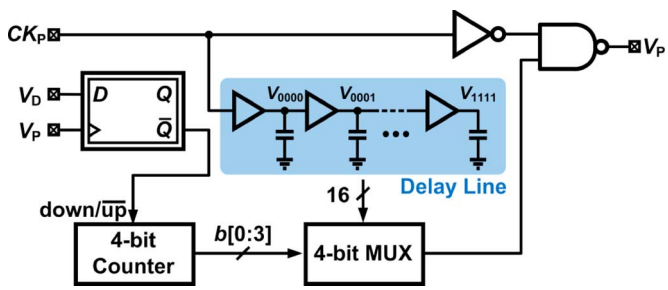


Fig. 15. Circuit implementations of the self-PWM controller.

turn-on time of M_P is implemented by the information of V_D at the rising edge of V_P, facilitating a dynamic self-PWM control.

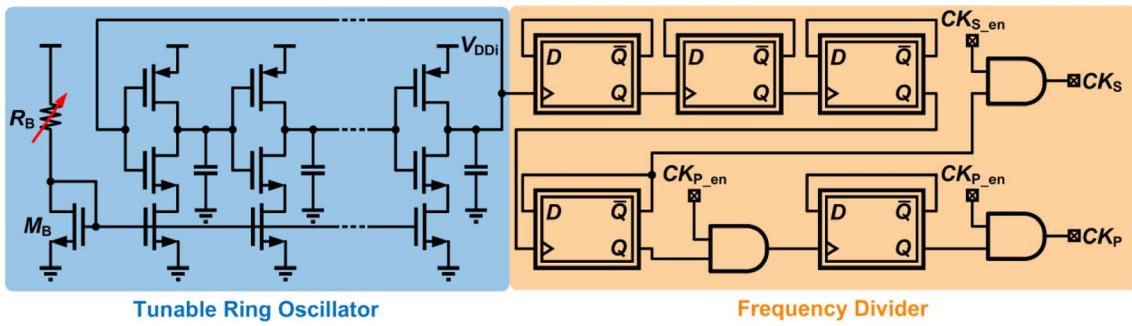
The circuit schematic of the self-PWM controller is shown in Fig. 15, which is realized in digital domain with a 4-bit successive approximation algorithm by sequential search on the delay time in the pulse generator for M_P control. A D-flip flop is employed to sense the polarity of V_D at the rising edge of V_P, providing the required information to either reduce or extend the pulse window selected from the delay chain. In this controller, the tunable delay ranges from 0.8 to 4 μs which covers the input voltage from 37 to 200 mV for a 1.2-V regulated output with 25-kHz switching frequency. With a 4-bit control, the effective resolution on the input voltage is roughly 10 mV, yielding an equivalent temperature resolution smaller than 0.5°C with the TEG sample adopted in this work.

Fig. 16(a) shows the circuit schematic of the clock generator which is composed of a tunable current-starved ring oscillator followed by a series of gated frequency dividers. By utilizing static D-flip flops as the divider stages, 50% duty cycle and rail-to-rail output clocks are provided, simplifying the design of the auxiliary step-up converter with minimum switch losses. Based on circuit simulations, the ring starts to oscillate for V_{DDi} higher than 250 mV. The schematic of the on-chip reference generator is shown in Fig. 16(b), where a forward-biased *pn*-junction diode is utilized as the global reference and resistor ladders are employed to generate thresholds for circuit operations and output regulations. Circuit simulations indicate that the reference generator starts to work as the internal voltage V_{DDi} exceeds 500 mV. It is noted that the absolute precision of the reference generator directly affects the accuracy of the output regulated voltage while the requirement for threshold generations is more relaxed. The proposed circuit demonstrates a simple and energy-efficient regulation scheme with acceptable line regulations.

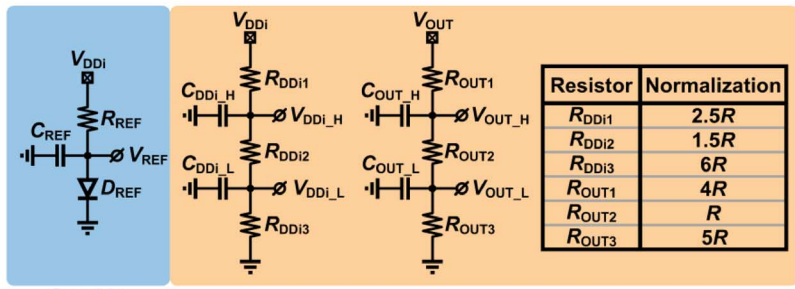
IV. Experimental Results

The proposed ultra-low input voltage dc-dc boost converter for thermoelectric applications is designed and implemented by using a standard 65-nm CMOS process. Fig. 17(a) shows the die photograph of the fabricated circuit with a chip area of $1.05 \times 0.95\ \mathrm{mm}^2$, including the pads. Based on the fabricated circuit, a converter module along with a miniaturized TEG device is realized as shown in Fig. 17(b). By modeling the TEG device as a Thévenin's equivalent circuit, the converter is characterized for its electrical properties. In addition, thermoelectric characterizations of the converter module and the TEG device are performed as well.

In order to characterize the electrical properties, the input voltage source is modeled by an ideal voltage source (V_{TH}) ranging from 50 ~ 200 mV and a 6.2-Ω equivalent series resistance (R_{TH}). Fig. 18 shows the transient settling responses of the internal node V_{DDi} and output node V_{OUT} with capacitance values of 4.7 and 1,000 nF, respectively. For both cases where the input voltages are 50 and 100 mV, the 3-stage stepping-up operations are clearly shown in the measurement. As the voltage is boosted to approximately 1 V, the short-enable signal is activated, shorting the two capacitors at V_{DDi} and V_{OUT}. With a simple on-chip reference, the output voltage is successfully boosted and regulated to provide a 1.2-V output. The measurement results of peak conversion efficiency are demonstrated in Fig. 19(a). Note that the peak efficiency is defined as the ratio between the maximum available power delivered to a resistive load when $V_{IN} = V_{TH}/2$ and the maximum available power from the voltage source as described in [11], which are measured by controlling the potentiometer as the load, as depicted



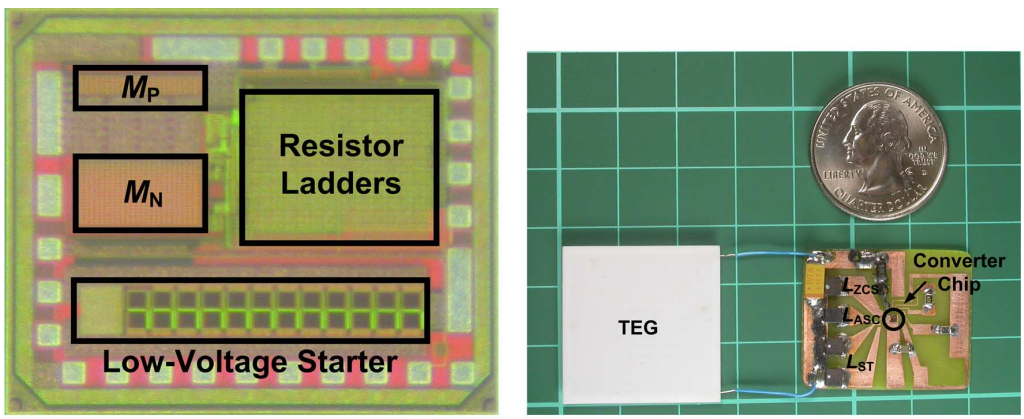
(a)



Resistor	Normalization
R_{DDi1}	2.5R
R_{DDi2}	1.5R
R_{DDi3}	6R
R_{OUT1}	4R
R_{OUT2}	R
R_{OUT3}	5R

(b)

Fig. 16. Circuit schematics of the (a) clock generator and (b) on-chip reference generator.



(a) (b)

Fig. 17. (a) Die photograph of the fabricated low-startup voltage batteryless boost converter and (b) the TEG converter module with miniaturized TEG device.

in Fig. 19(b). The peak efficiency can, therefore, be expressed as

$$\text{Peak Efficiency} = \frac{P_{\text{OUT}}|_{\text{V}_{\text{OUT}}=1.2\text{ V}}}{P_{\text{IN}}|_{\text{V}_{\text{IN}}=\text{V}_{\text{TH}}/2}} = \frac{P_{\text{OUT,max.}}}{P_{\text{IN,max.}}}. \quad (17)$$

Experimental results indicate that the minimum V_{TH} for startup is 50 mV while the minimum V_{TH} for sustained converter operation is 30 mV. The conversion efficiency saturates at 73% as V_{TH} is higher than 100 mV and no significant efficiency degradation is observed even if V_{TH} increases up to 200 mV. With an input voltage V_{TH} of 100 mV, the measured output power and simulated power consumption of the individual building blocks are tabulated in Table II. It is observed that the dissipated energy is mainly from the device parasitics and the switching loss associated with the ZCS-controlled boost converter rather than from the first two converter stages and the peripheral control circuitry.

TABLE II
POWER CONSUMPTION BREAKDOWN OF THE PROPOSED CONVERTER AT $V_{\text{TH}} = 100$ mV AND $R_{\text{TH}} = 6.2\ \Omega$

Power/Power Consumption	Value (μW)	Percentage (%)
From Measurement		
P_{IN}	403.2	100
P_{OUT}	282.2	69.99
From Simulation		
Low-Voltage Starter	16.0	3.97
Auxiliary Step-up Boost Converter	~0	0.00
Reference Generator	0.6	0.15
Peripheral Controller	3.0	0.74
From Estimation		
ZCS-Controlled Boost Converter (Parasitic & Switching Loss)	101.4	25.15

For the thermoelectric characterizations, a TEG device provided by Industrial Technology Research Institute (ITRI) of

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	[1] JSSC '10	[3] ISSCC '10	[5] ISSCC '11	[6] ISSCC '12	This Work
Process	0.13-μm CMOS	0.35-μm CMOS	65-nm CMOS	0.13-μm CMOS	65-nm CMOS
Startup Mechanism	External Pre-Charge	Mechanical Switch	Fully Electrical†	Miniaturized Transformer	Fully Electrical
Min. Startup Voltage	650 mV	35 mV	95 mV	40 mV	50 mV
Output Voltage	1 V	1.8 V	0.9 V	2.0 V	1.2 V
Peak Efficiency	75 % @0.1-mA Load†††	58 %	72 % @1.5-mA Load†††	37 / 61 %††	73 %

†Post-fabrication with V_{TH}-trimming is required
††37 % for V_{IN} < 100 mV; 61 % for V_{IN} > 100 mV
†††Boost converter only: measured with ideal input voltage sources

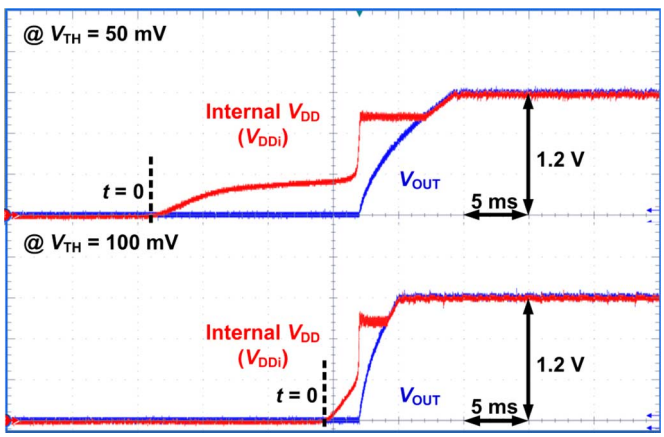


Fig. 18. Measured transient settling responses with $V_{\rm TH} = 50$ and 100 mV.

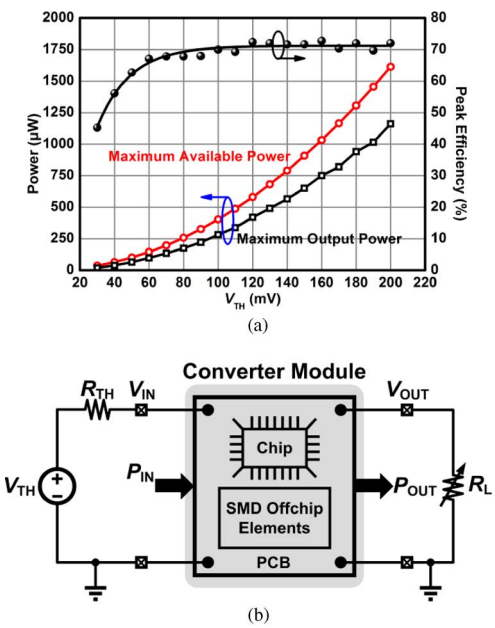


Fig. 19. (a) Measured maximum output power and peak efficiency versus $V_{\rm TH}$ and (b) the measurement setup.

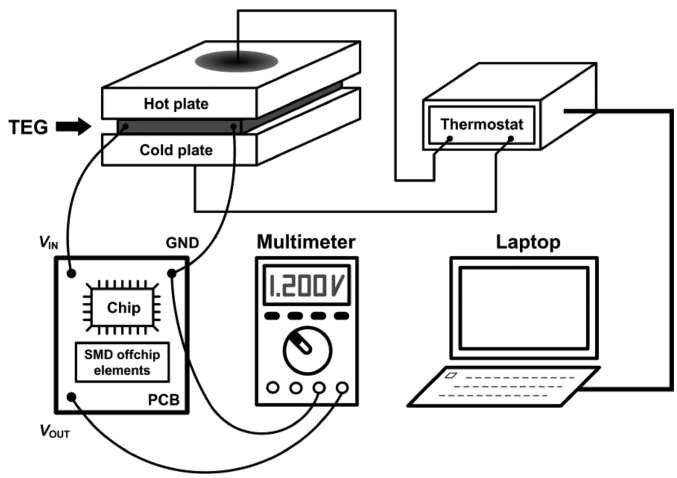


Fig. 20. Measurement setup of thermoelectric characterizations.

Taiwan is utilized for the experiment. The TEG sample consists of 127-pair *pn*-junctions and its physical size is $2.6 \times 2.6\ \mathrm{cm}^2$. Fig. 20 illustrates the measurement setup where a micro-controller heater is adopted to maintain the temperature difference between the two plates with a fixed temperature of 25°C at the bottom plate. The TEG is connected to the input of the converter module while the output of the converter is monitored by a multi-meter. Similar to the electrical characterizations, a potentiometer is still used as a variable resistive emulated load to measure the maximum available output power. To have better understanding of the thermoelectric properties, 4 converter modules based on 4 different fabricated chips are tested with the same TEG device. With a temperature difference from 2 to 8°C across the TEG device, the maximum output power of the converter module is illustrated in Fig. 21, indicating an output power generally higher than 1 mW for a temperature difference of 4°C. The performance of the proposed boost converter is summarized in Table III along with state-of-the-art results from recent publications for comparison.

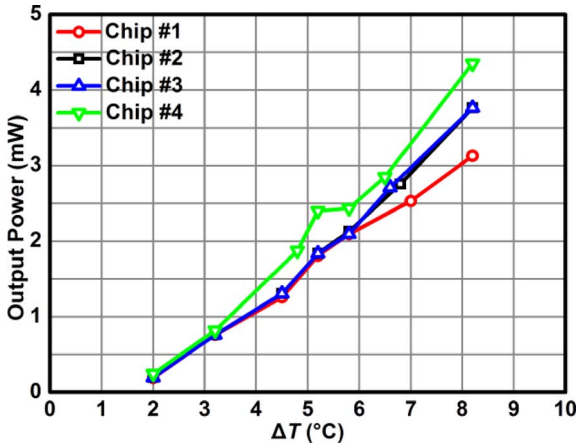


Fig. 21. Measured maximum available output power with $\Delta T = 2 \sim 8°\mathrm{C}$.

V. Conclusion

In this paper, a fully-electrical startup dc-dc boost converter is presented for batteryless operation. With a 3-stage stepping-up architecture, the proposed boost converter is fabricated in a standard 65-nm CMOS process, providing a regulated 1.2-V output voltage with a minimum input voltage of 50 mV and maximum efficiency of 73%. In addition, a TEG converter module is realized to characterize the electrical and thermoelectric properties. With a miniaturized TEG device, the module demonstrates an output power higher than 1 mW at a temperature difference of 4°C, making it well suited for thermoelectric energy harvesting from body heat.

Acknowledgment

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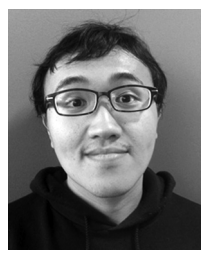

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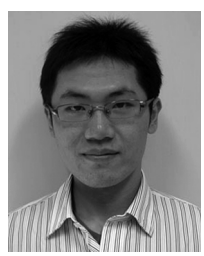

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