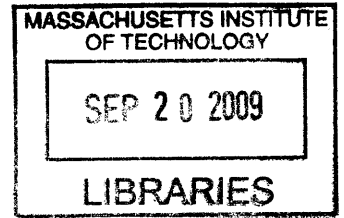# Energy Processing Circuits for Low-Power Applications

by

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Energy Processing Circuits for Low-Power Applications

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Abstract

Portable electronics have fueled the rich emergence of new applications including multi-media handsets, ubiquitous smart sensors and actuators, and wearable or implantable biomedical devices. New ultra-low power circuit techniques are constantly being proposed to further improve the energy efficiency of electronic circuits. A critical part of these energy conscious systems are the energy processing and power delivery circuits that interface with the energy sources and provide conditioned voltage and current levels to the load circuits. These energy processing circuits must maintain high efficiency and reduce component count for the final solution to be attractive from an energy, size and cost perspective.

The first part of this work focuses on the development of on-chip voltage scalable switched capacitor DC-DC converters in digital CMOS processes. The converters are designed to deliver regulated scalable load voltages from 0.3V up to the battery voltage of 1.2V for ultra-dynamic voltage scaled systems. The efficiency limiting mechanisms of these on-chip DC-DC converters are analyzed and digital circuit techniques are proposed to tackle these losses. Measurement results from 3 test-chips implemented in 0.18μm and 65nm CMOS processes will be provided. The converters are able to maintain >75% efficiency over a wide range of load voltage and power levels while delivering load currents up to 8mA. An embedded switched capacitor DC-DC converter that acts as the power delivery unit in a 65nm subthreshold microcontroller system will be described.

The remainder of the thesis deals with energy management circuits for battery-less systems. Harvesting ambient vibrational, light or thermal energy holds much promise in realizing the goal of a self-powered system. The second part of the thesis identifies problems with commonly used interface circuits for piezoelectric vibration energy harvesters and proposes a rectifier design that gives more than 4X improvement in output power extracted from the piezoelectric energy harvester. The rectifier designs are demonstrated with the help of a test-chip built in a 0.35μm CMOS process. The inductor used within the rectifier is shared efficiently with a multitude of DC-DC converters in the energy harvesting chip leading to a compact, cost-efficient solution. The DC-DC converters designed as part of a complete power management solution achieve efficiencies of greater than 85% even in the micro-watt

power levels output by the harvester.

The final part of the thesis deals with thermal energy harvesters to extract electrical power from body heat. Thermal harvesters in body-worn applications output ultra-low voltages of the order of 10's of milli-volts. This presents extreme challenges to CMOS circuits that are powered by the harvester. The final part of the thesis presents a new startup technique that allows CMOS circuits to interface directly with and extract power out of thermoelectric generators without the need for an external battery, clock or reference generators. The mechanically assisted startup circuit is demonstrated with the help of a test-chip built in a $0.35\mu m$ CMOS process and can work from as low as 35mV. This enables load circuits like processors and radios to operate directly of the thermoelectric generator without the aid of a battery. A complete power management solution is provided that can extract electrical power efficiently from the harvester independent of the input voltage conditions. With the help of closed-loop control techniques, the energy processing circuit is able to maintain efficiency over a wide range of load voltage and process variations.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

Energy efficiency of integrated circuits continues to be a major factor in determining the size, weight and cost of portable electronic systems. Sophisticated battery operated electronic systems and self-powered devices have found diverse applications recently. They exist as autonomous or hand held objects in every environment around us and in some cases even within us, significantly improving the quality of life and connectivity of users. Specific applications include portable multi-media handsets, implantable and wearable biomedical devices, wireless sensor networks, and RFID tags, to name a few. In all of these cases, long-term battery life/self-powered operation and low cost are paramount. Accordingly, highly aggressive low-power circuit design and efficient power delivery is required to meet battery or energy harvesting constraints [4].

1.1   Power Delivery in Portable Systems

The integrated circuit explosion in the last few decades have benefited greatly from technological advances which follow Moore's law. The doubling of transistors in a die every 2 years has given rise to smaller, faster, less power hungry transistors which have greatly enhanced the processing capabilities and features provided by modern portable devices. As technology scaling has progressed, the nominal core voltage of transistors has dropped from

2.5V in a 0.25μm CMOS process to $\sim$1V in the currently used 45nm CMOS processes. Most portable electronic systems used today are powered by a battery. The physical limits of electro-chemistry have prevented battery technologies to advance at the same rapid rate as the shrinking of transistor sizes or the cramming of more transistors in a given area. Table 1.1 gives the typical characteristics of commonly used rechargeable batteries in portable systems.

Table 1.1: Characteristics of commonly used rechargeable batteries

	NiCd	NiMH	Li-ion	Li-ion polymer	Reusable Alkaline
Gravimetric Energy Density (Wh/kg)	45-80	60-120	110-160	100-130	80(initial)
Volumetric Energy Density (Wh/l)	50-150	140-300	270	300	80(initial)
Cycle Life (to 80% of initial capacity)	1500	300-500	500-1000	300-500	50 (to 50%)
Cell Voltage (nominal)	1.25V	1.25V	3.6V	3.6V	1.5V

Owing to its large gravimetric and volumetric densities, Li-ion based batteries are becoming increasingly popular for a variety of portable electronic applications like cell phones, laptops etc. This helps in minimizing the size and weight of the battery. The Li-ion battery has a nominal voltage of 3.6V. However, during its discharge cycle, the voltage output by the battery can be widely variant from 4.2V to 2.6V. Figure 1-1 shows the typical discharge characteristic of a Li-ion battery. Due to the battery voltage being very different from the nominal voltage of the circuits in a given CMOS technology node and because the battery voltage varies along its discharge cycle, intermediate DC-DC converters are essential in portable electronic systems to act as the voltage conversion circuits between the battery on one side and the load circuits on the other.

Figure 1-2 shows what the inside of a typical cellphone looks like. The complex func-
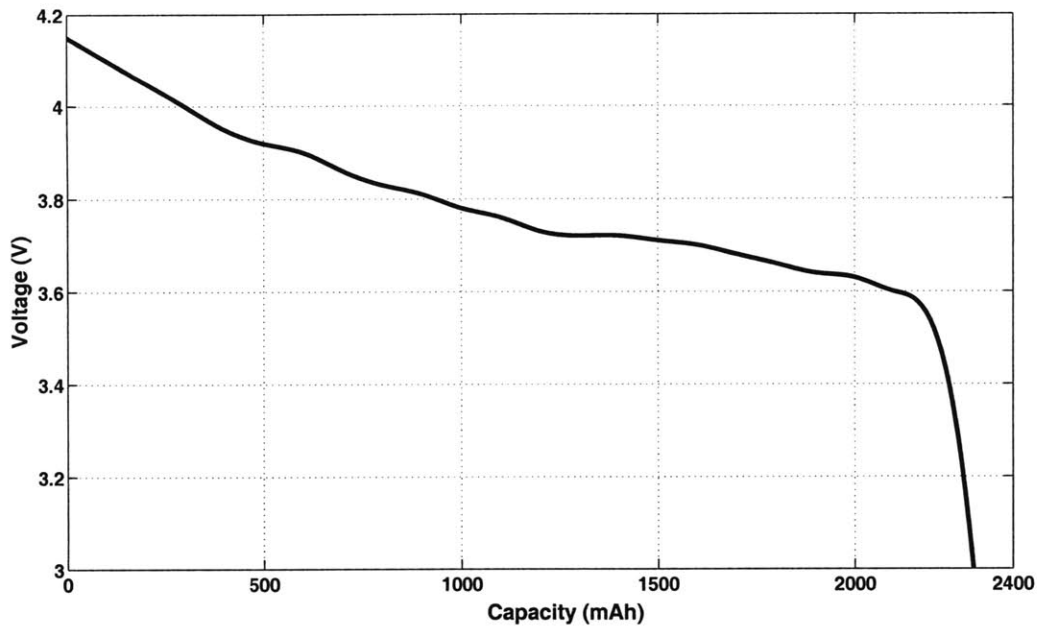
Figure 1-1: Typical discharge characteristics of a Li-ion battery.

tionality within a cellphone is implemented using a variety of different circuits and blocks each of which is powered using a Li-ion battery. Since the functionalities and operating methods of the different blocks are usually different, each needs a specific voltage to operate. For eg. the digital baseband of a cellphone might run at the core voltage for its technology (say 1V) while certain analog, RF and I/O circuits might require higher voltages to function properly. This varied splitting of voltage domains requires multiple voltage regulators to cater to each of the individual blocks. Further, there are certain blocks like the power amplifier and the core digital baseband processor which consume the majority of the power within a cellphone. These blocks are supplied by their own individual inductor-based DC-DC converters to get above 95% efficiency. The intermediate voltages that these inductor-based DC-DC converters provide is used by other voltage regulators to provide power to the various other sub-blocks within the cellphone system. Every block cannot have its own dedicated inductor-based DC-DC converter because of the cost and volume penalities imposed by these converters. Hence, most of the other voltage regulators are linear regulators (LDO's) owing

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to the small on-die size occupied by them. By design, these linear regulators provide very poor efficiency when their drop-out voltage is large. The initial section of this thesis looks into the design of switched capacitor DC-DC converters as a more efficient alternative to linear regulators. Switched capacitor DC-DC converters are switching regulators which make use of just switches and capacitors to perform voltage conversion. This makes it possible to implement them on-die reducing the number of off-chip components. The first half of this thesis talks about switched capacitor DC-DC converters implemented in digital CMOS processes as high efficiency alternatives to linear regulators.
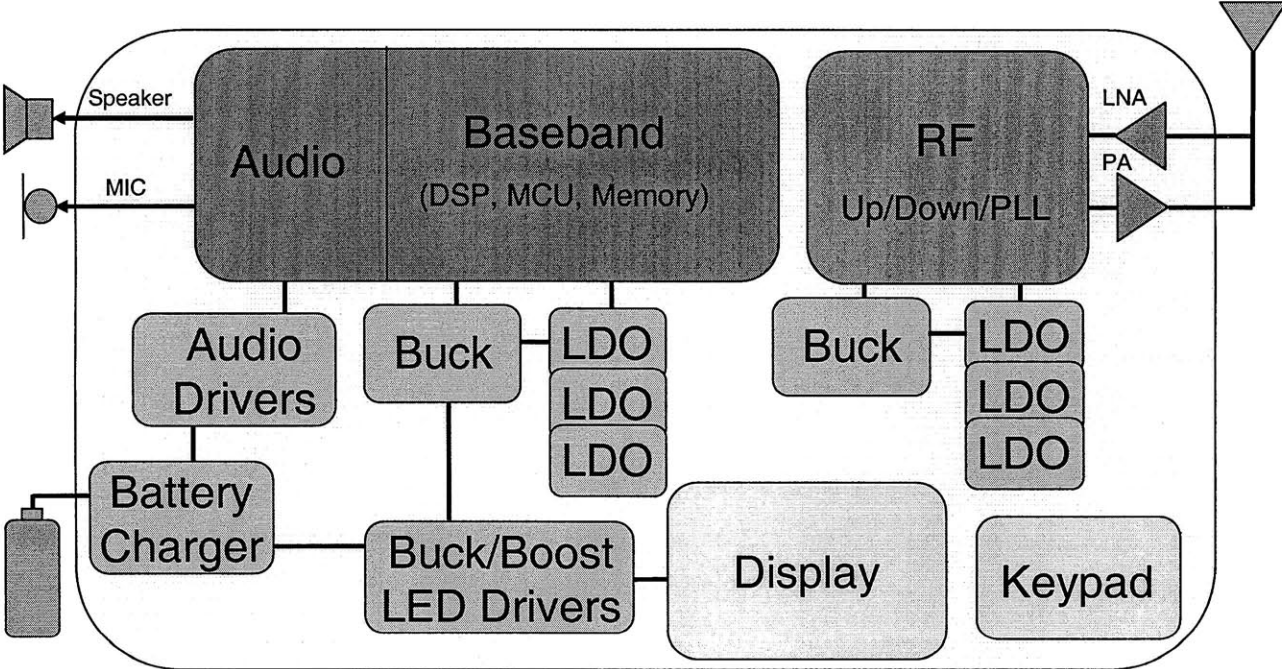
Figure 1-2: Illustration of different circuit blocks within a cellphone and how they are powered.

1.2 Voltage Scaling and Minimum Energy Operation

In the evolution of modern portable electronic devices, digital data processing is taking an increasing role and a commensurate fraction of the power consumption. For example, in a second generation (2G) code division multiple access (CDMA) phone, the digital baseband

and the memory circuit take about 10% of the total power that the handset chip set consumes. While in a third generation (3G) wide band CDMA (WCDMA) phone, this percentage is 30-50% of the overall power consumption, since functions associated with filtering and digital data streaming are now handled with digital circuitry [5]. Reducing the power consumed by the digital baseband and memory circuits is of paramount importance to bring down the overall power consumption of portable electronics and increase battery lifetime.

Supply voltage scaling is one of the most popular methods to reduce power consumption of integrated circuits. Specifically, in a digital circuit, the active CV_{DD}^2 energy, E_{ACT}, required to complete an operation reduces quadratically with supply voltage. Thus by decreasing the operating voltage of circuits, their power consumption can be brought down significantly. However, the decrease in voltage comes at a cost of reduced operating speed. Most digital circuits do not operate at their highest operating speed all the time. There are large periods of time when the workload required of them is much smaller.

A video decoding chip is shown as a specific example of the varying workloads of a digital system and how the system can be operated at different voltages corresponding to the workload. In video decoding, the frame rate and resolution of the playback video dictates the performance requirement of the video decoder hardware [1]. Over the past years, the number of different types of video content has been growing rapidly ranging from professional cinema to news reports to, most recently, user-generated content. In addition, the numerous modes of transmission of the video have also expanded from broadcast and playback from local storage (e.g. DVD), to streaming across the internet and cellular network. Both of these factors cause the frame rate and resolution of todays video content to vary widely. Figure 1-3 shows the measured power of a 65nm H.264/AVC video decoder when performing real-time decoding of video streams of different resolutions.

Dynamic Voltage Scaling (DVS) [6] [7] has become a standard method to minimize power consumption of digital circuits when their performance requirements vary. As V_{DD} decreases, transistor drive currents decrease, bringing down the speed of operation of a circuit. A DVS system adjusts the supply voltage, operating the circuit at just enough voltage to meet
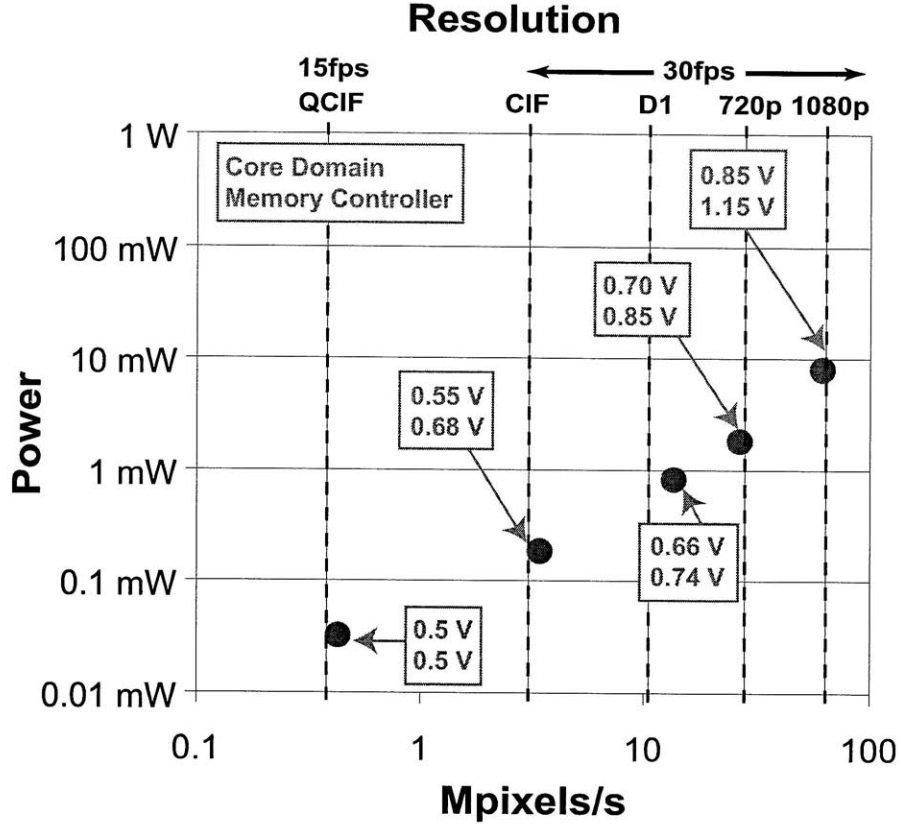
Resolution

Figure 1-3: Measured power of a 65nm H.264/AVC video decoder when performing real-time decoding of video streams of different resolutions [1].

performance, thereby achieving overall savings in total power consumed. While DVS is a popular method to minimize power consumption in digital circuits given a performance constraint, certain emerging applications like wireless micro-sensor networks [8] [9], implantable medical electronics [10] and RFID systems are severely energy-constrained. Subthreshold operation [11] [9] [12] of digital circuits, i.e. operating the circuits at a V_{DD} lesser than the threshold voltage of its devices, is a solution to the energy constrained applications. Though subthreshold operation makes the circuits operate slower due to the reduced drive currents, it offers the promise of minimum energy operation. Since, the goal of energy constrained applications is to minimize the overall energy consumed per operation performed, subthreshold operation is a viable solution for these applications.

The total energy per operation of a digital circuit can be split into two components :

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an active energy part and a leakage energy part. The active energy component as is well known scales down quadratically with V_{DD} as is shown in Figure 1-4 which shows the active and leakage energy profiles of a 65nm 7-tap FIR filter. The leakage energy component is due to the leakage power which integrates over the time period of an operation. While it is negligible at higher voltages, the leakage energy component increases exponentially as V_{DD} is decreased close to the threshold voltage. These opposing trends of the active and leakage energy components give rise to a minimum in the total energy consumed per operation. As in the case shown, this minimum energy voltage occurs below the threshold-voltage for most practical digital circuits [4] [13].
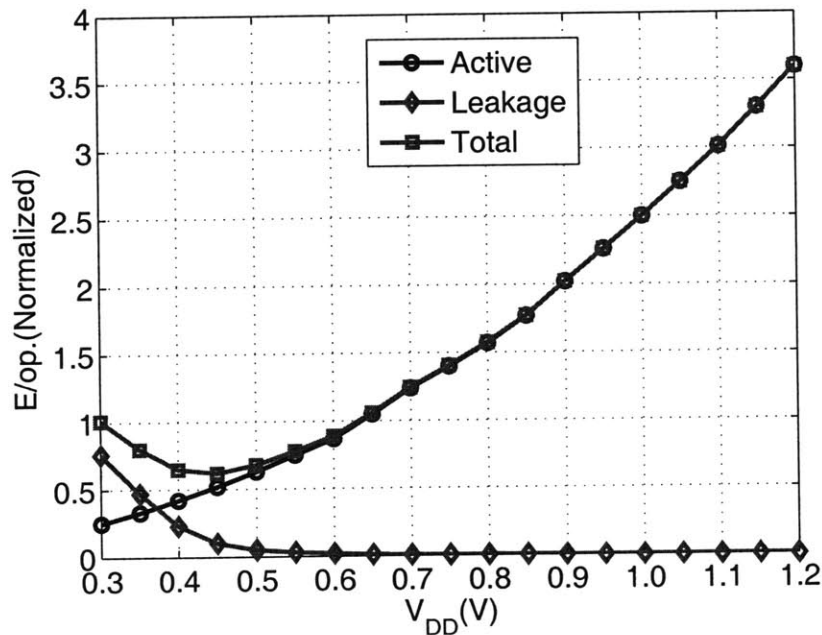
Figure 1-4: Active and leakage energy profiles for an FIR filter in 65nm CMOS. The two profiles result in a minimum energy supply voltage of approximately 0.4V.

By introducing the capability of sub-threshold operation, DVS systems can be made to operate at their minimum energy operating voltage [12] in periods of very little activity, leading to further savings in total energy consumed. This way ultra-dynamic voltage scaling (U-DVS) can be achieved. To enable ultra-dynamic voltage scaling systems, it is critical to

address the severe challenges faced by low-voltage circuits, particularly as they attempt to leverage advanced technologies fraught with issues of statistical variation, leakage, and rising cost. Considerable work has been done in building logic [14] and memory [15] circuits that can function at low voltages and still have the ability to operate at the maximum voltage at high speeds. Apart from the digital circuits, a DC-DC converter supplying ultra-low voltages at high efficiencies is essential to realize the full energy savings that can be achieved by reducing V_{DD} in a U-DVS system. Most of these systems also comprise of multiple voltage domains each requiring a distinct voltage. Using traditional switched inductor regulators would mean using multiple inductors to cater to these different voltage domains. This is prohibitive in terms of cost and motivates the need to look into an on-chip solution that can provide scaled supply voltages at good efficiencies. Switched capacitor DC-DC converters is a viable option for such systems. One of the main drawbacks of traditional on-chip switched capacitor DC-DC converter is its low efficiency compared to regular inductor-based switching converters. In this work, the major efficiency limiting losses in an on-chip switched capacitor converter are addressed and the voltage scalability of the converter is improved. Further, since the power consumed by ultra-low voltage systems can be of the order of micro-watts, maintaining the efficiency of the DC-DC converter at these low power levels is a key requirement. Work done in this thesis addresses this growing need by effective digital control techniques that enable constant efficiency over a wide range of load current/power levels.

1.3 Self-powered Operation

With the need for portable and lightweight electronic devices on the rise, highly efficient power generation approaches are a necessity. The dependence on the battery as the only power source is putting an enormous burden in applications where either due to size, weight or lifetime constraints, doing away with the battery is the only choice. Emerging applications like wireless micro-sensor networks [16], implantable medical electronics and tire-pressure sensor systems [17] are examples of such a class. It is often impractical to operate these systems on a fixed energy source like a battery owing to the difficulty in replacing the battery.

A 1cm^3 primary lithium battery has a typical energy storage capacity of 2800J [2]. This can potentially supply an average electrical load of $100\mu\text{W}$ for close to a year but is insufficient for systems where battery replacement is not an easy option. It therefore becomes necessary to look for alternative sources of energy to power these systems. The ability to harvest ambient energy through energy scavenging technologies is a practical solution for battery-less operation. The most common energy harvesters transduce solar, vibrational or thermal energy into electrical energy. The vibrational harvesters use one of three methods: electromagnetic (inductive) [18], electrostatic (capacitive) [19] or piezoelectric [2]. Here, mechanical energy in the form of vibrations is converted to electrical energy. The thermoelectric harvesters exploit temperature gradients to generate electrical power. It is also possible to extract electrical energy from electromagnetic radiation emitted by RF sources. This generates tens of μWs of usable power and has been used in RFID tags [20] and several implanted medical devices. However, this method is not energy scavenging in the true sense because the RF power has to be provided by a dedicated external RF source which is positioned close to the harvester. Most energy harvesters in practically usable forms can provide an output power of 10 - $100\mu\text{W}$ as can be seen from Table 1.2. This sets a constraint on the average power that can be consumed by the load circuitry for self-powered operation. This low power output necessitates not only the design of ultra-low power logic circuits but also efficient power delivery interface circuits that can extract the maximum power available out of the energy harvesters.

One of the main limitations of existing energy processing circuits that extract power from energy harvesters is in their interface circuitry. In the specific example of piezoelectric energy harvesters, the rectifier circuits that interface with the harvester severely limit the electrical power extractable from the piezoelectric harvesting element. Further, the power consumed in the control circuits of these energy processors reduces the amount of usable electrical power. The interface circuits to energy harvesters must be optimized not just for energy efficiency but also to provide the right impedance to extract the optimum power out of the energy harvesters. Also, integration of the energy processor electronics onto the same chip

Table 1.2: Examples of Energy Harvesting Sources

Source	Output Power	Comments
Photovoltaic		
Guilar [21]	5μW	150μm x 150μm, 20k LUX
Das [22]	120μA/cm^2	Protein based, 10W/cm^2 excitation
Thermal		
Lhermet [23]	4μW/cm^2/°c	1V at ΔT = 60°c
Leonov [24]	250μW	Ambient indoor temperature
Stark [25]	24μW	2.7V at ΔT = 5°c
Vibrational		
Renaud [26]	40μW	Piezoelectric, 35mg mass, 1.8kHz
Roundy [27]	335μW	Piezoelectric, 2.25ms^{-2}, 60Hz

that also contains the load circuits would be of great benefit in reducing the size and cost of the overall solution. This thesis looks into the interface circuits specific to piezoelectric and thermoelectric energy harvesters. For the piezoelectric energy harvesters, new rectifier designs are developed which are then used within an integrated CMOS power management solution that enables small form-factor portable applications. In the case of thermoelectric harvesters, this thesis looks at circuit design techniques that will enable electrical power extraction from the heat energy output by the human body. This poses new challenges of operating CMOS circuits from ultra-low voltages ($<$50mV). Circuit techniques are looked at to solve this problem and digital control strategies are employed to maximize the power extracted from the energy harvesting elements.

1.4   Thesis Contributions and Organization

Minimizing the energy consumption of integrated circuits is essential for enhanced battery life-times and the possibility of self-powered operation. Dynamic voltage scaling (DVS) [28] is a popular method to achieve energy efficiency in systems that have widely variant

performance demands. U-DVS systems require a variable voltage supply that can deliver subthreshold voltages ($\sim$300mV) at low load power levels (1μW) when idling, and close to the nominal voltage of the process at high load power levels when performing active operation. Sub-threshold operation is essential to minimize leakage power in always ON blocks like SRAM's and reduce energy/operation of digital circuits that can be turned OFF after finishing their operations.

As mentioned in Section 1.2, voltage scaling is an extremely attractive technique to minimize circuit energy. However, the scalable voltages required by the circuits need to be delivered efficiently from off-chip voltage sources. The ability to do this voltage conversion completely on-chip is important to reduce the cost and volume of the final solution. The need for multiple voltage domains further cements this case. The initial part of the thesis deals with switched capacitor DC-DC converters as viable alternatives to inductor-based switching regulators for on-chip applications. They can be used to provide load currents in the order of 10's of milli-amps with around 80% efficiency. Chapter 2 describes the different efficiency loss mechanisms within a switched capacitor DC-DC converter with on-chip charge transfer capacitors. Analytical expressions are provided for these loss mechanisms. The current handling capability of switched capacitor converters are looked into and insights are given on how to pick the region of operation of the converter to maximize load current handling capabilities and efficiency. The analysis done in this chapter is used in the implementation of CMOS switched capacitor DC-DC converters described in chapter 3.

To demonstrate on-chip voltage scalable DC-DC conversion, three different designs are implemented in chapter 3. The first design is in a 0.18μm CMOS process and demonstrates a voltage scalable switched capacitor DC-DC converter that can provide >70% efficiency over a wide range of load voltages from 0.3V to 1.1V. The converter introduces new techniques to mitigate some of the common loss mechanisms in a switched capacitor design. With the help of completely digital control circuitry, the switched capacitor DC-DC converter is able to maintain high efficiencies over a wide load power range from 5μW to 1mW. The second design builds on the techniques utilized in the first converter. It is built in a 65nm

CMOS process and employs improved gain setting architectures which can handle higher load currents for the same silicon area. It also employs a charge recycling technique to mitigate bottom-plate parasitic losses which leads to a 5% improvement in efficiency. Chapter 3 concludes with a switched capacitor DC-DC converter design that is embedded within a subthreshold microcontroller system. The DC-DC converter acts as the power delivery unit to the system. It occupies a small fraction of the total area of the system and enables the microcontroller to operate at subthreshold voltages at >75% efficiency. The analysis and designs presented in chapter 2 and 3 demonstrate the feasibility of using switched capacitor DC-DC converters as a high efficiency alternative to linear regulators and as a low cost alternative to inductor-based switching regulators. Close to 10mA of output current can be handled by the converters described and even higher current handling capability is possible with high frequency switching and denser capacitors. Digital control techniques employed enable the DC-DC converters to maintain a constant efficiency over a wide range of load voltage and orders of magnitude change in load current.

Extending the battery life-time to over 10 years or eliminating the battery completely is of prime importance in many sensor-node and medical applications where it is prohibitive to replace the battery every few years. Harvesting ambient vibrational, light or thermal energy holds much promise in realizing this goal. Self-powered operation is an exciting area which is widely researched upon. As discussed in Section 1.3, the interface circuits to energy harvesters must be optimized not just for energy efficiency but also to provide the right impedance to extract the optimum power out of the energy harvesters. In the specific case of piezoelectric energy harvesters, the interface circuit must rectify the AC waveform output by the harvester and condition it suitably to provide the right voltage to the circuits that are powered by the harvester. Chapter 4 talks about the commonly used interface circuits for piezoelectric energy harvesters and identifies the problems with them. Two new rectifier designs are proposed. The first one enables 2X improvement in output power with the help of just a CMOS switch. The second rectifier design with the help of an inductor gives more than 4X improvement in output power extracted from the piezoelectric energy harvester.

Chapter 4 demonstrates these rectifier designs with the help of a test-chip built in a 0.35μm CMOS process. The inductor used within the rectifier is shared efficiently with a multitude of DC-DC converters in the piezoelectric energy harvesting chip leading to a compact, cost-efficient solution. The DC-DC converters designed as part of a complete power management solution achieve efficiencies of greater than 85% even in the micro-watt power levels output by the harvester.

Chapter 5 deals with thermoelectric energy harvesters. Thermoelectric elements can be used to harvest thermal energy present in everyday surroundings like on the human body to provide usable electrical power. The voltage output by the thermoelectric elements are proportional to the temperature difference across them. This is of concern while using thermal harvesters in body-worn applications as the voltage output by the harvester is only 25-50mV in most cases. Chapter 5 talks about some of the commonly used circuits to startup from ultra-low voltages. A new technique is then presented that allows CMOS circuits to interface directly with and extract power out of thermoelectric generators. The mechanically assisted startup circuit demonstrated with the help of a test-chip built in a 0.35μm CMOS process makes use of human motion to generate high voltages which is used to power load circuits. This enables load circuits like processors and radios to operate directly of the thermoelectric generator without the aid of a battery. A complete power management solution is provided that could extract electrical power efficiently from the harvester independent of the input voltage conditions. With the help of closed-loop control techniques, the energy processing circuit is able to maintain efficiency over a wide range of load voltage and process variations. Chapter 6 provides conclusions for the work done as part of this thesis and suggests open problems for future research related to this work.

Chapter 2

On-Chip Switched Capacitor DC-DC Converters

Dynamic Voltage Scaled systems are fast becoming increasingly relevant in modern day power constrained electronic systems. DVS is one of the most effective techniques to minimize power consumption while meeting performance requirements. DVS systems usually require a DC-DC converter that can supply scalable voltages as demanded by the load circuit. These converters not only have to supply these scalable voltages but also maintain their efficiency over a wide range. As battery life becomes a key specification, many portable electronic systems today are designed to consume extremely low amounts of power (<10mW). Even in more complex electronic systems like cell phones, many power domains within the system consume less than 10mA of total current. In this space, it becomes feasible to introduce switched capacitor DC-DC converters as the power delivery units to integrated circuits. With the help of on-chip capacitors, these DC-DC converters provide higher efficiencies than possible on-chip with linear regulators while providing the flexibility of scalable load voltages. DVS systems often require multiple on-chip voltage domains with each domain having specific power requirements. A switched capacitor (SC) DC-DC converter is a good choice for such battery operated systems because it can minimize the number of off-chip components or even eliminate them and does not require any inductors. Switched capacitor DC-DC converters

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widely referred to in literature as charge pumps have been in use for a long time as voltage doublers [29] and for generating higher voltages to drive memories and displays [30]. Previous implementations of SC converters have commonly used off-chip charge-transfer capacitors [31] [32] to output high load power levels. Some of these converters employ gain hopping to support a wide range of input voltages [33]. A SC DC-DC converter which integrates the charge-transfer capacitors was described in [34]. In this chapter, detailed analysis is provided on the efficiency limiting mechanisms of on-chip voltage scalable switched capacitor DC-DC converters. This is followed by an analysis on the current handling capabilities of these converters. The actual implementation of the switched capacitor DC-DC converters is described in the next chapter.

2.1 DC-DC Converters for U-DVS

2.1.1 Linear Regulators

Low-Dropout (LDO) linear regulators [35] are widely used to supply analog and digital circuits and feature in several standalone or embedded power management IC's. The main advantage of LDO's is that they can be completely on-chip, occupy very little area and offer good transient and ripple characteristics, together with being a low-cost solution. Using LDO's for U-DVS however is detrimental because of the linear loss of efficiency in an LDO. A linear regulator essentially controls the resistance of a transistor in order to regulate the output voltage as shown in Figure 2-1(a). As a result, the current delivered to the load flows directly from the battery and hence the maximum efficiency achievable is limited to the ratio of the output voltage to the input voltage (V_L/V_{BAT}). Thus, the farther away the load voltage is from the battery voltage, the lower the efficiency of the LDO. This hampers the potential savings in power consumption that can be achieved by lowering the voltage through dynamic voltage scaling.
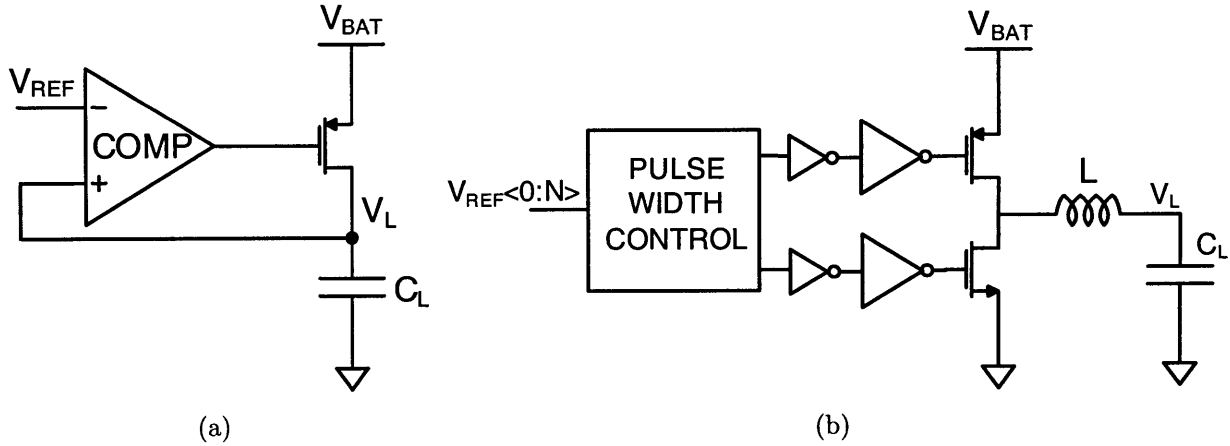
Figure 2-1: Simplified representation of (a) Low-dropout regulator and (b) Inductor-based buck regulator

2.1.2 Inductor based DC-DC Converter

The most efficient DC-DC voltage converters in general are off-chip inductor based switching regulators, which normally generate a reduced DC voltage level by filtering a pulse-width modulated (PWM) signal through a simple LC filter as shown in Figure 2-1(b). A buck-type regulator can generate different DC voltage levels by varying the duty-cycle of the PWM signal. Given ideal devices and passives, an inductor based DC-DC converter can theoretically achieve 100% efficiency independent of the load voltage being delivered. Moreover, in the context of DVS systems, scaling the output voltage can be done with completely digital control circuitry [36] which consumes very little overhead power. An implementation of an inductor based switching regulator for voltage conversion is described in Section 4.7. While buck converters [37] can operate at very high efficiencies (>90%), they generally require off-chip filter components. This might limit their usefulness for integrated power converter applications. Integrating the filter inductor on-chip requires very high switching frequencies (>100MHz) [38] in order to minimize area consumed. This increases the switching losses in the converter and together with the increase in conduction losses due to the low inductor Q-factors achievable on-chip, severely affects the efficiency that can be obtained out of the converter.

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2.1.3 Switched Capacitor DC-DC Converter

Switched capacitor (SC) DC-DC converters (charge pumps) [29] are widely used in applications where a voltage higher than, or of the opposite polarity to, the input voltage is needed. A switched capacitor converter comprises only of capacitors and switches and hence does not need the magnetic storage elements used by inductor-based buck converters. It employs these capacitors and switches to perform voltage conversion. U-DVS systems often require multiple on-chip voltage domains with each domain having specific power requirements. Using traditional switched inductor regulators would mean using multiple inductors to cater to these different voltage domains. This is prohibitive in terms of cost and motivates the designer to look into an on-chip solution that can provide scaled supply voltages at good efficiencies. Switched capacitor DC-DC converters are a viable option for such systems. One of the main drawbacks of traditional on-chip switched capacitor DC-DC converters is their low efficiency compared to regular switching converters. The focus of this work is to minimize efficiency limiting losses of on-chip switched capacitor converters and improve their voltage scalability.
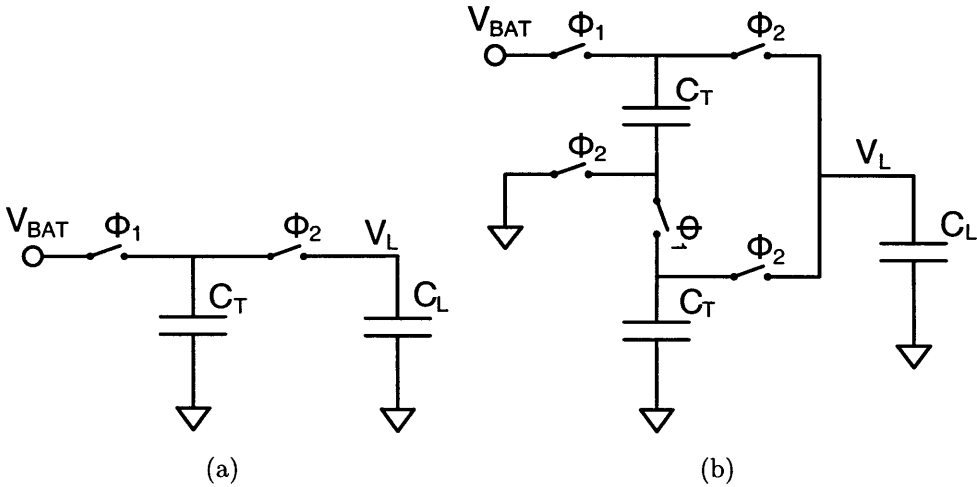
Figure 2-2: Switched capacitor DC-DC converter

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2.2 Scalable Voltage Generation

The fundamental problem with capacitive charge transfer is that a capacitor cannot be charged from a battery or from another capacitor with 100% efficiency with the help of only switches. Figure 2-2(a) shows a load capacitor C_L being charged from a battery through a charge transfer capacitor C_T. Assuming that C_L is held at the voltage V_L, in steady state, let the charge that flows into C_T from the battery in phase ϕ_1 be q. This must equal the charge flowing out of C_T into C_L in phase ϕ_2. Since the same amount of charge is extracted from V_{BAT} and flows into V_L, the fundamental limit on the efficiency of this circuit can be given by

$$Efficiency = \frac{Energy\ delivered\ to\ load\ /\ cycle}{Energy\ extracted\ from\ battery\ /\ cycle} = \frac{qV_L}{qV_{BAT}} = \frac{V_L}{V_{BAT}} \qquad (2.1)$$

The second scenario shown in Figure 2-2(b) shows a voltage divide-by-2 circuit. Here, 2 capacitors of equal value C_T are charged in series in phase ϕ_1 and in phase ϕ_2 they discharge in parallel to the load capacitor C_L. Here again in steady state, the charge transfer capacitors C_T discharge into C_L two times the amount of charge they extract from the battery during phase ϕ_1. Hence, every cycle if q amount of charge is extracted from the battery, $2q$ amount of charge flows into C_L. Thus, the overall efficiency of this circuit can be given by $V_L/(V_{BAT}/2)$. Thus, we see that in both cases the efficiency of charge transfer is linearly dependent on the load voltage V_L. This can be extended to any topology of a switched capacitor DC-DC converter all of which are fundamentally limited in efficiency to V_L/V_{NL} where V_{NL} is the no-load voltage of the specific topology. This fundamental limitation in efficiency is because of conduction losses resulting from capacitive charge transfer using switches. The efficiency might be further degraded due to the presence of other loss mechanisms which will be discussed in more detail later in this chapter.

This linear efficiency drop means that in order to get good efficiencies over a wide load voltage range, more gain settings are needed that have their no-load voltages closer to the load voltage desired. The first switched capacitor DC-DC converter implemented as part of
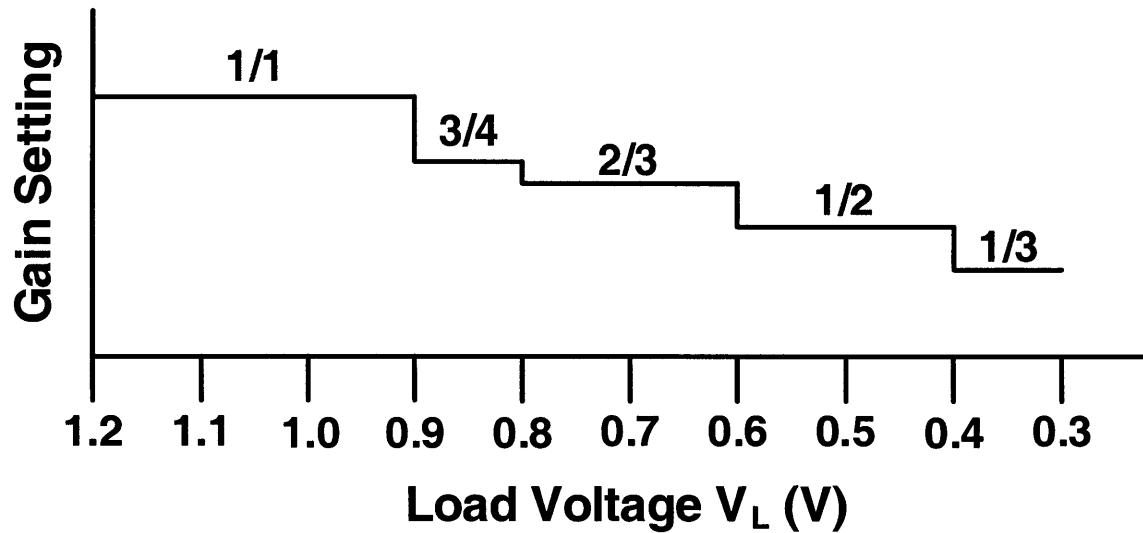
Figure 2-3: Different gain settings employed to maintain efficiency over a wide load voltage range.

this work was designed to deliver scalable load voltages from 0.3V to 1.1V from a 1.2V input voltage source. Figure 2-3 shows how different gain settings can be used to cater to different load voltages. Consider the case where a load voltage of 550mV is to delivered. Using a 1/1 gain setting, which behaves very much like a linear regulator, limits the efficiency to 45.8%. Using a 1/2 gain setting increases the theoretical efficiency limit to 91.7%.
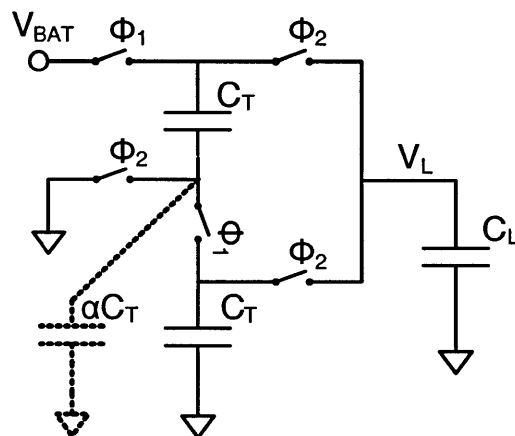
Figure 2-4: Implementation of a voltage divide-by-2 circuit which shows the bottom-plate parasitic capacitor.

2.3 Primary Loss Mechanisms in a Switched Capacitor DC-DC Converter

Efficiency of a power converter is a key metric for battery operated electronics and energy starved systems. The principal contributors to efficiency loss in a switched capacitor DC-DC converter are listed below. The loss mechanisms will be explained with respect to the voltage-divide-by-2 circuit shown in Figure 2-4 for easier understanding. They can be extended with little effort to other topologies of switched capacitor DC-DC converters.

2.3.1 Conduction loss in transferring charge from battery to load

As was described in the previous section, this is a fundamental loss mechanism which arises from charging a capacitor through a switch. When charge flows from the battery to the load, some part of it is dissipated within the switches of the DC-DC converter. The farther away the desired load voltage is from the no-load voltage of a given gain setting, the greater the dissipation is.

2.3.2 Loss due to bottom-plate parasitic capacitors

The second main contributor to efficiency loss is that due to parasitic bottom-plate capacitors. This arises due to charging the bottom-plate parasitic capacitance [39] of the charge-transfer capacitors every cycle. This is of specific concern for on-chip capacitors in digital CMOS processes. For capacitors implemented using 2 metals, the parasitic arises due to the capacitance from the bottom-plate to the substrate. For gate-oxide capacitors implemented with the N-well as the bottom-plate, the parasitic arises due to the reverse biases diode capacitance of the N-well, P-substrate junction. The bottom-plate capacitance C_{BP}, scales with the capacitor area and can be expressed as $C_{BP} = \alpha C$, where α can be as high as 20% for on-chip capacitors in digital CMOS processes. Consider the circuit shown in Figure 2-4. During the phase ϕ_1 when the 2 charge-transfer capacitors are charged to one-half the battery voltage, the bottom-plate parasitic capacitance of the top capacitor

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also gets charged to $V_{BAT}/2$. In phase ϕ_2 when these capacitors are connected in parallel to charge the load, the energy stored in the bottom-plate parasitic capacitance is lost by connecting it to ground. The energy lost per cycle in steady-state due to C_{BP} of the top capacitor is

$$E_{BP} = \frac{\alpha C_T V_{BAT}^2}{4} \tag{2.2}$$

2.3.3 Gate-drive loss

The power lost due to switching the gate capacitances of the charge-transfer switches is a significant contributor to the total power loss. The energy expended in switching the gate capacitances of the charge- transfer switches every cycle can be given by

$$E_{SW} = C_{ox} W_{EFF} L V_{BAT}^2 \tag{2.3}$$

where C_{ox} is the gate-oxide capacitance per unit area, W_{EFF} is the cumulative width of switches that are turned ON / OFF per cycle, and L is the minimum channel length of the technology node in which the switched capacitor converter is implemented.

2.3.4 Power loss in the control circuitry

The circuit shown in Figure 2-4 will be surrounded with control circuits that are used to achieve voltage regulation. The power lost in the control circuitry is of specific concern while delivering ultra-low load power levels. The energy lost in the control circuitry every switching cycle can be broken into a switching and a leakage component and is given by

$$E_{CONT} = C_{CONT} V_{BAT}^2 + I_{leak} V_{BAT} T_{SW} \tag{2.4}$$

where C_{CONT} is the equivalent capacitance switched in the control circuit per cycle, I_{leak} is the total leakage current consumed by the control circuitry and T_{SW} is the average time-period of a switching cycle.

The overall efficiency taking into account all the above mentioned losses can be expressed as the ratio between the total energy delivered to the load per cycle (E_L) to the sum of the energy extracted from the battery (E_{BAT}) and the energy losses per cycle.

$$\eta = \frac{E_L}{E_{BAT} + E_{BP} + E_{SW} + E_{CONT}} \quad (2.5)$$
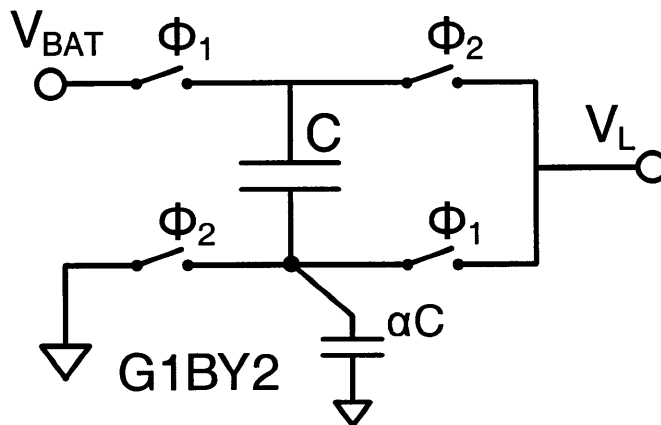
Figure 2-5: Alternate implementation of a voltage divide-by-2 circuit.

2.4 Load Current and Equivalent Resistance Analysis

This section presents an analysis of the current delivered to the load by the switched capacitor DC-DC converter. Consider an alternate implementation of a voltage divide-by-2 circuit shown in Figure 2-5. Let it deliver a load voltage $V_L = V_{NL} - V_{DIFF}$, where $V_{NL} = V_{BAT}/2$, is the no-load voltage for this gain setting. All the switches are assumed to be sized such that they have a resistance of $R\Omega$ when they are ON. In steady state, let V_{c1} and V_{c2} be the voltage across the capacitor C at the end of phase ϕ_1 and ϕ_2 respectively. They can be represented as

$$V_{c1} = V_{BAT} - V_L + [V_{c2} - (V_{BAT} - V_L)]e^{-t/\tau} \quad (2.6)$$

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$$V_{c2} = V_L + [V_{c1} - V_L]e^{-t/\tau} \tag{2.7}$$

where $\tau = 2RC$, and t is the time for which the switches are ON in one phase. Assuming that the time for which the switches are ON in both the phases is the same, $t \sim 1/2f_s$ where f_s is the frequency of operation of the switched capacitor circuit. The voltage swing across C every half-cycle is given by

$$V_s = V_{c1} - V_{c2} = \frac{(V_{BAT} - 2V_L)(1 - e^{-1/4f_sRC})}{(1 + e^{-1/4f_sRC})} \tag{2.8}$$

Let us define the term k as

$$k = \frac{(1 - e^{-1/4f_sRC})}{(1 + e^{-1/4f_sRC})} \tag{2.9}$$

Since $V_L = V_{BAT}/2 - V_{DIFF}$, V_s can be written as

$$V_s = 2kV_{DIFF} \tag{2.10}$$

The current supplied to the load by the voltage divide-by-2 circuit can be given by

$$I_L = 2CV_sf_s = 4kCV_{DIFF}f_s \tag{2.11}$$

An idealized equivalent circuit of the switched capacitor voltage divide-by-2 circuit is shown in Figure 2-7. The equivalent circuit does not take into account any of the non-conduction loss mechanisms and hence is not suitable for efficiency analysis. However, it can be used to figure out the load current and power delivered by a switched capacitor DC-DC converter. In the equivalent circuit, R_{EQ} represents the equivalent source resistance of a switched capacitor DC-DC converter. From Equation 2.11, we can define the R_{EQ} of the switched capacitor circuit shown in Figure 2-5 as

$$R_{EQ} = \frac{1}{4kCf_s} \tag{2.12}$$
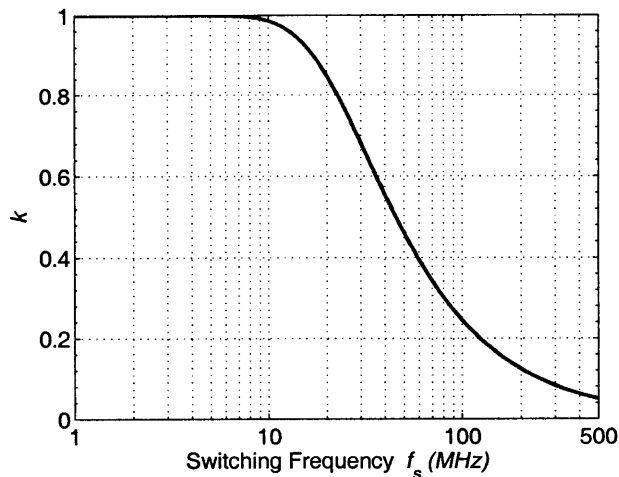
(a)
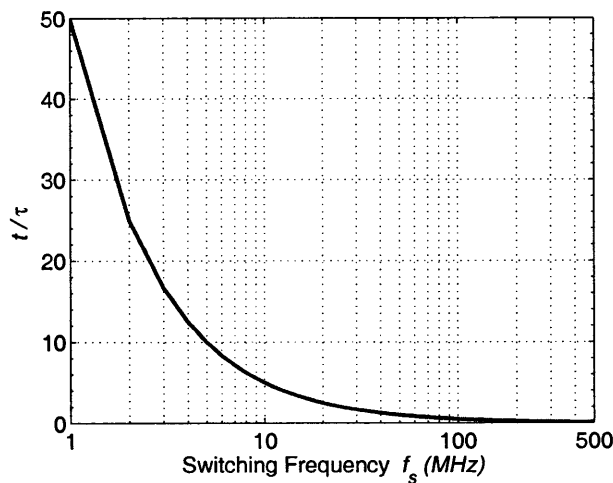
(b)

Figure 2-6: Effect of switching frequency on k and t/τ for $C=1\text{nF}$ and $R=5\Omega$

In the limit as f_s is increased to ∞, R_{EQ} reaches $2R$. To understand this intuitively, it is essential to recognise that in the high frequency limit, the voltage across C does not change. Hence, it behaves like a voltage source. Also, since the time periods of phase ϕ_1 and ϕ_2 are equal, the current through C during phase ϕ_1 must be the same as the current out of it during phase ϕ_2. This forces the voltage across C to be constant at $V_{BAT}/2$. Hence, the current to the load during both the phases can be given by $V_{DIFF}/2R$. This is the same as having an equivalent resistance of $2R$.
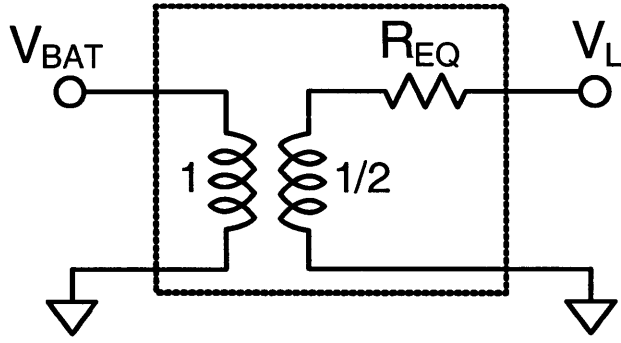
Figure 2-7: Idealized equivalent circuit of a voltage divide-by-2 circuit.

For C=1nF and R=5Ω, the equivalent resistance of the switched capacitor DC-DC converter with change in f_s is shown in Figure 2-8. It can be seen from the figure that in the high frequency limit, R_{EQ} reaches 10Ω as expected. This curve is similar to the ones described in [40], [41] and [42]. The equivalent resistance exhibits asymptotic limits in the slow and fast switching ends as was discussed in the above references.
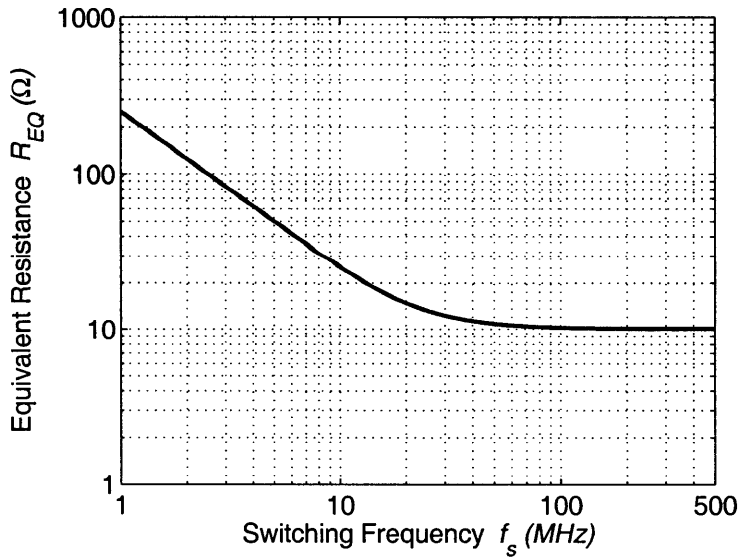
Figure 2-8: Equivalent resistance of the switched capacitor voltage divide-by-2 circuit with change in f_s.

With V_{BAT}=1.2V, Figure 2-9 shows the load current output by the switched capacitor

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DC-DC converter for varying load voltage values. The load current saturates as f_s is increased beyond a certain value. Also, the current increases as V_L decreases. This is to be expected from Figure 2-7 where for a given R_{EQ}, more current can flow into the output as V_L decreases.
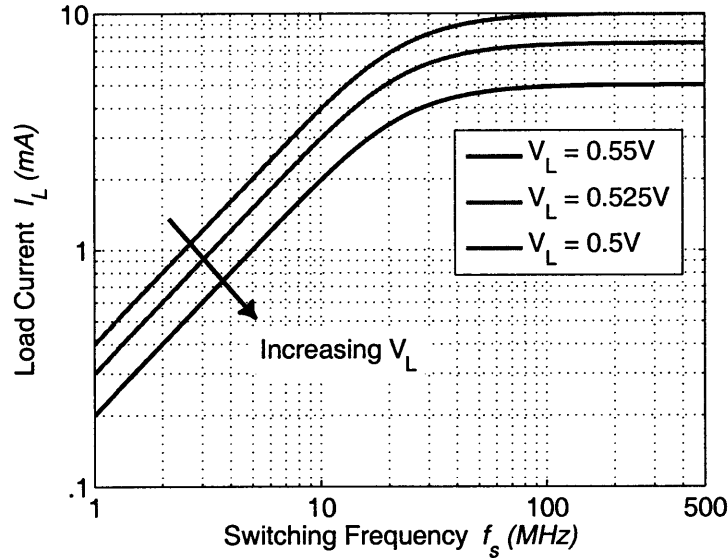
Figure 2-9: Load current delivered by the switched capacitor voltage divide-by-2 circuit with change in f_s for varying values of V_L.

Figure 2-10 shows the load current output by the switched capacitor DC-DC converter if the switch resistance is varied. V_L was set to 0.5V to get these curves. As R decreases, the load current delivered increases. Also, the knee in the load current curve gets pushed to higher values of f_s with smaller R.

2.5 Efficiency Analysis

The discussion in the above section centered around the equivalent resistance of a switched capacitor DC-DC converter and the current that it can deliver to the load as its switching frequency is changed. This section will deal with the efficiency of the switched capacitor DC-DC converter. It was noted in the above section that increasing f_s increases the load
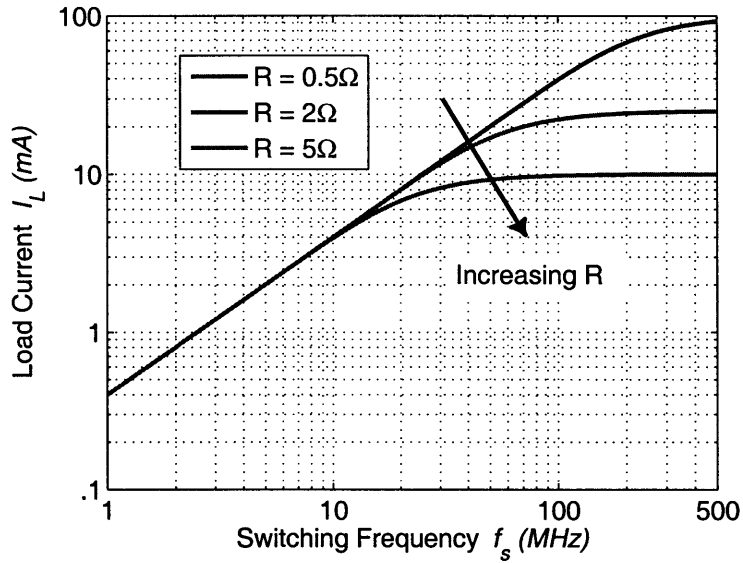
Figure 2-10: Load current delivered by the switched capacitor voltage divide-by-2 circuit with change in f_s for varying values of the switch resistance R.

current delivered. This section will give insights as to how much can we increase f_s before the efficiency loss becomes significant.

The equivalent resistance in Figure 2-7 takes into account only the conduction losses within the switched capacitor DC-DC converter. None of the other losses which occur are accounted for. Section 2.3 talked about the other major sources of loss within a switched capacitor DC-DC converter. For the converter in Figure 2-5, the gate-switching loss can be approximated as

$$P_{SW} = 4C_{ox}WLV_{DD}^2 f_s \qquad (2.13)$$

where C_{ox} is the oxide capacitance per unit area, L is the minimum channel length of the technology and W is the width of the transistor used. The driver stage gate-switching loss is assumed to be a small fraction of the overall gate-switching loss. There are 4 switches being turned ON and OFF every cycle and hence the factor 4 in the equation. It is assumed here that all the switches are identical. This may not be the case since some of the switches in

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Figure 2-5 that are ground referenced are made of NMOS while the ones referenced to V_{DD} are made of PMOS. However, it should be easy to incorporate different switches of varying widths by just summing up their widths into Equation 2.13.

The switches are sized up to achieve a specific resistance across them. Hence, the widths of the switches can be normalized with respect to the width W_o required to achieve 1Ω resistance. The power lost due to switching the gates of the transistors can then be expressed as

$$P_{SW} = (4C_{ox}W_oLV_{DD}^2)\frac{f_s}{R} = P_{so}\frac{f_s}{R} \tag{2.14}$$

where P_{so} is a constant that depends on the gain-setting and technology node being used. The power lost due to bottom-plate parasitics can be expressed as

$$P_{BP} = \alpha CV_L^2 f_s \tag{2.15}$$

where α is the fraction of the bottom-plate parasitic capacitance to the actual capacitance of the capacitor. Taking these losses into account, the overall efficiency of the switched capacitor circuit shown in Figure 2-5 can be expressed as

$$\eta = \frac{I_L V_L}{I_L V_{DD}/2 + P_{SW} + P_{BP}} \tag{2.16}$$

Plugging in the values from Equation 2.14 and Equation 2.15, the efficiency of the switched capacitor converter is given by

$$\eta = \frac{1 - \frac{V_{DIFF}}{V_{NL}}}{1 + \frac{P_{so}}{2kRCV_{DIFF}V_{DD}} + \frac{\alpha V_L^2}{2kV_{DIFF}V_{DD}}} \tag{2.17}$$

The numerator takes into account the conduction losses. The 2nd and 3rd terms in the denominator take into account the gate-switching and bottom-plate parasitic losses respectively. We can now plot the efficiency of the voltage divide-by-2 circuit of Figure 2-5 assuming C=1nF, R=5Ω, α=0.05 and P_{so}=7.488x10^{-12}. Figure 2-11 shows the efficiency of the
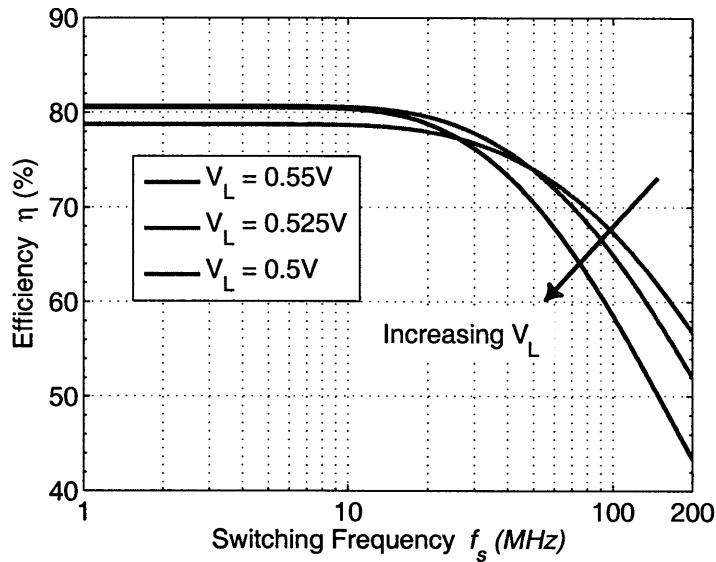
Figure 2-11: Efficiency of the switched capacitor voltage divide-by-2 circuit with change in f_s for varying values of V_L.

switched capacitor converter as f_s is varied. If just conduction loss was taken into account, the efficiency of the converter will have remained constant with change in f_s at 91.66% for V_L=0.55V, 87.5% for V_L=0.525V and 83.33% for V_L=0.5V. The presence of gate-switching and bottom-plate parasitic losses make efficiency a function of f_s. Since V_{DIFF} increases as V_L decreases, the effect of gate-switching and bottom-plate parasitic losses reduce as V_L decreases. This can be seen from the denominator in Equation 2.17. Thus, the efficiency of the switched capacitor converter is nearly the same for the three different load voltage values at low f_s. As f_s increases, the factor k decreases sharply after a certain point (see Figure 2-6(a)). This decrease in k brings down the efficiency of the switched capacitor converter. Since the gate-switching and bottom-plate parasitic losses are more pronounced at larger V_L values, efficiency drops faster at high V_L as can be seen from Figure 2-11.

Figure 2-12 shows the efficiency of the switched capacitor converter with change in the switch resistance R for V_L=0.5V. The efficiency starts higher but begins to drop faster for higher values of R. Hence, if a large load current needs to be delivered for a given total capacitance, it is best to use a small R and operate at very high frequencies. Figure 2-
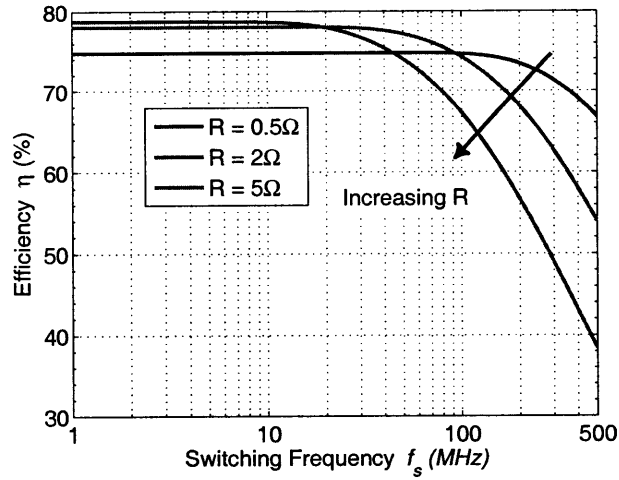
Figure 2-12: Efficiency of the switched capacitor voltage divide-by-2 circuit with change in f_s as the switch resistance R is varied.

13 shows the efficiency of the switched capacitor converter with change in the factor α for V_L=0.55V. Higher values of α lead to more bottom-plate losses and severely affect the efficiency.
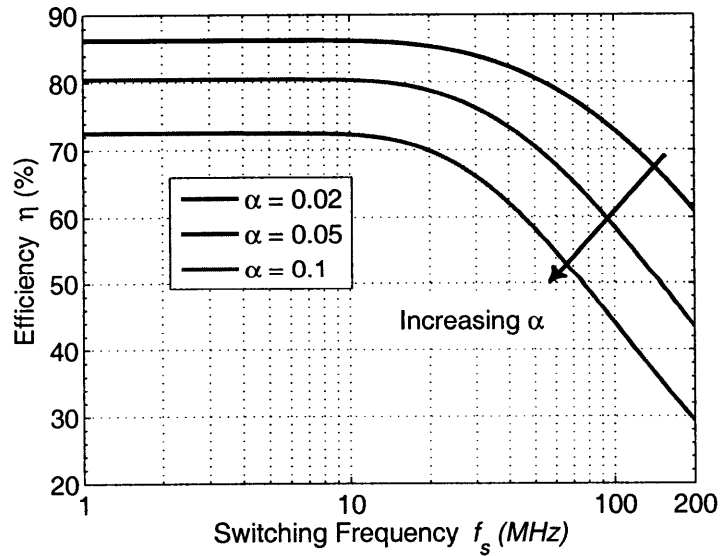
Figure 2-13: Efficiency of the switched capacitor voltage divide-by-2 circuit with change in f_s for varying values of α.

When the load current and efficiency plots of Figure 2-9 and Figure 2-11 are examined together, it can be observed that operating the DC-DC converter above 30MHz, does not lead to any significant increase in the load current I_L while the efficiency degrades significantly. Hence, from a practical point of view, it is prudent to operate the DC-DC converter at 30MHz to maximize I_L and not lose too much in terms of efficiency. However, this decision depends on factors such as α, R, V_{DIFF}, P_{so} and the gain setting in use. A very low value for α and P_{so} might lead to the efficiency staying constant for a longer range of f_s. In that case, the frequency of operation of the converter might be pushed higher without losing too much in efficiency. The decision regarding the frequency of operation (f_s)and size of the switches (R) needs to be made after examining the load current and efficiency curves to figure out the correct region of operation.

2.6   Summary and Conclusions

Switched capacitor DC-DC converters are a viable option for power delivery in on-chip integrated circuit applications. They can be used to provide load currents in the order of 10's of milli-amps with around 80% efficiency. This chapter has explained the different efficiency loss mechanisms within a switched capacitor DC-DC converter with on-chip charge transfer capacitors. Analytical expressions were provided for these loss mechanisms. It was seen that the bottom-plate parasitic loss is a significant contributor to the overall power lost within the converter. While the switched capacitor DC-DC converter cannot match the efficiencies obtained by using off-chip inductor-based DC-DC converters, it can be designed to maintain an efficiency of close to 80% by using various digitally assisted control techniques. This efficiency obtained will be better than those obtained using on-chip linear regulators or inductor-based regulators with CMOS inductors, making the switched capacitor converter an attractive choice for on-chip power converters. The current handling capability of switched capacitor converters were looked into and insights were given on how to pick the region of operation of the converter to maximize load current handling capabilities and efficiency. From the analysis provided, it was seen that increasing the switching frequency of the converter

above a certain value does not lead to a proportional increase in output current handling capability. The analysis done in this chapter will be used in the implementation of CMOS switched capacitor DC-DC converters to be described in the next chapter.

Chapter 3

CMOS Implementation of Switched Capacitor DC-DC Converters

The previous chapter provided analysis on the efficiency and load current handling capabilities of switched capacitor DC-DC converters. It was shown that with on-chip charge transfer capacitors, the converters can achieve high efficiencies of around 80% while supplying load currents of up to 10mA. The analysis will be transformed into practical designs in this chapter where three different implementations of on-chip switched capacitor DC-DC converters will be described. The first implementation is in a 0.18μm CMOS process and it presents techniques to achieve scalable load voltages with an efficiency which stays almost constant. New techniques are presented to mitigate bottom-plate parasitic, switching and control losses. The second implementation is in a 65nm digital CMOS process and it builds on the techniques developed in the first prototype. The second design also provides newer designs for gain settings and a charge recycling approach to mitigate bottom-plate parasitics. The third design is of an embedded switched capacitor DC-DC converter in a subthreshold microcontroller digital IC. It is a smaller version of the second design and demonstrates the application of switched capacitor DC-DC converters as embedded power supplies in integrated circuits.

3.1 A Voltage Scalable Switched Capacitor DC-DC Converter

This section explains the implementation of a switched capacitor DC-DC converter with on-chip charge transfer capacitors that can deliver a continuous voltage supply quantized to 10mV. The key specifications for the DC-DC converter are listed here.

- CMOS Technology Node = 180nm

- Battery Voltage (V_{BAT}) = 1.2V

- Load Voltage Deliverable (V_L) = 0.3V to 1.15V

- Load Power = 1μW to 1mW

The targeted application for the DC-DC converter is an ultra-dynamic voltage scaled system consuming a peak power of 1mW at its high voltage end and microwatts in the low subthreshold voltage end. It was shown in Section 2 that multiple gain settings are needed in a switched capacitor DC-DC converter to maintain constant efficiency over a wide range of load voltages. This section describes how scalable load voltages are generated from a 1.2V off-chip battery. Consider the G1BY2 gain setting in Figure 3-1. The charge-transfer capacitors are equal in value and help in transferring charge from the battery to the load. Switches with ϕ_1 marked on them turn ON when ϕ_1 goes high and charge the charge-transfer capacitors from the battery (V_{BAT}). In the other phase of the clock switches marked ϕ_2 turn ON, and the charge-transfer capacitors dump the charge gained onto the load capacitor (V_L). At no load, the G1BY2 gain setting circuit tries to maintain the output voltage V_L at $V_{BAT}/2$ (0.6V), where V_{BAT} is the battery voltage. The actual value of V_L that the circuit settles down to is dependent on the load current I_L, the switching frequency and C_B. The equations for energy extracted per cycle and the power delivered to the load are presented in Section 3.3. Figure 3-1 shows the different gain settings that were employed in the SC DC-DC converter. The output load voltage is scalable between 0.3V to 1.15V. Each gain

setting is clocked by two non-overlapping phases ϕ_1 and ϕ_2 of a system clock. In the first phase ϕ_1, the on-chip charge-transfer capacitors are charged from the battery. In ϕ_2, this charge gained is passed on to the load.
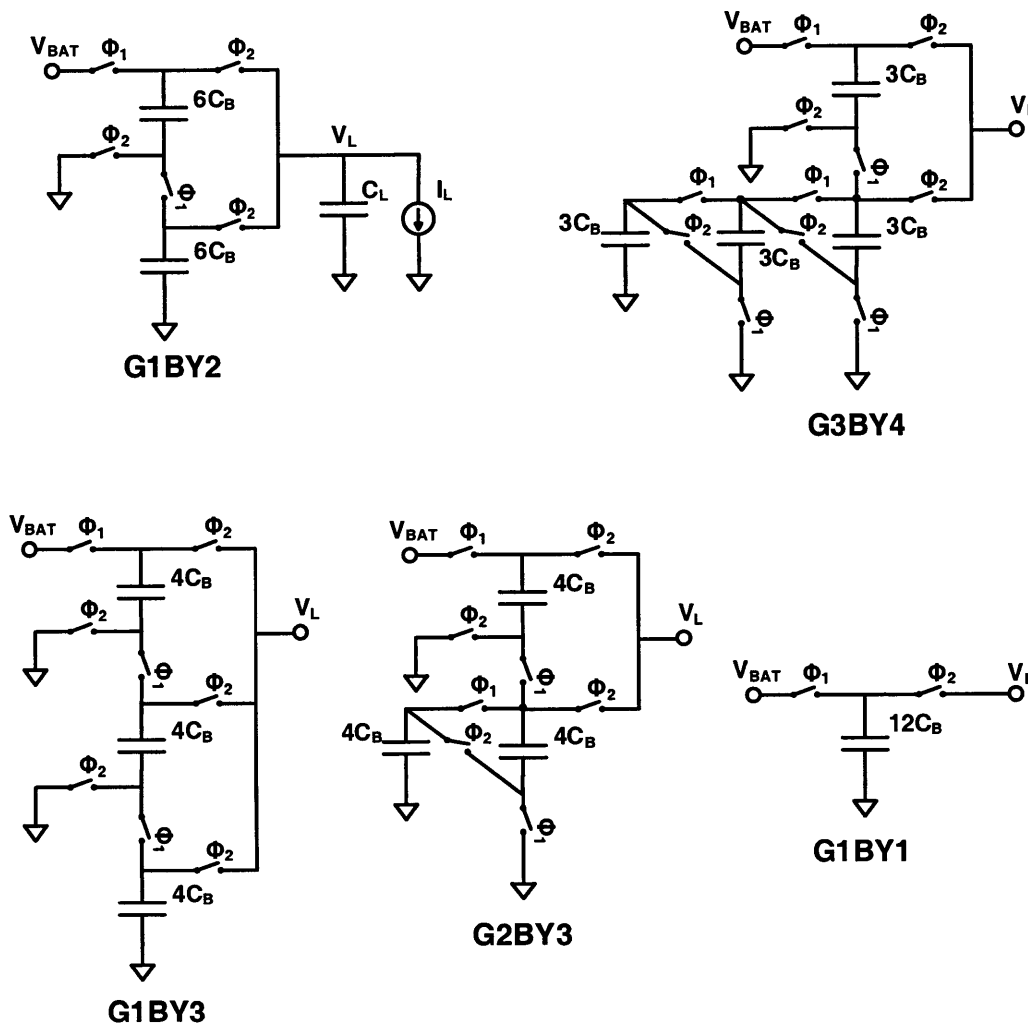
Figure 3-1: Gain settings used to generate efficiently a wide range of load voltages from a 1.2V supply.

The G1BY1 gain setting provides 1.2V at no-load. This gain setting behaves essentially like a linear regulator and it is used to provide load voltages between 0.9V and 1.2V. The G1BY2 gain setting with a no-load voltage of 0.6V is a simple voltage divide-by-2 circuit, where 2 capacitors of equal value $6C_B$ are charged in series and discharge to the load in

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parallel. This gain setting caters to load voltages between 0.4V and 0.6V. The G1BY3 gain setting is a divide-by-3 circuit and it caters to load voltages of 0.4V and below. Here 3 capacitors of equal value are charged in series in one phase and discharge to the load in parallel in the other phase.
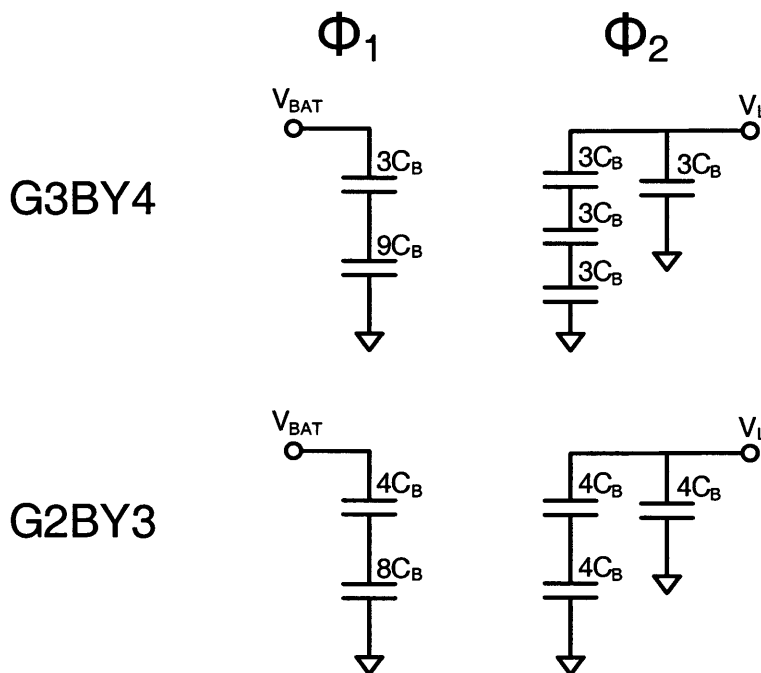
Figure 3-2: Arrangements of capacitors during phases ϕ_1 and ϕ_2 in the G3BY4 and G2BY3 gain settings.

The G2BY3 gain setting has a no-load voltage of 0.8V and it provides a $2/3^{rd}$ voltage ratio output. Its functioning can be explained by looking at the configuration of its capacitors during phases ϕ_1 and ϕ_2 as shown in Figure 3-2. In G2BY3, during ϕ_1, two capacitors of value $4C_B$ and $8C_B$ are charged in series from the battery. In steady state with low bottom-plate parasitics and assuming the switches are designed to allow the capacitors to settle, the top capacitor of value $4C_B$ gets charged to 800mV or $2/3^{rd}$ of the battery voltage and the bottom capacitor of $8C_B$ to 400mV or $1/3^{rd}$ of the battery voltage. During ϕ_2, the top $4C_B$ capacitor is connected directly to the load while the bottom $8C_B$ capacitor is split into two and connected in series with the load. This way the total voltage across the

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series combination is 800mV. The G2BY3 gain setting is used to deliver load voltages below 800mV. The G3BY4 gain setting is a ratio 3/4 circuit and has a no-load voltage of 0.9V. Its operation is similar to the G3BY4 gain setting. But here, during ϕ_1, a series combination of $3C_B$ and $9C_B$ gets charged from the battery. In phase ϕ_2, the $9C_B$ capacitor is broken down into three $3C_B$ capacitors that are connected in series to charge the load. The G3BY4 gain setting is used to deliver load voltages below 0.9V.
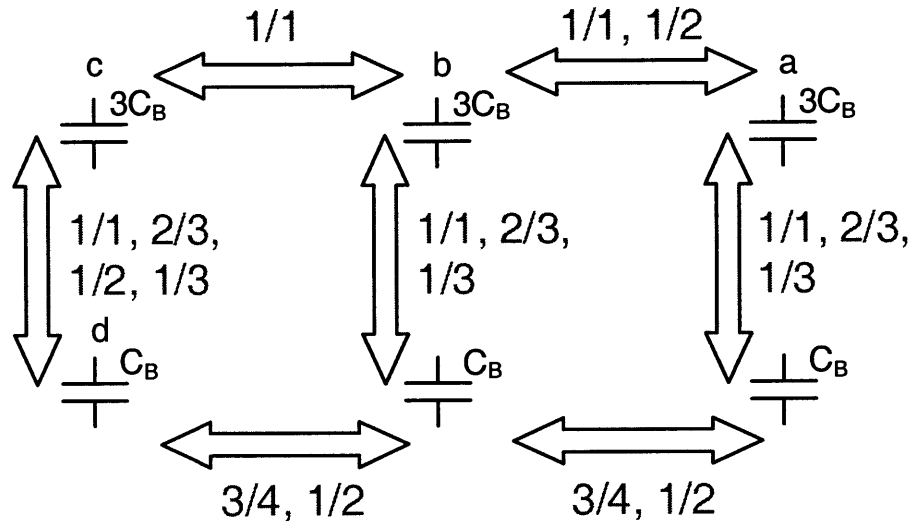
Figure 3-3: Topology switches used to piece together capacitor fragments for a given gain setting.

All the gain settings employ the same amount of charge transfer capacitance of $12C_B$. The ability to split a given amount of capacitance into multiple parts to achieve different gain settings is possible on-chip. Doing the same thing with off-chip capacitors might involve multiple discrete capacitors which will raise the board area occupied by the converter. The capacitor fragments are joined together with the help of topology switches as shown in Figure 3-3. A topology switch represented by a two-headed arrow joins two capacitors. It consists of 2 switches, one to connect the top plates and one for the bottom plates. The topology switch is turned ON when the gain setting marked on top of the arrow is employed.

Apart from the topology switches, charge-transfer switches are employed within each gain setting. These switches are driven by either ϕ_1 or ϕ_2. All the charge-transfer switches used in

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	TOP	MID	BOT	X
G1BY1	$12C_B$	–	–	–
G3BY4	$3C_B$	$3C_B$	$3C_B$	$3C_B$
G2BY3	$4C_B$	$4C_B$	$4C_B$	–
G1BY2	$6C_B$	–	$6C_B$	–
G1BY3	$4C_B$	$4C_B$	$4C_B$	–
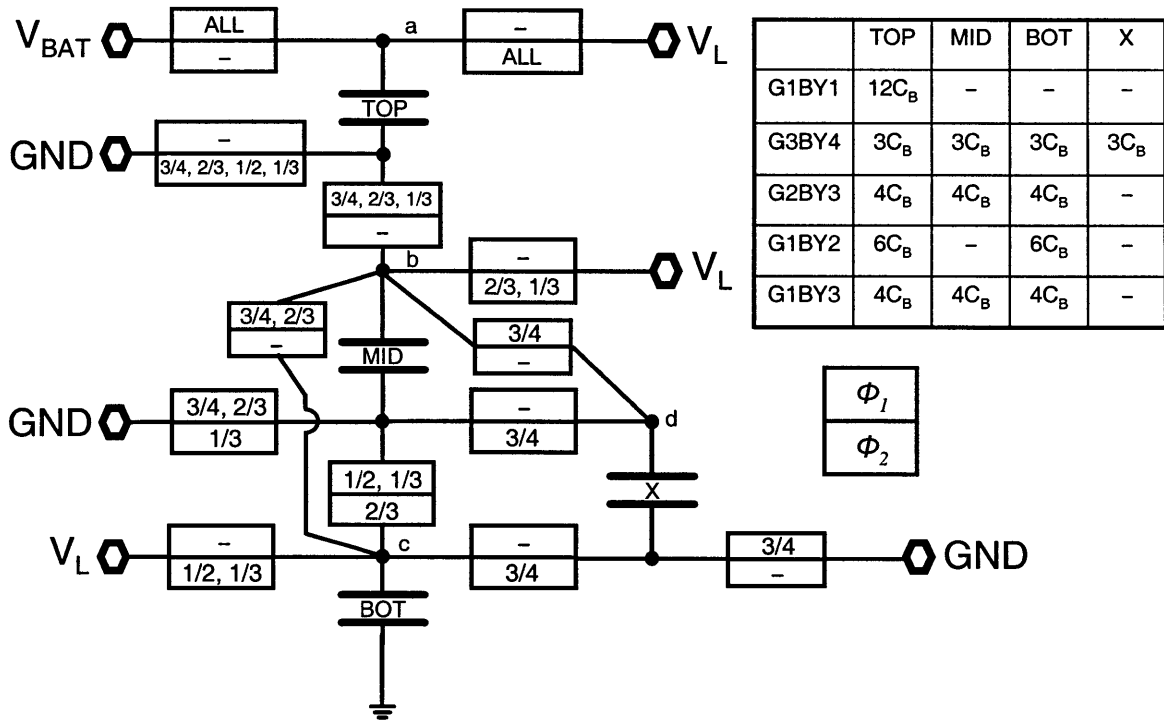
Figure 3-4: Charge-transfer switch array (each box represents a switch).

the individual gain settings are realized from a total of only 13 switches as can be seen from the switch array in Figure 3-4. Each box in the array is representative of a switch which is turned ON depending on the gain setting in use and the phase of the clock. For instance, the switch which connects the top plate of capacitor TOP to the battery is turned ON in phase ϕ_1 for all gain settings while the switch that connects the bottom plate of capacitor MID to ground (GND) turns ON during ϕ_1 for gain settings G3BY4, G2BY3 and during ϕ_2 for gain setting G1BY3. The table inside Figure 3-4 shows the value of the individual capacitors used in the different topologies. The nodes marked a, b, c and d correspond to the similarly named nodes shown in the topology switches of Figure 3-3. The charge-transfer switches are realized using PMOS or NMOS transistors or a combination of them depending on the location of the switch in the array (see Section 3.4.3). A very simple digital control scheme is utilized to turn ON the switches depending on the gain setting in use. This arrangement of the switch array enables efficient sharing of charge-transfer switches between multiple gain

settings.
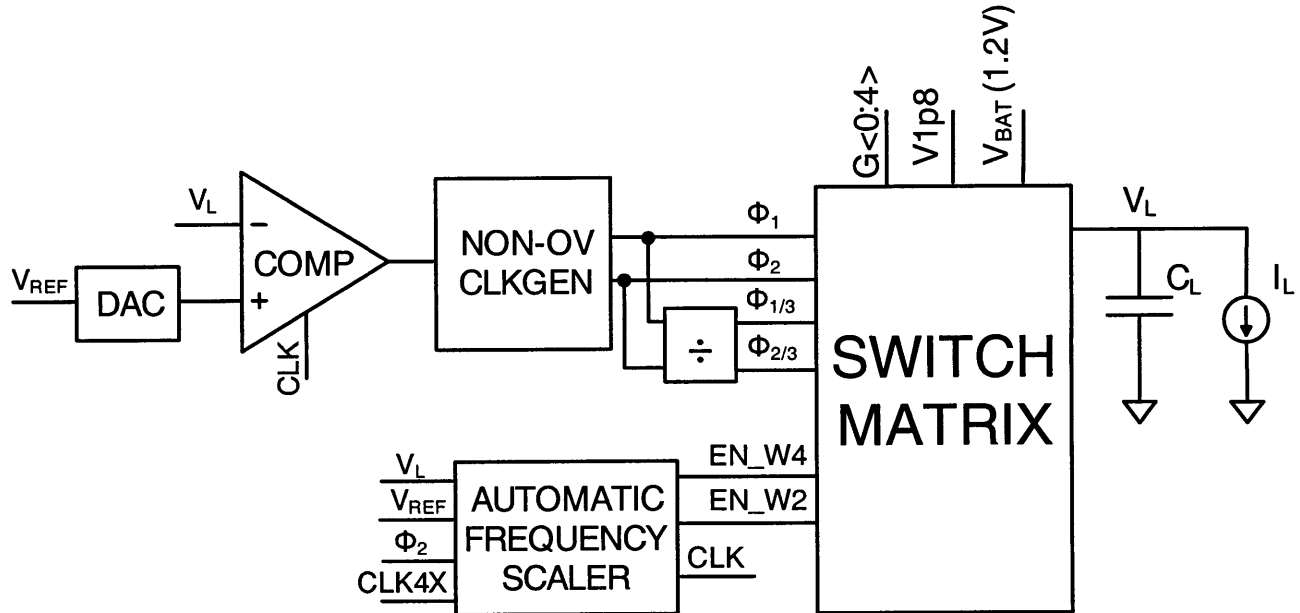
Figure 3-5: Architecture of the switched capacitor DC-DC converter system.

3.2 Switched Capacitor DC-DC Converter System Architecture

Figure 3-5 shows the architecture of the SC DC-DC converter. At the core of the system is the switch matrix which contains the charge-transfer capacitors, and the topology, charge-transfer switches as shown in Figure 3-1. A suitable gain setting is chosen depending on the reference voltage V_{REF}, which is set digitally. The digital reference is converted to an analog value using an on-chip charge redistribution digital-to-analog converter. The entire circuit except for the topology switches operates out of a 1.2V voltage supply. A 1.8V supply is used only for the topology switches. In steady state, as there is no switching involved in the topology switches, negligible power is consumed from the 1.8V supply. A pulse frequency modulation (PFM) mode control is used to regulate the output voltage to the desired value. A dynamic comparator clocked by the signal CLK is used for this purpose. When the

output voltage V_L is above V_{REF}, the switches are all set to the ϕ_1 mode. When V_L falls below V_{REF}, the comparator triggers a ϕ_2 pulse, which charges up the output load capacitor. The non-overlapping clock generator block prevents any overlap between the ϕ_1 and ϕ_2 ON phases. A clock divider is used to generate $\phi_{1/3}$ and $\phi_{2/3}$ phases. The use of these phases is explained in Section 3.4.2.

3.2.1 Automatic Frequency Scaler

To minimize gate-switching losses, the circuit automatically adjusts the switching frequency depending on the load power demand. The automatic frequency scaling (AFS) block which performs the frequency selection is shown in Figure 3-6. An additional comparator called the overload comparator is used in the AFS block. The reference voltage of the overload comparator is set to $V_{REF}-V_{OFF}$, where V_{OFF} is an offset voltage ($\sim$20mV) which again is set digitally. When the DC-DC converter, operating in steady state, cannot supply the desired load power at a given switching frequency, V_L begins to fall below V_{REF} (see Equation 3.3). As V_L falls below $V_{REF}-V_{OFF}$, the overload comparator triggers the $INCR$ signal. This signal is used to double the switching frequency which in turn doubles the width of the charge-transfer switches. The charge-transfer switches are sized such that the capacitors just settle to their final voltage at the end of the clock phases. Hence, on doubling the switching frequency, the switch sizes are also doubled. At low load powers, the switching frequency is brought down with the help of a counter mechanism. If the number of ϕ_2 pulses for every 4 CLK cycles is found to be less than 3, the CLR_W4 signal is triggered which halves the switching frequency and the width of the charge-transfer switches. The signals EN_W2 and EN_W4 determine the switching frequency. When EN_W2 is high, 2X the minimum clock frequency is used and when EN_W4 is high, 4X the minimum clock frequency is used. The signals EN_W2 and EN_W4 are fed into the switch matrix to suitably size the charge-transfer switches. While the PFM mode control effectively reduces the frequency of ϕ_2 pulses as load power decreases, the AFS block helps in bringing down the overall system switching frequency together with the width of the charge-transfer switches, thereby

reducing the switching losses in the gate-drive and the control circuitry. The entire control circuitry is digital and consumes no static power, which is a critical feature to achieve good efficiency at ultra-low load power levels. It is extremely scalable in terms of complexity to suit the load power and voltage demands of the target application.
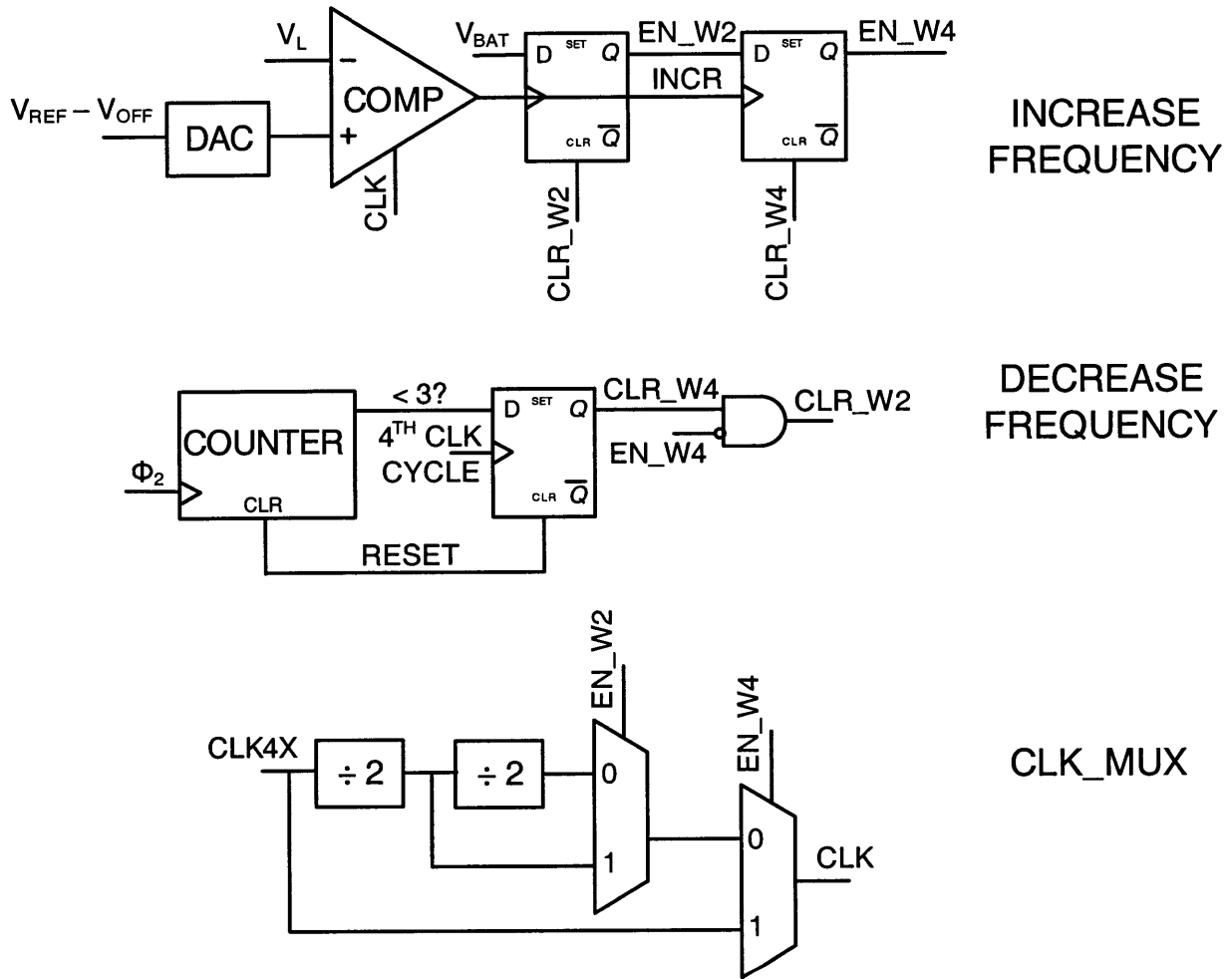
Figure 3-6: Automatic frequency scaling Block.

3.3   Power Delivery

This section presents an analysis of the power delivered to the load by the DC-DC converter. Consider the G1BY2 gain setting shown in Figure 3-1. Let the G1BY2 gain setting deliver

a load voltage $V_L = V_{NL} - V_{DIFF}$, where $V_{NL} = V_{BAT}/2$, is the no-load voltage for this gain setting. The switches are designed to let the capacitors just settle during phase ϕ_1 or ϕ_2. This presents a good trade-off between the frequency of operation, switch size, output current handling capability and overall efficiency as was seen from the analysis presented in chapter 2. While operating in steady-state, during phase ϕ_2, both the $6C_B$ charge-transfer capacitors discharge down to V_L when the load capacitor is much larger than $6C_B$. When they are connected back in series again during phase ϕ_1, both these capacitors get charged back to $V_{BAT}/2$. The energy extracted from the battery during this process is given by

$$E_{BAT} = 6C_B V_{BAT} V_{DIFF} \qquad (3.1)$$

During ϕ_2, this excess charge is transferred to the load capacitor. The charge-transfer capacitors transfer twice the charge gained from the battery during ϕ_1. However, this charge is delivered at a voltage V_L and hence, as was explained before, the energy delivered to the load every cycle is a linear scaled version of the energy extracted from the battery and is given by

$$E_L = E_{BAT} \frac{V_{NL} - V_{DIFF}}{V_{NL}} = 12C_B V_L V_{DIFF} \qquad (3.2)$$

The maximum power that can be delivered to the load by this gain setting when switching at a frequency f_s is then given by

$$P_L = E_L f_s = 12C_B V_L V_{DIFF} f_s = E_{BAT} f_s \eta_{lin} \qquad (3.3)$$

where η_{lin} is the linear efficiency loss. From this expression it can be seen that for a given load voltage to deliver more load power, C_B or f_s need to be increased. Increasing C_B increases the energy extracted from the battery every switching cycle, whereas increasing f_s increases the rate of delivery of the charge packets. The power delivered to the load also depends on the gain setting being used. Table 3.1 gives a breakdown of E_{BAT} and η_{lin} for the various gain settings.

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Table 3.1: Energy extracted from battery every cycle

Gain Setting	E_{BAT}	η_{lin}
G1BY1	$12C_B V_{BAT} V_{DIFF}$	$V_L/1.2V$
G3BY4	$3C_B V_{BAT} V_{DIFF}$	$V_L/0.9V$
G2BY3	$4C_B V_{BAT} V_{DIFF}$	$V_L/0.8V$
G1BY2	$6C_B V_{BAT} V_{DIFF}$	$V_L/0.6V$
G1BY3	$4C_B V_{BAT} V_{DIFF}$	$V_L/0.4V$

It can also be noted that the larger V_{DIFF} is, i.e. the farther V_L is from the no-load voltage, the more power that the converter can deliver. This again is due to increased E_{BAT}. Thus, if a given gain setting is unable to meet the load power requirement even at the highest switching frequency, the next higher gain setting is used. This is the reason that even at moderate load power levels of $100\mu W$, the G2BY3 gain setting delivers a load voltage of 590mV and not the G1BY2 gain setting from a 1.2V battery. This leads to a drop in efficiency than that could have otherwise been achieved had the load power requirement been low.

3.4 Techniques to Increase Efficiency

A variety of techniques were employed to increase the efficiency of the switched capacitor DC-DC converter. These are classified here based on the key source of loss they target.

3.4.1 Reducing Conduction Loss

To minimize conduction loss, different gain settings (Figure 3-1) are switched in, to reduce the difference between the no-load voltage (V_{NL}) of a gain setting and V_L. Assuming that a

load voltage less than 600mV is being supplied by the G2BY3 gain setting, conduction loss imposes a limit on the maximum efficiency that can be achieved to $\eta_{max} = V_L \: / \: 0.8$. By switching to the G1BY2 gain setting, this efficiency limit can be improved to $\eta_{max} = V_L \: /$ 0.6.

3.4.2   Reducing Loss due to Bottom-plate Parasitic Capacitors

The energy lost per cycle in steady-state due to C_{BP} of the top capacitor in the G1BY2 gain setting is

$$E_{BP} = 1.5\alpha C_B V_{BAT}^2 \qquad (3.4)$$

while the energy extracted from the battery per cycle is given by

$$E_{BAT} = 6C_B V_{BAT} V_{DIFF} \qquad (3.5)$$

Let the ratio of E_{BP} to E_{BAT} be given by the following equation:

$$\frac{E_{BP}}{E_{BAT}} = K_P \frac{V_{BAT}}{V_{DIFF}} = 0.25\alpha \frac{V_{BAT}}{V_{DIFF}} \qquad (3.6)$$

For normal switching, the factor K_P is 0.25α. The factor 0.25 in K_P is a gain setting-dependent parameter (Table 3.2) while α is a technology-dependent parameter which depends on process parameters and the type of capacitor being used.

Divide-by-3 Switching

A divide-by-3 switching scheme was used to address the problem of bottom-plate parasitic capacitors. In the G1BY2 gain setting shown in Figure 3-7, both the top and bottom charge-transfer capacitors contribute to energy delivery to the load. However, only the top charge-transfer capacitor contributes to bottom-plate loss. So, in order to reduce the percentage losses due to bottom-plate parasitics, the top charge-transfer capacitor in the G1BY2 gain setting is not allowed to get involved in energy transfer to the load every
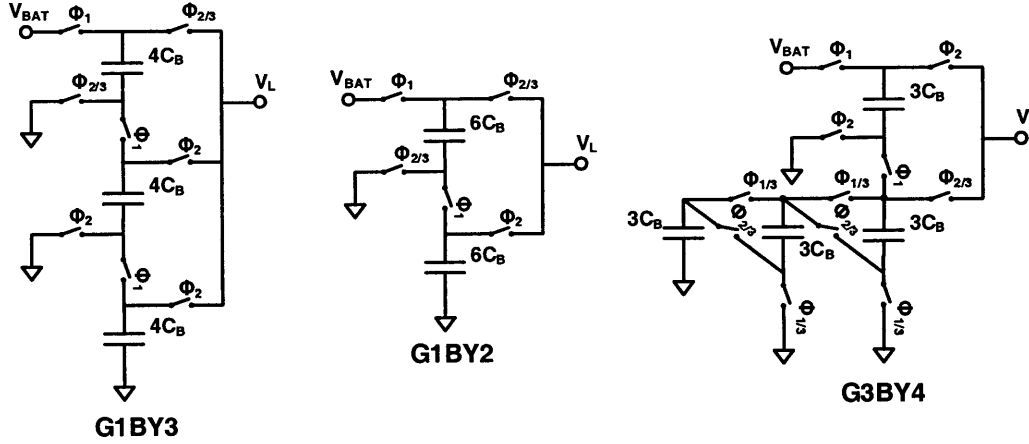
Figure 3-7: Divide-by-3 switching applied to three different gain settings.

cycle. Instead, it is only connected to the load once every few cycles. This way an overall improvement in efficiency is achieved. In the divide-by-3 switching scheme, for every gain setting, the capacitance that leads to significant bottom-plate parasitic loss is identified and it is switched to the load only once every 3 clock cycles. This way, the fraction of the energy lost due to bottom-plate parasitics is decreased. For the G1BY2 gain setting as shown in Figure 3-7, the top capacitor $6C_B$ is switched on to the load only once every 3 cycles. The energy extracted from the battery over 3 cycles is

$$E_{B,3} = 6C_B \times 1.75 V_{BAT} V_{DIFF} = 10.5 C_B V_{BAT} V_{DIFF} \tag{3.7}$$

while the energy lost due to C_{BP} remains the same as given by Equation 3.4. Thus, there is a 1.75X improvement in K_P when divide-by-3 switching is employed. For the G1BY3 gain setting, the top capacitor contributes the most to bottom-plate loss and is switched only once in 3 charge transfer cycles. Since no marked improvement was observed in the G2BY3 gain setting, the divide-by-3 switching scheme was not employed. For the G3BY4 gain setting, the bottom capacitors are switched once in every 3 cycles. This is different from the other gain settings because in G3BY4 gain setting, the top capacitor contributes $3/4^{th}$ to the energy transfer per cycle but the bottom capacitors contribute more to the parasitic

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loss. Thus by switching the bottom capacitors once in 3 cycles, a significant fraction of the energy can still be transferred per cycle while reducing the bottom-plate parasitic loss. While divide-by-3 switching improves efficiency by reducing the contribution of bottom-plate losses, it requires a higher switching frequency for a given load power level due to decreased energy transfer per cycle. While this increases gate switching losses in gain settings G1BY3 and G1BY2, the divide-by-3 switching scheme decreases switching losses in G3BY4 because of the reduction in the number of switches being switched every cycle (see Table 3.3). The improvements obtained in K_P can be seen from Table 3.2.

Table 3.2: Improvement in K_P by Divide-by-3 Switching

Gain Setting	K_P	$K_{P,div-by-3}$
G1BY1	0	n/a
G3BY4	0.375α	0.216α
G2BY3	0.222α	n/a
G1BY2	0.25α	0.141α
G1BY3	0.555α	0.368α

Section 3.6.2 shows a different method of attacking bottom-plate parasitics which makes use of an inductor. The expected improvement in efficiency due to using divide-by-3 switching is shown in Figure 3-8 when an $\alpha=0.05$ is considered. The improvement in efficiency is large when V_{DIFF} is small because this is the region where the bottom-plate parasitics significantly affect the efficiency. As V_{DIFF} increases, the effect of bottom-plate losses go down and hence, the improvement in efficiency due to divide-by-3 switching is also minimal.

3.4.3 Reducing Gate-drive Loss

The energy expended in switching the gate capacitances of the charge- transfer switches every cycle can be given by

$$E_{SW} = nC_{ox}WLV_{BAT}^2 \tag{3.8}$$
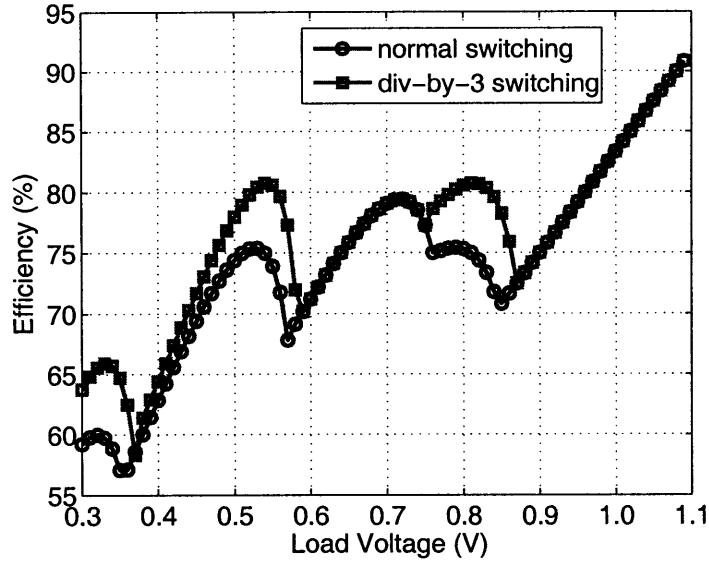
Figure 3-8: Expected improvement in efficiency due to divide-by-3 switching.

where n is the number of switches used and it is dependent on the gain setting, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the charge-transfer switches. The width of each switch is however proportional to the total charge-transfer capacitance and the frequency of switching. E_{SW} can then be expressed as

$$E_{SW} = n\beta C_B f_s V_{BAT}^2 \qquad (3.9)$$

where the constant β depends on C_{ox}, L, the mobility μ and the threshold voltage of the devices. The ratio of E_{SW} to E_B can be expressed by Equation 3.10. Here again n is a gain setting dependent parameter while β is technology dependent.

$$\frac{E_{SW}}{E_B} = K_s f_s \frac{V_{BAT}}{V_{DIFF}} = n\beta f_s \frac{V_{BAT}}{V_{DIFF}} \qquad (3.10)$$

To minimize the gate-switching loss, depending on the location of the charge-transfer switch and the gain setting in use, either only a PMOS or an NMOS switch is used instead of a transmission gate comprising both PMOS and NMOS devices. The automatic frequency scaling technique described in Section 3.2.1 scales the width of the charge-transfer switches

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as the switching frequency changes. This way, if the load power decreases by half, the AFS block halves both the switching frequency and the width of the charge-transfer switches, thereby effectively halving the ratio of E_{SW} to E_{BAT}.

3.4.4 Reducing Power Loss in the Control Circuitry

The power lost in the control circuitry is of specific concern while delivering ultra-low load power levels. The energy lost in the control circuitry every switching cycle can be broken into a switching and a leakage component and is given by

$$E_{CONT} = K_c V_{BAT}^2 + I_{leak} V_{BAT} T_{SW} \tag{3.11}$$

where I_{leak} is the total leakage current consumed by the control circuitry and T_{SW} is the average time-period of a switching cycle. The control circuitry employed does not consume any static power other than the subthreshold leakage currents in the digital circuitry. This is a critical feature in this application. Further, the AFS block scales the switching loss in the control circuitry with load power by suitably adjusting the switching frequency.

The overall efficiency taking into account all the above mentioned losses can be expressed as the ratio between the total energy delivered to the load per cycle to the sum of the energy extracted from the battery and the energy losses/cycle.

$$
\begin{aligned}
\eta &= \frac{E_L}{E_{BAT} + E_{BP} + E_{SW} + E_{CONT}} \\
&= \left(1 - \frac{V_{DIFF}}{V_{NL}}\right)\left(\frac{1}{1 + K_p \frac{V_{BAT}}{V_{DIFF}} + K_s f_s \frac{V_{BAT}}{V_{DIFF}} + K_c \frac{V_{BAT}}{C_B V_{DIFF}} + \frac{I_{leak} T_{SW}}{C_B V_{DIFF}}}\right) \tag{3.12}
\end{aligned}
$$

On dividing the numerator and denominator by E_{BAT}, the overall efficiency can be expressed in a more compact form where the pre-factor is due to the linear efficiency loss due to conduction. The 2nd term in the denominator is due to the bottom plate parasitic loss. The next term is due to gate-drive switching loss, and the 4th and 5th terms are due to

switching and leakage loss in the control circuitry. We see that while the linear conduction loss increases as V_{DIFF} increases, the other losses decrease with V_{DIFF}. Thus, for any given gain setting there is an optimum V_{DIFF} where the efficiency is maximized. The contribution of the switching losses in the control circuitry and the gate-drive can be minimized by increasing C_B. The leakage loss however is independent of C_B for a given load power because as C_B increases, the switching period T_{SW} also increases. In ultra-low load power levels, this leakage power component can be significant as the last term in the efficiency equation is just a ratio of the leakage power to load power.
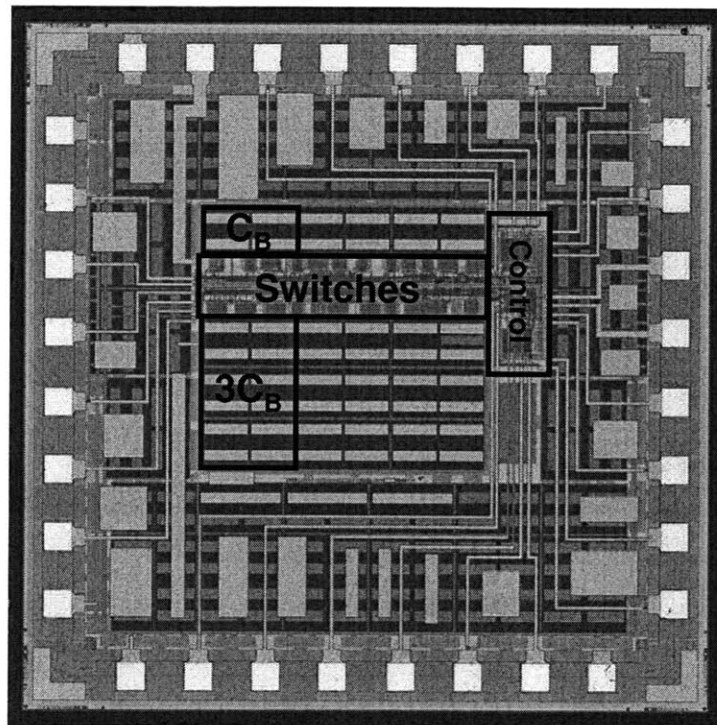
Figure 3-9: Die photo of the switched capacitor DC-DC Converter.

3.5 Measurement Results

A switched capacitor DC-DC converter test-chip, incorporating all the features explained in the sections above, was fabricated in National Semiconductor's 0.18μm CMOS process.

Figure 3-9 shows a die-photo of the implemented chip. The chip occupies a die area of 1.6 x 1.6mm^2 with the active circuitry consuming just 0.57mm^2, bulk of which was occupied by the charge-transfer capacitors. Gate-oxide capacitors were used for charge-transfer because of their high density and low bottom-plate parasitics. A total of 2.4nF of charge-transfer capacitance was used. The maximum clock frequency (CLK_4X in Figure 3-6) employed was 15MHz. The DC-DC converter was able to deliver load voltages from 300mV to 1.1V.

The efficiency of the SC converter with change in load voltage while delivering 100μW to the load from a 1.2V supply is shown in Figure 3-10(a). The converter was able to achieve >70% efficiency over a wide range of load voltages. The increase in efficiency of close of 5% due to the divide-by-3 switching scheme can be seen at voltages catered to by the gain settings G3BY4, G1BY2 and G1BY3. The measured efficiency plot closely matches the simulated efficiency values as obtained by using Equation 3.12 with an α=0.05. The topology switch into the G3BY4, G2BY3, G1BY2 and G1BY3 gain settings was made at 850mV, 750mV, 570mV and 350mV respectively, when divide-by-3 switching was employed. When normal switching was employed, the switch into G3BY4 was made at 825mV. The switching between gain settings does not occur at the no-load voltages of the individual gain settings. This is because at very low V_{DIFF}'s the efficiency is low due to the bottom-plate and switching losses. The optimum load voltage where efficiency is maximized for each gain setting can also be seen from the peaks in Figure 3-10b. The reason for this was explained in the previous section. The efficiency of the SC converter with change in load power is shown in Figure 3-10(b). The G1BY1 gain setting was used to deliver 1V and G1BY2 gain setting was used to deliver 0.5V. At 0.5V, the DC-DC converter was able to achieve close to 74% efficiency over a wide range of load powers. The effect of switching losses in bringing down the efficiency can be seen at load power levels above 150μW.

Table 3.3 shows a breakdown of the power lost in the different loss mechanisms while delivering 100μW at 0.8V through the G3BY4 gain setting. A quantitative estimate of the reduction in bottom-plate losses due to divide-by-3 switching can be seen.

Figure 3-11 shows a measured plot of the transient in load voltage when the reference
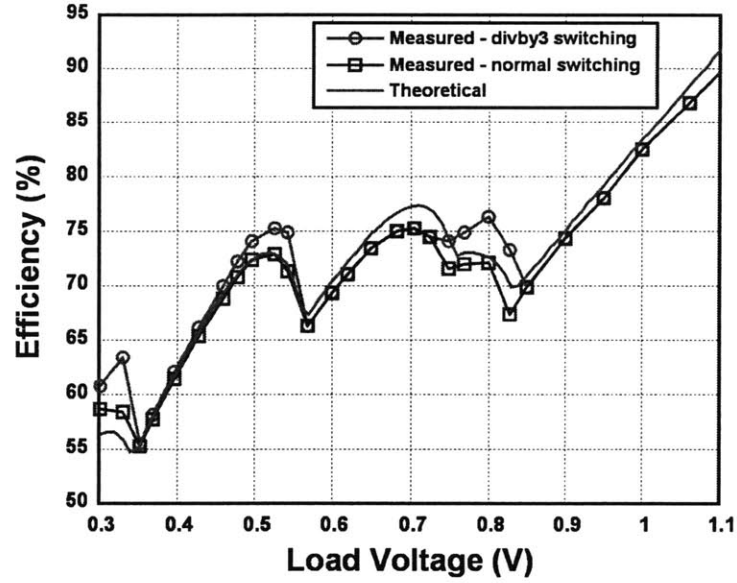
(a)
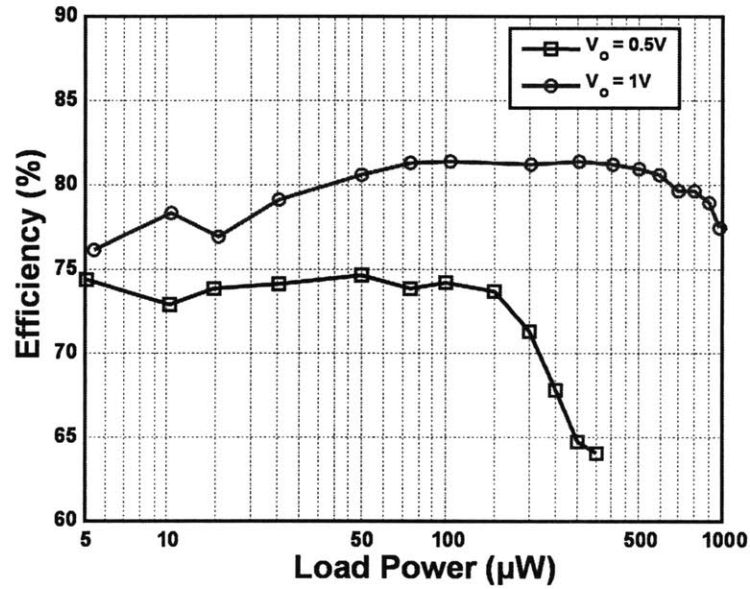
(b)

Figure 3-10: (a) Efficiency plot with change in load voltage (b) Efficiency plot with change in load power

voltage is raised from 0.3V (G1BY3) to 1V (G1BY1). The SC DC-DC converter takes close to $6\mu s$ to raise the output voltage to 1V when $100\mu A$ is being delivered to the load. The waveforms corresponding to the EN_W4 and $INCR$ signals show the operation of the automatic frequency scaling block explained in Section 3.2.1. The EN_W4 signal remains

Table 3.3: Breakdown of the different loss mechanisms while delivering 100μW at 0.8V ($\eta_{normal} = 0.717$, $\eta_{divby3} = 0.763$)

Loss Mechanism	Power Loss	
	Normal	Div-by-3
Conduction	12.45μW	12.45μW
Bottom-plate	14.68μW	7.47μW
Gate-drive	8.32μW	6.38μW
Control	4μW	4.69μW

Tek   Stopped Single Seq   1 Acqs   20 Apr 07 09:58:45

V_L

EN_W4

INCR

Ch1 500mV   Ch2 500mV   M 4.0µs 1.25GS/s   IT 80.0ps/pt
Ch3 1.0V   A Ch2 ƒ 600mV
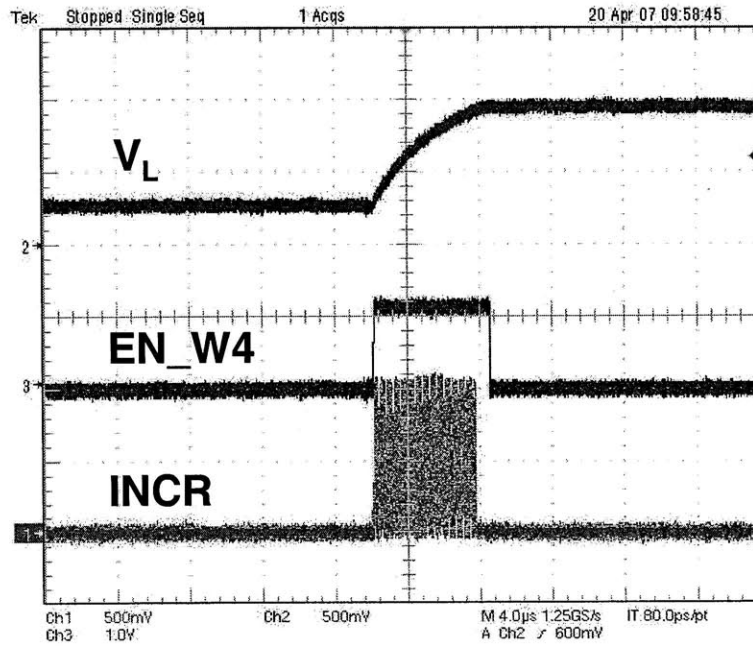
Figure 3-11: Transient response of the switched capacitor DC-DC converter as the load voltage is changed.

high till the desired load voltage is reached, thereby enabling a fast transient response. Once, the converter settles close to 1V, the EN_W4 signal goes low to reduce the switching losses.

3.6 Switched Capacitor DC-DC Converter with Improved Gain Settings and Charge Recycling

The previous implementation demonstrated the feasibility of using switched capacitor DC-DC converters as on-chip power supplies offering high efficiencies. However, the converter could handle load currents of only up to 1mA. The ability to handle higher load currents is very valuable for switched capacitor DC-DC converters. This expands the application scope of the converter, enabling it to be the power delivery source for a variety of low to medium power circuits. This section deals with the design of a 65nm CMOS 10mA switched capacitor DC-DC converter that improves upon the concepts developed in the previous implementation. This implementation introduces newer gain setting architectures that enable higher load current handling ability together with reduced bottom-plate losses. Also, issues related to bottom-plate parasitics are dealt with differently in this design using charge recycling approaches.
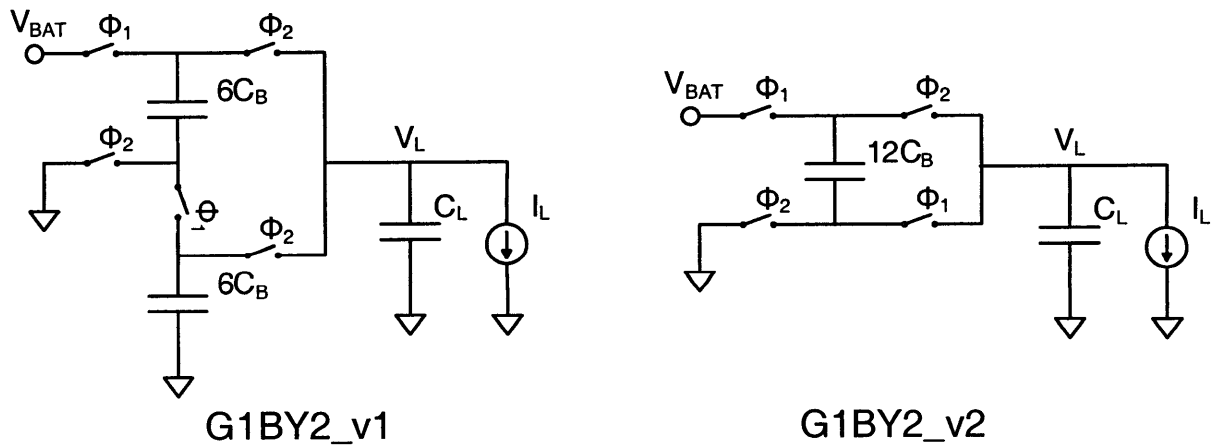
Figure 3-12: The G1BY2 gain setting implementation of version 1 and 2 of the switched capacitor DC-DC converter.

3.6.1 Improved Gain Settings

One of the limitations of the switched capacitor DC-DC converter described in Section 3.1 is the low amount of output currents it can handle. The current handling capability is limited by the arrangement of the capacitors within the gain settings. The gain settings described in Section 3.1 were of the indirect kind in that there was no direct transfer of charge from the battery to the load during any of the phases. The charge transfer was isolated by charging the charge-transfer capacitors from the battery during phase ϕ_1 and letting those intermediate capacitors charge the output load capacitor during phase ϕ_2.

Consider the G1BY2 gain setting of version 1 of the switched capacitor DC-DC converter in Figure 3-12. The charge-transfer capacitors are equal in value and get charged from the battery during ϕ_1. The charge these capacitors gained in phase ϕ_1 is delivered to the load in phase ϕ_2. Two capacitors of equal value are required to get a 1BY2 gain setting. The circuit on the right of Figure 3-12 shows the newer implementation of the 1BY2 gain setting. Here, the load capacitor itself is used as part of the charge transfer process during ϕ_1. This has two main advantages. Firstly, it helps in transferring charge to the output capacitor during both phases of the clock. Next, the two separate charge-transfer capacitors needed in the first implementation can be clubbed into one bigger capacitor thereby extracting more charge from the battery every cycle.

These advantages can be expressed quantitatively as follows. From Equation 3.3, it was shown that the G1BY2 gain setting of the first implementation could handle a maximum current of $12C_B V_{DIFF} f_s$ while supplying a load voltage of $V_L = V_{BAT}/2 - V_{DIFF}$ and switching at a frequency f_s. For the G1BY2 setting in version 2, during phase ϕ_2, the $12C_B$ charge-transfer capacitor discharges down to V_L. During ϕ_1 when the charge-transfer capacitor is connected in series with the load capacitor, the charge-transfer capacitor gets charged to $V_{BAT}/2 + V_{DIFF}$. The energy extracted from the battery during this process is given by

$$E_{BAT} = 24C_B V_{BAT} V_{DIFF} \tag{3.13}$$

The charge obtained from the battery in ϕ_1 also flows into the load capacitor. During

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ϕ_2, this excess charge which went into the charge-transfer capacitor is transferred to the load capacitor. Thus the load capacitor gets twice the charge extracted from the battery. However, this charge is delivered at a voltage V_L and hence, the energy delivered to the load every cycle is a linear scaled version of the energy extracted from the battery and is given by

$$E_L = E_{BAT}\frac{V_{NL} - V_{DIFF}}{V_{NL}} = 48C_B V_L V_{DIFF} \qquad (3.14)$$

The maximum current that can be delivered to the load by this gain setting when switching at a frequency f_s is then given by

$$I_L = 48C_B V_{DIFF} f_s \qquad (3.15)$$

This is 4 times the current handling capability of the G1BY2 gain setting in the first version. Thus, a significant improvement in current handling capability can be obtained by efficient ordering of the charge-transfer and load capacitors. The added benefit of the new arrangement is the reduced effect of bottom-plate losses. This can be intuitively understood by seeing that the new G1BY2 setting delivers 4 times as much charge per cycle as the old version but only increases the bottom-plate losses by 2 times every cycle. Thus on the whole the effect of the bottom-plate losses decrease by 2 times. This can be obtained quantitatively as follows:

The energy lost per cycle in steady-state due to the bottom-plate capacitance C_{BP} of the charge-transfer capacitor in the G1BY2 gain setting is

$$E_{BP} = 3\alpha C_B V_{BAT}^2 \qquad (3.16)$$

while the energy extracted from the battery per cycle is given by Equation 3.13. Thus the term K_P defined in Section 3.4.2 for the new G1BY2 setting is 0.125α. This is half of the value obtained by the old G1BY2 setting, which confirms the reduction in the effect of bottom-plate losses by a factor of 2. The basic difference in this design is to utilize
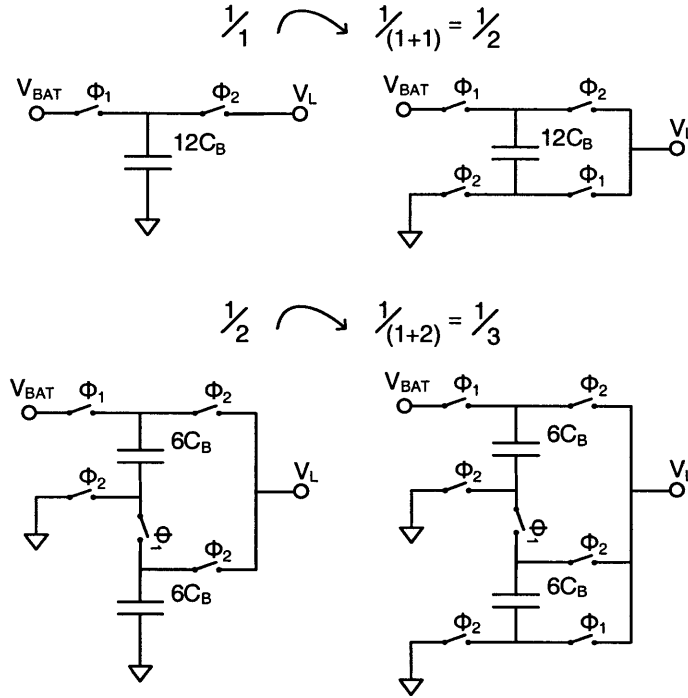
Figure 3-13: Examples to show how new gain settings are obtained by rearranging switches of the gain settings in the first implementation.

the load capacitor in the charge-transfer process. This reduces the stack of charge-transfer capacitors needed to achieve a particular gain setting and also helps in delivering more charge per cycle to the load capacitor. If a particular gain setting in the previous version gave out a voltage ratio of p/q, then by connecting the ground terminal of the bottom-most charge-transfer capacitor during phase ϕ_1 to the load terminal, a gain setting with a voltage ratio of $p/(p+q)$ can be obtained. This is illustrated with examples in Figure 3-13. The circuit at the top shows how the G1BY1 setting is transformed into the G1BY2 setting in the new implementation by connecting the bottom-plate of the $12C_B$ capacitor to the load during ϕ_1. Similarly, by connecting the bottom-plate of the lower $6C_B$ capacitor to the load during ϕ_1, the old G1BY2 setting can be transformed to the new G1BY3 setting. The various gain settings employed in this design are shown in Figure 3-14. The G1BY1 gain setting is the same as the old version. The G3BY4 gain setting is obtained by doing a p/q to $p/(p+q)$ transformation on an older G3BY1 gain setting. The G2BY3 gain setting

is obtained by doing a transformation on an older G2BY1 gain setting. Two new gain settings are introduced in this version. The G3BY5 and G2BY5 gain settings are obtained by doing the transformation on older G3BY2 and G2BY3 gain settings respectively. These gain settings were not used in the older version because the capacitive stack would have been too large to achieve them. This would have significantly increased the bottom-plate losses while lowering the current handling capability. The G2BY5 gain setting gives a 0.48V output at no-load and the G3BY5 gain setting provides 0.72V at no-load. All the gain settings are 2-way interleaved in this implementation to reduce the input current and output voltage ripple.
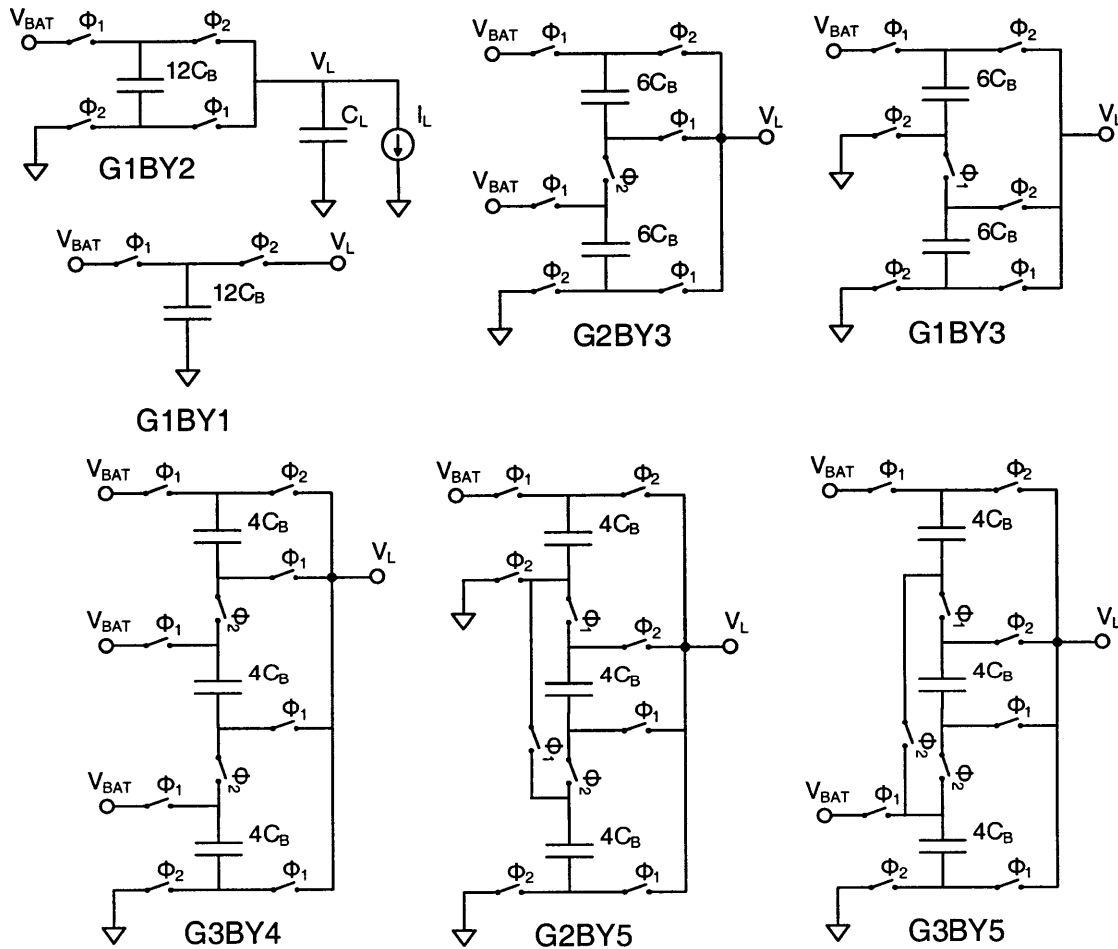
Figure 3-14: Gain settings used in the second implementation to generate efficiently a wide range of load voltages from a 1.2V supply.

Table 3.4: Energy extracted from battery every cycle for the 2 versions of gain-settings

Gain Setting	E_{BAT} (ver. 1)	E_{BAT} (ver. 2)	Improvement
G1BY1	$12C_B V_{BAT} V_{DIFF}$	$12C_B V_{BAT} V_{DIFF}$	same
G3BY4	$3C_B V_{BAT} V_{DIFF}$	$16C_B V_{BAT} V_{DIFF}$	5.33X
G2BY3	$4C_B V_{BAT} V_{DIFF}$	$18C_B V_{BAT} V_{DIFF}$	4.5X
G3BY5	n/a	$10C_B V_{BAT} V_{DIFF}$	n/a
G1BY2	$6C_B V_{BAT} V_{DIFF}$	$24C_B V_{BAT} V_{DIFF}$	4X
G2BY5	n/a	$6.66C_B V_{BAT} V_{DIFF}$	n/a
G1BY3	$4C_B V_{BAT} V_{DIFF}$	$9C_B V_{BAT} V_{DIFF}$	2.25X

The improvement in energy extracted from the battery and thereby the output load current handling capability of the newer gain settings is shown in Table 3.4. It can be seen that greater than 4X the current handling capability can be attained with the newer version for most of the gain settings. On top of this, the newer gain settings offer improvement in the bottom-plate parasitic loss for some of the gain settings as shown in Table 3.5.

Table 3.5: Improvement in bottom-plate parasitic loss

Gain Setting	K_P (ver. 1)	K_P (ver. 2)	Improvement
G1BY1	0	0	same
G3BY4	0.375α	0.281α	1.33X
G2BY3	0.222α	0.222α	same
G3BY5	n/a	0.32α	n/a
G1BY2	0.25α	0.125α	2X
G2BY5	n/a	0.36α	n/a
G1BY3	0.555α	0.37α	1.5X

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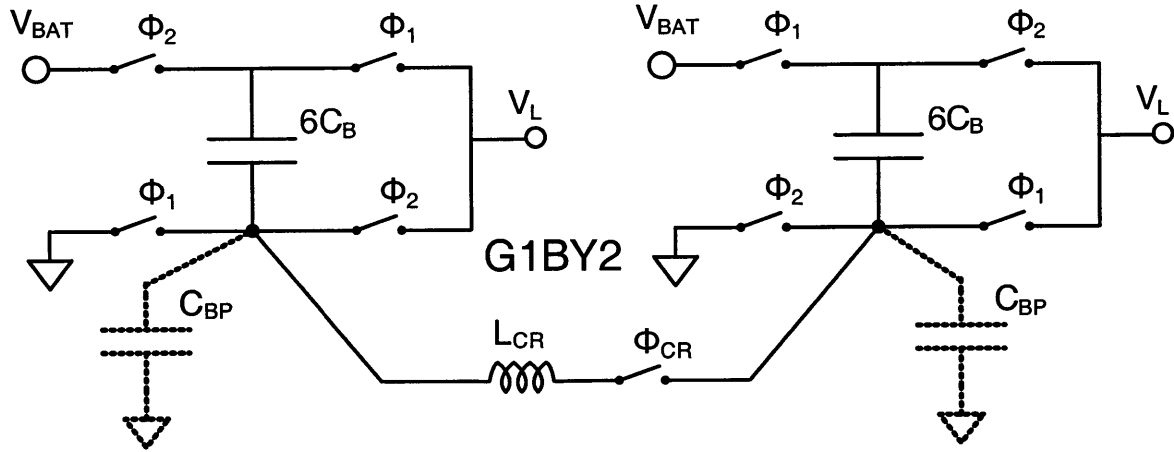
Figure 3-15: Charge Recycling used to recover the energy stored in the bottom-plate parasitic capacitor.

3.6.2 Charge Recycling

The problem of efficiency loss due to bottom-plate parasitics was described in Section 2.3.2. The first implementation of the switched capacitor DC-DC converter in 0.18μm CMOS used divide-by-3 switching (Section 3.4.2) to reduce the effect of bottom-plate parasitics on efficiency. While this technique could provide an improvement in efficiency, it leads to a reduction in the current handling capability. A different approach is used in this implementation to tackle the problem due to bottom-plate parasitics. The bottom-plate loss arose because the charge stored in it was dumped to ground when the clock phase transitioned. In this implementation, the energy stored in some of the bottom-plate parasitic capacitors is recycled to the equivalent capacitor in another interleaved bank before it is lost to ground. Figure 3-15 shows the implementation of the charge recycling circuit. The G1BY2 setting is shown in the figure. The figure shows two interleaved banks of the gain setting each working out of phase. During the ϕ_1 phase, the bottom-plate parasitic capacitor C_{BP} of the right bank gets charged to the load voltage. Normally, this energy is lost when the circuit transitions to the ϕ_2 phase. In the period between when ϕ_1 turns OFF and phase ϕ_2 turns ON, the charge recycling (CR) switch is turned ON using the pulse ϕ_{CR}. This helps in transferring the charge across C_{BP} of one bank to the bottom-plate parasitic of the

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other interleaved bank with the help of an on-chip bondwire inductor L_{CR}. The amount of energy transferred depends on the resistance along the recycling path. Assuming that the voltage across the bottom-plate capacitor is V_L for one bank, the voltage obtained at the bottom-plate capacitor of the other bank after charge recycling can be given by
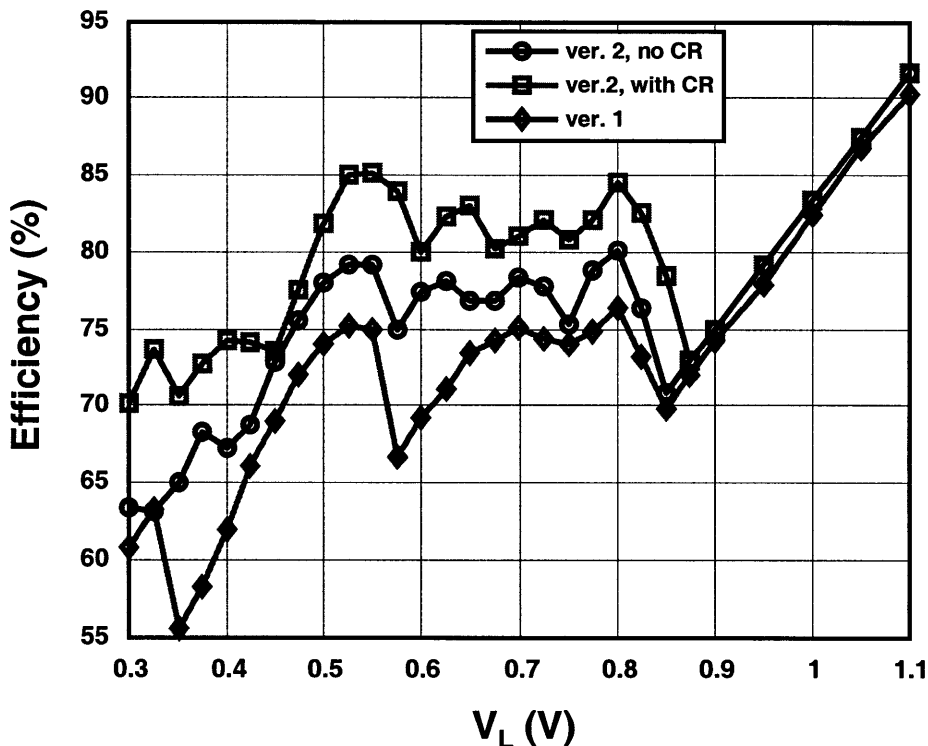
Figure 3-16: Comparison of the simulated efficiency curves of the second version of the switched capacitor DC-DC converter with the measured efficiency of the first version.

$$V(afterCR) = \frac{V_L}{2} + \frac{V_L}{2}e^{\frac{-\pi\beta}{\omega}} \qquad (3.17)$$

where $\beta = R/2L_{CR}$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/\sqrt{L_{CR}C_{BP}/2}$. Here, R is the resistance along the recycling path. This has to be minimized for effective recycling. The derivation of the above equation is provided in Appendix A. The charge-recycling switch needs to be turned ON for just enough time to achieve zero-current switching of the inductor current. Once charge recycling has taken place, only the remaining charge has to be provided to the bottom-plate capacitor to bring it up to V_L. This reduces the efficiency loss due to bottom-

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plate parasitics. A similar approach is taken in the other gain settings, where the capacitor which leads to the most bottom-plate loss is identified and is charge shared using the same inductor with the corresponding capacitor of the interleaved bank. Figure 3-16 shows the improvement in efficiency obtained by using charge recycling with the help of an on-chip bondwire inductor of size 1nH. The simulated efficiency obtained is much better than the measured efficiency obtained by the first implementation with divide-by-3 switching. While the inductor based charge recycling approach holds much promise, the quality factor of the bondwire inductors obtained on-chip for this implementation was not as high as expected. Hence, the improvement attained did not match up with simulated values. In the presence of low quality inductors, the final voltage obtained after charge recycling on the bottom-plate capacitor is effectively $V_L/2$ as can be seen from Equation 3.17. This can be obtained with the help of just the charge recycling switch without the inductor. In the case where just the switch is used, the improvement in K_P obtained is shown in Table 3.6.

Table 3.6: Improvement in bottom-plate parasitic loss with charge recycling

Gain Setting	K_P (ver. 2, no CR)	K_P (ver. 2, with CR)	Improvement
G1BY1	0	0	same
G3BY4	0.281α	0.211α	1.33X
G2BY3	0.222α	0.148α	1.5X
G3BY5	0.32α	0.32α	1.33X
G1BY2	0.125α	0.0625α	2X
G2BY5	0.36α	0.252α	1.43X
G1BY3	0.37α	0.222α	1.67X

3.7 Measurement Results

The second version of the switched capacitor DC-DC converter was implemented in Texas Instruments' 65nm CMOS process. Figure 3-17 shows a die photo of the implemented chip.
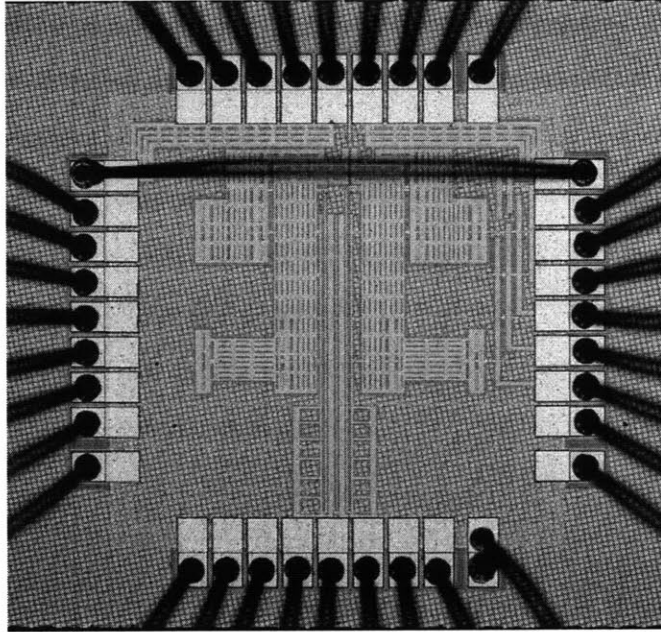
Figure 3-17: Die photo of the second version of the switched capacitor DC-DC Converter.

The chip occupies a die area of 1mm x 1mm with the active circuitry consuming just 0.52mm^2, bulk of which was occupied by the charge-transfer capacitors. Gate-oxide capacitors were used for charge-transfer because of their high density and low bottom-plate parasitics. A total of 3nF of charge-transfer capacitance was used. The die photo of the chip also shows the bondwire inductor connected between the pads on the die.

The efficiency of the SC converter with change in load voltage while delivering 500μA to the load from a 1.2V supply is shown in Figure 3-18. The converter was able to achieve >75% efficiency over a wide range of load voltages. The increase in efficiency due to the charge recycling scheme can be seen. The switch-only charge recycling scheme was used for measurements due to the poor quality inductors obtained on-chip. The measured efficiency plot closely matches the simulated efficiency values as obtained by using Equation 3.12 with α=0.05. The addition of 2 new gain settings helps prevent the efficiency from going below 75% at around 0.6V and below 65% at around 0.4V. The efficiency of the SC converter with change in load current while delivering 0.5V to the output using a G1BY2 gain setting is shown in Figure 3-19. The DC-DC converter was able to achieve greater than 75% efficiency

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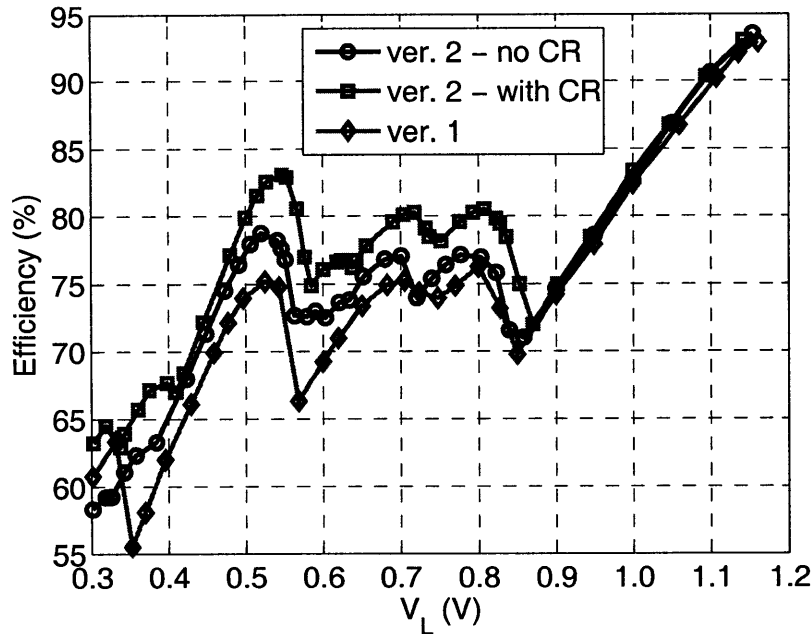
Figure 3-18: Efficiency plot with change in load voltage with I_L=500μA. The efficiency plot for version 1 switched capacitor converter was obtained with I_L=100μA.

over a wide range of load currents. The newer gain setting architecture enables this converter to support a load current of up to 8mA while keeping the overall area occupied the same. This is a significant improvement over the previous version. The fundamental efficiency limit due to conduction losses at this load voltage is 83.3%. The bottom-plate parasitic losses reduce the efficiency achieved by 3% over the load current range. The efficiency at the higher load current regions is further brought down by switching losses while below 10μA, the control losses bring down the efficiency.

The second implementation of the switched capacitor DC-DC converter was able to provide more than 4X the current handling capability of the previous version for the same area occupied. This was achieved by modifying the gain settings architecture. A new approach was taken to tackle bottom-plate parasitics in this implementation. The approach involved the use of an on-chip inductor to effectively recycle the bottom-plate charge. While this method is beneficial when high quality inductors are available on-chip, in the absence of
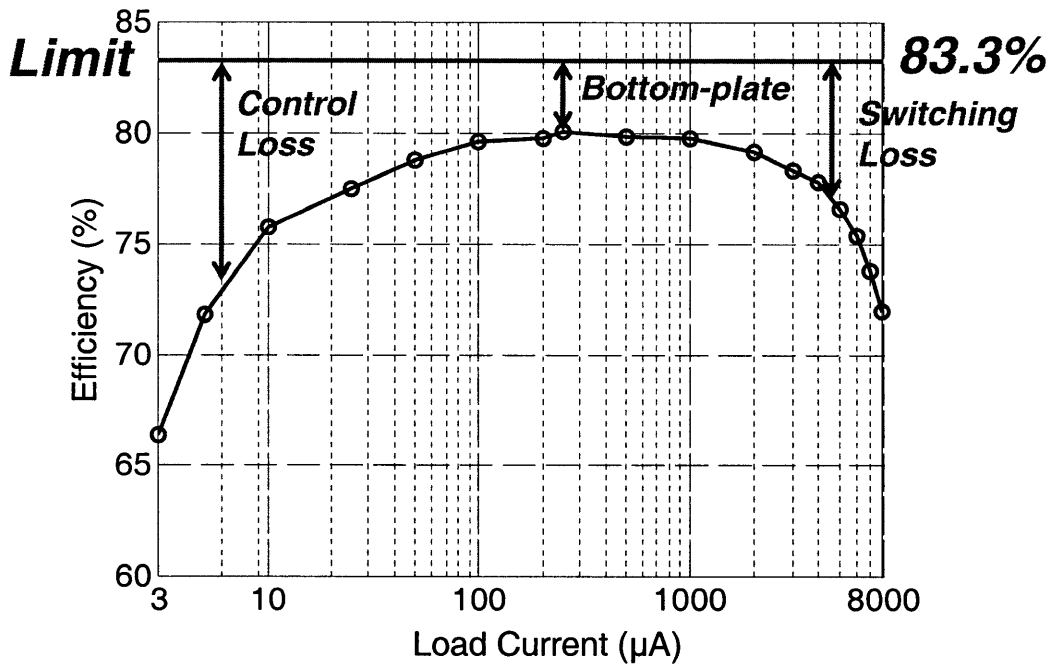
Figure 3-19: Efficiency plot with change in load current at $V_L = 0.5$V.

it, a switch-only scheme can provide moderate recycling benefits as can be seen from the improvement in efficiency in Figure 3-18. Also, in the second version, the addition of newer gain settings helped in keeping the efficiency nearly constant over the wide load voltage range of 0.3V to 1.15V.
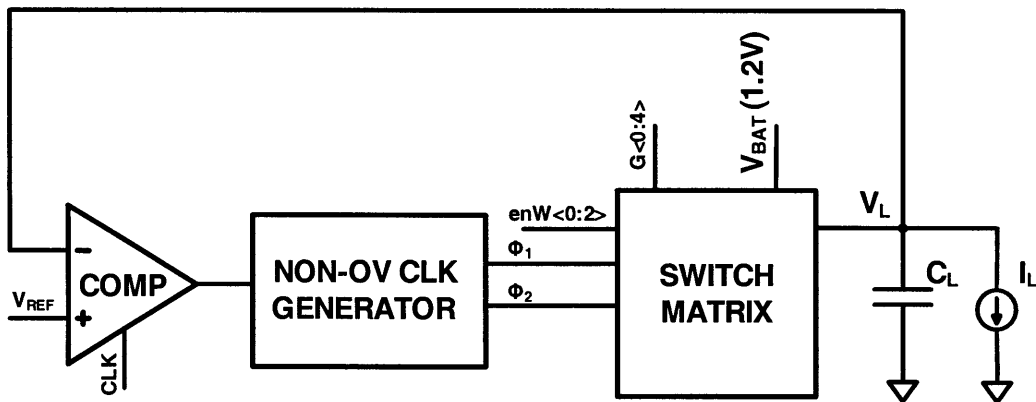
Figure 3-20: Architecture of the embedded ultra-low-power switched capacitor DC-DC converter.

3.8 Ultra-Low-Power Switched Capacitor DC-DC Converter for an MSP430 Microcontroller

The previous sections have described standalone switched capacitor DC-DC converters which could provide scalable load voltages at high efficiencies. This section describes the implementation of an embedded DC-DC converter which functions as the power delivery unit in a subthreshold MSP430 microcontroller system [14]. The microcontroller is designed to operate in the subthreshold region where substantial energy savings can be achieved by reducing the V_{DD} of digital and memory circuits. A DC-DC converter supplying ultra-low voltages at high efficiencies is essential to realize the full energy savings that can be achieved by reducing V_{DD} in a subthreshold system. Since, the power consumption of the logic and SRAM load circuits drop exponentially at subthreshold voltages, the DC-DC converter was designed to deliver a maximum of 500μW of load power. This reduced load power demand makes switched capacitor DC-DC conversion an ideal choice for this application. The switched-capacitor (SC) DC-DC converter is based on the design described in the previous section, and makes us of 600pF of total on-chip charge transfer (flying) capacitance to provide scalable load voltages from 0.3V to 1.1V. The logic and SRAM circuits however, utilize voltages only up to 0.6V.

Figure 3-20 shows the architecture of the DC-DC converter. The converter uses an all-digital Pulse Frequency Modulation (PFM) mode of control to regulate the output voltage. In this method of control, the converter stays idle till the load voltage V_L falls below the reference voltage (V_{REF}), at which point a clocked comparator enables the switch matrix to transfer one charge packet to the load. A PFM mode control is crucial to achieving high efficiency for the extremely low power system being built. The switch matrix block contains the charge transfer switches and the charge transfer capacitors.

One of the main efficiency limiting mechanisms in a switched capacitor DC-DC converter is the linear conduction loss [43]. To maintain efficiency over the wide load voltage range of 0.3V to 1.1V, this converter employs five different gain settings (G<0:4>). Figure 3-21
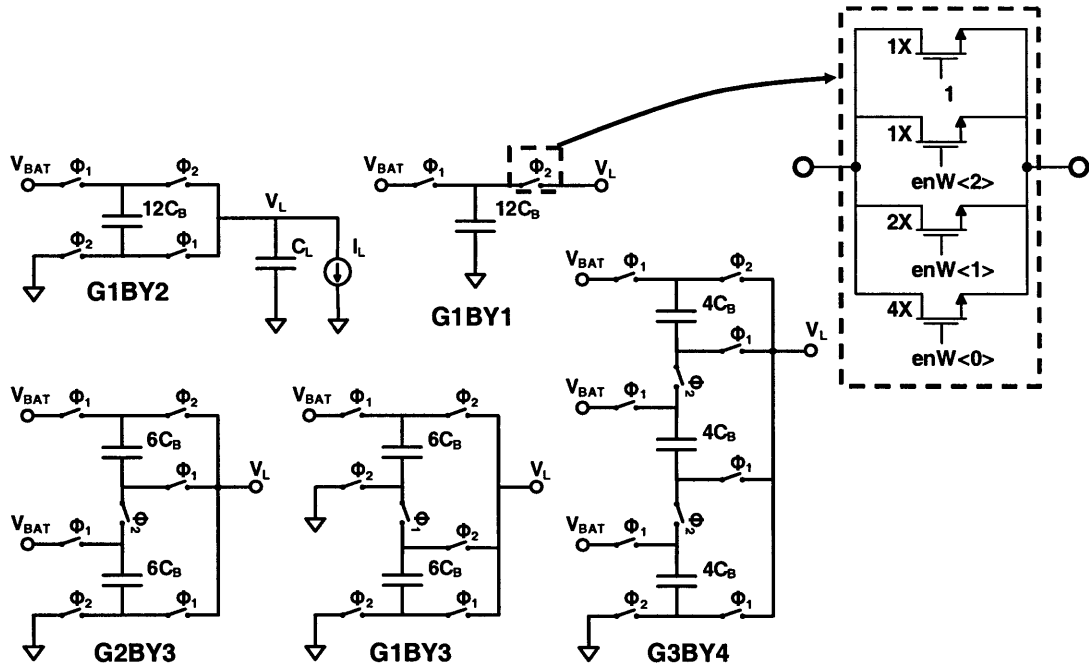
Figure 3-21: The different gain settings used within the switch matrix. A simplified representation of the switch size control is shown in the inset.

shows how the different gain settings are achieved from a total charge transfer capacitance of $12C_B$ (600pF). The external voltage input to the system is 1.2V. Each gain setting at no-load provides a voltage ratioed output of the input voltage. A suitable gain setting (G<0:4>) is chosen depending on the proximity of its no-load voltage to the load voltage being delivered and its ability to provide the load power demand [43]. Since, the logic and SRAM load circuits utilize voltages only up to 0.6V, in the actual testing of the chip, only gain modes G2BY3, G1BY2 and G1BY3 were used.

The switching losses in the converter are dominated by the energy expended in turning the charge transfer switches ON and OFF. The switch widths are designed such that the charge transfer capacitors just settle at the end of a charge transfer cycle. In order to scale switching losses with load power, the charge transfer switches have adjustable widths which are enabled by the signal enW<0:2> as shown in the inset in Figure 3-21. Any decrease (increase) in the load power by a factor of 2, halves (doubles) the clock frequency (CLK) of the comparator and correspondingly the width of the charge transfer switches is also
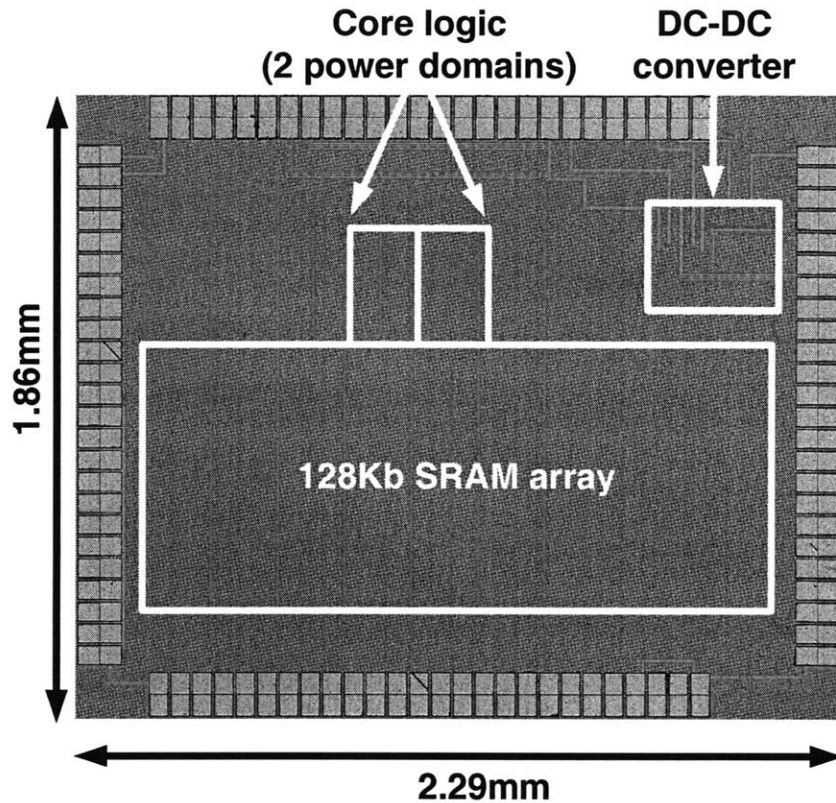
Figure 3-22: Die Photo of the MSP430 microcontroller chip showing the embedded switched capacitor DC-DC converter.

halved (doubled). This helps to decrease the switching power by 4X when the load power decreases by 2X leading to an increase in efficiency at lower load power levels. [43] describes a method to automatically determine the signal enW<0:2> as the load power varies. The gain in efficiency as the load power decreases close to 320μW and 160μW in Figure 3-23 is due to the scalable switch width design. However, at very low load power levels (sub-5μW), leakage and other fixed losses in the control circuitry bring down the efficiency of the switched capacitor DC-DC converter.

The MSP430 microcontroller system together with the embedded DC-DC converter was implemented in a 65nm CMOS process. The DC-DC converter, including charge transfer capacitors, occupies just 0.12mm^2. It is a small fraction of the overall area occupied by the chip as shown in Figure 3-22. The minimum energy point of the microcontroller occurs at
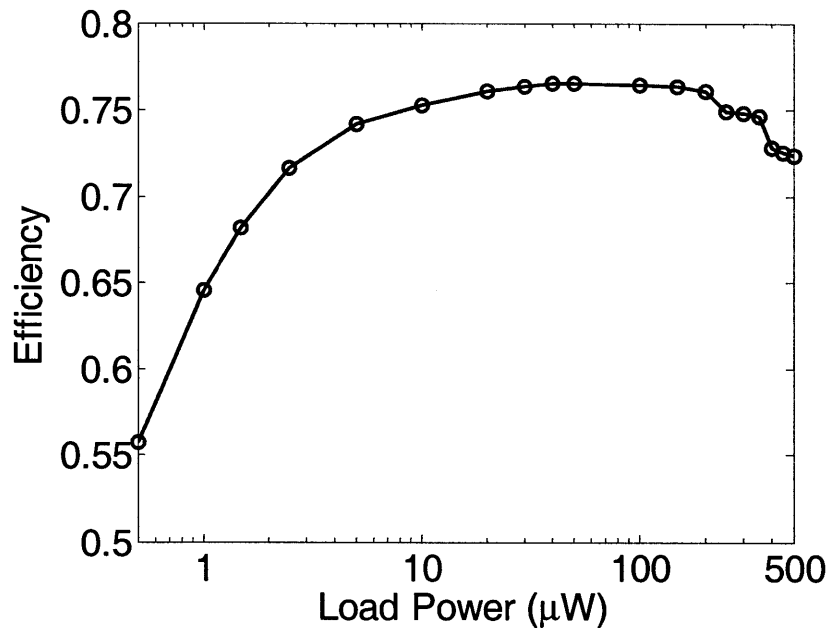
Figure 3-23: Efficiency of the embedded ultra-low-power switched capacitor DC-DC converter while delivering 500mV output voltage.

500mV, and functionality was verified down to 300 mV. The inclusion of a DC-DC converter enables the system to dynamically scale to 300mV during standby mode, where memory and logic together consume less than 1μW. The efficiency of the DC-DC converter delivering a load voltage of 500 mV is shown in Figure 3-23. The converter achieves more than 75% efficiency with an order of magnitude change in load power, between 10μW to 250μW. With the microcontroller as a load, the converter provides 75% efficiency at 12μW. When measured standalone, the converter reaches a peak efficiency of 78%.

3.9   Summary and Conclusions

This chapter has presented the implementation of three different switched capacitor DC-DC converter designs. Each of the designs employ on-chip charge-transfer capacitors that can deliver scalable load voltages from 300mV to 1.1V. To maintain efficiency over this wide range of load voltages, multiple gain settings were introduced in the designs. These

help in minimizing the conduction losses within the SC DC-DC converter. In the first implementation of the SC DC-DC converter, the gain settings employed were of the indirect type in which the load capacitor got charged during one phase of the clock cycle. The second and third implementations employed modified gain settings where the load capacitor was used within the charge transfer process. This helped these implementations to handle more load current for the same area occupied. The presence of on-chip capacitors made it possible to split the charge-transfer capacitance into small fragments to obtain the different gain settings. This will be a difficult thing to achieve with off-chip capacitors owing to the increases in the total number of capacitors required off-chip. Different strategies were discussed in the chapter to tackle bottom-plate parasitic losses. This loss mechanism was identified as a significant problem when using on-chip capacitors. The first implementation used a divide-by-3 switching scheme to minimize the bottom-plate losses. This mechanism requires very little overhead area and power and hence can be implemented easily. However, it reduces the current handling capability. To preserve the current delivery, the second implementation made use of charge recycling to mitigate bottom-plate losses. Two flavors of this solution were presented. The one which uses an inductor can recover most of the bottom-plate losses. However, this requires a high quality on-chip inductor which may not be feasible in certain designs. In the absence of an inductor, a switch-only charge recycling scheme was shown to reduce the bottom-plate losses by a factor of 2. This scheme only requires a small CMOS switch and hence is a low overhead solution. All the converters discussed employed completely digital control with no static power losses to achieve voltage regulation. This not only helped to minimize switching losses but also kept the control power loss to a minimum thereby helping the converters to achieve high efficiencies at microwatt power levels. The third implementation demonstrated the feasibility of embedding switched capacitor DC-DC converters inside bigger digital systems to deliver power to the unit. The converter by itself only occupies a small fraction of the total area while improving the efficiency of the whole system. This type of approach is more efficient than using on-chip linear regulators to power the digital unit.

Chapter 4

Piezoelectric Energy Harvesting Interface Circuit

With the need for portable and lightweight electronic devices on the rise, highly efficient power generation approaches are a necessity. The dependence on the battery as the only power source is putting an enormous burden in applications where either due to size, weight or lifetime constraints, doing away with the battery is the only choice. Emerging applications like wireless micro-sensor networks [16], implantable medical electronics and tire-pressure sensor systems [17] are examples of such a class. It is often impractical to operate these systems on a fixed energy source like a battery owing to the difficulty in replacing the battery. The ability to harvest ambient energy through energy scavenging technologies is necessary for battery-less operation. A 1cm^3 primary lithium battery has a typical energy storage capacity of 2800J [2]. This can potentially supply an average electrical load of 100μW for close to a year but is insufficient for systems where battery replacement is not an easy option. The most common harvesters transduce solar, vibrational or thermal energy into electrical energy. The vibrational harvesters use one of three methods: electromagnetic (inductive), electrostatic (capacitive) or piezoelectric. The thermoelectric harvesters exploit temperature gradients to generate power. Most harvesters in practically usable forms can provide an output power of 10 - 100μW (see Table 1.2), setting a constraint on the average

power that can be consumed by the load circuitry for self-powered operation. It is also possible to extract energy from electromagnetic radiation emitted by RF sources. This generates tens of μWs of usable power and has been used in RFID tags [20] and several implanted medical devices. However, this method is not energy scavenging in the true sense because the RF power has to be provided by an external source.

For the applications mentioned above, the presence of ambient vibrations makes it possible to scavenge mechanical energy. Harvesting ambient vibration energy through piezoelectric (PE) means is a popular energy harvesting technique which can potentially supply 10 - 100's of μW of available power [2]. This low power output necessitates not only the design of ultra-low power logic circuits but also efficient power delivery interface circuits that can extract the maximum power available out of the energy harvesters. One of the limitations of existing PE harvesters is in their interface circuitry. Commonly used full-bridge rectifiers and voltage doublers [44] severely limit the electrical power extractable from a PE harvesting element. Further, the power consumed in the control circuits of these harvesters reduces the amount of usable electrical power. In this chapter, a bias-flip rectifier that can improve upon the power extraction capability of existing full-bridge rectifiers by greater than 4X is presented. An efficient control circuit with embedded DC-DC converters that can share their filter inductor with the bias-flip rectifier thereby reducing the volume and component count of the overall solution is demonstrated.

4.1 Equivalent Circuit of a Piezoelectric Harvester

Using piezoelectric elements is a popular way to harvest ambient mechanical energy. An input vibration applied on to a piezoelectric material as shown in Figure 4-1 causes mechanical strain to develop in the device which is converted to electrical charge. Conversely, applying an electric voltage to this material produces a mechanical strain. Because of these bi-directional effects, piezoelectric materials are widely used for making sensors and actuators. For micro-power applications, the piezoelectric laminate is mechanically forced to vibrate and thus, it works as a generator to transform the mechanical energy into electrical energy. The
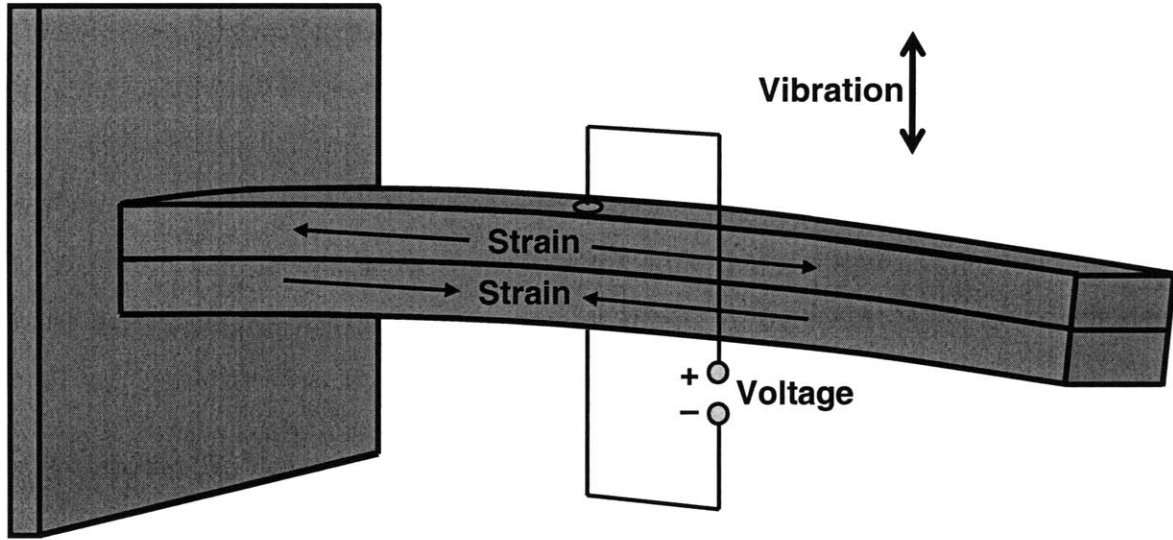
Figure 4-1: Input vibration applied to a piezoelectric device in the shape of a cantilever beam

piezoelectric material used for this power generation circuit is lead-zirconate-titanate (PZT). The equivalent circuit of the unimodal piezoelectric harvester [2] [45] can be represented as a mechanical spring mass system coupled to an electrical domain as shown in Figure 4-2. Here, L_M represents the mechanical mass, C_M the mechanical stiffness and R_M takes into account the mechanical losses. The mechanical domain is coupled to the electrical domain through a transformer that converts strain to current. On the electrical side, C_P represents the plate capacitance of the piezoelectric material. At or close to resonance, we can transform the whole circuit to the electrical domain, where the piezoelectric element when excited by sinusoidal vibrations can be modeled as a sinusoidal current source in parallel with a capacitance C_P and resistance R_P. The model presented here represents most piezoelectric vibration energy harvesters that are based on cantilever designs which require their resonant frequency to match the environmental vibration frequency. One of the main disadvantages of this type of harvester is that the energy conversion efficiency of the harvester drops dramatically if the resonant frequency is mismatched. Multi-mode piezoelectric energy harvesters [46] are being researched upon which can extend the operating frequency range of these vibration harvesters. The equivalent circuit model presented above only deals with

unimodal piezoelectric energy harvesters. One of the challenges in a power generator of this type is the design and construction of an efficient power conversion circuit to harvest the energy from the PZT membrane. Unlike conventional power supplies and batteries, which typically have very low internal impedance, the piezoelectric generators internal impedance is relatively high. This high internal impedance restricts the amount of output current that can be driven by the PZT source to the micro-amp range. Another unique characteristic of this power source is the relatively low output voltage of the piezoelectric device. This low output voltage makes it challenging to develop rectifier circuits that are efficient since many half wave or full wave diode rectifiers require nonzero turn-on voltages to operate.
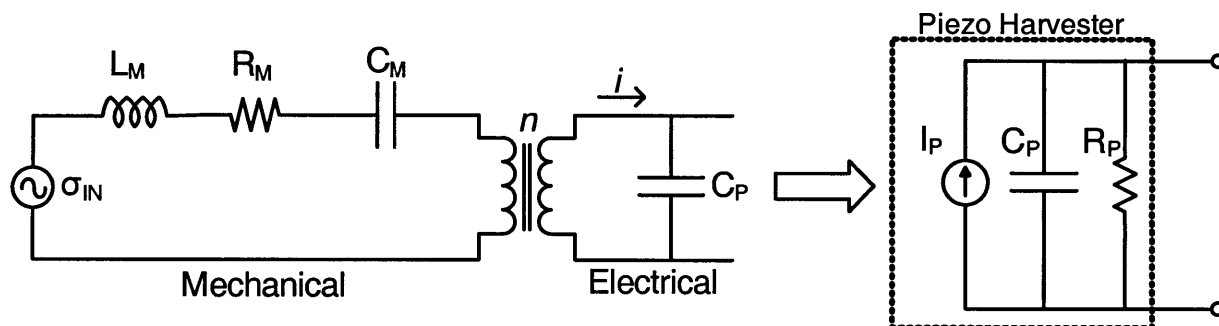
Figure 4-2: Equivalent circuit of a piezoelectric energy harvester showing the mechanical and electrical sides of the device [2].

4.2 Commonly used interface circuits to piezoelectric harvesters

A piezoelectric harvester is usually represented electrically as a current source in parallel with a capacitor and resistor [2] [44] [47]. The current source provides current proportional to the input vibration amplitude. For the sake of the following analysis, the input vibrations are assumed to be sinusoidal in nature and hence the current is represented as,

$$i_P = I_P \sin \omega_P t \tag{4.1}$$

where $\omega_P{=}2\pi f_P$ and f_P is the frequency with which the piezoelectric harvester is excited.
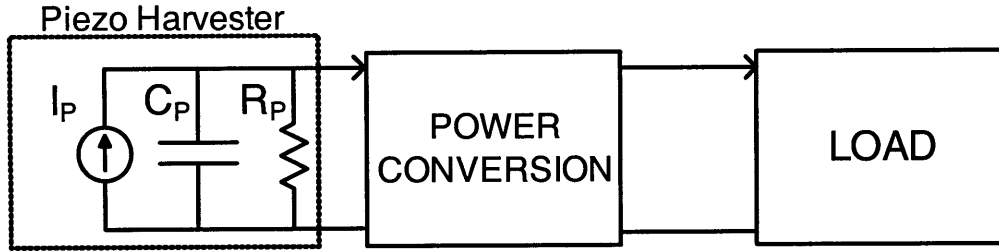
Piezo Harvester

Figure 4-3: Schematic of power generation using a piezoelectric energy harvester.

The power output by the piezoelectric harvester is not in a form which is directly usable by load circuits such as micro-controllers, radios etc. which the harvester powers. As shown in Figure 4-3, the voltage and current output by the harvester needs to be conditioned and converted to a form usable by the load circuits. The power conditioning and converting circuits should also be able to extract the maximum power available out of the piezoelectric energy harvester.

Considering Figure 4-3, maximum power can be extracted from the piezoelectric harvester if the power conversion and load circuits present a conjugate impedance match to the harvester. Given that the input impedance of the harvester is a parallel combination of R_P and $1/j\omega_P C_P$, the conjugate match should present an impedance as shown in Figure 4-4.
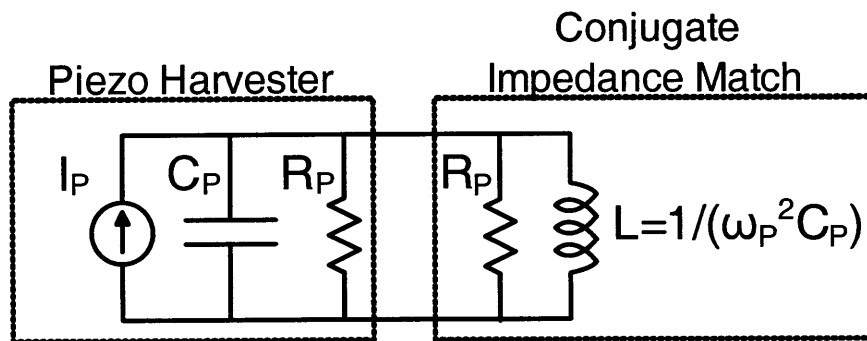
Figure 4-4: Presenting a conjugate impedance match for maximum power extraction.

If such a conjugate impedance match can be presented, the theoretical maximum power

that can be extracted from the piezoelectric harvester can be given by

$$P_{RECT,THE}(max) = \frac{I_p^2 R_p}{8} = \frac{Q_P^2 V_P^2}{8R_P} \tag{4.2}$$

where the term V_P is the open-circuit voltage amplitude at the output of the piezoelectric harvester. V_P can be represented as $V_P = I_P/\omega_P C_P$. $Q_P = \omega_P C_P R_P$ is the Q-factor of the piezoelectric harvester.

For a commercial piezoelectric harvester from Mide (V22W), the internal impedance of the device can be modeled as C_P=12nF and R_P=600kΩ. When this device is excited at close to its resonance frequency of 225Hz, the conjugate impedance match to extract maximum power must have a resistance of 600kΩ and an inductance of 41.69H. The amount of inductance needed to present a conjugate match is impractical. Also, most practical load circuits are not simple resistors. Commonly used analog and digital circuits require a regulated supply voltage to operate from. Since the piezoelectric harvester outputs a sinusoidal current, it first needs to be rectified before it can be used to power circuits. Some of the commonly used rectifier circuits are discussed below.
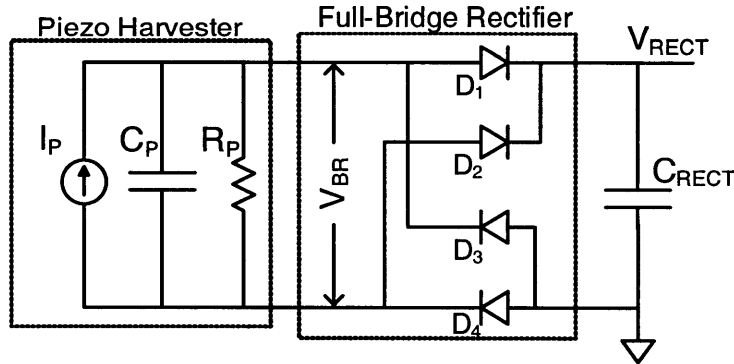
Figure 4-5: A full-bridge rectifier to extract power from a piezoelectric energy harvester.

4.2.1   Full-bridge Rectifier

A full-bridge rectifier [47] [48] [49] [50] is one of the most commonly used rectifier circuits to convert the AC output of a piezoelectric harvester into a DC voltage. A typical implementation of the full-bridge rectifier circuit is shown in Figure 4-5. At the output of the rectifier is the capacitor C_{RECT}. For the sake of this analysis, assume that the value of C_{RECT} is large compared to C_P and that the voltage at the output of the rectifier (V_{RECT}) is essentially constant. These assumptions would be justified in later sections. Further, ideal diodes are considered for the time being to determine the power output by the piezoelectric harvester connected to a full-bridge rectifier. The voltage and current waveforms associated with this circuit is shown in Figure 4-6. Every half-cycle of the input current waveform can be split into 2 regions. In the interval between $t = t_0$ and $t = t_{OFF}$, the piezoelectric current i_P flows into C_P to charge it. In this interval, all the diodes are reverse-biased and no current flows into the output capacitor C_{RECT}.
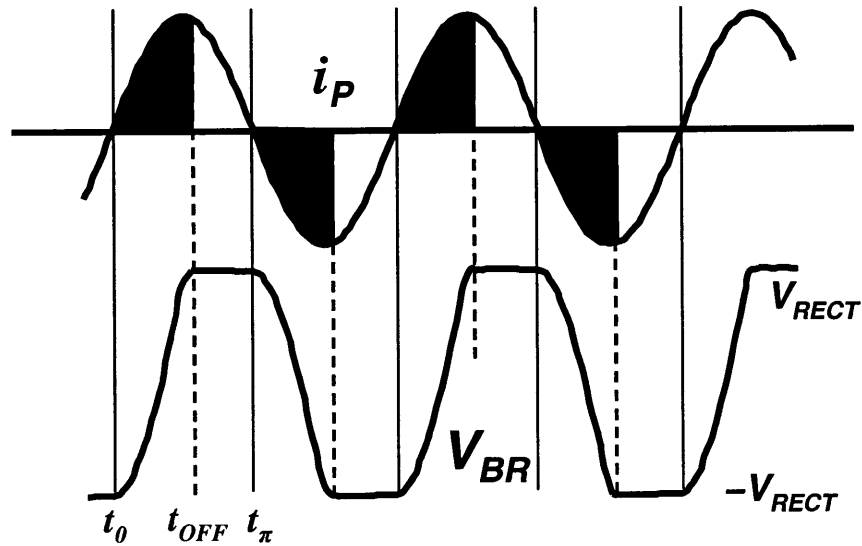
Figure 4-6: Simulated voltage and current waveforms for a full-bridge rectifier connected to a piezoelectric energy harvester.

This condition continues till the voltage across the capacitor C_P which is labeled as V_{BF} in Figure 4-5 is equal to the output voltage V_{RECT}. When this happens, the diodes D_1 and

D_4 turn ON and the piezoelectric current starts flowing into the output. This interval lasts till the current i_P changes direction. In the first part of the negative half-cycle again, all the diodes are OFF and the current from the harvester flows into C_P to discharge it. The other set of diodes D_2 and D_3 turn ON only after the voltage across C_P is brought down to $-V_{RECT}$. The shaded portion of the current waveform shows the amount of charge not delivered to the output every half-cycle. The total amount of charge available from the piezoelectric harvester every cycle is given by

$$Q_{av/cy} = \int_0^{2\pi/\omega_P} i_P \, dt = \frac{4I_p}{\omega_P} = 4C_PV_P \tag{4.3}$$

where V_P is the open-circuit voltage amplitude output by the harvester. Out of this charge, the shaded portion of charge does not reach the output. Every cycle, the piezoelectric current has to charge C_P from $-V_{RECT}$ to $+V_{RECT}$ and vice-versa before the diodes turn-ON. This amount of charge lost every cycle can be given by

$$Q_{lost/cy} = 2 \times C_P \times (V_{RECT} - (-V_{RECT})) = 4C_PV_{RECT} \tag{4.4}$$

The charge that actually flows into the output capacitor C_{RECT} is just the difference between the total charge available and the charge lost. This can be given by

$$Q_{RECT/cy} = Q_{av/cy} - Q_{lost/cy} = 4C_PV_P - 4C_PV_{RECT} \tag{4.5}$$

Once we know the charge that flows into the output, the total energy delivered to C_{RECT} every cycle is just the product of charge times the output voltage and can be given by

$$E_{RECT/cy} = Q_{RECT/cy} \times V_{RECT} = 4C_PV_{RECT}(V_P - V_{RECT}) \tag{4.6}$$

The cycle repeats at a frequency of f_P. The power delivered to the output by the full-bridge rectifier is

$$P_{RECT,FB} = E_{RECT/cy} \times f_P = 4C_PV_{RECT}f_P(V_P - V_{RECT}) \tag{4.7}$$

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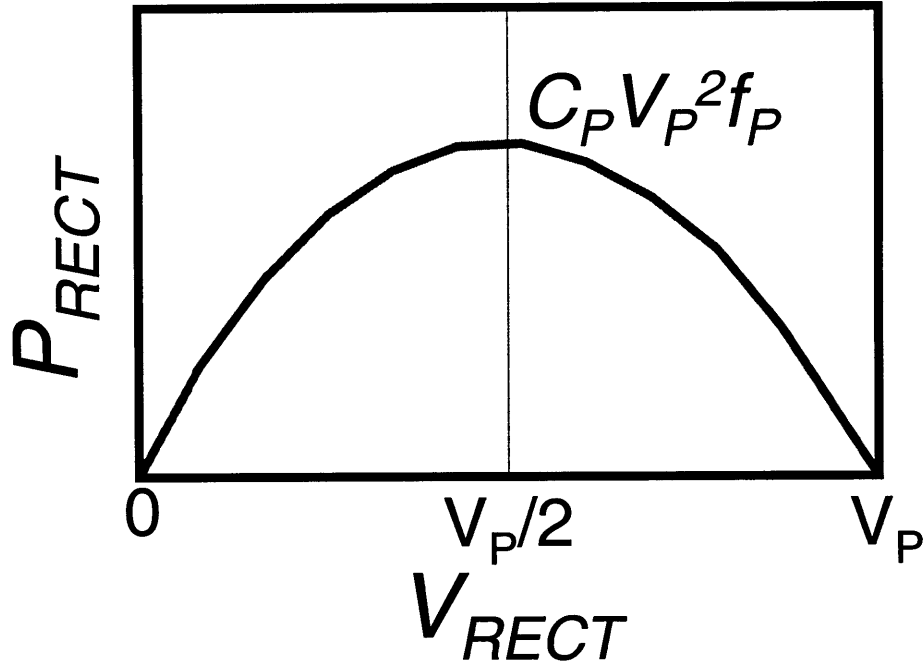
Figure 4-7: The output power obtained using a full-bridge rectifier as a function of V_{RECT}.

This shows that the output power obtained is a function of V_{RECT}. Figure 4-7 shows how the power obtained at the output of the full-bridge rectifier with ideal diodes varies with V_{RECT}. At low values of V_{RECT}, most of the charge available flows from the harvester into the output but the output voltage is low. At high values of V_{RECT}, very little charge flows into the output. These opposing trends causes the full-bridge rectifiers output power to vary with V_{RECT} and reach a maximum at

$$V_{RECT} = \frac{V_P}{2} \tag{4.8}$$

The maximum power that can be obtained using the full-bridge rectifier is given by

$$P_{RECT,FB}(max) = C_P V_P^2 f_P \tag{4.9}$$

Compared to the maximum theoretical power available as shown in Equation 4.2, the ratio of the power obtained using a full-bridge rectifier is given by

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$$\frac{P_{RECT,FB}(max)}{P_{RECT,THE}(max)} = \frac{4}{\pi Q_P} \tag{4.10}$$

For an input vibration frequency of 225Hz, C_P=12nF and R_P=600kΩ, the full-bridge rectifier outputs only 12.5% of the actual maximum power available. This analysis has assumed ideal diodes. The output power extracted is smaller when non-ideal diodes are taken into account. The non-idealities of the diodes can be introduced by using a single parameter V_D which is the voltage drop across the diode when current from the piezoelectric harvester flows through it. Now, the piezoelectric current has to charge C_P upto $V_{RECT}+2V_D$ before it can turn the diodes ON. This can be easily incorporated into the output power equations by substituting V_{RECT} in Equation 4.4 by $V_{RECT}+2V_D$. Going through the same exercise as before, the output power obtained by the full-bridge rectifier in the presence of diode non-idealities can be given by

$$P_{RECT,FB} = 4C_P V_{RECT} f_P (V_P - V_{RECT} - 2V_D) \tag{4.11}$$

Using a single parameter (V_D) to take into account the diode non-idealities helps in keeping the mathematical expressions simple. It also gives good insight into the effect the non-ideal diode has in introducing losses into the system. A simple way to determine V_D is to average the voltage across the diode when current flows through it over a half-cycle of the input current. Figure 4-8 shows a comparison between the simulated power obtained at the output of the full-bridge rectifier and that obtained by using Equation 4.11. A value of 0.38V was used for V_D. The close match between the theoretical prediction and simulated results validates using a single parameter to describe diode non-idealities.

The diode used in the simulation was obtained using a PMOS transistor with its source as the P-end and the gate, drain and bulk connected together as the N-end of the diode. Considerable work [44] [51] [52] [53] has been done on using synchronous rectifiers that use MOS transistors to replace the diodes. These have much lower forward voltage loss compared to p-n junction diodes or transistor-based diodes.

The analysis till now has ignored the presence of the damping resistance R_P. Appendix
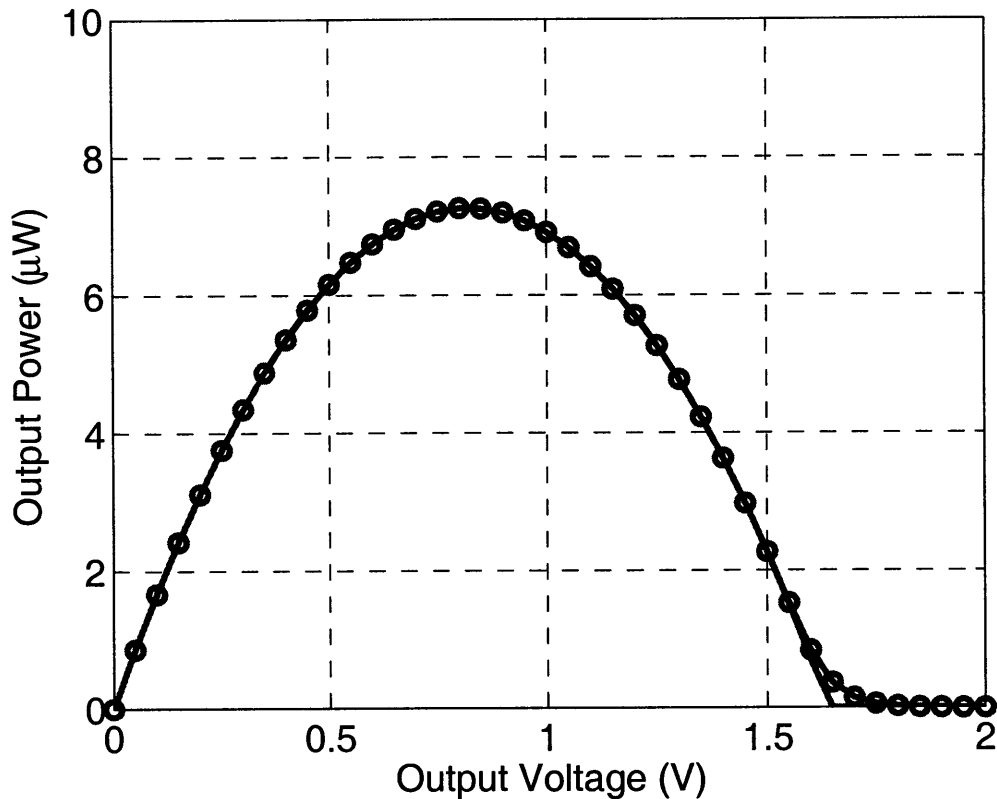
Figure 4-8: Theoretical and simulated power obtained at the output of the full-bridge rectifier with non-ideal diodes with change in V_{RECT}. Circular markers show simulated values.

B presents an analysis of the power obtained at the output of the full-bridge rectifier taking into account this resistance.

4.2.2 Voltage Doubler

Another commonly used rectifier design is that of a voltage doubler [44] [51] [52]. The voltage doubler makes use of only 2 diodes as shown in Figure 4-9. At the output of the rectifier is the capacitor C_{RECT}. Here again ideal diodes are assumed for the initial part of the analysis. The voltage and current waveforms associated with this circuit is shown in Figure 4-10. In the case of the voltage doubler, the current flow into the output does not occur every half-cycle. During the negative half-cycle of the input current, the diode in parallel with the
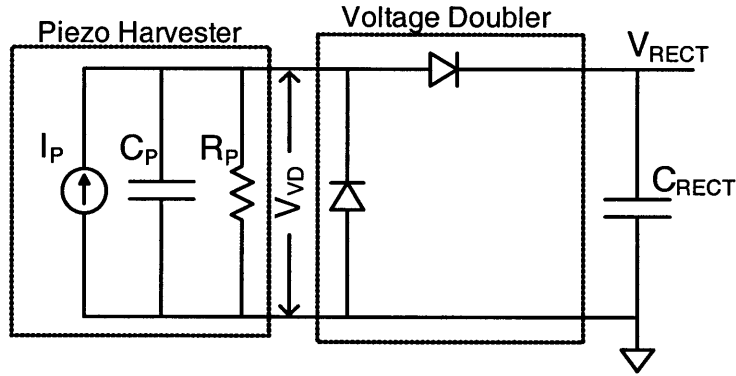
Figure 4-9: A voltage doubler circuit to extract power from a piezoelectric energy harvester.

harvester turns ON and it essentially keeps the voltage across the harvester (V_{VD}) at zero. There is no current flow into the output during this period. As the current becomes positive, i_P flows into the capacitor C_P first to charge it up to $+V_{RECT}$ before the series diode can turn ON for the current to flow to the output.
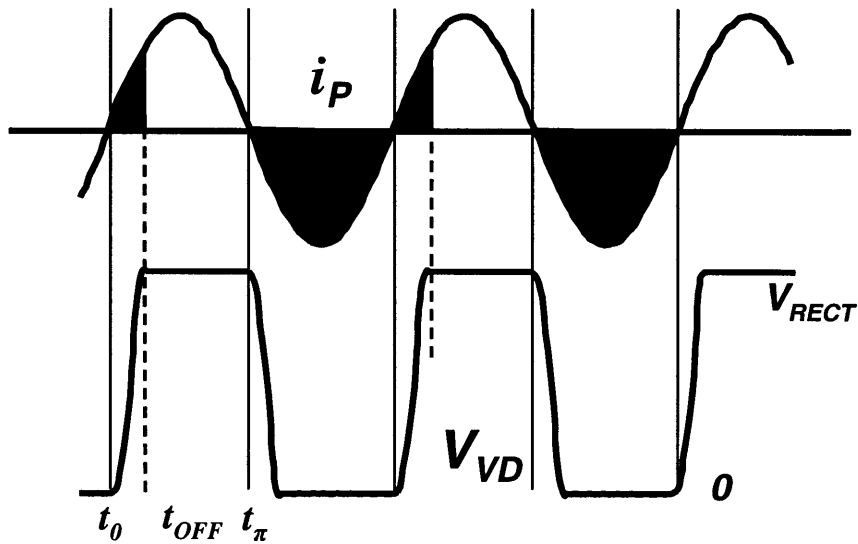
Figure 4-10: Simulated voltage and current waveforms for a voltage doubler connected to a piezoelectric energy harvester.

The amount of charge not flowing to the output every cycle can be given by

$$Q_{lost/cy} = 2C_PV_P + C_PV_{RECT} \qquad (4.12)$$

The charge that actually flows into the output capacitor C_{RECT} is just the difference between the total charge available given by Equation 4.3 and the charge lost. This can be given by

$$Q_{RECT/cy} = Q_{av/cy} - Q_{lost/cy} = 2C_PV_P - C_PV_{RECT} \qquad (4.13)$$

The power delivered to the output by the voltage doubler is the product of the charge delivered, V_{RECT} and f_P and can be given by

$$P_{RECT,VD} = C_PV_{RECT}f_P(2V_P - V_{RECT}) \qquad (4.14)$$

The power output by the voltage doubler is also a function of V_{RECT}. The output power expression looks similar to that obtained using a full-bridge rectifier (Equation 4.7). The power output by the voltage doubler however reaches a maximum at

$$V_{RECT} = \frac{I_P}{\omega_PC_P} = V_P \qquad (4.15)$$

which is twice the value of the maximum for a full-bridge rectifier. The maximum power that can be obtained however is the same as that obtained using a full-bridge rectifier and can be given by Equation 4.9. Hence, if ideal diodes are used there is no power improvement in using a voltage doubler. It however reduces the number of diodes by 2 and also shares a common ground with the piezoelectric harvester which can be of advantage in some applications. The voltage doubler can provide 2 times the maximum voltage. This is beneficial in increasing the output power when diode non-idealities are introduced. In the case of the voltage doubler, in the presence of non-ideal diodes, the piezoelectric current has to charge C_P from $-V_D$ to $V_{RECT}+V_D$ when the current goes positive. This increases the amount of charge lost every cycle by $2C_PV_D$ in Equation 4.12. This reduces the output power obtained to

$$P_{RECT,VD} = C_P V_{RECT} f_P (2V_P - V_{RECT} - 2V_D) \qquad (4.16)$$
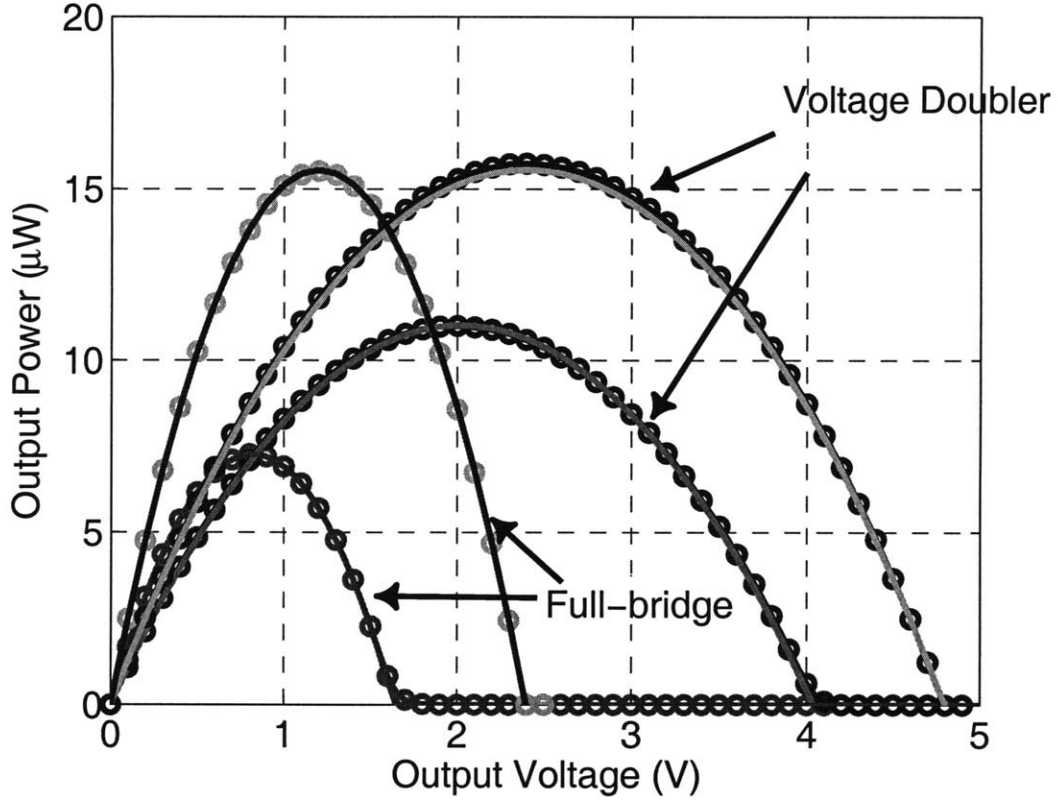
Figure 4-11: Theoretical and simulated power obtained at the output of the full-bridge rectifier and voltage doubler with and without ideal diodes as V_{RECT} is changed. Circular markers show simulated values.

Figure 4-11 shows a comparison between the simulated and theoretical power obtained at the output of the rectifier for both the full-bridge and voltage doubler cases. The plots show the power output with ideal and CMOS diodes. For the CMOS diode, a value of 0.38V was used for V_D when calculating the output power. It can be seen from the figure that the diode non-idealities affect the full-bridge rectifier more than the voltage doubler. Appendix B presents an analysis of the power obtained at the output of the voltage doubler taking into account the effect of resistance R_P.

4.3 Proposed rectifier schemes

The main limitation of the full-bridge rectifier and voltage doubler is that, most of the current available from the harvester does not go into the output at high voltages. The loss in charge due to charging and discharging of C_P limits the maximum power that can be extracted using these rectifier circuits. This section presents the design of advanced rectifier circuits that can improve the power extraction capabilities from piezoelectric harvesters thereby trying to reach the theoretical maximum power output possible.

4.3.1 Switch-only rectifier

Before we look into the switch-only rectifier, it is worthwhile to observe how the operation of the voltage doubler differs from that of the full-bridge rectifier. Both these circuits provide the same amount of maximum output power when ideal diodes are considered. However, the voltage doubler provides current to the output only during the positive half-cycle of i_P. During the negative half-cycle, its parallel diode helps in pre-discharging C_P to ground. This way during the positive half-cycle, i_P only needs to do half the work to charge up C_P to V_{RECT} before it can flow into the output. The question that can be raised is, do we need to spend an entire half-cycle just to discharge C_P to ground?
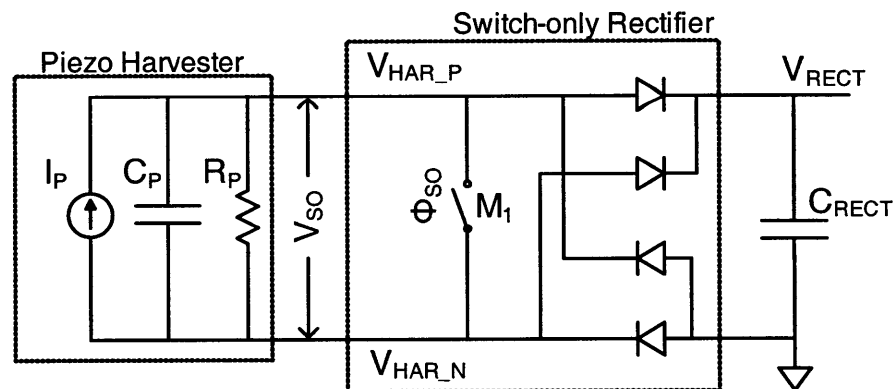
Figure 4-12: A switch-only rectifier circuit to extract power from a piezoelectric energy harvester.

This leads to the design of the switch-only rectifier where a simple switch M_1 is connected across the piezoelectric harvester driving a full-bridge rectifier as shown in Figure 4-12. For the moment, assume that the switch is turned ON for a brief time at every zero-crossing of the piezoelectric current i_P. When the switch is ON, it discharges the capacitor C_P immediately to ground. Once C_P has been discharged, M_1 is turned OFF. This frees up the rectifier to conduct during both the half-cycles of the input current. Assuming ideal diodes for the initial part of the analysis, the voltage and current waveforms associated with this circuit is shown in Figure 4-13. At every half-cycle, when i_P changes direction, the switch M_1 is turned ON briefly to discharge the voltage across C_P. Now, the piezoelectric current only has to charge up C_P from 0 to $\pm V_{RECT}$ before it can flow into the output. The switch-only rectifier combines the advantages of the full-bridge rectifier and the voltage doubler by conducting current in both the half-cycles while charging C_P up from only 0 to $\pm V_{RECT}$ every half-cycle. The amount of charge lost during a cycle in the switch-only rectifier can be given by

$$Q_{lost/cy} = 2C_P V_{RECT} \qquad (4.17)$$

The charge that actually flows into the output capacitor C_{RECT} is just the difference between the total charge available given by Equation 4.3 and the charge lost. This can be given by

$$Q_{RECT/cy} = Q_{av/cy} - Q_{lost/cy} = 4C_P V_P - 2C_P V_{RECT} \qquad (4.18)$$

The power delivered to the output by the switch-only rectifier is the product of the charge delivered, V_{RECT} and f_P and can be given by

$$P_{RECT,SO} = 2C_P V_{RECT} f_P (2V_P - V_{RECT}) \qquad (4.19)$$

When ideal diodes are considered, the power output by the switch-only rectifier is exactly twice that output by the voltage doubler. The power output by the switch-only rectifier
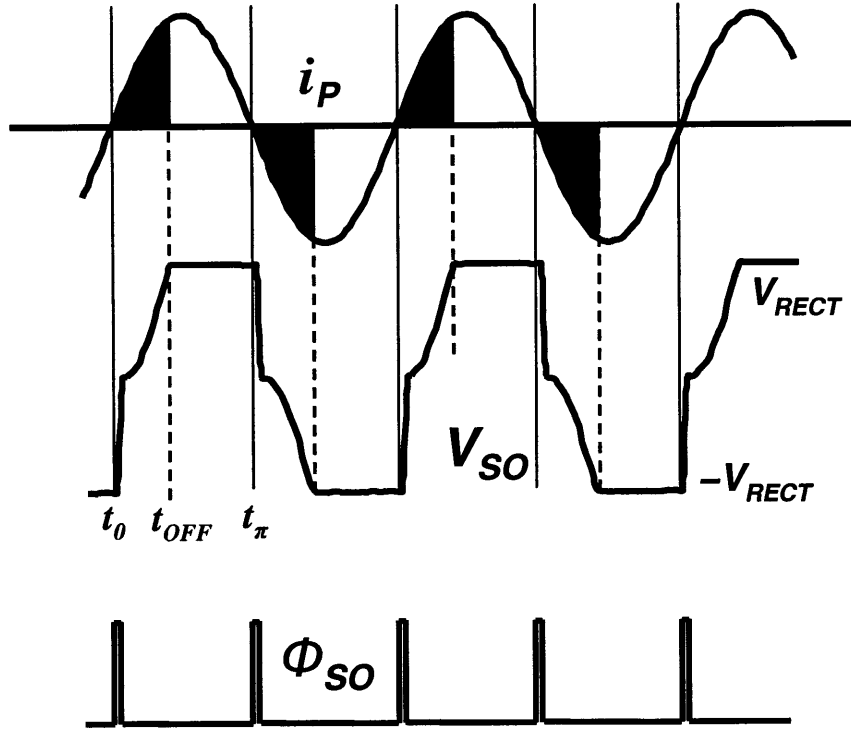
Figure 4-13: Simulated voltage and current waveforms for a switch-only rectifier connected to a piezoelectric energy harvester.

also reaches a maximum at V_P. The maximum power that can be obtained is twice that obtained using a full-bridge rectifier or voltage doubler. This is considering ideal diodes. In the presence of non-ideal diodes, the piezoelectric current has to charge C_P from 0 to $\pm(V_{RECT}+2V_D)$. This increases the amount of charge lost every cycle by $4C_P V_D$ in Equation 4.17. This reduces the output power obtained to

$$P_{RECT,SO} = 2C_P V_{RECT} f_P(2V_P - V_{RECT} - 2V_D) \tag{4.20}$$

which is also twice that obtained using a voltage doubler in the presence of non-ideal diodes as given by Equation 4.16.

Figure 4-11 shows a comparison between the simulated and theoretical power obtained at the output of the rectifier for the full-bridge rectifier, voltage doubler and switch-only rectifier cases. A value of 0.38V was used for V_D. It can be seen from the figure that the
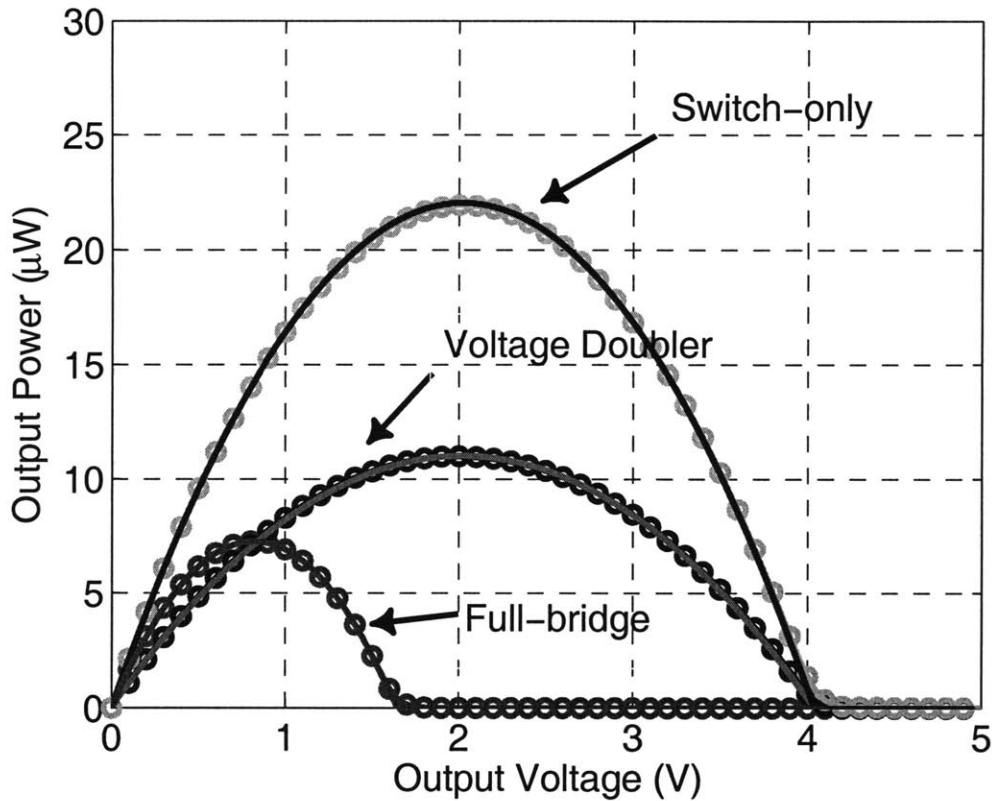
Figure 4-14: Theoretical and simulated power obtained at the output of the full-bridge rectifier, voltage doubler and switch-only rectifier employing CMOS diodes with change in V_{RECT}. Circular markers show simulated values.

power versus voltage profile for the switch-only rectifier is very similar to that obtained using the voltage doubler. The switch-only rectifier in effect works similar to two voltage doublers of opposite phase working in tandem. With the addition of a simple switch, the switch-only rectifier is able to provide 2X the amount of electrical power that was provided by the full-bridge rectifier or the voltage doubler. Appendix B presents an analysis of the power obtained at the output of the switch-only rectifier taking into account the effect of resistance R_P. The implementation of the switch M_1 and its gate-drive circuitry is explained in Section 4.6.

4.3.2 Bias-flip rectifier

The switch-only rectifier was able to utilize both half-cycles of the input current. However, there was still significant amount of charge lost in the rectifier due to charging C_P up from 0 to $\pm V_{RECT}$ every half-cycle. Any further increase in output power can only be obtained if this charge lost is reduced further. The basic problem with rectifiers delivering charge to a constant voltage is that every half-cycle the voltage in front of the diodes has to flip from $+V_{RECT}$ to $-V_{RECT}$ or vice-versa. This would not be a problem if the input impedance of the source did not have a capacitive component. However, the presence of C_P in the equivalent circuit of a piezoelectric harvester means that while flipping the voltage across C_P, the current i_P loses a significant amount of charge. The switch-only rectifier was able to reduce the charge lost by a factor of 2 by using a switch to discharge C_P to ground thereby leaving i_P to only do half the work in flipping the voltage. Can we do better than this?
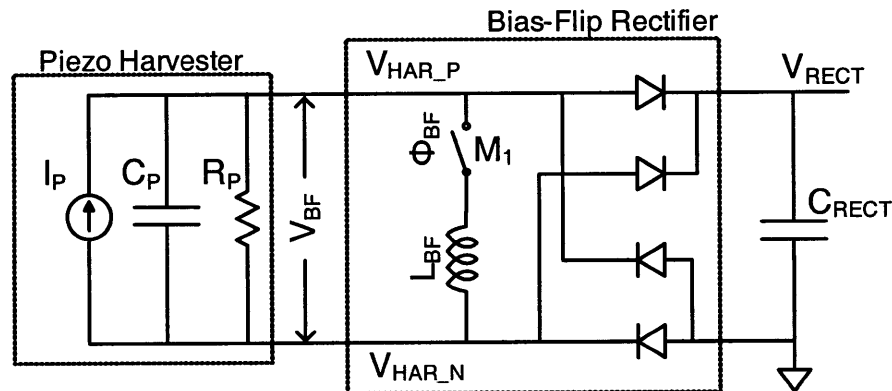
Figure 4-15: A bias-flip rectifier circuit to extract power from a piezoelectric energy harvester.

Figure 4-15 shows the circuit implementation of a bias-flip rectifier. Compared to the switch-only rectifier, an additional inductor (L_{BF}) has been added in series with the switch M_1. An inductor can passively flip the voltage across a capacitor. So instead of just using a switch, the bias-flip rectifier utilizes an inductor to flip the voltage across C_P. Assuming ideal diodes for the initial part of the analysis, the voltage and current waveforms associated with this circuit is shown in Figure 4-16. At every half-cycle, when i_P changes direction, the switch M_1 is turned ON briefly to allow the inductor to flip the voltage across C_P. The

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switch is turned OFF when the current in the inductor reaches zero. If the current flow path in the L_{BF}, C_P network were ideal, the voltage flipping would be perfect. However, the resistances along this path limits the magnitude of the voltage inversion as shown in Figure 4-16. Now, the piezoelectric current only has to charge up C_P from the flipped voltage to $\pm V_{RECT}$ before it can flow into the output. This significantly reduces the amount of charge lost. This way the majority of the charge available from the harvester can go into the output capacitor without having to charge and discharge C_P. To derive the amount of output power extractable using a bias-flip rectifier, let us assume that the resistance along the L_{BF}, C_P path is R_{BF}.
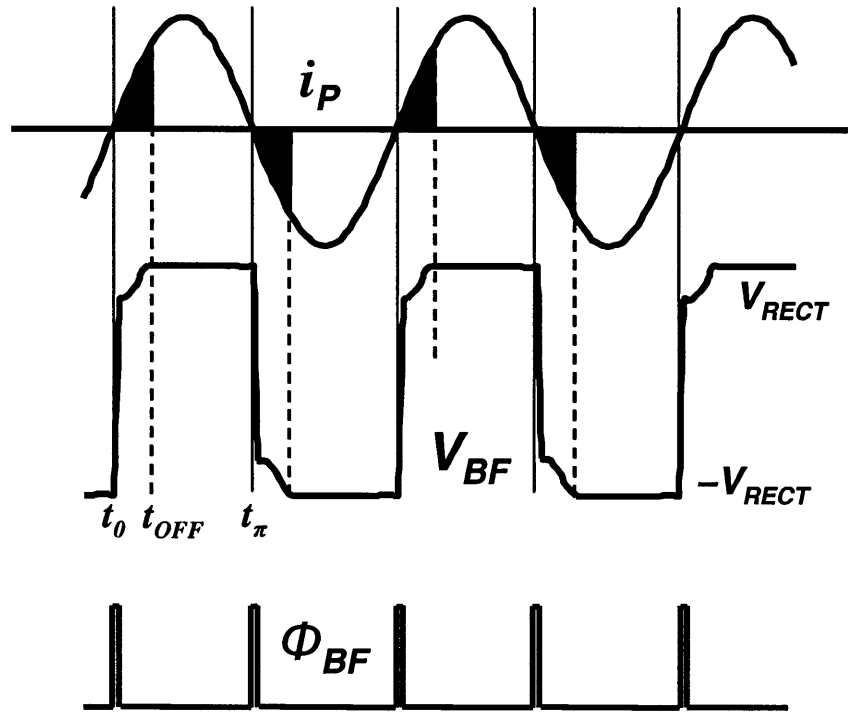
Figure 4-16: Simulated voltage and current waveforms for a bias-flip rectifier connected to a piezoelectric energy harvester.

Figure 4-17 shows the L_{BF}, C_P path when the switch M_1 is turned ON. When the switch is ON, the inductor helps in flipping in an efficient manner, the voltage (V_{BF}) across C_P. The resistance R_{BF} limits the magnitude of this voltage inversion. Ideally, the switch needs to be turned OFF exactly when the inductor current reaches zero to achieve maximal flipping

of the voltage across C_P. For the moment, assume that this is the case. Section 4.6 explains how this issue is tackled in the actual implementation of the bias-flip rectifier. Figure 4-17 shows the waveforms for the current through the inductor and the voltage across C_P when the switch is ON. Assuming the voltage across C_P starts at V_{RECT} when the switch is turned ON, Appendix A provides the equations to derive the voltage across C_P when the switch turns OFF. From the equations, the final voltage across C_P can be derived to be

$$V_{BF}(final) = -V_{RECT}e^{\frac{-\pi\beta}{\omega}} \qquad (4.21)$$

where $\beta = R_{BF}/2L_{BF}$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/\sqrt{L_{BF}C_P}$.
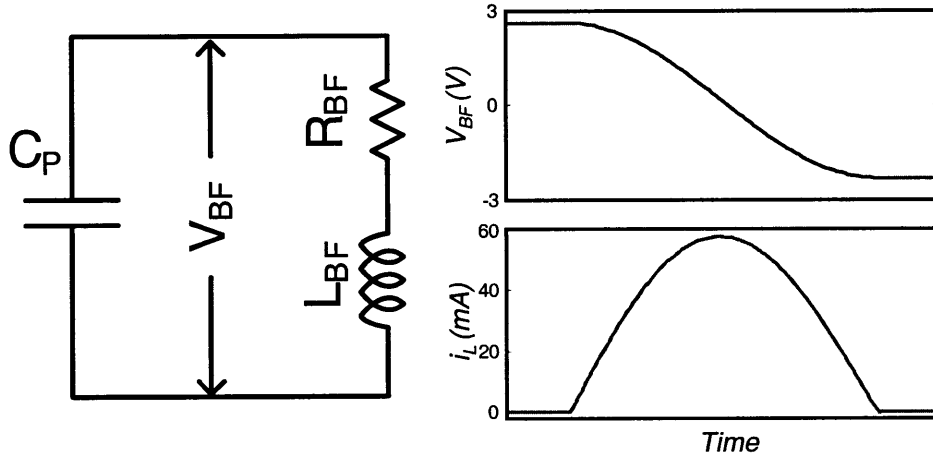
Figure 4-17: Simulated voltage and current waveforms of the bias-flipping network when switch M_1 is ON.

Once the bias-flipping takes place, the piezoelectric current i_P has to only charge C_P from the voltage across it after the flipping to $\pm V_{RECT}$. The charge lost in doing this every cycle can be given by

$$Q_{lost/cy} = 2C_P V_{RECT}(1 - e^{\frac{-\pi\beta}{\omega}}) \qquad (4.22)$$

The charge that actually flows into the output capacitor C_{RECT} is just the difference between the total charge available given by Equation 4.3 and the charge lost. This can be

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given by

$$Q_{RECT/cy} = Q_{av/cy} - Q_{lost/cy} = 4C_P V_P - 2C_P V_{RECT}(1 - e^{\frac{-\pi\beta}{\omega}}) \qquad (4.23)$$

The power delivered to the output by the bias-flip rectifier is the product of the charge delivered, V_{RECT} and f_P and can be given by

$$P_{RECT,BF} = 2C_P V_{RECT} f_P \left(2V_P - V_{RECT}(1 - e^{\frac{-\pi\beta}{\omega}})\right) \qquad (4.24)$$

Hypothetically, if we can build an ideal switch with R_{BF}=0, then the power that can be extractable using the bias-flip rectifier boils down to

$$P_{RECT,BF}(idealM_1) = 4C_P V_P V_{RECT} f_P \qquad (4.25)$$

This equation suggests that if we keep increasing V_{RECT}, we can get more output power. In the limit, it looks like we can get infinite power out of the harvester! This power output is however consistent with the simplistic model we have assumed till now in deriving P_{RECT}. The resistance R_P has not been taken into account till now. Without this resistance, the source should be capable of providing any amount of power without any limitation. This can also be seen by sending R_P to ∞ in Equation 4.2. The derivation for the output power extractable using a bias-flip rectifier in the presence of R_P is provided in Appendix B. From Equation B.23, the power output by the bias-flip rectifier is given by

$$P_{RECT,BF} = 2C_P V_{RECT} f_P \left(2V_P - (V_{RECT} + 2V_D)(1 - e^{-\tau}) - \frac{\pi k_{BF}(V_{RECT} + 2V_D)}{Q_P}\right)$$
$$(4.26)$$

where

$$k_{BF} = \frac{(V_P + (V_{RECT} + 2V_D)e^{-\tau})\omega_P t_1}{\pi(V_{RECT} + 2V_D)} - \frac{V_P \sin \omega_P t_1}{\pi(V_{RECT} + 2V_D)} + \frac{\pi - \omega_P t_1}{\pi} \qquad (4.27)$$

and

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$$\omega_P t_1 = \cos^{-1}\left(1 - \frac{(V_{RECT} + 2V_D)(1 - e^{-\tau})}{V_P}\right) \qquad (4.28)$$

From Equation 4.26 it can be seen that the output power reaches a maximum at

$$V_{RECT,BF}(max) = \frac{V_P}{1 - e^{-\tau} + \frac{\pi k_{BF}}{Q_P}} - V_D \qquad (4.29)$$

We can introduce a new term Q_{BF} which can qualitatively be thought of as the parallel combination of the Q-factors of the piezoelectric harvester and that of the L_{BF}, C_P resonant path.

$$Q_{BF} = \frac{1}{1 - e^{-\tau} + \frac{\pi k_{BF}}{Q_P}} \qquad (4.30)$$

The maximum power output by the bias-flip rectifier can now be given by

$$P_{RECT,BF}(max) = 2C_P \left(V_P - \frac{V_D}{Q_{BF}}\right)^2 Q_{BF} f_P \qquad (4.31)$$

Figure 4-18 shows a comparison between the simulated and theoretical power obtained at the output of the bias-flip rectifier. A value of 0.38V was used for V_D. It can be seen from the figure that there is a close match between the theoretical power calculated using Equation 4.26 and the simulated value of output power. Increasing the value of L_{BF} decreases τ and hence helps in improving the bias-flip magnitude thereby providing more output power. The implementation of the bias-flip rectifier is discussed in more detail in Section 4.6.

The analysis above suggests that using an inductor and switching it suitably can lead to a significant increase in the output power obtained from piezoelectric energy harvesters. This conclusion was arrived at by analyzing the equivalent circuit of a piezoelectric energy harvester and by trying to increase the charge delivered to the output every cycle. This same conclusion was arrived at by the authors of [54] who with the help of the synchronized switch harvesting (SSH) technique, were able to demonstrate a 2.6X improvement [55] in output power extracted compared to conventional full-bridge rectifiers. The authors were able to
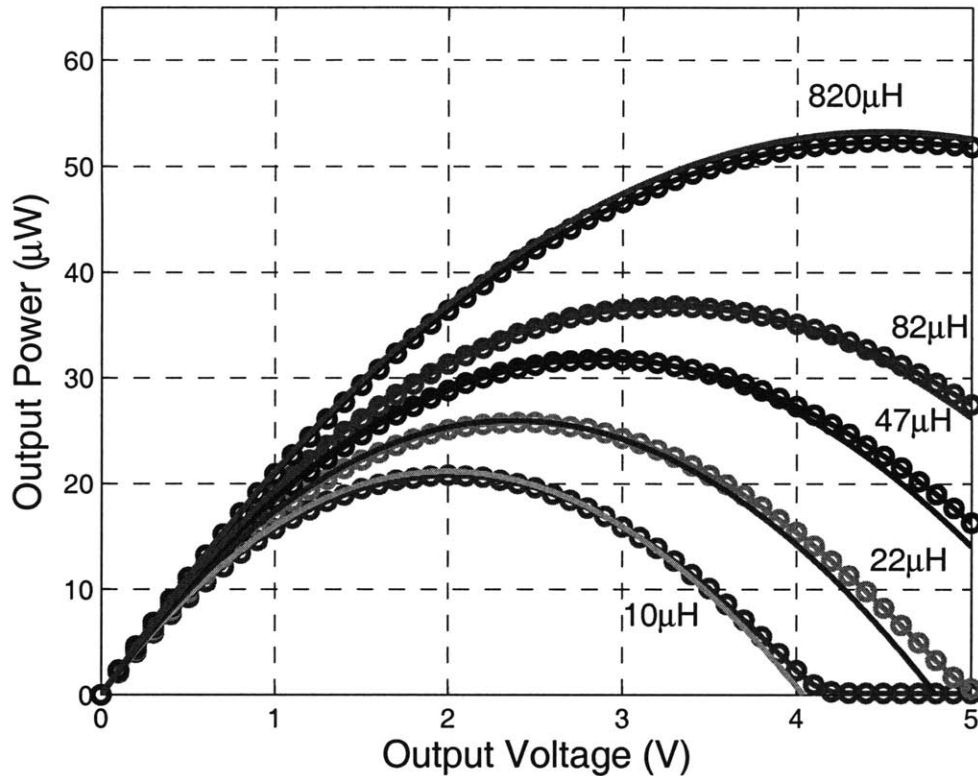
Figure 4-18: Theoretical and simulated power obtained at the output of the bias-flip rectifier with change in V_{RECT}.

arrive at the SSH circuit by using the synchronized switch damping (SSD) method [56], which is a nonlinear technique developed to address the problem of vibration damping on mechanical structures. The solution they present is however on a macro scale with discrete board-level components which is not amenable to integrated CMOS applications.

4.3.3 Comparison between power extraction capabilities of full-bridge rectifier and bias-flip rectifier

We can now compare the maximum power output by the full-bridge rectifier and bias-flip rectifier and how they match up to the theoretical maximum possible as given by Equation 4.2.

The maximum power output by the full-bridge rectifier can be derived from Equation 4.11 as

$$P_{RECT,FB}(max) = C_P(V_P - 2V_D)^2 f_P \qquad (4.32)$$

Compared to the maximum theoretical power available as shown in Equation 4.2, the ratio of the power obtained using a full-bridge rectifier is given by

$$\frac{P_{RECT,FB}(max)}{P_{RECT,THE}(max)} = \frac{4(V_P - 2V_D)^2}{\pi Q_P V_P^2} \qquad (4.33)$$

The maximum power output by the bias-flip rectifier is given by Equation 4.31. Compared to the maximum theoretical power available, the ratio of the power obtained using a bias-flip rectifier is given by

$$\frac{P_{RECT,BF}(max)}{P_{RECT,THE}(max)} = \frac{8Q_{BF}\left(V_P - \frac{V_D}{Q_{BF}}\right)^2}{\pi Q_P V_P^2} \qquad (4.34)$$

It can be thus seen that, the bias-flip rectifier improves upon the maximum power extractable by a factor of

$$\frac{P_{RECT,BF}(max)}{P_{RECT,FB}(max)} = \frac{2Q_{BF}\left(V_P - \frac{V_D}{Q_{BF}}\right)^2}{(V_P - 2V_D)^2} \qquad (4.35)$$

Assuming C_P=12nF, R_P=600kΩ, f_P=225Hz and V_P=2.4V, the maximum power output possible from the piezoelectric harvester as given by Equation 4.2 is 124.3μW. Considering ideal diodes (V_D=0), the full-bridge rectifier provides a power output of 15.55μW. Assuming τ=0.36 and a conservative estimate of k_{BF}=1, the bias-flip rectifier with ideal diodes provides an output power of 51.16μW, which is a 3.29X improvement over the full-bridge rectifier. If the bias-flipping is perfect (i.e. τ=0), then the power improvement is 6.48X. A further advantage of the bias-flip rectifier scheme is that it pushes the optimal voltage for power extraction to be higher than that obtained using only a full-bridge rectifier, thereby minimizing the losses which occur when diode non-idealities are introduced. In the presence

of CMOS diodes (V_D=0.38V), the full-bridge rectifier provides 7.26μW, while the bias-flip rectifier with moderate bias-flipping (τ=0.36) provides 39.64μW which is a 5.46X power improvement. With perfect bias-flipping (τ=0), the power improvement improves to 12.55X in the presence of CMOS diodes. From Equation 4.34, it can be seen that in the presence of ideal diodes and with perfect bias-flipping, the bias-flip rectifier can reach $8/\pi^2 = 81\%$ of the theoretical maximum possible. It was seen earlier that any attempt to tune out the input capacitance C_P using an inductor would require close to 41.7H of inductance, which is impractical. The bias-flip rectifier however does not attempt to resonate out the input capacitance C_P. Hence, it can get close to the theoretical maximum with only a small amount of inductance.
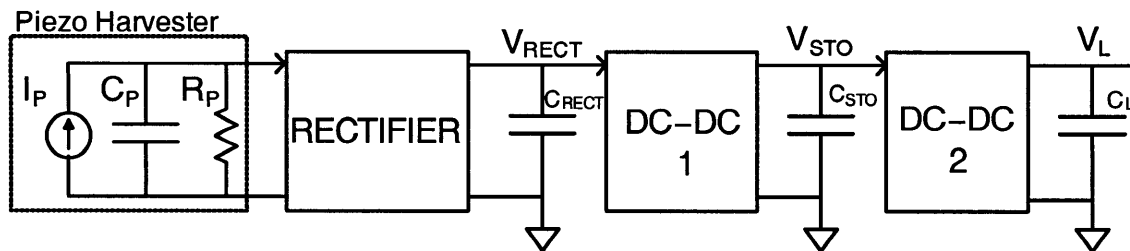
Figure 4-19: A general architecture of a piezoelectric energy harvesting system.

4.4 General architecture for a piezoelectric energy harvesting system

The rectifiers described in the previous section cannot directly power load circuits. It was seen in the earlier section that the output voltage of the rectifier V_{RECT} needs to be set at its optimum point for maximal power transfer. This optimum voltage can change as the input vibrations' amplitude or frequency changes. Hence, it becomes essential to regulate the output voltage of the rectifier using a voltage regulator. Figure 4-19 shows the general architecture of a piezoelectric energy harvesting system. The harvester is connected to a rectifier which has an output capacitor C_{RECT}. The voltage V_{RECT} at the output of the

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rectifier is regulated using a DC-DC converter. At the output of the first DC-DC converter is a storage capacitor C_{STO}. The storage capacitor can also be a rechargeable battery in cases where the piezoelectric energy harvester is used in rechargeable systems. The first DC-DC converter regulates V_{RECT} at its optimum voltage and transfers the energy obtained from the piezoelectric harvester on to the storage capacitor. Unlike commonly used DC-DC converters, this is used to regulate the input voltage as opposed to the output voltage. Since the power output by the piezoelectric harvester can be intermittent, the storage capacitor is used as a buffer to smoothen out the power flow into and out of the system. The voltage V_{STO} can move up or down depending on the power fluctuations. The second DC-DC converter is used to provide a constant regulated voltage V_L to the load circuits. Hence, on either side of C_{STO}, the voltages are regulated. For the system to function correctly, the average power input to the system must be close to the average power taken out of it. Otherwise, the voltage V_{STO} can rise to very large values or discharge down to 0. Hence, appropriate stops need to be provided at either end to prevent V_{STO} from reaching the extremes. On one side, if the input power is large, then once V_{STO} reaches its maximum set limit, either the first DC-DC converter needs to be turned OFF or a suitable current sink needs to be activated across C_{STO} to use the excess power. In the other case when the average power used in the system is larger, the load circuits need to be duty-cycled to reduce their average power consumption once V_{STO} has reached its set minimum limit. This type of architecture demands that the storage capacitor is large.

4.5   Architecture of the bias-flip rectifier

Figure 4-20 shows the architecture employed for the bias-flip rectifier system. The piezo-electric harvester is connected to the bias-flip rectifier which contains within it, the bias-flip switches and the control circuitry which determine the timing and gate-overdrive control of the switches. The power output by the rectifier goes into C_{RECT}. A buck DC-DC converter is used to regulate V_{RECT} and efficiently pass on the energy obtained from the harvester on to a storage capacitor C_{STO}. In this implementation, the storage capacitor was in the form
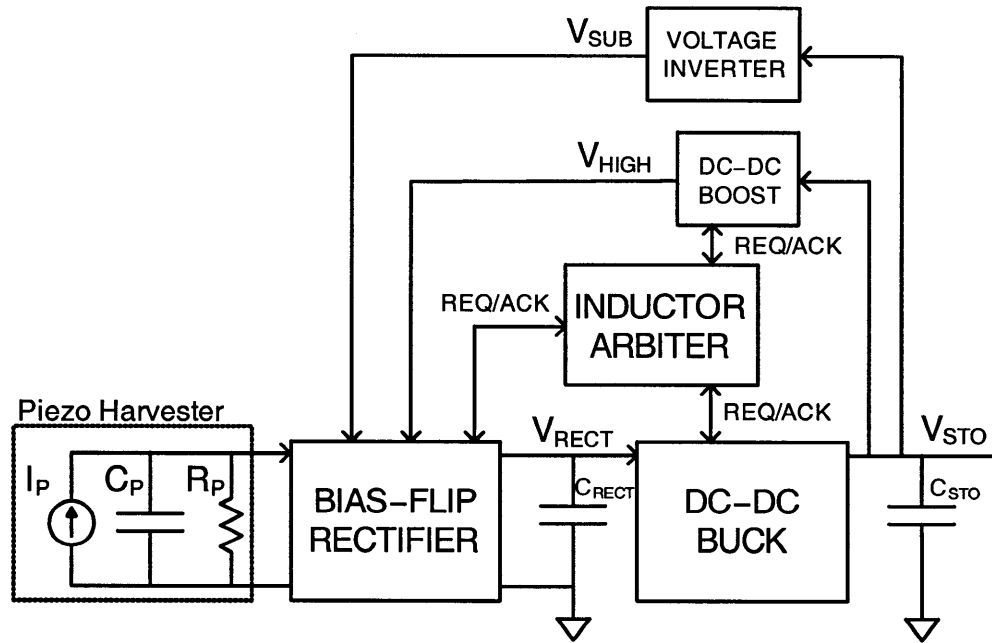
Figure 4-20: Architecture of the bias-flip rectifier system. The inductor arbiter controls access to the shared inductor L_{SHARE}.

of a rechargeable battery with a nominal voltage of 1.8V. A boost DC-DC converter is used to generate a high voltage V_{HIGH} ($\sim$5V) which is used to power the switches of the bias-flip rectifier. Driving the bias-flip switches with a high voltage helps to reduce their resistance thereby improving the bias-flip magnitude and power output by the rectifier. Both the buck and boost DC-DC converters employ an inductor-based architecture [57] for improved efficiency. The bias-flip rectifier also uses an inductor in the rectification process. The arbiter block shown in Figure 4-20 is used to control access to a shared inductor L_{SHARE}, which is shared between the bias-flip rectifier, buck and boost DC-DC converters. Section 4.9 explains the need and feasibility of inductor sharing and how the arbiter is implemented. The voltage inverter block is used to generate a negative voltage for feeding the substrate voltage in the CMOS implementation of the bias-flip rectifier. Section 4.10 talks about this block in more detail.
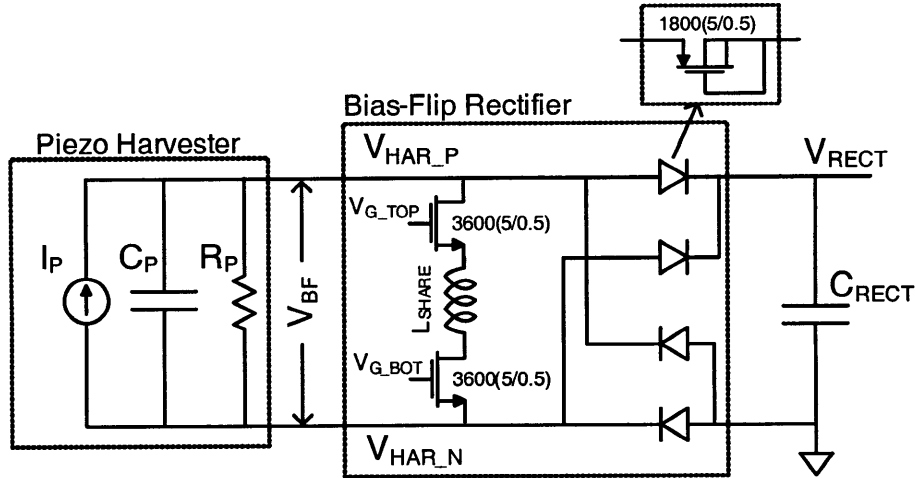
Figure 4-21: The bias-flip rectifier circuit showing the shared inductor and bias-flip switches. The substrate of the NMOS switches is connected to V_{SUB}.

4.6 Circuit implementation of the bias-flip rectifier

This section describes the implementation of the bias-flip rectifier as a CMOS circuit. The bias-flip rectifier is shown with the bias-flip switches and the shared inductor in Figure 4-21. The switches are implemented using NMOS transistors. It was assumed in Section 4.3.2 that the bias-flip switches are turned ON when the current i_P from the harvester crosses zero. Also, it is essential to keep the switches ON for just enough time to achieve zero-current switching of the inductor current. This timing control circuitry is described in Section 4.6.1. Let the maximum gate overdrive allowed by the technology in use be V_{HIGH}. For most efficient charge transfer through the inductor, the gate overdrive of the bias-flip switches needs to be as high as possible. The gate-drive circuitry described in Section 4.6.2 accomplishes this while maintaining the bias-flip switches within breakdown limits. The voltages at the nodes V_{HAR_P} and V_{HAR_N} shown in Figure 4-21 can go as low as one diode drop below ground when in operation. Assuming a pessimistic value of V_D=0.7V, this can easily turn on the P-N junction diodes of the substrate-N+ interface in the bias-flip switches. Hence, it is essential to keep the substrate connection of the bias-flip switches at least as low as -0.6V to prevent any unwanted diode leakage of the piezoelectric current. Since most

CMOS processes including the one used for this implementation are twin-well processes, it becomes essential to keep the substrate potential of the entire chip at a negative voltage (V_{SUB}). Section 4.10 describes how this negative voltage is generated. The diodes used in the rectifier were obtained using a PMOS transistor with its source as the P-end and the gate, drain and bulk connected together as the N-end of the diode as shown in Figure 4-21. Considerable work [44] [51] [52] [53] has been done on using synchronous rectifiers that use MOS transistors to replace the diodes. These have much lower forward voltage loss compared to p-n junction diodes or transistor-based diodes.
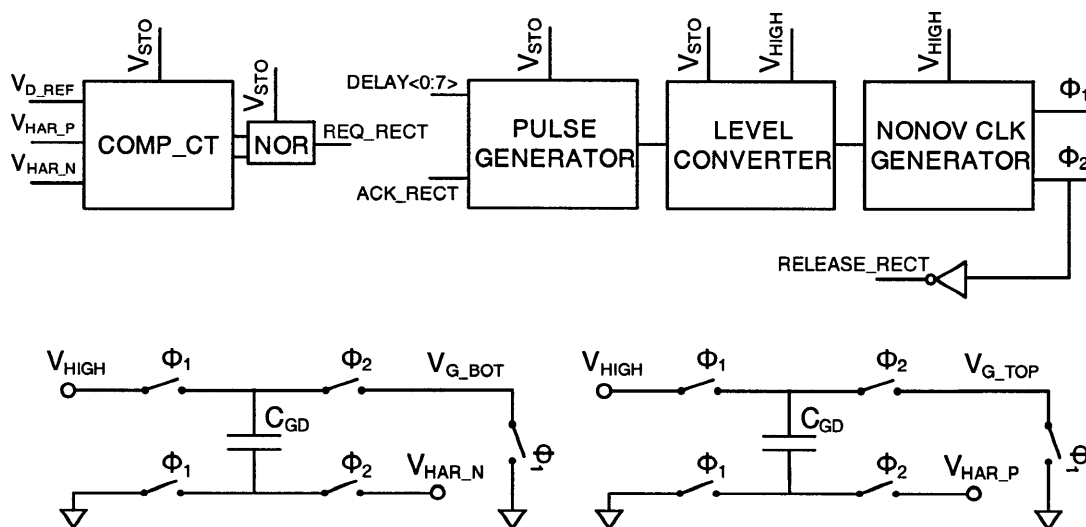
Figure 4-22: Block diagrammatic representation of the circuit for timing and gate-overdrive control of the bias-flip rectifier.

4.6.1 Timing control circuit

Figure 4-22 shows the block diagrammatic representation of the control circuitry that determines the timing and gate-overdrive control of the switches in the bias-flip rectifier. The switches need to be turned ON when i_P crosses zero. When i_P is close to zero, the diodes are just on the verge of turning OFF. At this point one of the voltages V_{HAR_P} or V_{HAR_N} is close to $V_{RECT} + V_D$ and the other one is close to $-V_D$. The zero-crossing of i_P is detected by comparing (depending on the direction of current) either V_{HAR_P} or V_{HAR_N} with

a reference voltage V_{D_REF}. This comparison is done using a continuous-time comparator shown in Figure 4-23. The comparator is modeled based on the circuit described in [44]. The same bias current generation circuit is shared between the two arms of the comparator. The reference voltage V_{D_REF} is set very close to the negative value of the voltage across a diode when a small amount of current ($< 1\mu$A) is flowing through it. In this implementation of the bias-flip rectifier system, this reference voltage was set externally. When the current i_P is positive and diodes 1 and 4 of the bias-flip rectifier are ON, the voltage V_{HAR_P} is close to $V_{RECT} + V_D$. This keeps OUT_1 low. At the same time, V_{HAR_N} is close to $-V_D$ which is lower than the V_{D_REF} set. Hence, OUT_2 is high.
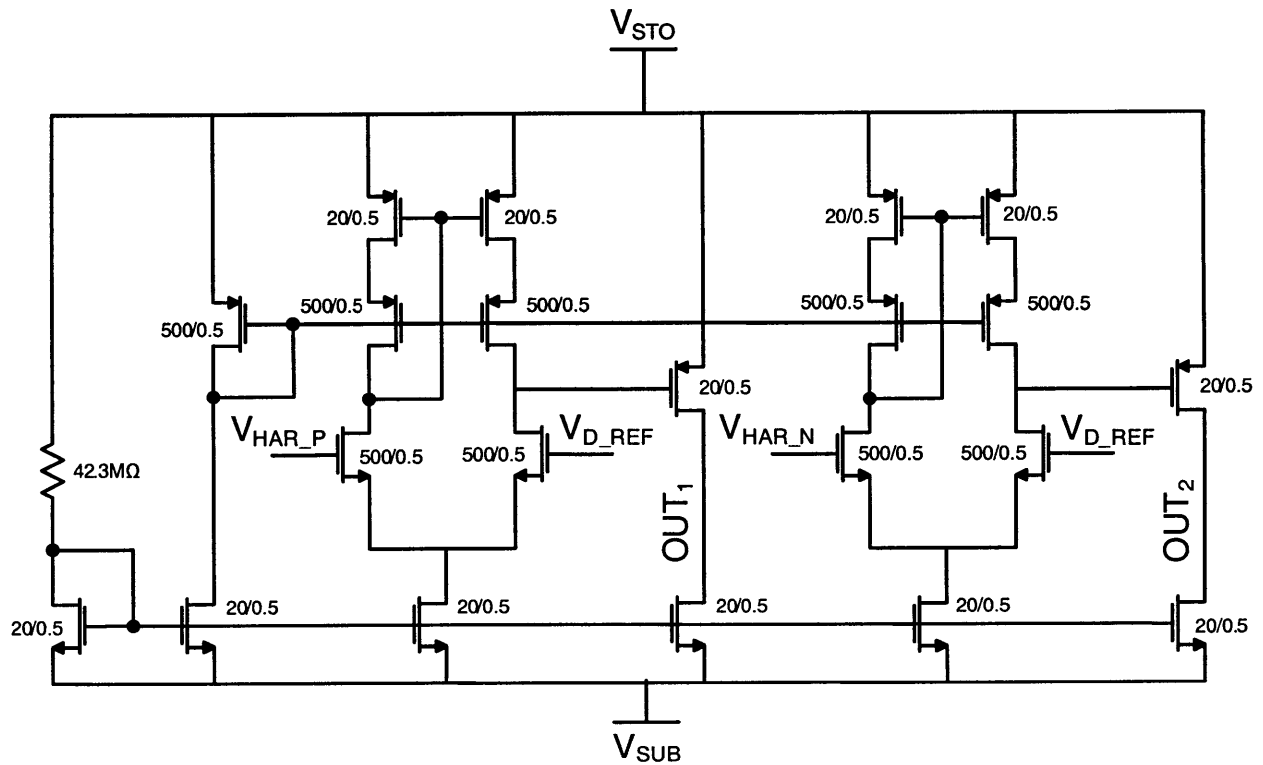
Figure 4-23: Continuous time comparator to detect the zero-crossing of the piezoelectric current.

When i_P reaches close to zero, V_{HAR_N} approaches V_{D_REF} and this causes OUT_2 to go low. This causes the output of the NOR gate REQ_RECT in Figure 4-22 to go high. This same process repeats when i_P is negative and approaches zero. This way the comparator

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is able to detect the zero-crossing of i_P in either direction. In simulations, the comparator consumes a constant current of 225nA from the 1.8V V_{STO} supply. The REQ_RECT signal going high signals that the bias-flipping is to begin soon. Since, the inductor used within the bias-flip rectifier is shared with the buck and boost DC-DC converters, before bias-flipping can begin, the access to the common inductor L_{SHARE} needs to be obtained. The REQ_RECT signal does this function by requesting the inductor arbiter to grant access to the inductor. The arbiter block is described in Section 4.9. The arbiter grants access through the ACK_RECT signal which triggers a pulse generator whose width can be controlled by the signal $DELAY < 0 : 7 >$.
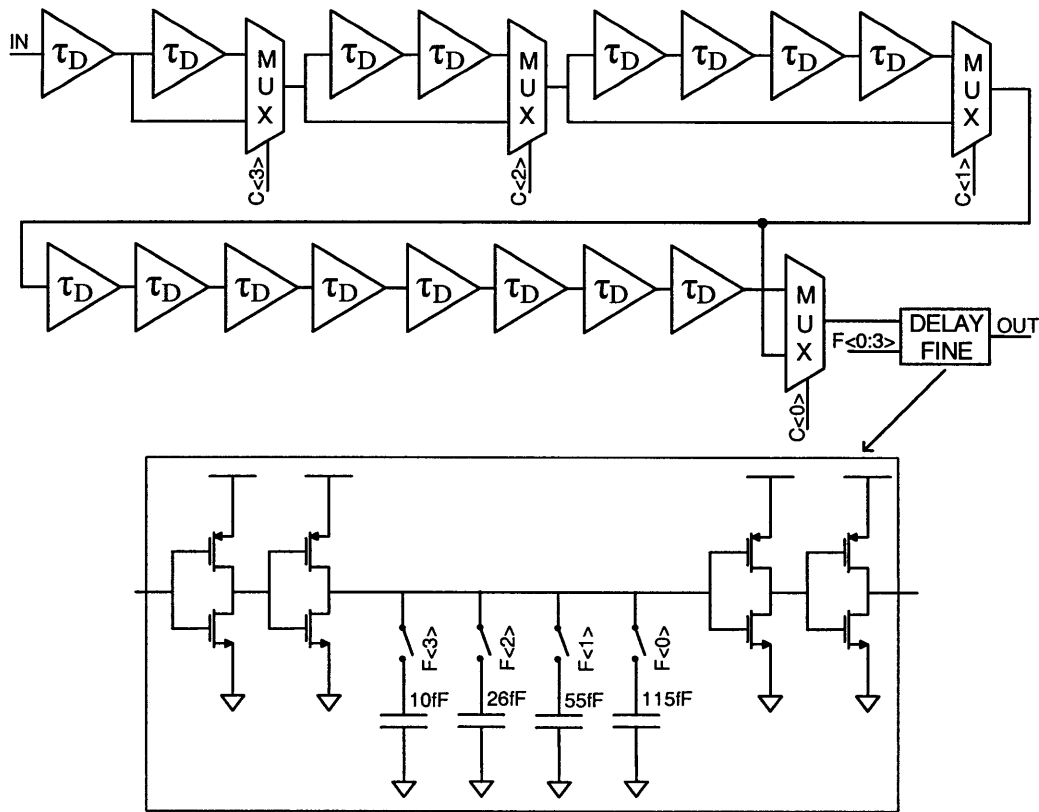
Figure 4-24: Delay block to control the ON-time of the bias-flip switches.

The pulse generator is a simple AND gate where the signal ACK_RECT is ANDed with a delayed inverted version of itself. The delay block shown in Figure 4-24 is used for delaying the ACK_RECT signal. The delay block is controlled by an 8-bit signal out of which 4-bits

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$(C < 0 : 3 >)$ are used for coarse control and the other 4-bits $(F < 0 : 3 >)$ are used for fine control of the delay. The delays themselves are generated using weak inverters charging up capacitances. A look into the fine delay block is provided in Figure 4-24. The coarse delay elements are obtained similar to the fine delay block with all capacitances activated. The partitioning of delay into a coarse and fine set allows a large range of delays to be achieved with fine granularity in the delay. The large delay range is necessary to accommodate a wide change in inductor value and CMOS process variations. The delay control signal $DELAY < 0 : 7 >$ controls the duration for which the bias-flip switches are ON. It is adjusted to achieve zero-current switching of the current through the shared inductor when bias-flipping is taking place. In this implementation of the bias-flip rectifier system, the delay control signal was fed in externally. Once a suitable inductor value is chosen for L_{SHARE}, the amount of time the bias-flip switches need to be ON is fixed. So, it is possible to do a one-time calibration of the delay control signal.
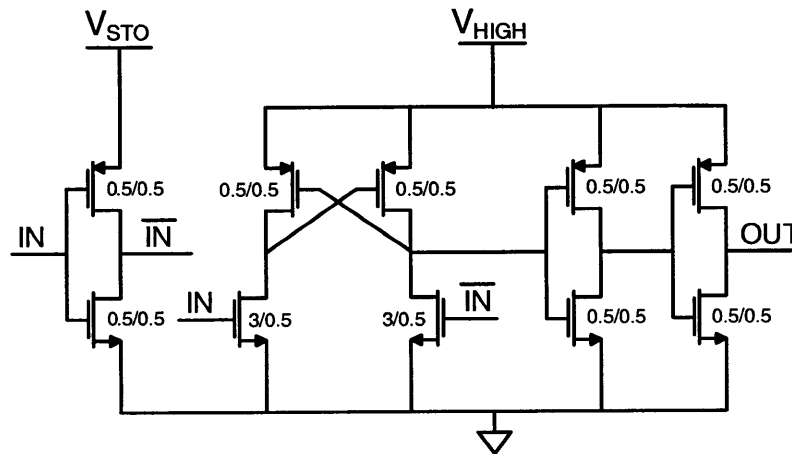
Figure 4-25: Level converter circuit to shift signals from V_{STO} to V_{HIGH}.

The pulse generated by the pulse-generator block is then level converted to get a pulse which transitions from 0 to V_{HIGH}. The level converter block used is shown in Figure 4-25. It is a simple cross-coupled structure which does not consume any quiescent current.

0.1

0.05

0

i_{LSHARE} (A)

8

V_{G_TOP},

4

V_{G_BOT}

0

4

V_{HAR_P},

2

V_{HAR_N}

0
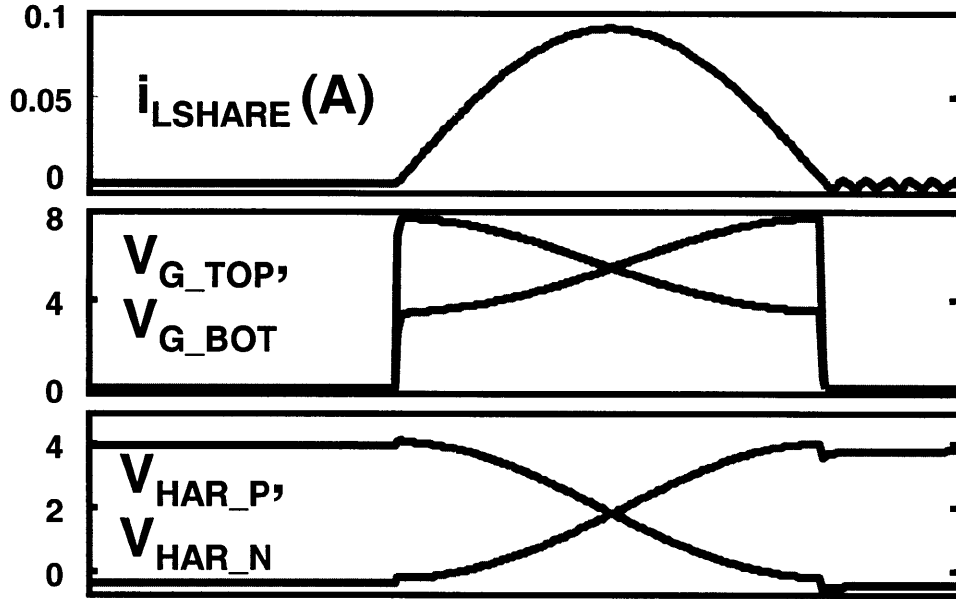
Figure 4-26: Simulation plots of the voltage at the output nodes of the harvester and the gate-drive of the bias-flip switches.

4.6.2 Gate-overdrive control circuit

The pulse obtained at the output of the level converter cannot be used directly to feed the gates of the bias-flip switches. The reason for this can be understood by observing Figure 4-26. When the bias-flipping takes place, the voltages V_{HAR_P} and V_{HAR_N} transition from close to $V_{RECT} + V_D$ to $-V_D$ or vice-versa. Assume that V_{RECT} is 4V and V_D is 0.4V. If the switches are turned ON using V_{HIGH} which is close to 5V, the gate-overdrive of one of the bias-flip switches will just be (5 - 4.4 = 0.6V) initially. This is very close to the threshold voltage of the transistors used and the bias-flipping will not even start. It is essential to maintain a constant gate over-drive of V_{HIGH} when the voltages V_{HAR_P} and V_{HAR_N} are transitioning. The switched capacitor circuit shown in the bottom of Figure 4-22 allows the bias-flip switches to have a gate-overdrive of V_{HIGH} when they are ON irrespective of the value of V_{RECT}. The gate-drive circuitry consists of switches and a capacitor C_{GD} which is implemented on-chip. During phase ϕ_1 when the bias-flip switches are OFF, the capacitor C_{GD} gets charged to V_{HIGH} and the gate voltages of both the bias-flip switches are brought

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to ground. When the bias-flipping has to take place, phase ϕ_2 begins, where the voltage across C_{GD} remains almost the same, but the voltage referenced to ground at V_{G_TOP} and V_{G_BOT} becomes $(V_{HIGH} + V_{HAR\_P})$ and $(V_{HIGH} + V_{HAR\_N})$ respectively as shown in Figure 4-26. This turns ON the bias-flip switches and keeps them ON till maximal possible flipping of voltage across C_P has taken place. After this, phase ϕ_2 ends and the bias-flip switches are turned OFF. When ϕ_2 goes low, the $RELEASE\_RECT$ signal is sent to the inductor arbiter to free up the shared inductor. This signal signifies that the bias-flip rectifier has finished utilizing the inductor for now. The voltage V_{HIGH} is obtained using a boost DC-DC converter as described in Section 4.8.
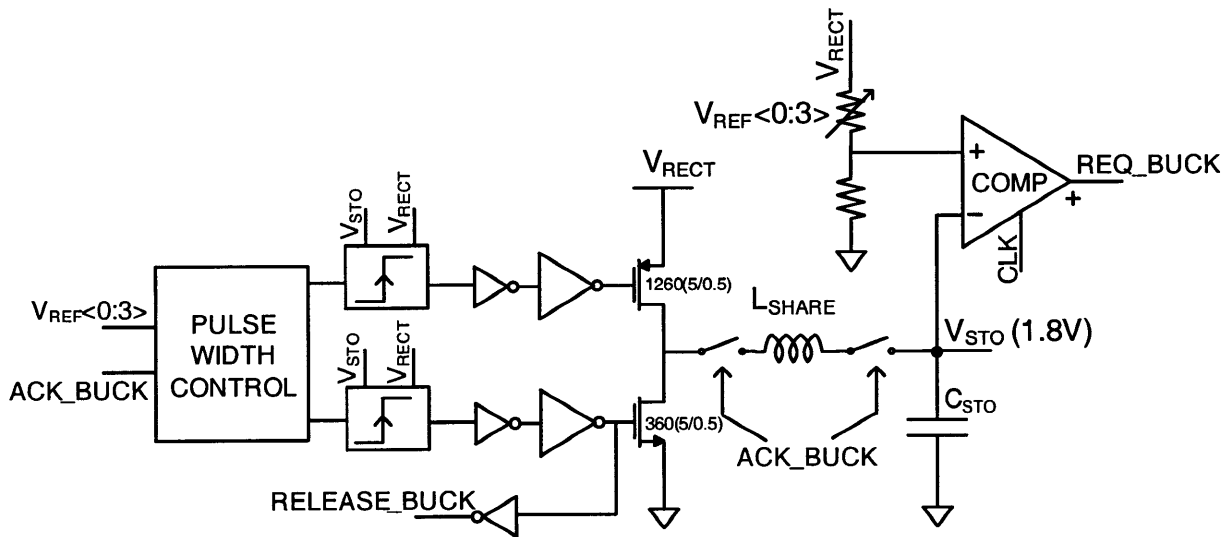
Figure 4-27: Architecture of the buck DC-DC converter for regulating V_{RECT}.

4.7 DC-DC Buck Converter

This section talks about the design of the DC-DC buck converter that is used to efficiently transfer the energy obtained from the piezoelectric energy harvester on to the storage capacitor C_{STO} which is fixed at 1.8V in this implementation. Figure 4-27 shows the architecture of the buck converter. Most DC-DC converter designs are used to provide power to a regulated output voltage from a fixed input voltage. In this DC-DC converter, the power is

provided to a storage capacitor which is fixed at 1.8V. The regulation happens at the input side (V_{RECT}). The buck converter is designed to regulate V_{RECT} from 2.2V to 5V with 4 bits of precision ($V_{REF} < 0 : 3 >$). The power provided by the harvester and that handled by the DC-DC converter is in the order of 1-100μW. This low power output demands extremely simple control circuitry design with minimal overhead power to get good efficiency.
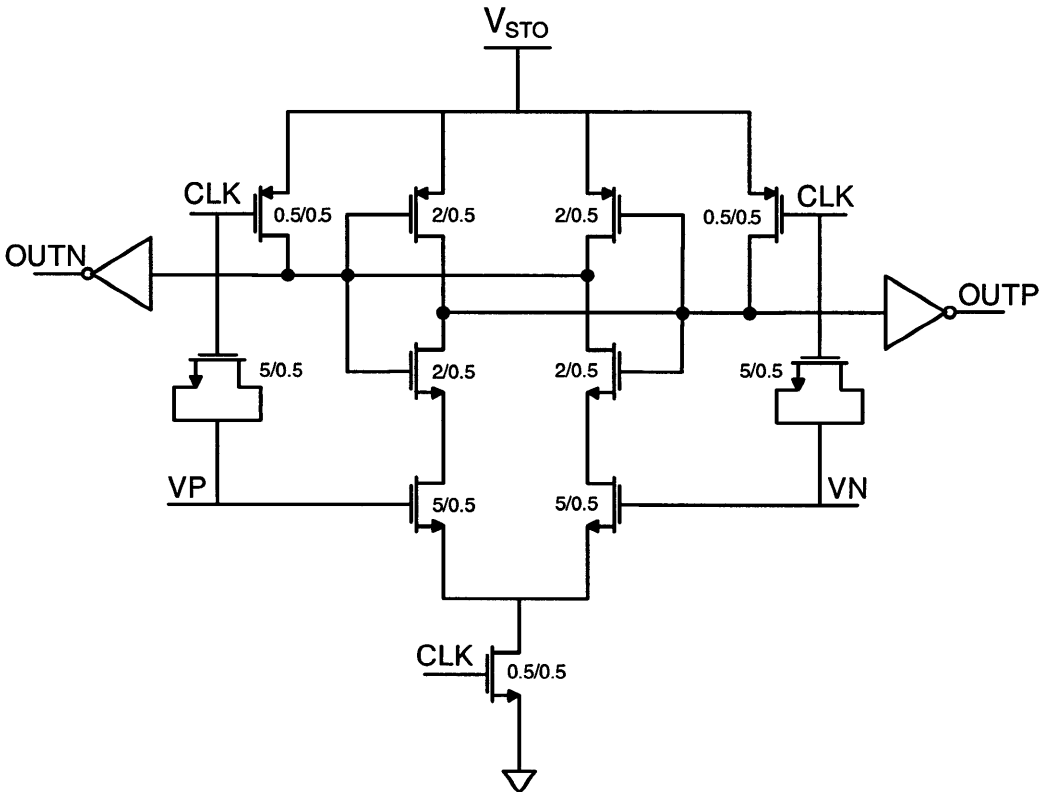
Figure 4-28: Implementation of the discrete time comparator.

The converter designed is a synchronous rectifier buck regulator and employs a pulse frequency modulation (PFM) mode of control [57]. PFM mode of control is essential to achieve high efficiencies at the micro-watt power levels handled by the converter. The control achieves regulation with the help of a discrete time comparator, the implementation of which is shown in Figure 4-28. A divided version of V_{RECT} is compared with V_{STO} (1.8V) and if it is found to be higher, the comparator sends the REQ_BUCK signal to the inductor arbiter to request access to the shared inductor. Once the arbiter grants access through

the *ACK_BUCK* signal, the pulse width control block turns the PMOS and NMOS power transistors ON sequentially with suitable pulse widths to transfer energy from the rectifier to C_{STO}.
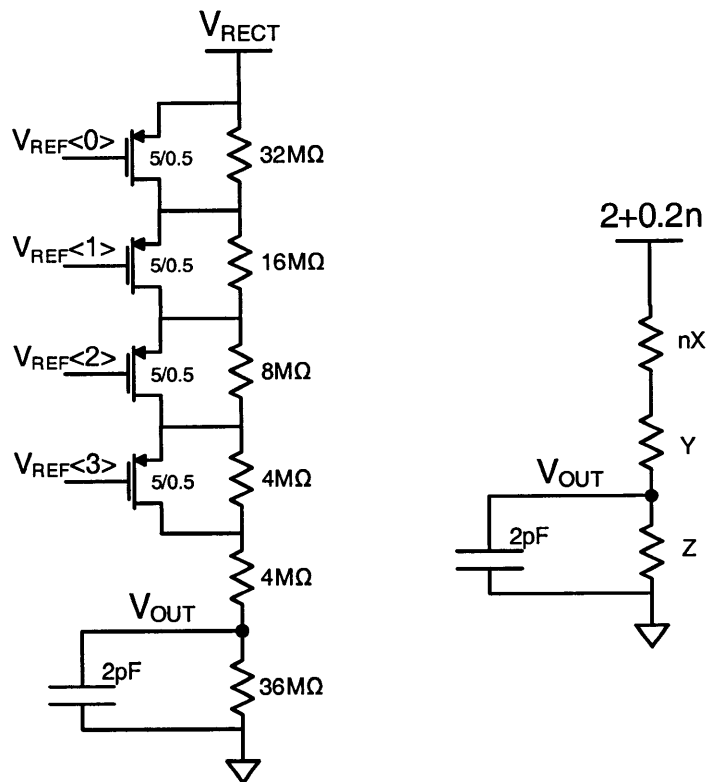
Figure 4-29: Reference ladder used to regulate V_{RECT} with 4-bits of precision. The circuit on the right is used to describe the design methodology.

4.7.1 Reference ladder design

The 4-bits of precision in regulating V_{RECT} is obtained using the reference ladder shown in Figure 4-29. The DC-DC converter should be able to regulate V_{RECT} to a voltage of $(2+0.2n)$V where n varies from 0 to 15. The presence of 1.8V means that no further external reference is necessary. The reference ladder is used to bring down $(2+0.2n)$V to 1.8V. The right hand side of Figure 4-29 will be used to describe the design of the reference ladder. The following equation governs the ladder design.

$$\frac{(2+0.2n)Z}{nX + Y + Z} = 1.8 \qquad (4.36)$$

When $n=0$, this equation boils down to

$$\frac{Z}{Y + Z} = 0.9 \qquad (4.37)$$

which gives $Z = 9Y$. Substituting this in Equation 4.36 gives

$$\frac{(2+0.2n)9Y}{nX + 10Y} = 1.8 \qquad (4.38)$$

which implies that $X = Y$. Hence, for the reference ladder design $X = Y = Z/9$. The overall current consumed by the reference ladder is given by $(2 + 0.2n)/(nX + Y + Z)$ which is equal to $0.2/Y$. For the reference ladder design implemented, the current consumption of the reference ladder was limited to 50nA. This current flows constantly and hence has to be kept to a minimum to achieve good efficiency. From this current limit, it is easy to figure out the values of the different resistances required. The final value of the resistances is shown in Figure 4-29.

4.7.2 Approximate Zero-Current Switching

The ultra-low load power levels demand extremely simple control circuitry to achieve good efficiency. This precludes the usage of high gain amplifiers to detect zero-crossing and thereby do zero-current switching of the inductor current [58]. In order to keep the control circuitry simple and consume little overhead power, an all-digital open loop control [59] as shown in Figure 4-30 is used to achieve zero-current switching. The pulse width control block which accomplishes this functions as follows: When the comparator senses that V_{RECT} is above the reference voltage, it sends a request to access the shared inductor. Once the arbiter grants access through the ACK_RECT signal, a PMOS ON pulse of fixed pulse width τ_P is generated. This ramps up the inductor current from zero. Once, the PMOS is turned OFF, the NMOS power transistor is turned ON. This ramps down the inductor current. Ideally,

Figure 4-30: Pulse width control block for the buck converter used to achieve approximate zero-current switching.

in the discontinuous conduction mode (DCM) used in this implementation, the NMOS has to be turned OFF just when the inductor current reaches zero. The amount of time it takes for the inductor current to reach zero is dependent on the reference voltage set and in steady state, the ratio of the NMOS to PMOS ON-times is given by the following equation:

$$\frac{\tau_N}{\tau_P} = \frac{V_{RECT} - 1.8}{1.8} \tag{4.39}$$

where τ_N and τ_P are the NMOS and PMOS ON-times and V_{STO} is set to 1.8V. Thus, by fixing τ_P, the values of τ_N for specific values of V_{RECT} can be pre-determined. By fixing τ_P to $9\tau_D$, the value of τ_N can be easily determined to be equal to $(1+n)\tau_D$ by using Equation 4.39.

The pulse width control block then suitably multiplexes the required number of τ_D delays in depending on the 4-bit reference voltage set to achieve approximate zero-current switching. Increasing the number of these delay elements and the complexity of the multiplexer block gives a better approximation to zero-current switching. Since only the ratios of the NMOS and PMOS ON-time pulse widths need to match, this scheme is independent of absolute delay values and any tolerance in the inductor value. The value of τ_D can be chosen by the designer taking into account energy delivery, ripple and efficiency considerations.

4.7.3 Efficiency of the DC-DC converter

The efficiency of the DC-DC converter operating in the PFM mode can be given by a simple equation as follows:

$$\eta = \frac{E_{LOAD}}{E_{LOAD} + E_{COND} + E_{SW} + E_{PARA} + E_{CONT}} \tag{4.40}$$

Here, E_{LOAD} is the energy delivered by the converter to the load every switching cycle. E_{COND} is the amount of energy lost every switching cycle due to conduction losses which occur primarily due to current flow through power transistors with finite on-state resistances. The gate-switching losses labeled as E_{SW} are due to the energy lost turning ON or OFF the gates of the power transistors every switching cycle. The energy (E_{PARA}) lost due to non-zero voltage switching of the intermediate parasitic capacitance at the drains of the power transistors dominates the timing error related losses [58]. While zero-voltage switching was not actively tackled in this implementation of the DC-DC converter, E_{PARA} was reduced by introducing a finite delay between the PMOS and NMOS ON pulses. Also, the energy delivered to the load per cycle, E_{LOAD} was increased by having a sufficiently large PMOS ON time τ_P. This helps in reducing the contribution of the parasitic power losses compared to E_{LOAD}, thereby increasing the efficiency. E_{CONT} is the energy lost every switching cycle due to switching and leakage related losses in the control circuitry. This loss mechanism affects significantly the low load efficiency of the DC-DC converter. PFM mode control reduces the switching frequency of the converter as load power drops. While the other

loss mechanisms remain constant as the switching frequency is varied, the control circuitry leakage loss integrates over the time period of a switching cycle and hence increases in value as the load power and thereby the switching frequency decreases. This leads to a drop in efficiency as the load power decreases. In order to minimize the control circuitry losses, the DC-DC converter uses a simple all-digital PFM mode control which does not consume any static power. The approximate zero-current switching block removes the need for any high gain amplifiers. The constant current consumed by the reference ladder is minimized by using large values of on-chip resistances.
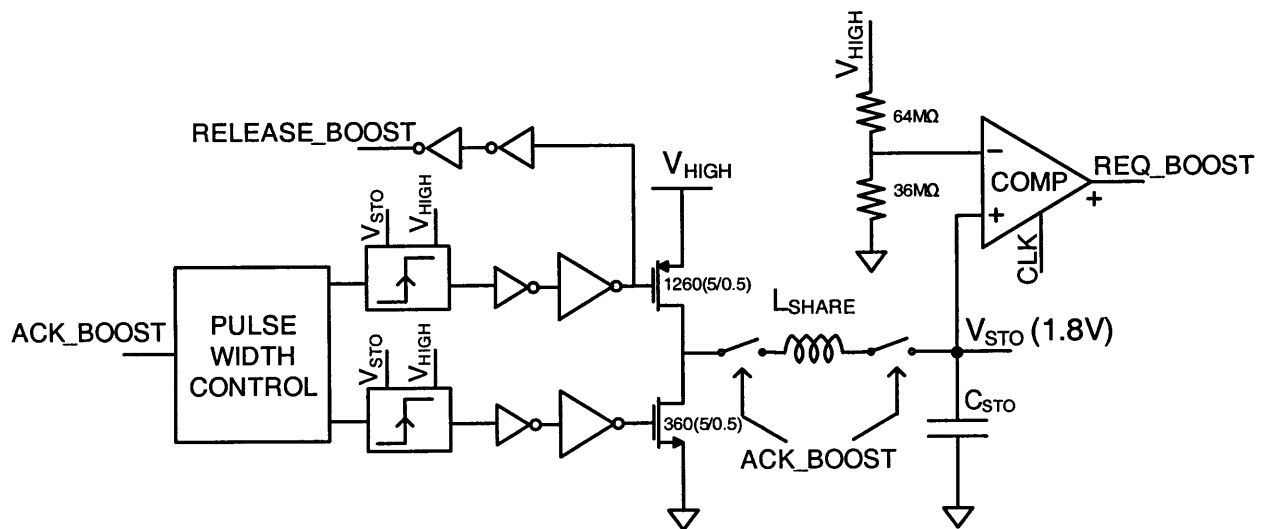
Figure 4-31: Architecture of the boost DC-DC converter used to generate V_{HIGH}.

4.8 DC-DC Boost Converter

This section talks about the design of the DC-DC boost converter that is used to generate the voltage V_{HIGH} which is close to 5V. This voltage is used to drive the switches of the bias-flip rectifier helping to reduce their resistance. The boost converter is designed very similar to the buck converter. It also employs pulse frequency modulation mode of control to regulate V_{HIGH}. This is again because of the extremely low power ($\sim 10\mu$W) handled by the boost converter. The boost converter is designed to regulate V_{HIGH} to a fixed voltage of

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5V. Hence, there is no reference ladder employed in its design. The resistive divider shown in Figure 4-31 has a fixed voltage division ratio of 0.36. This is used to bring down 5V to 1.8V for comparison with V_{STO}. When the voltage V_{HIGH} falls below 5V, the comparator sends the REQ_BOOST pulse to the arbiter to request access to the shared inductor L_{SHARE}. The arbiter grants access to the inductor through the ACK_BOOST signal. Once, the request is granted the pulse width control block sequentially turns the NMOS and PMOS power transistors. The pulse width control block for the boost converter is shown in Figure 4-32. Unlike the buck converter, there is no multiplexed delay elements here. This is again because the boost converter is used to regulate V_{HIGH} to a fixed voltage. In a boost converter, the NMOS power transistor has to be turned ON first. This causes current to flow in the inductor L_{SHARE} in the negative direction. After a set-time τ_N, the NMOS power transistor is turned OFF and the PMOS transistor is turned ON. During this time, the current in the inductor ramps down. Ideally, the PMOS transistor should be turned OFF just when the inductor current reaches zero to achieve zero-current switching. The NMOS and PMOS ON times can be pre-determined to be

$$\frac{\tau_P}{\tau_N} = \frac{V_{STO}}{V_{HIGH} - V_{STO}} = \frac{1.8}{5 - 1.8} \approx \frac{5}{9} \qquad (4.41)$$

The pulse width control block is designed to provide the right amount of delays to generate the NMOS and PMOS ON-pulses to achieve approximate zero-current switching. After the PMOS power transistor turns OFF, the boost converter sends the $RELEASE\_BOOST$ signal to the arbiter to signify that the boost converter has finished utilizing the inductor for this cycle. This frees up the inductor for use by other blocks.

4.9   Inductor Sharing using an Arbiter

The bias-flip rectifier described in this chapter can help to significantly improve the power extracted from piezoelectric harvesters compared to conventionally used rectifier schemes. However, its one main disadvantage is that it requires an inductor which has to be off-chip

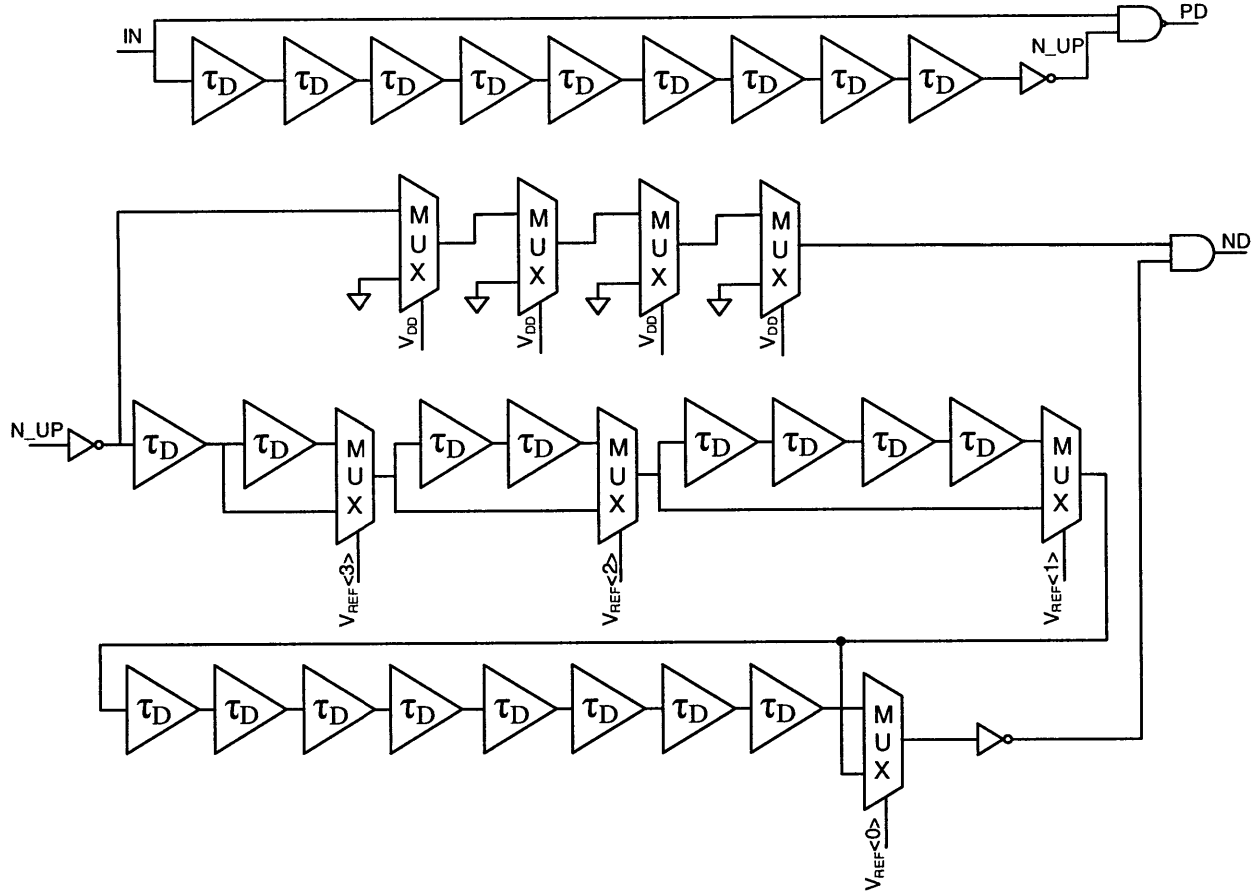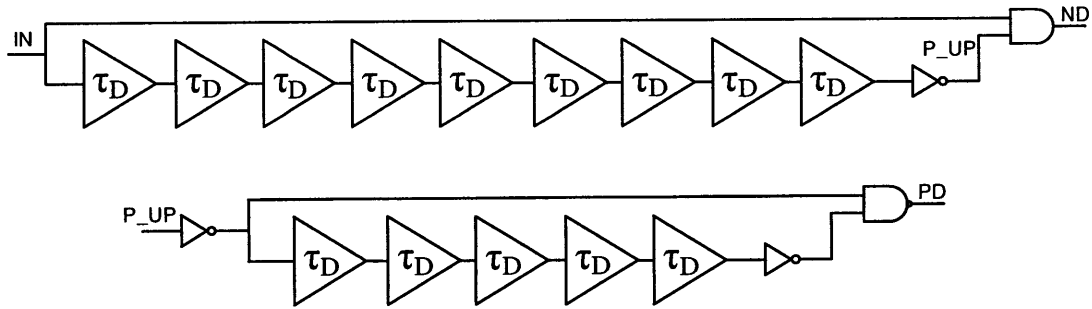Figure 4-32: Pulse width control block for the boost converter used to achieve approximate zero-current switching.

owing to its size and quality factor requirements. On the plus side, the bias-flip rectifier needs to use the inductor only for brief fractions of time when the input current i_P crosses zero. The buck and boost DC-DC converters used in the system also employ an inductor-based architecture to provide high efficiencies. As was explained in Section 4.7 and Section 4.8, these DC-DC converters work in discontinuous conduction mode. This means that even the DC-DC converters need to utilize the inductor only for fractions of the time based on the load power they deliver. Figure 4-33 shows the typical inductor utilization times for the three blocks along with their respective inductor current, request and release waveforms. For the bias-flip rectifier, the inductor utilization is around $1.47\mu s$ and it happens every 1.25ms. These numbers are arrived at assuming a 400Hz input vibration frequency and a $22\mu H$ inductor. The current through the inductor is sinusoidal when bias-flipping is taking place and once the current reaches zero, the bias-flip switches are turned OFF and the inductor is free. For the buck converter with a clock frequency of 20kHz, the utilization is $0.55\mu s$. In the worst case, this happens every $50\mu s$. The effect of discontinuous mode of conductor is evident from the inductor current waveform which ramps up when the PMOS power transistor is ON and ramps down to zero when the NMOS power transistor is ON. Here again after the inductor current reaches zero, the buck converter does not need the inductor anymore till the next clock cycle begins. The same is true for the boost converter where a typical utilization time is $0.42\mu s$ every $250\mu s$. The boost converter supplies very little load power and hence its inductor utilization is infrequent. We can see from these

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numbers that the inductor utilization is very sparse. This makes it possible to share the inductor between the 3 blocks thereby saving the volume and cost of the final solution.
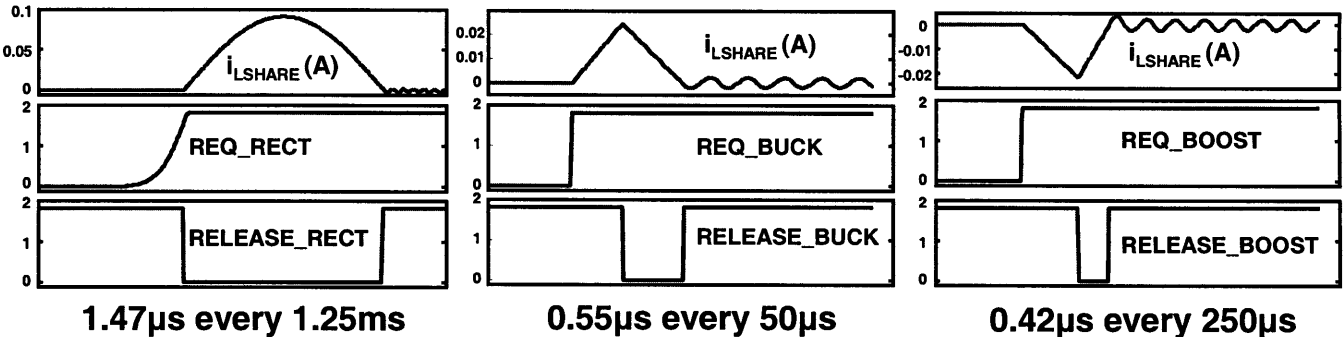
Figure 4-33: Inductor utilization times of the bias-flip rectifier, buck and boost DC-DC converters.

Since the clock for the DC-DC converters is not synchronous with the input vibration of the harvester, the DC-DC converter blocks and the bias-flip rectifier may require to use the inductor at the same time. To prevent any conflicts in the access to the shared inductor, an arbiter block is used to control the access. The arbiter block takes in the request and release signals from the three different blocks and it outputs the acknowledge signal which allows a specific block to access the inductor as shown in Figure 4-34. The arbiter consists of simple register based digital logic where the request and release signals are edge triggered.
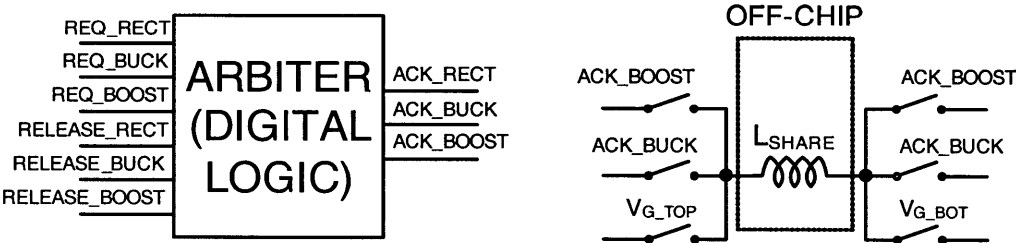
Figure 4-34: Simple representation of the arbiter block.

The arbiter is designed to perform the following functions

1. If the inductor is free, allocate access of the inductor to the next block which requests it

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2. If the inductor is occupied when a request comes in, put the request in a queue and acknowledge it once the inductor frees up based on a priority access scheme

3. The inbuilt priority is given to the buck converter followed by the bias-flip rectifier followed by the boost converter
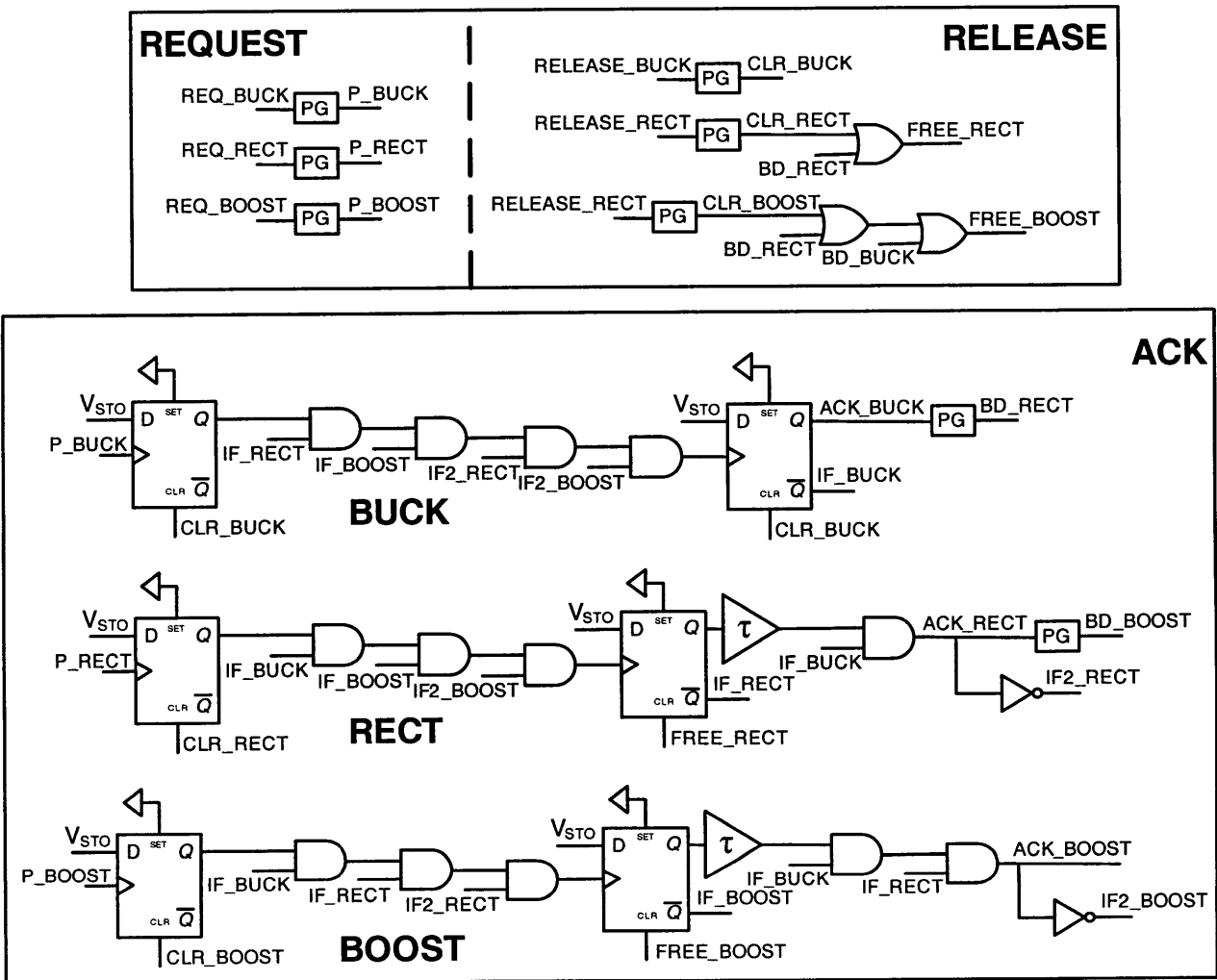
Figure 4-35: Gate-level implementation of the inductor arbiter.

A detailed gate-level implementation of the arbiter is shown in Figure 4-35. The circuit is divided into three sections for easier understanding. The request section consists of three pulse generator (PG) blocks which are used to generate request pulses when a rising edge

occurs in any of the request signals. The PG block is just a simple AND gate where the input signal is ANDed with a delayed inverted version of itself to generate a pulse. The release section also contains PG blocks to generate pulses when rising edges of release signals come in. The OR gates in the path of the RECT and BOOST release paths are used to prioritize access to the inductor. The ACK block is used to generate the acknowledge signals. Consider a scenario when the inductor is free. When this is the case, all the IF_* and $IF2\_*$ signals are high. IF being high just means that the inductor is free. When this is the case, suppose a request signal comes in from the BUCK block. This triggers the P_BUCK signal which makes ACK_BUCK go high and makes IF_BUCK go low. This signifies that the inductor is no more free and basically locks up the inductor for use by the $BUCK$ block. This situation exists till the $RELEASE\_BUCK$ signal comes in which brings down ACK_BUCK and makes IF_BUCK go high. In the meantime if any other request signal came in, then the corresponding block has to wait till IF_BUCK goes high to be acknowledged. The delay elements and additional gates in the RECT and BOOST sections are used to provide priority to the BUCK block followed by the RECT block. The arbiter is designed to guarantee acknowledgment of any inductor request within 4μs.

4.9.1 Effect of Inductor Sharing on System Performance

While inductor sharing helps to minimize the number of off-chip components and overall form factor and cost of the final power management solution, it comes at a penalty. The two main problems with inductor sharing is the delayed acknowledgment of request signals and the additional switches added in the path of current flow to accommodate sharing of the inductor. Its effect on the three main blocks are as follows:

1. **Bias-flip Rectifier:** The bias-flip rectifier requires the addition of one more switch in series with L_{SHARE} to enable inductor sharing. If the inductor was not shared, one of the bias-flip switches would not be necessary. This additional switch adds resistance in the L_{SHARE}, C_P resonant path. This reduces the magnitude of the flipped voltage and hence reduces the overall power output. The amount of power reduction can be

found by including this additional resistance to the value of R_{BF} in Equation 4.21. It is usually in the order of 10-15%. The other issue with inductor sharing is that there may be a delay of up to $4\mu s$ from the time the bias-flip rectifier requests the inductor till when it is granted access. Since the time scales of the input vibration is of the order of milli-seconds, this has a negligible effect on the performance of the bias-flip rectifier.

2. **DC-DC Converters:** Inductor sharing requires the addition of 2 switches on either side of L_{SHARE} in the buck and boost converters as shown in Figure 4-27 and Figure 4-31. This adds more resistance in the conductive path and also additional switching loss. The measurement results presented in Section 4.11 show that a 2-3% drop in efficiency of the DC-DC converter is seen because of inductor sharing. This is an acceptable penalty to pay considering the benefits of inductor sharing. Further, once the inductor is shared between two blocks, the addition of further blocks to share the same inductor only results in more delays in accessing the inductor. It does not affect the additional resistance due to the multiplexer switches. Since the time delay is still very small, additional DC-DC converters can be allowed to access L_{SHARE} with little to no penalty.

4.10 DC-DC Converter to Generate Negative Voltage

The need to keep the substrate voltage of the entire chip at a negative value was explained in Section 4.6. The negative voltage is generated by a switched capacitor voltage inverter as shown in Figure 4-36. This switched capacitor converter does not regulate its output voltage to a specified value. Instead, the converter switches at every cycle. The capacitors are switched in such a way that the output voltage V_{SUB} reaches $-V_{STO}/2$ at no-load. Apart from diode leakage losses, the voltage V_{SUB} only provides power to the continuous time comparator block which is used to identify the zero-crossing of i_P. The comparator consumes only 225nA of current. So, in the worst case, the V_{SUB} supply needs to provide not more
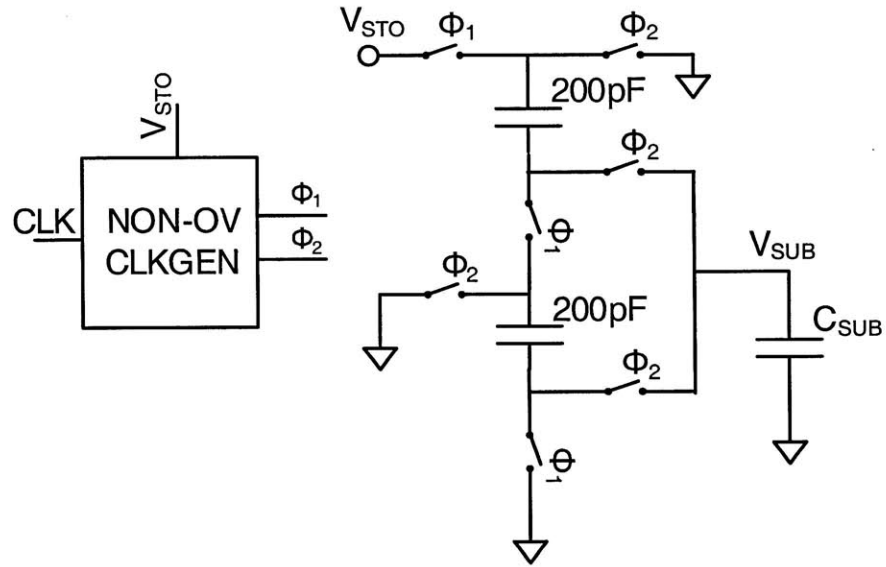
Figure 4-36: Switched capacitor circuit to generate a negative voltage.

than $1\mu A$ of total current. The capacitors are sized such that V_{SUB} stays below -0.8V.
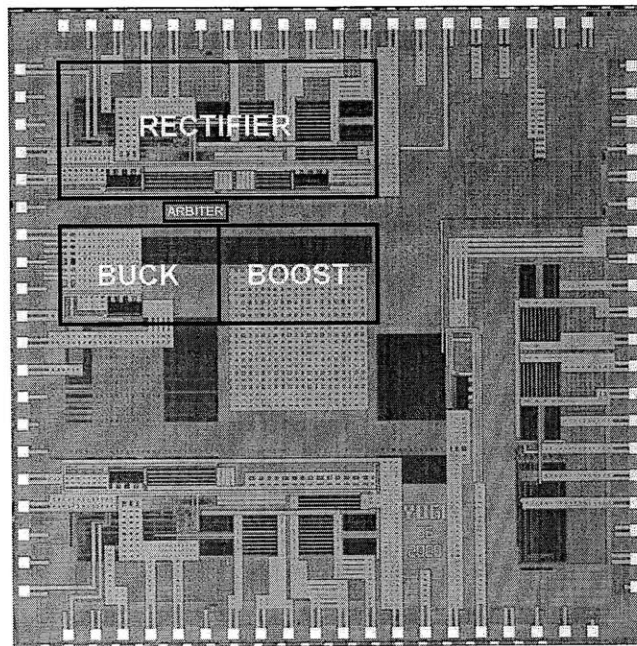
Figure 4-37: Die photo of the piezoelectric energy harvesting chip.

4.11 Measurement Results

The piezoelectric energy harvester interface circuit [60] was implemented in a $0.35\mu m$ CMOS process. Figure 4-37 shows the die photo of the test chip. The active area of the interface circuitry together with the DC-DC converters is 4.25 mm^2. The majority of this area is occupied by passive elements like resistors and capacitors implemented as part of the resistive ladder, delay blocks and the continuous time comparator. The die photo identifies the areas occupied by the rectifier, buck and boost DC-DC converters and the inductor arbiter.
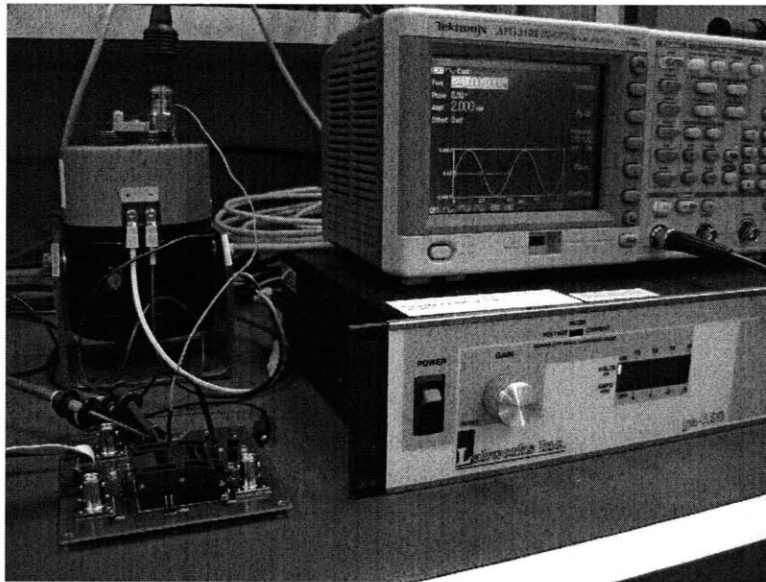
Figure 4-38: Experimental setup showing the piezoelectric device mounted on a shaker table.

A commercially available piezoelectric device (model v22b) [61] from Mide was used to perform all the measurements reported in this section. The piezoelectric device was mounted on a shaker table (Labworks ET-126-B1) which was excited using a sine wave from a signal generator amplified through a power amplifier (Labworks PA-138). The experimental setup is shown in Figure 4-38.

Figure 4-39 shows oscilloscope waveforms of the output voltage of the piezoelectric harvester for the different rectifier scenarios. The amplitude of the open-circuit voltage (V_P) of the piezoelectric harvester was 2.4V for this measurement. The waveforms obtained are

Full-Bridge Rectifier	Switch-only Rectifier	Bias-Flip Rectifier
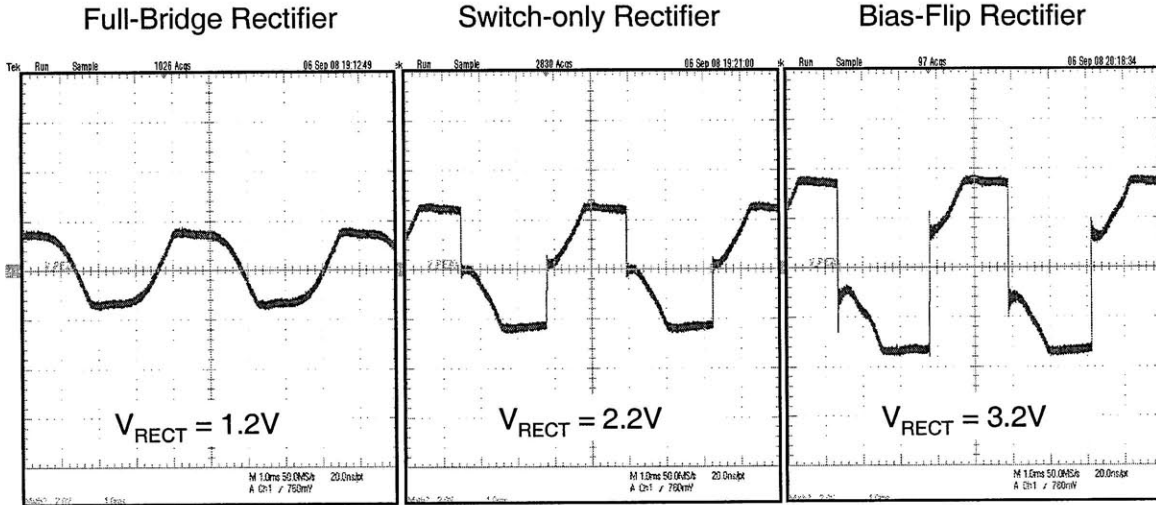
Figure 4-39: Measured waveforms of the output voltage across the piezoelectric harvester for the full-bridge, switch-only and bias-flip rectifier cases.

consistent with the operation of the different rectifiers as described in Section 4.2 and Section 4.3. The voltage V_{RECT} for the full-bridge rectifier case was set to 1.2V. For the switch-only rectifier, V_{RECT} was set to 2.2V. The switch-only rectifier brings the voltage to ground almost instantly, thereby using the piezoelectric current i_P to only do half the job in inverting the voltage. The bias-flip rectifier with V_{RECT} set at 3.2V, goes further and inverts the voltage across the piezoelectric harvester. A 47μH inductor was used with the bias-flip rectifier.

Figure 4-40 shows the measured power obtained at the output of the rectifier as the rectifier voltage is changed. The shaker was excited using a 225Hz vibration with an acceleration of 3.35g for this measurement. The piezoelectric device output a sinusoidal open-circuit voltage with a frequency of 225Hz and an amplitude of 2.4V. The red curve at the bottom is the power output by a conventional full-bridge rectifier. The full-bridge rectifier was able to provide a maximum power output of 14μW at an optimal rectifier voltage of 1.1V which closely matches theoretical predictions. The switch-only rectifier shown in the blue curve improved upon the extractable power by 1.9X compared to the full-bridge rectifier. It was able to push the optimal voltage for maximal power transfer up by close to 2X. The top four curves show the power output by the bias-flip rectifier for different values of the inductor.
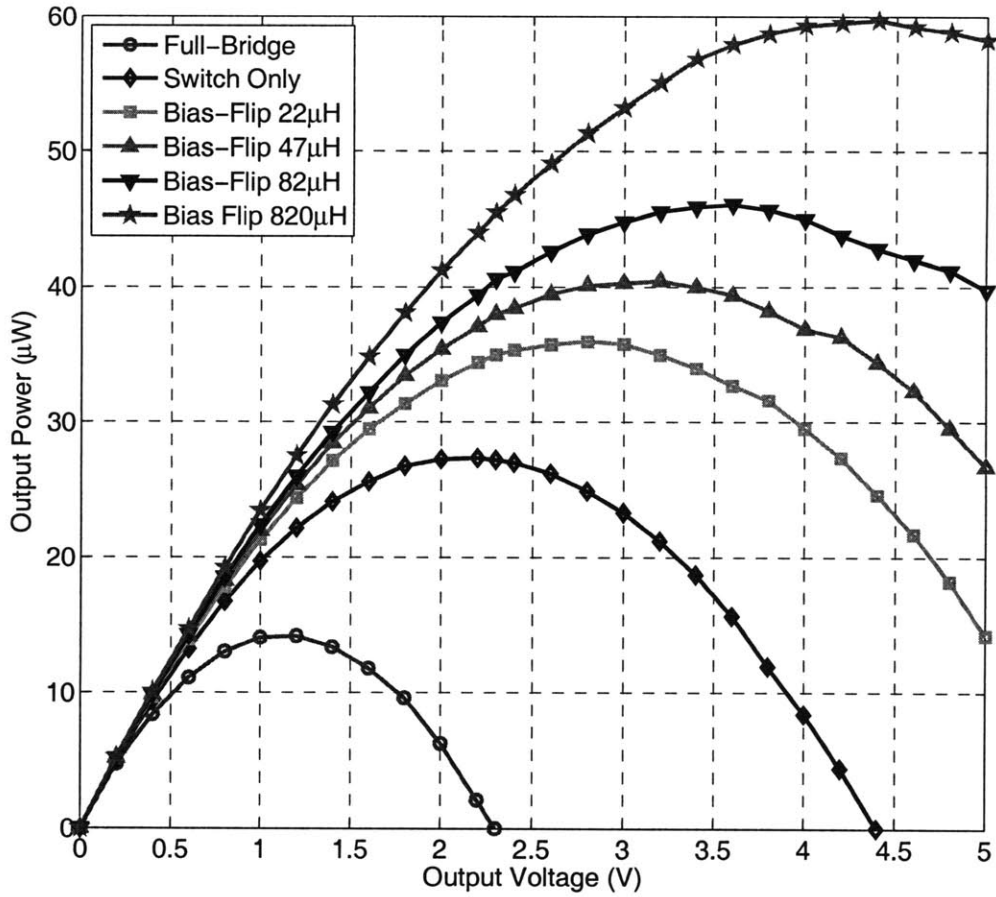
Figure 4-40: Measured electrical power output by the piezoelectric energy harvester with off-chip diodes.

The effectiveness of the bias-flip rectifier improves as the inductance is increased as this increases the Q of the resonant network. With an 820μH inductor, the bias-flip rectifier was able to provide a 4.2X improvement in power extracted compared to the full-bridge rectifier. These measurements were done with off-chip diodes which are close to ideal (V_D=0.05V). It was noted earlier that another big advantage of using the bias-flip rectifier scheme is that it pushes the optimal voltage for power extraction to be higher than that obtained using only a full-bridge rectifier as can be seen from Figure 4-40. This helps in reducing the effect of the losses which occur when diode non-idealities are introduced. When these same measure-

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ments were done with on-chip diodes (V_D=0.38V), the improvement in power extracted on using a bias-flip rectifier increases to above 7X.
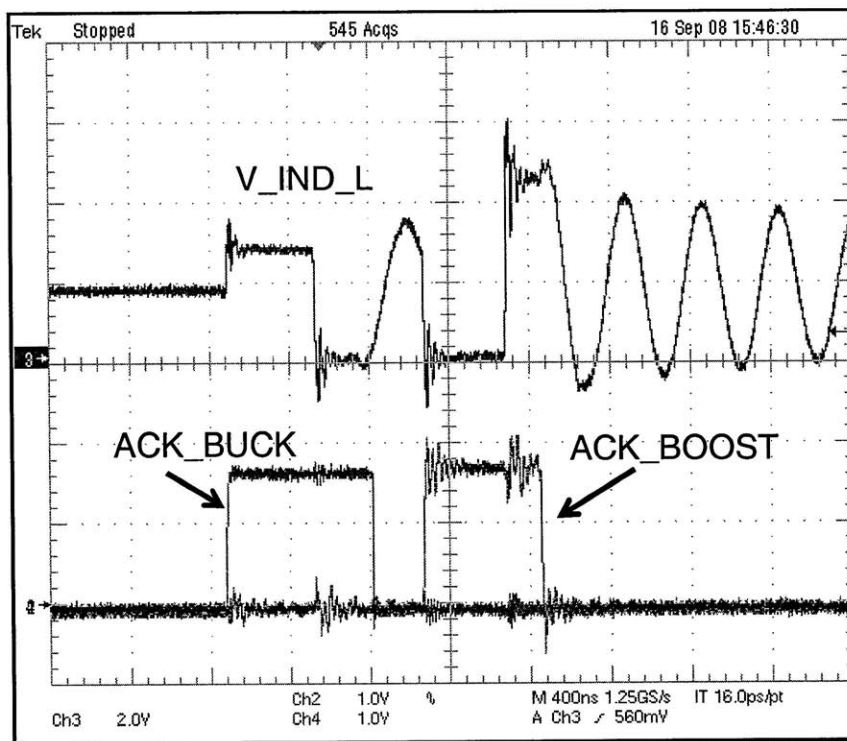
Figure 4-41: Measured waveform of the voltage at one end of L_{SHARE} that demonstrates inductor sharing.

Figure 4-41 shows measured waveforms of the voltage at one end of the shared inductor L_{SHARE} when accessed by the buck converter followed by the boost converter. When ACK_BUCK is high, the buck converter uses the inductor. It turns its PMOS power transistor ON first followed by its NMOS power transistor. The node voltage at the left end of L_{SHARE} reflects this by going close to V_{RECT} when the PMOS is ON and being close to 0 when the NMOS is ON. Once both the power transistors are OFF, the buck converter releases the inductor which causes ACK_BUCK to go low. In the scenario shown in Figure 4-41, the boost converter requests the inductor at the same time the buck converter requests it. Due to the inbuilt priority in the arbiter, the buck converter is given access first. After ACK_BUCK goes low, the boost converter is given access. When the boost converter is

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active, it turns its NMOS power transistor ON first followed by its PMOS transistor. This can be seen from the node voltage which stays close to 0 when the NMOS is ON and close to V_{HIGH} ($\sim$5V) when the PMOS transistor is ON. Once both transistors turn OFF, the boost converter releases the inductor. The ringing seen in the voltage V_IND_L is due to the parasitic capacitance at that node which resonates with L_{SHARE}. The voltage will eventually settle at V_{STO} due to the resistance along the path. Figure 4-42 shows measured waveforms of the voltage at the left end of L_{SHARE} when accessed by the buck converter followed by the bias-flip rectifier. When the rectifier is ON, the voltage is more sinusoidal due to the bias-flipping action.
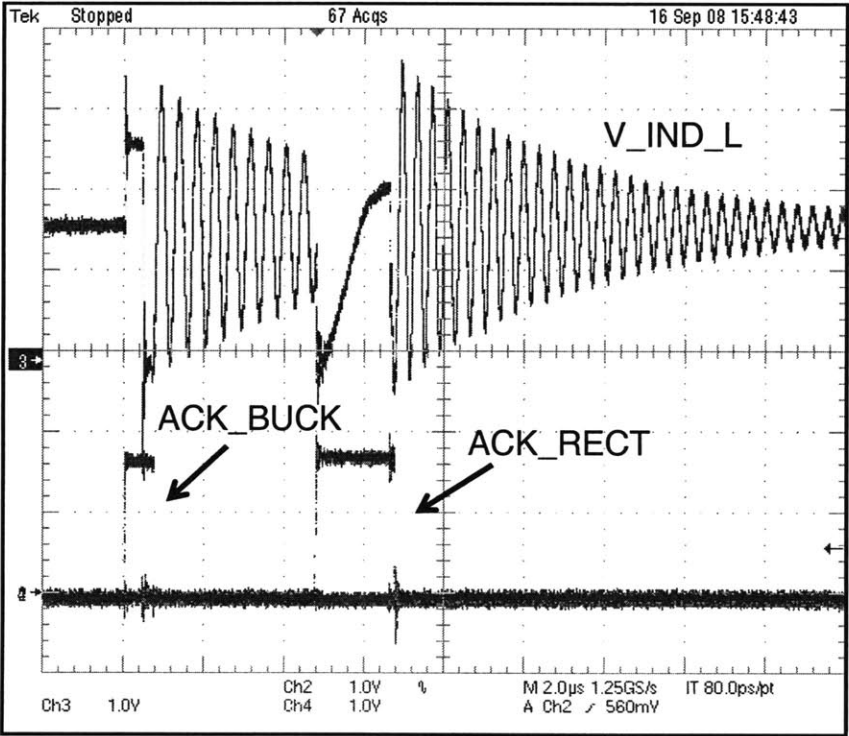
Figure 4-42: Measured waveform of the voltage at the left end of L_{SHARE} when it is accessed by the buck converter followed by the bias-flip rectifier.

Figure 4-43 and Figure 4-44 show the measured efficiency of the buck converter with change in the rectifier voltage with and without the shared inductor. With the shared inductor, the DC-DC converter achieves an efficiency of around 85% across the voltage
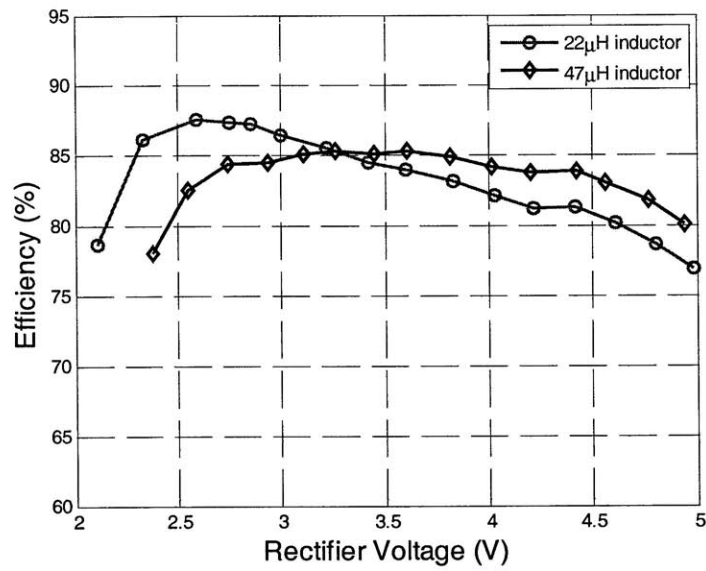
Figure 4-43: Measured efficiency of the buck converter with the shared inductor.
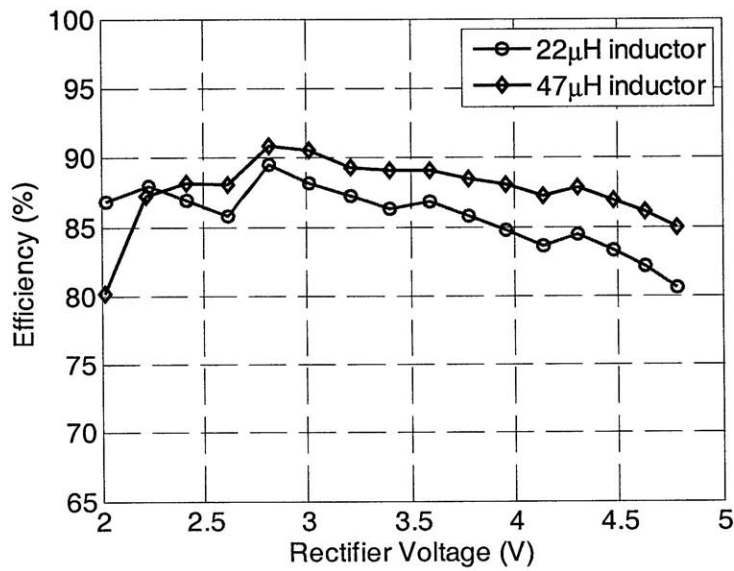
Figure 4-44: Measured efficiency of the buck converter without the shared inductor.

range when a handling a current of only 20μA. At the lower values of V_{RECT}, the efficiency is primarily limited by switching losses and at the higher values, by conduction losses. The inductor sharing approach leads to a compact system with only a small drop of (2-3%)

in efficiency. On connecting the rectifier to the buck DC-DC converter and using a $47\mu H$ inductor, a total output power of $32.5\mu W$ is obtained at the storage capacitor C_{STO}. This includes the loss due to the efficiency of buck and boost regulators and the power consumed by the control circuitry.

4.12   Summary and Conclusions

This chapter has identified problems with existing rectifier schemes in extracting power out of piezoelectric energy harvesters. Mathematical expressions for the power extractable using different rectifier schemes was presented and it matched well with simulated and experimental results. New rectifier designs were presented that can improve the power extracted from piezoelectric harvesters by greater than 4X compared to commonly used full-bridge rectifiers and voltage doublers. In systems where it is prohibitive to use an inductor to improve power output, a switch-only rectifier scheme was proposed that could improve the extracted power by 2X with the help of a simple CMOS switch. The bias-flip rectifier provides further improvement in power extracted but requires the usage of an inductor. In order to minimize the cost and area penalty of this inductor, the inductor used by the bias-flip rectifier was shared efficiently with a multitude of DC-DC converters used within the system. The rectifier designed were integrated with DC-DC converters to provide a complete power management solution that interfaces to the piezoelectric energy harvester on one side and provides suitable voltage levels to the load circuits on the other end. The entire system was controlled digitally providing great flexibility in the control and minimizing the area and power overhead of the control circuits. Parallels can be drawn between the switch-only and bias-flip rectifier schemes presented in this chapter and the switch-only and inductor-based charge recycling schemes used to mitigate bottom-plate losses in switched capacitor DC-DC converters. This supports the notion of how common energy processing constructs can be used in different applications to obtain more efficient solutions.

Chapter 5

Thermoelectric Energy Harvesting Interface Circuit

The previous chapter showed that piezoelectric energy harvesters can be used to deliver 10's of μW of usable output electric power from ambient vibrations. The circuits designed for the piezoelectric energy harvester were not only able to interface well with the harvesting device but also efficiently process the energy obtained out of it to power load circuits. These energy processing circuits were designed to work at ultra-low load power levels. Mechanical vibrations is just one of the different sources of ambient energy that can be harvested. Light and heat energy are the other two main sources which have been widely used to harvest electrical power. On the macro scale,the number of solar panels being installed for both domestic and industrial purposes are increasing steadily to reduce dependence on non-renewable sources of energy. While this is in the scale of providing power to the utility grid, using solar cells to power miniature portable electronic devices on the micro scale [62] [21] [63] is also becoming increasingly popular. Heat energy in the form of temperature differences has been employed on a macro scale in industrial and automotive settings to extract electrical power from heat exhausts [64] [65]. In these systems the presence of large temperature differences near the exhausts presents a suitable medium to harvest 100's of watts of electrical power. Radioisotope thermoelectric generators have long been used in spacecrafts [66] to

power their electronics systems. Here, heat energy is obtained indirectly from the nuclear reaction of the isotopes which is then converted to electrical energy. With respect to portable electronics, the heat generated by humans can be a potential source of energy which can be harvested to power micro scale body-worn devices. Previous studies have shown that harvesting ambient thermal energy through thermoelectric means can supply 100's of μW of available power [67] [24].

A thermoelectric element converts thermal energy in the form of temperature differences into electrical energy and vice-versa. The fundamental physical process involved in thermo-electrics is the Seebeck effect. The Seebeck effect is the generation of an electromotive force within two dissimilar metals when their junctions are maintained at different temperatures. A common application of this principle is the use of thermocouples to measure temperature. For temperature measurements, the electromotive force generated by the thermocouple is countered by an applied voltage so that no current flows. The main differences between using the thermoelectric effect for temperature measurement and power generation is that semiconductor materials are used for power generation instead of metals, and current flows in the generator to produce power. Semiconductor materials have significantly higher See-beck coefficients than metals and hence are more suited to power generation. Thermoelectric power generators have three main advantages: No human intervention is required through-out their lifetime; they are highly reliable and quiet, since there are no moving mechanical parts; and the materials used are environmentally friendly.

A typical thermoelectric device [3] includes multiple n-type and p-type thermoelectric legs sandwiched between two high-thermal-conductivity substrates as shown in Figure 5-1. The n- and p-type legs are electrically connected in series by alternating top and bottom metal contact pads. The Seebeck effect in the n-type material creates a flow of excess electrons from the hot junction to the cold junction. In the p-type material, holes migrate toward the cold side creating a net current flow which is in the same direction as that of the n-type material. The Seebeck coefficient is defined as the change in voltage per degree of temperature gradient.
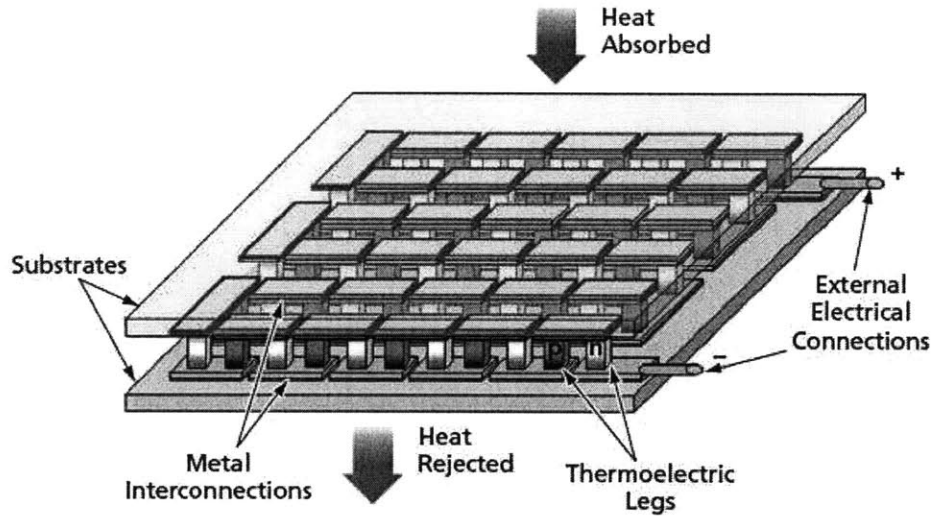
Figure 5-1: A typical thermoelectric generator [3].

$$S = \frac{dV}{dT} volts/K \tag{5.1}$$

Because heat flows from the top to the bottom, all of the thermoelectric legs are thermally connected in parallel. In the cooling mode, an externally applied current forces the heat to flow from the top to the bottom. In the power-generation mode, heat flowing from the top to the bottom drives an electric current through an external load. The voltage obtained at the output of the thermal harvester is proportional to the temperature difference across the thermoelectric element. This poses a major problem while using thermoelectric harvesters powered by human heat because of the small temperature differences available. In most cases, an output voltage of 25 - 50mV is all that can be produced using a 10cm^2 thermal harvester. It is not possible to use this voltage to directly power CMOS circuits. In this chapter, a mechanically assisted startup circuit is presented that helps to interface CMOS circuits directly with the thermal generator without the aid of a battery. Once the startup block provides enough voltage, suitable control strategies are employed to efficiently transfer the maximum power available out of the thermal energy harvester by presenting the correct

impedance levels.
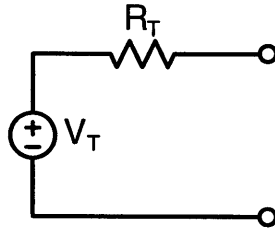
Figure 5-2: Equivalent electrical circuit of a thermoelectric generator.

5.1 Equivalent circuit of a thermoelectric harvester

The thermoelectric generator can be modeled electrically as a voltage source in series with a resistance [68] [69] as shown in Figure 5-2. The open-circuit voltage V_T is proportional to the temperature difference between the hot and cold sides of the thermogenerator and can be given as,

$$V_T = S\Delta T \tag{5.2}$$

where S is the Seebeck coefficient of the thermoelectric generator and ΔT is the temperature difference between the hot and cold sides of the thermoelectric device. Most commercial thermoelectric modules use Bismuth Telluride as the thermoelectric material owing to its high Seebeck coefficient, high electrical and low thermal conductivities. The Seebeck coefficient of n-type Bismuth Telluride is -287μV/K and that of the p-type is 81μV/K. Seebeck coefficients for n-type materials are often expressed as negative values. The low value of the Seebeck coefficient makes it impractical to use just one p- or n- leg by itself to power any device. To boost up the Seebeck coefficient and thereby the output voltage delivered, many p- and n-legs of the material are connected in series as shown in Figure 5-1. The variation of the open-circuit voltage and maximum power extractable from a commercial thermoelectric generator from Tellurex can be seen from Figure 5-3. The figure shows the linear dependence

of the open-circuit voltage on the temperature difference. The Tellurex device has 127 legs connected in series to give an overall Seebeck coefficient of 127 x 0.164 = 23.4mV/K. From measurements, the obtained Seebeck coefficient of the device is 23mV/K by taking the slope of the curve in Figure 5-3(a). The Seebeck coefficients of most commercial thermoelectric harvesters is of the same order. The value of R_T is 5Ω. From Figure 5-2, it can be seen that for a given open-circuit voltage, the maximum power output should be proportional to the square of the voltage. This quadratic relationship is confirmed by the measured results of the maximum power obtained.
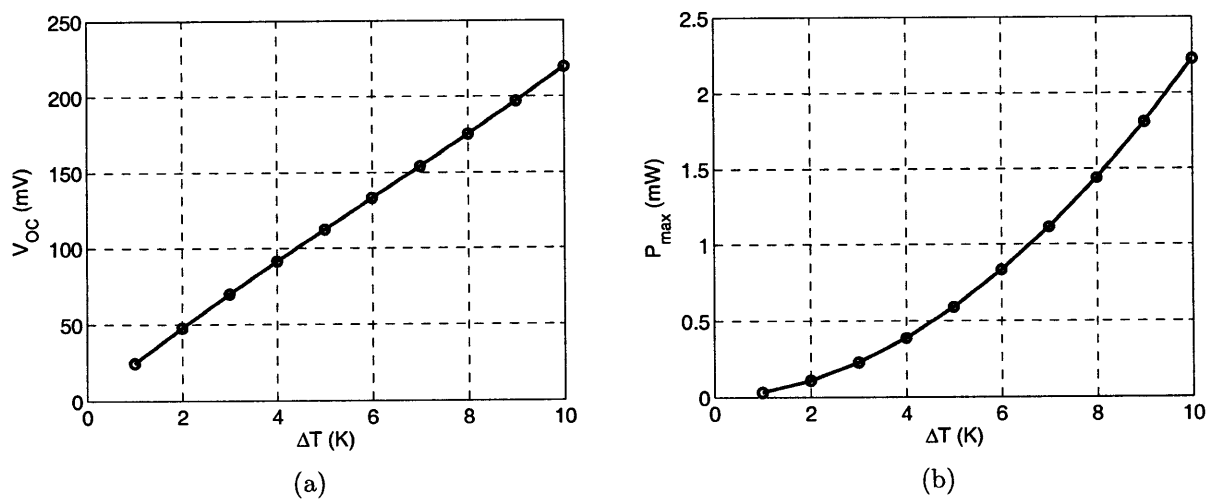
Figure 5-3: (a) Open circuit voltage (b) Maximum power output by a Tellurex thermoelectric energy harvester

Assuming that a temperature difference of 2K is feasible across the thermoelectric device, and that the material of a thermocouple is bismuth telluride, one could obtain an average open-circuit voltage of 0.328mV generated by one thermocouple. Therefore, the total number of thermocouples in the thermoelectric generator must be 3049 to obtain a 1 V output. A 1V output is assumed to be the voltage from which CMOS circuits can be reliably expected to function in the process technology used. In standard thermoelectric modules offered by different companies, one thermocouple usually occupies 7 mm^2 or more. There are two reasons for this relatively large size: 1) these modules are mainly used as thermoelectric coolers, where low electrical resistance is an important factor and 2) the fragility of bismuth

telluride, which limits further miniaturizing [24]. So, to get 1V output, the thermoelectric generator would have to be 3049 x 7mm^2 = 213cm^2 which is impractical for devices worn on the wrist or arm of a person. Only a few commercial products feature thermocouples occupying a smaller area, down to about 1mm^2. Even in this case, the area needed to be occupied to get 1V output is impractical. The low value of Seebeck coefficient of common thermal generators implies that for low temperature difference (<10K), the voltage output by the harvester is very small. This makes it harder to interface conventional CMOS circuits to extract power out of the thermogenerator. Hence, if the harvester is used to extract electrical power from places with very little temperature difference (eg. between the human body and air), the output voltage that can be obtained from the harvester might be 50mV. This is assuming a 2K temperature difference across the thermoelectric generator. The electrical circuit that interfaces with the thermoelectric harvester must be able to operate from this extremely low voltage of ~50mV. Also, to reduce the cost of the overall system and to increase its longevity, batteries must be avoided. This poses a very challenging problem of how to startup from very low voltages and transfer energy to circuits that are powered by the thermoelectric harvester.

5.2   Commonly used startup circuits
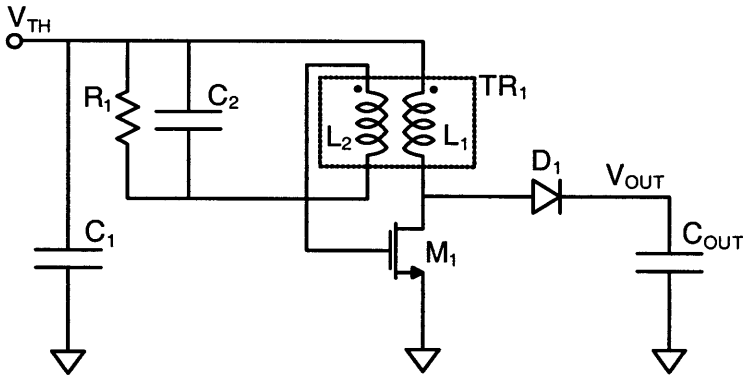
Figure 5-4: A low voltage startup circuit using a transformer and normally ON switch.

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Since thermoelectric harvesters for body-wearable applications output extremely low voltage, startup circuits are essential to generate higher voltages for proper functioning of the interface circuitry. Multiple researchers have worked on this problem and this section lists some of the commonly used startup circuits. Figure 5-4 shows a startup circuit that was proposed a decade ago [68] [70]. The key component in this circuit with coupled inductors is an always-on junction FET (JFET) M_1. If a small voltage is present at the terminal V_{TH} of the voltage converter, current flows through the primary winding L_1 of the transformer TR_1. According to the relationship between voltage and current for an inductor, the current follows an increasing exponential function and the voltage decreases with the same exponential function. The deviation of this current is positive, so a positive voltage is induced in the secondary winding L_2. The positive terminal of the inductor L_2, which is connected to the gate of M_1, is driven to a fixed voltage level by the diode of the JFET M_1. Thus with the positive induction voltage the negative terminal is shifted to a negative voltage level, charging the capacitor C_2 to a negative level. When the current in the primary winding L_1 reaches saturation, the deviation and so the induced voltage in the secondary winding L_2 is zero, producing a drop in the secondary voltage. The sum of the voltage of capacitor C_2 and the secondary winding L_2 becomes negative, making the transistor M_1 to switch off. So the current through the primary inductor is decreasing and a positive voltage is induced in the primary winding L_1, delaying the current decrease. Because the transistor M_1 has a high resistance, the output capacitor C_{OUT} is charged via diode D_1. When the primary current reaches zero, the induced voltage in L_2 becomes zero too and C_2 is discharged by R_1 to the level of the input voltage. Thus the JFET starts conducting again and the operation cycle repeats.

While this circuit is completely electronic and does not need other peripherals to assist startup, it needs a bulky transformer with a huge turns ratio to achieve startup from low voltages. The JFET transistor M_1 needs to be normally ON and supply a large current with 0 V_{GS} and very low V_{DS} ($\sim$25mV). [68] uses an N-channel JFET J105 and a 1:61 turns ratio transformer in its startup circuit. Even with these elements, it is difficult to

achieve startup with this circuit and it is not very well suited to portable applications. [71] proposed using Reed switches and tunnel diodes to assist in the startup operation. The authors were able to demonstrate startup from 200mV. Starting up from even lower voltages is a problem with tunnel diodes, while Reed switches suffer from reliability issues. [72] proposed a startup circuit for fuel cell powered operations which could start from 0.7V. The method proposed uses an external mechanical switch which the person using the device has to manually turn ON every time the device needs to be started. The boost converter circuits presented in [23] [73] [74] use traditional inductor-based or charge pump boost circuits that require atleast 0.6V to startup. In this chapter, a mechanically assisted startup circuit is presented which can startup from as low as 35mV. The startup circuit is integrated with other energy processing circuits to provide a complete power management solution.
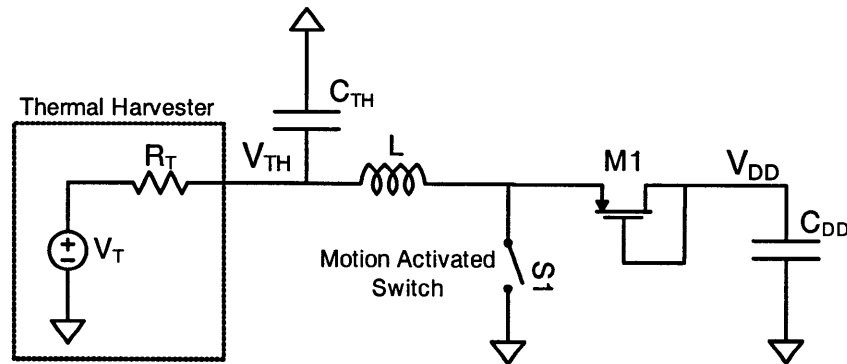
Figure 5-5: A low voltage startup circuit using a mechanically assisted startup switch.

5.3 Mechanically assisted startup circuit

The problem with thermoelectric inputs is that the voltage it outputs for temperature differences normally observed is around 25 - 50mV. It is not possible to operate CMOS switches out of these low voltages to use conventional boosting techniques. The voltage available needs to be close to 1V to suitably operate CMOS switches in the technology used to achieve efficient voltage boosting. Since the interface circuit designed is intended for body-wearable applications, the movement of humans presents small amount of ambient mechanical vibrations.

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These vibrations are put into use in a mechanically assisted startup circuit shown in Figure 5-5. The switch S_1 shown in the figure is a mechanical switch which turns ON and OFF on the application of very small amount of vibration of less than 0.1g in acceleration. The vibrations can be induced when the device is worn on a hand or on the body of a person. When the switch S_1 is ON, the voltage available from the thermoelectric harvester causes current to flow in the inductor L. When the switch turns OFF, the current in the inductor has to find an alternate path to flow. This causes the transistor M_1 which is connected as a diode to turn ON, and the energy flows into the capacitor C_{DD}. If the diode is considered ideal, assuming that there was no initial voltage across C_{DD}, the voltage obtained at C_{DD} at the end of the ON/OFF cycle is

$$V_C(final) = \frac{\sqrt{L/C_{DD}}}{R_T + R_L + R_{SW}} V_T = Q_T V_T \qquad (5.3)$$

where Q_T is the Q-factor of the startup network, R_T is the internal resistance of the thermoelectric harvester, R_L and R_{SW} are the parasitic series resistances of the inductor and the switch. This can be derived by equating the energy stored in the inductor when the switch S_1 is ON to the energy in the capacitor when the inductor current reaches zero. With a 30mV input, Q_T needs to be at least 34 to get more than 1V across C_{DD}. However, the diode formed by M_1 is not ideal and has a voltage drop across it. Hence, Q_T needs to be higher than 34 to get 1V across C_{DD}. In the presence of diode losses, the voltage across the capacitor comes up to

$$V_C(final) = \sqrt{V_D^2 + Q_T^2 V_T^2} - V_D \qquad (5.4)$$

If we assume a V_D of 0.6V, then with a Q_T of 42, the input open circuit voltage needs to be at least 35mV to obtain a 1V output. The value of L used is 22μH and that of C_{DD} is 470pF. The thermal harvester has a resistance of 5Ω, and the parasitic resistances add up to 150mΩ. This gives a Q_T of 42. The voltage gain can be increased by increasing L or decreasing C_{DD}. Increasing L too much increases the size of the system and cost. C_{DD} on the other hand cannot be decreased arbitrarily as it needs to have a moderate amount of

energy to power circuits. Reducing V_D also helps in decreasing the input voltage required for startup. This is however process dependent. Synchronous rectifiers are not possible during startup due to the lack of suitable voltage to turn ON the switches. 35mV of open-circuit voltage corresponds to a temperature difference of 1.5K across the thermoelectric harvester, which should be feasible in body-worn applications.
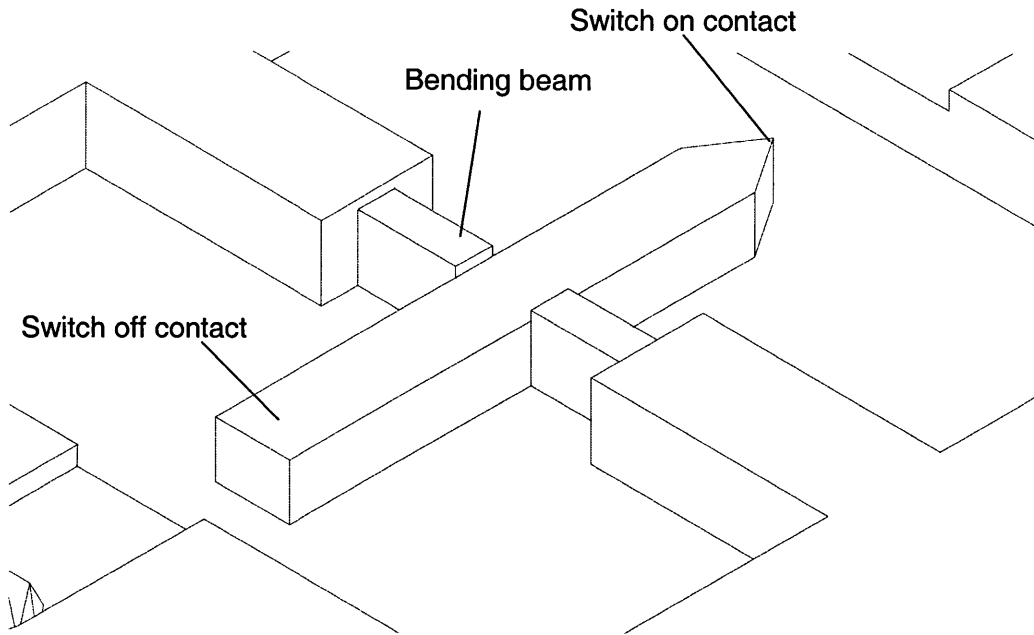
Figure 5-6: Motion activated switch to startup the thermoelectric harvester. Courtesy: Dr. Hanqing Li and Prof. Jeffrey Lang.

The mechanical switch S_1 is designed as a MEMS switch as shown in Figure 5-6. The switch is designed to be motion activated. Any slight motion of the human arm or body causes the bending beam to twist which allows the switch to make contact and break it after a short time. This helps to trigger the startup circuit and build voltage across C_{DD}. The MEMS switch is in fabrication as testing of the thermoelectric harvester is in progress. Hence the results presented in Section 5.8 are obtained using an external mechanical switch controlled by the user.

Once S_1 turns ON and OFF once, the capacitor C_{DD} gets charged to above 1V. After this the switch S_1 is not needed. The voltage across C_{DD} starts off an internal clock generator

block which is used to drive on-chip CMOS switches to help transfer power from V_{TH} to V_{DD}.
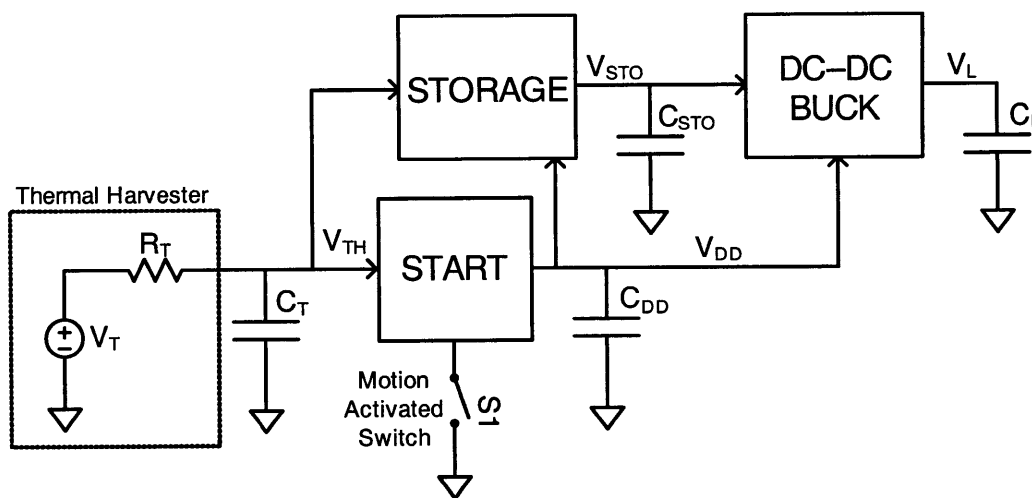
Figure 5-7: Architecture of the thermoelectric energy harvesting system.

5.4 Thermoelectric Energy Harvesting System Architecture

The overall architecture of the thermoelectric energy harvesting system is shown in Figure 5-7. The startup circuit starts the system operation from a completely OFF state where the voltage in all the main capacitors is below usable values. At this point, a mechanical vibration due to human motion triggers switch S_1 which enables the startup block to charge C_{DD} above 1V as explained in the previous section. This triggers an internal clock generator within the start block which powers CMOS switches to help pump in further charge into C_{DD} through the inductor L. This process repeats as long as V_{DD} is less than 1.8V. Once V_{DD} reaches 1.8V, the storage block begins to get activated. This turns on the storage part of the system. The storage capacitor C_{STO} is designed to be much higher than C_{DD}. The storage block shown in Figure 5-12 is necessary to act as a buffer to energy obtained from the thermoelectric harvester. We cannot use the voltage V_{DD} to directly power load circuits

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because by design, the value of C_{DD} is very small. The voltage across C_{DD} would drain very fast on connecting a significant load current across it. When V_{DD} goes above 1.8V, the power from the thermoelectric harvester is diverted towards C_{STO}. This builds up the voltage V_{STO}. The voltage V_{STO} varies depending on the power available from the thermoelectric harvester and the power consumed by the load. Hence, it cannot be used to directly power load circuits. To give a constant voltage to load circuits, a DC-DC converter is used after the storage capacitor to transfer energy to the load at a constant voltage. The DC-DC converter block shown in Figure 5-17 is only activated after V_{STO} goes above 2.4V. V_{DD} is used as the control voltage for both the storage and DC-DC converter blocks. The DC-DC converter is used to regulate V_L to 1.8V. Once, V_L reaches 1.8V, the capacitors C_{DD} and C_L are shorted to improve the energy harvesting efficiency of the thermoelectric harvester. The reason for this is explained in Section 5.7.

5.5 Startup Block and Associated Control

The mechanically assisted startup principle was explained in Section 5.3. It was noted that with the help of the mechanical switch, the voltage across C_{DD} could be raised to 1V and above. Once this happens, the electronics within the the startup block take over. The overall startup circuit is shown in Figure 5-8. The voltage V_{DD} powers the CLKGEN and REFGEN blocks. The voltage reference block shown in Figure 5-9(a) generates the voltage V_{REF} of close to 0.7V which is used as the reference voltage throughout the circuit. It is a simple circuit which makes use of an on-chip P+/N-well diode to generate the reference voltage which stays nearly constant as the input voltage (V_{DD}) changes as shown in Figure 5-9(b). It is not necessary for V_{REF} to be constant across all V_{DD} as comparisons only take place close to when V_{DD} is around 1.8V. The reference generator block consumes 230nA of current from the 1.8V V_{DD} supply. While this block makes sure V_{REF} does not change by much with change in V_{DD}, its regulation with change in temperature is not very good. A more complex bandgap reference circuit [75] would be necessary to keep V_{REF} independent of temperature.

V_{DD} simultaneously powers an internal clock generator block shown in Figure 5-10. The
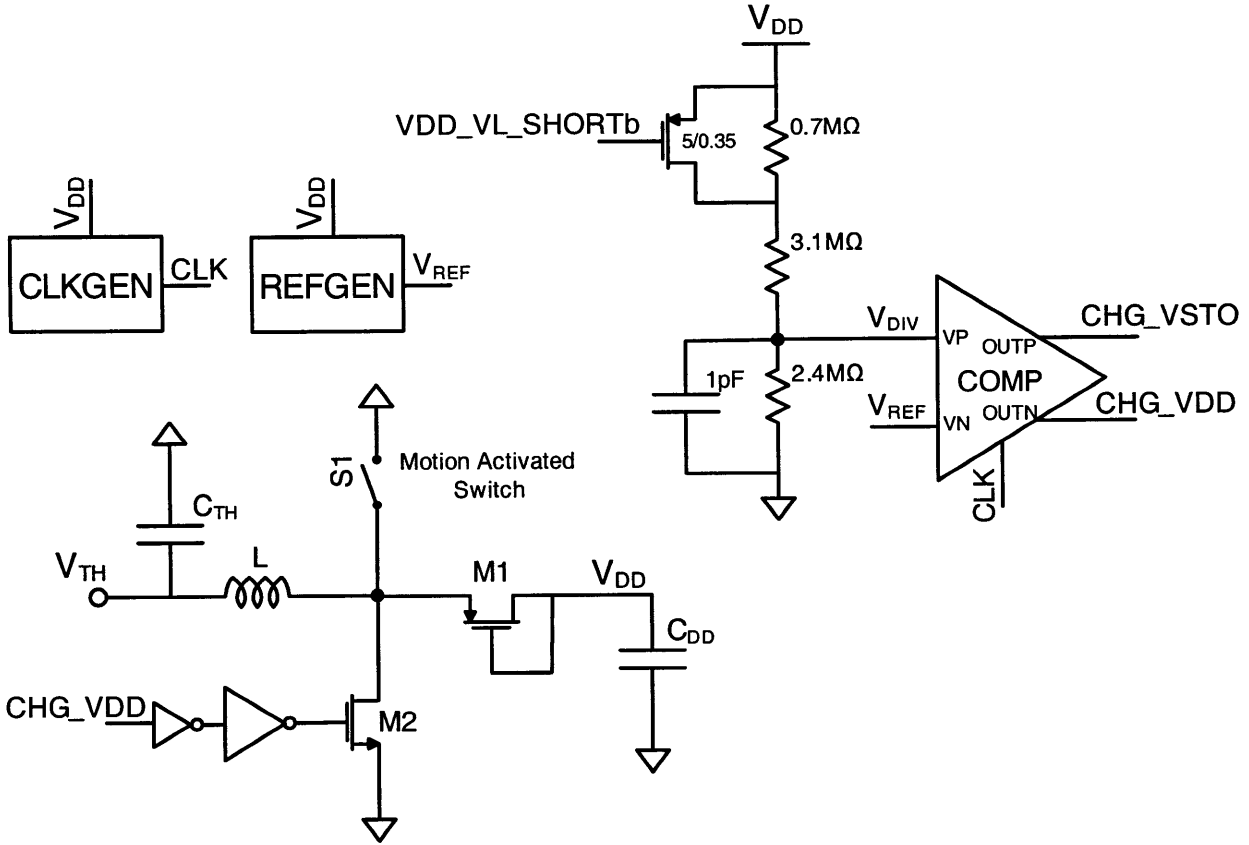
Figure 5-8: Circuits within the startup block.

clock generator consists of multiple delays arranged to form a ring oscillator. The clock frequency is controlled by a 2-bit signal $CLK < 0 : 1 >$. The frequency can be adjusted to correct for process variations and to achieve maximum power transfer as described in Section 5.6.2. An additional signal LOW_FREQ is used to select between the clock signal and a 4X faster version of it. Once V_{DD} is charged to above 1V, the clock generator block turns ON and outputs the CLK signal. This signal is used to clock the comparator shown in Figure 5-8. The comparator is used to compare a divided version of V_{DD} (V_{DIV}) with the reference voltage V_{REF}. The variation of both these voltages with V_{DD} is shown in Figure 5-9(b). For the moment, assume that the signal VDD_VL_SHORTb is held high. The function of this signal is explained in Section 5.7. As long as V_{DD} is less than 1.8V, the CHG_VDD signal is triggered which is used to transfer energy from the thermal input on to

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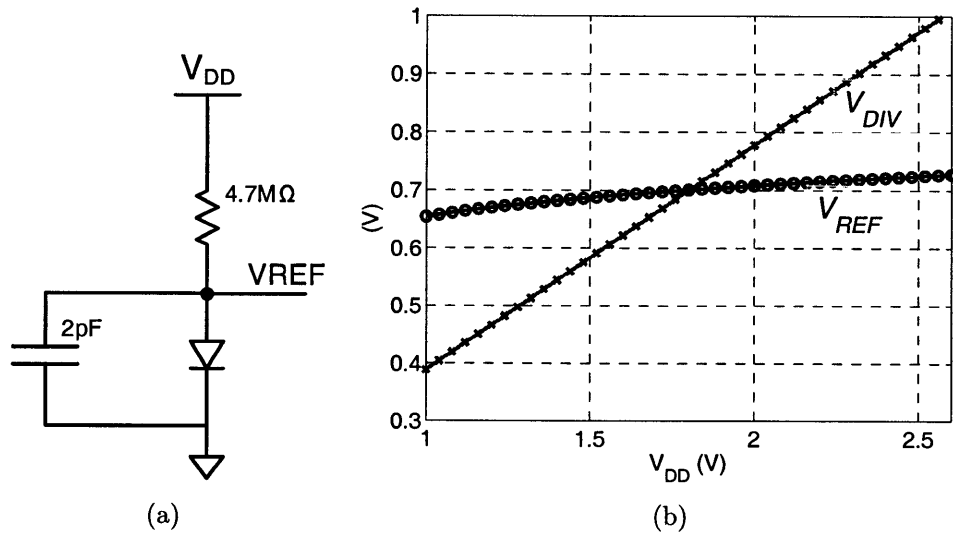
Figure 5-9: (a) Reference voltage generator (b) Variation in the reference voltage with change in V_{DD}.

C_{DD}. When CHG_VDD goes high, the CMOS switch M_2 turns ON and causes current to flow in the inductor L. CHG_VDD going low turns the switch M_2 OFF thereby turning on the diode M_1 and charging C_{DD}. This process repeats whenever V_{DD} falls below 1.8V. The comparator is designed very similar to the discrete-time comparator block shown in Figure 4-28 and described in Section 4.7. The only difference is that 3.3V devices are used in the design of this comparator as V_{DD} is designed to be much below 3.3V.
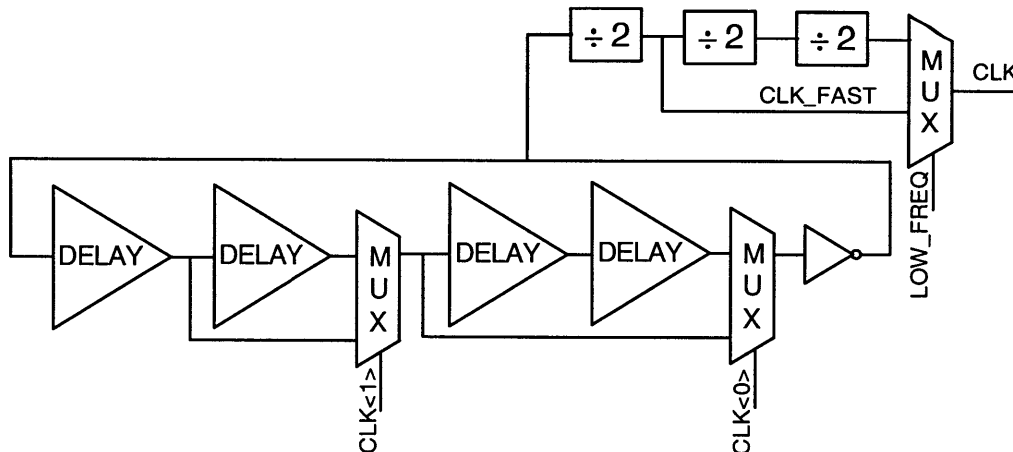
Figure 5-10: Internal clock generator block used to provide the clock signal to circuits.

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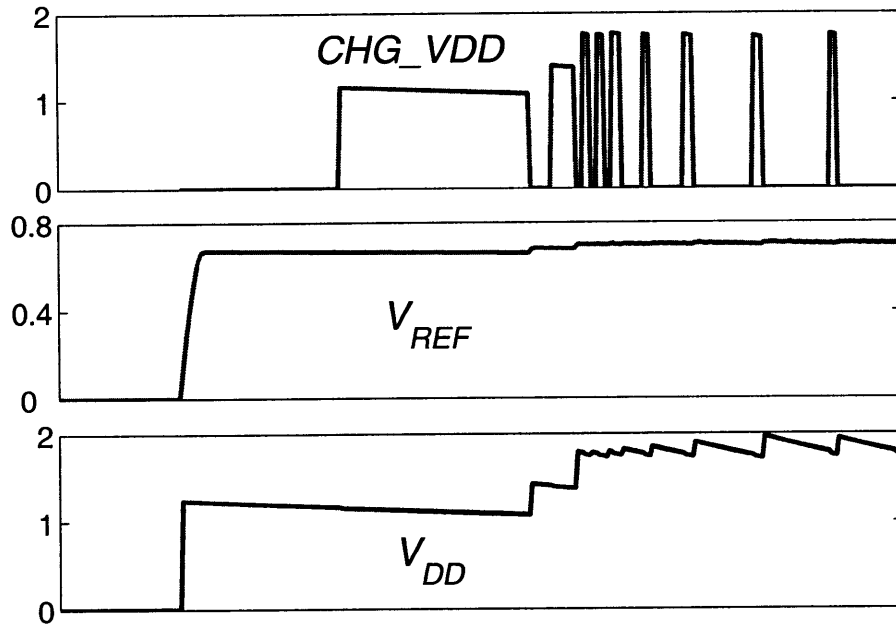
Figure 5-11: Simulated waveforms showing the functioning of the startup block.

Figure 5-11 shows simulated voltage waveforms of the startup block in operation. The moment the mechanical switch S_1 turns OFF, V_{DD} rises to above 1V. This starts up the reference voltage block where V_{REF} rises close to 0.7V. The clock generator block together with the comparator is also enabled and this makes the CHG_VDD signal go high whenever V_{DD} is less than 1.8V at the rising edge of the CLK signal. The V_{DD} signal is regulated to 1.8V by using ON-OFF control of the comparator. The ripple on the V_{DD} supply is high due to the low value of C_{DD}.

5.6 Storage Block

Any power delivery system where the rate of flow of energy into and out of the system are different and variable over long periods of time needs an intermediate storage unit to act as

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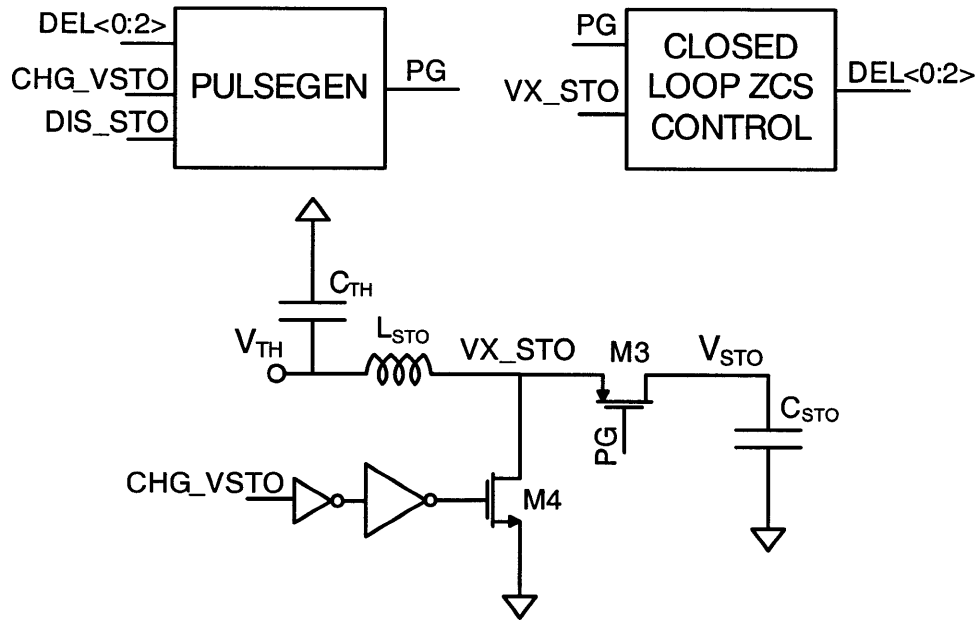
Figure 5-12: Storage circuit to transfer energy from the thermal harvester to the storage capacitor C_{STO}.

a buffer to efficiently use the energy available. In the case of the thermoelectric harvester, it is prudent to extract the energy available from the thermal harvester irrespective of whether the load circuit needs it at that point of time or not. This excess energy can be stored and used at a later time when the load demands increase. A storage block that acts as a buffer needs a large amount of capacitance to smoothen the instantaneous power spurts. The storage block shown in Figure 5-12 is used as the buffer in the thermoelectric energy harvesting interface circuit. The power flow path from the thermal harvester to the storage capacitor C_{STO} is similar to that in the startup block. A mechanical switch is not necessary in the storage block because by the time the storage block is activated, there is enough energy across C_{DD} to power the electronics. The storage block is activated when V_{DD} goes above 1.8V. During the rising edge of a CLK signal, if the comparator in Figure 5-8 senses that V_{DD} is greater than 1.8V, the CHG_VSTO signal goes high, which turns on transistor M_4 of the storage block. This causes current to flow in the inductor L_{STO}. Once CHG_VSTO goes low, the switch M_4 turns OFF. Unlike the start block, the switch M_3 in the storage block is

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not configured as a diode. The switch is turned ON strongly using the PG signal for better efficiency. This is possible with the storage block because, by the time the storage block is activated, there is enough voltage across C_{DD} to actively turn-ON CMOS switches. This configuration essentially looks like the boost converter described in Section 4.8. The switch M_4 needs to be ON long enough for the current in L_{STO} to reach zero. It should then turn OFF. The zero-current switching block shown in Figure 5-12 together with the PULSEGEN block takes care of the timing and width of the PG pulse to achieve zero-current switching of the inductor current.
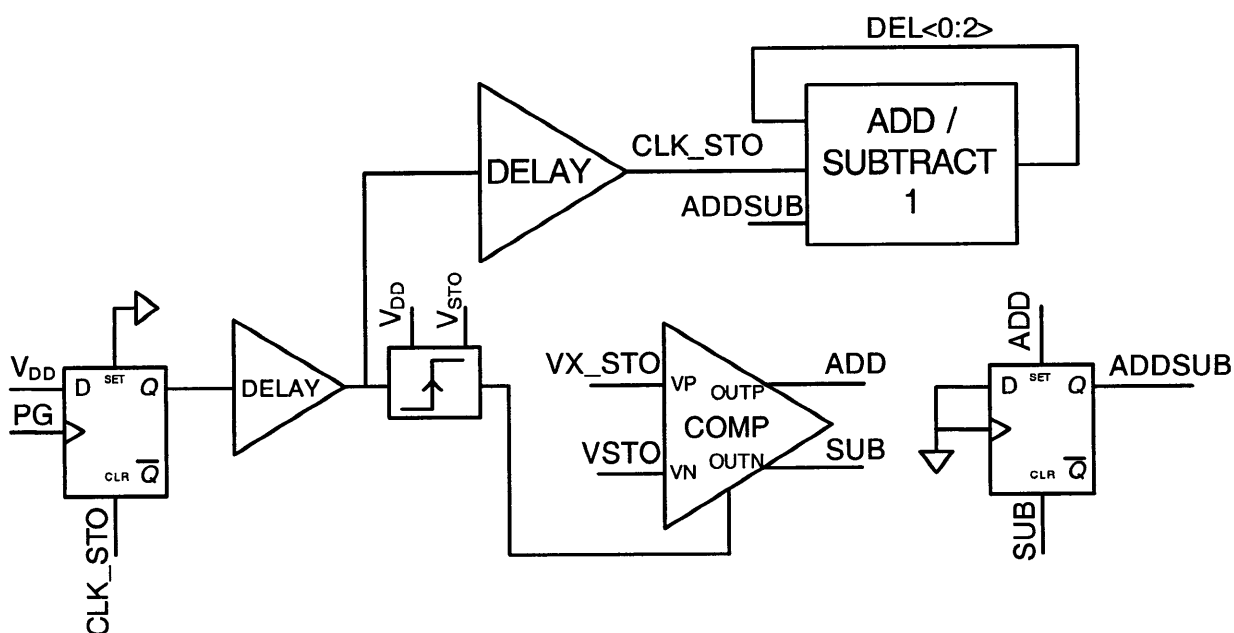
Figure 5-13: Closed-loop zero current switching control block.

5.6.1 Closed-loop zero-current switching control

To achieve zero-current switching (ZCS) of the current in inductor L_{STO}, the time for which the switch M_4 is ON (τ_N) is related to the time for which the switch M_3 is ON (τ_P) by

$$\frac{\tau_P}{\tau_N} = \frac{V_{TH}}{V_{STO} - V_{TH}} \tag{5.5}$$

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In this relation, both the voltages V_{TH} and V_{STO} are variable. This is in contrast to the relations given by Equation 4.39 and Equation 4.41 for the DC-DC buck and boost converters designed for the piezoelectric energy harvesting system. There, atleast one of the voltages at the ends of the inductor was fixed. This made it possible to use the open-loop approximate zero-current switching technique described in Section 4.7. This luxury is not available for the boost converter designed as part of the storage block. Hence, to achieve ZCS, closed-loop control is employed in this design. Figure 5-13 shows the closed-loop control block. The goal of this block is to increase or decrease the pulse width of PG to achieve ZCS of the inductor current. The time for which the NMOS transistor M_4 is ON is fixed by setting it to be equal to the pulse width of the CHG_VSTO signal, which is one-half the time period of the CLK signal. To achieve ZCS, the width of PG (τ_P) needs to be equal to that given by Equation 5.5. This is achieved by observing the voltage at the node VX_STO immediately after the switch M_3 is turned OFF. If the switch M_3 is turned OFF too quick, i.e. if the pulse width τ_P is lower than that required, the remaining inductor current in L_{STO} turns ON the parasitic diode across M_3. This forces the voltage at VX_STO to go above V_{STO}. On the other hand, if the switch M_3 is turned OFF too late, the inductor current reverses direction. This drains the parasitic capacitor on the drain node first before turning ON the parasitic diode across M_4. This forces the voltage VX_STO to go below V_{STO} first and eventually to below zero if τ_P is too large. Thus, by comparing VX_STO with V_{STO}, we can determine whether the pulse width τ_P is larger or smaller than necessary. This is precisely what the comparator in Figure 5-13 detects. The comparison takes place a fixed delay after the rising edge of PG. Depending on whether VX_STO is higher or lower than V_{STO}, either the ADD or SUB pulse goes high. Based on this, the 3-bit delay signal $DEL < 0 : 2 >$ is either incremented or decremented by 1.

This 3-bit delay signal controls the PULSEGEN block which provides the PG signal as shown in Figure 5-14. The PG pulse is generated during the falling edge of CHG_VSTO. The width of the PG pulse is controlled using $DEL < 0 : 2 >$. The delay line shown is tapered such that $\tau_1 < \tau_2 < ... < \tau_8$. This helps to have finer control of the pulse width in the

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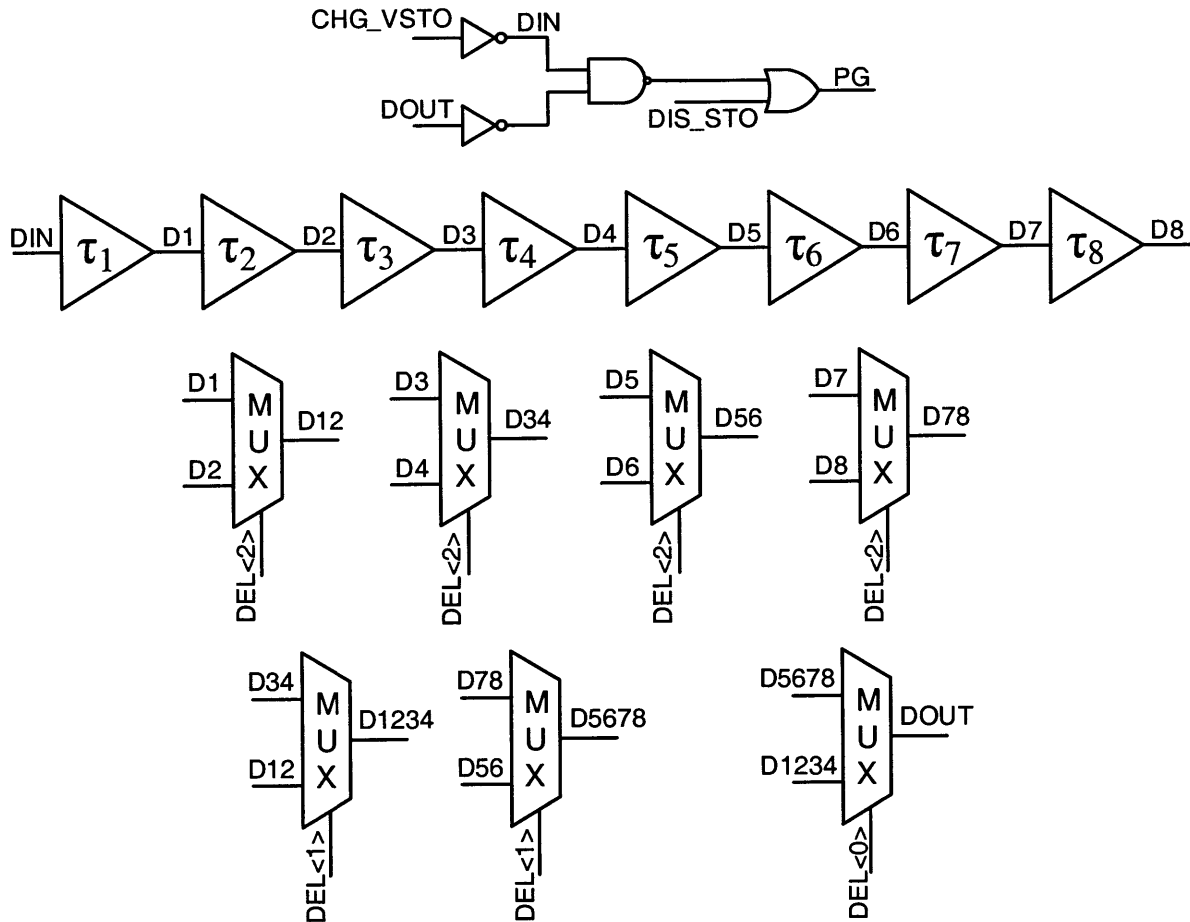
Figure 5-14: Pulse generator used to turn on the synchronous switch in the storage block.

lower order bits and coarser control in the higher order bits. If the delay line is kept uniform, then the resolution of the delay line affects the efficiency of the boost converter much more when the width of PG is small. To avoid this, the delay line is made tapered to keep the percentage increase of the delay almost constant. The DIS_STO signal is used to disable the pulse generator block. The pulse generator block is disabled till V_{STO} reaches 1.8V. This is because at low values of V_{STO}, the switch M_3 cannot be turned ON strong enough. When the pulse generator block is disabled, the signal PG is at V_{STO}. This makes the switch M_3 to behave like a diode and V_{STO} gets charged through the diode M_3. Figure 5-15 shows the circuit that is used to disable the pulse generator block. It consists of a comparator which compares V_{STO} with 1.8V and when found to be lower, makes the DIS_STO signal go high.

Once V_{STO} goes above 1.8V, the DIS_STO signal is brought low, and the pulse generator block behaves normally.
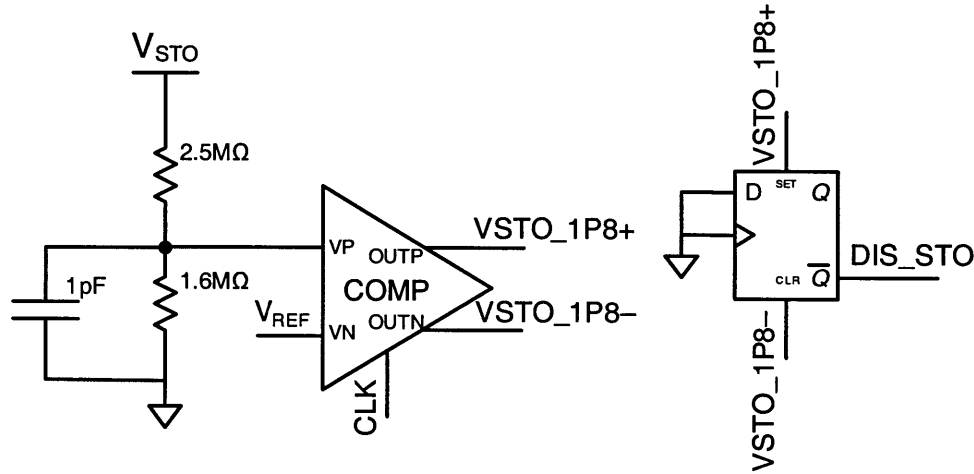
Figure 5-15: Circuit to disable the pulse generation part of the storage block.

5.6.2 Maximum Power Extraction Methodology

The description till now has been about how to startup the thermal energy harvesting circuit and to transfer power from the harvester on to the storage capacitor. No mention has been made about the amount of power being transferred. The maximum power that can be obtained from the thermoelectric harvester shown in Figure 5-2 can be given by

$$P_{max} = \frac{V_T^2}{4R_T} \tag{5.6}$$

This follows directly from the maximum power transfer theory. To get this maximum power, the load circuit following the thermoelectric harvester needs to present an impedance equal to R_T. Equivalently, we can extract maximum power available if the output voltage of the harvester (V_{TH}) is regulated close to $V_T/2$.

This is achieved with the help of a control strategy described here. Consider Figure 5-16 where the switch M_4 is constantly switched ON and OFF with the help of the CHG_VDD signal. The CHG_VDD signal is generated by a comparator clocked at a frequency f_s. Thus,
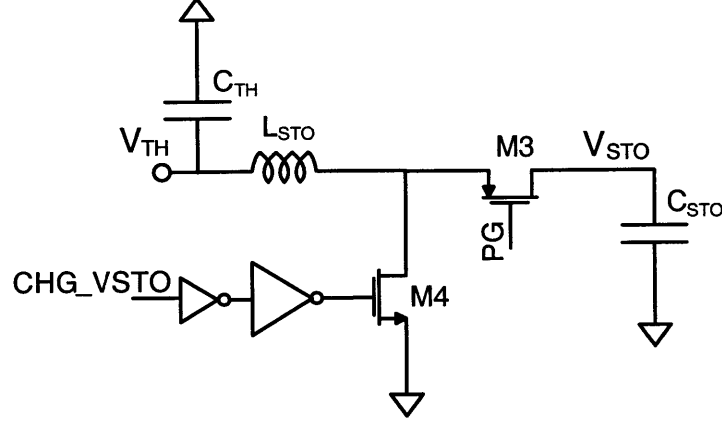
Figure 5-16: Circuit to explain maximum power extraction methodology.

if the comparator triggers CHG_VDD at every cycle, then the frequency of CHG_VDD is also f_s. Let the pulse width of the ON-time of CHG_VDD be τ_N. This means that the time for which M_4 is ON every cycle is τ_N. In steady state V_{STO} is regulated to be much higher than V_{TH}. Thus, the time for which the switch M_3 is ON is very small compared to τ_N. This can be seen from Equation 5.5. This being the case, the energy delivered to C_{STO} every cycle assuming ideal blocks can be approximately given by

$$E_{cycle} = \frac{V_{TH}^2 \tau_N^2}{2L_{STO}} \tag{5.7}$$

This repeats every cycle and hence the power delivered to C_{STO} is given by

$$P_{STO} = E_{cycle} \cdot f_s = \frac{V_{TH}^2 \tau_N^2}{2L_{STO}} f_s \tag{5.8}$$

In steady state, the power delivered to C_{STO} should be equal to the power extracted from the thermoelectric harvester. Hence, if we want to extract the maximum power, equating Equation 5.6 and Equation 5.8 gives the following

$$\frac{V_{TH}^2}{R_T} = \frac{V_{TH}^2 \tau_N^2}{2L_{STO}} f_s \Rightarrow \tau_N^2 f_s = \frac{2L_{STO}}{R_T} \tag{5.9}$$

If τ_N is designed to be one half the period of the CLK signal, then $\tau_N = 1/2f_s$. This

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gives the relation of f_s for maximum power extraction to be

$$f_s = \frac{R_T}{8L_{STO}} \tag{5.10}$$

Thus, if we can design f_s suitably for a given L and R_T, we can extract the maximum power from the thermoelectric harvester. For an R_T of 5Ω and an L_{STO} of 22μH, f_s should be 28.4kHz. The clock generator block shown in Figure 5-10 is designed to output a CLK with the above mentioned frequency in the nominal state. The extra bits of control is provided in the clock generator block not only to account for process variations but also to adjust the clock frequency with change in R_T and L_{STO}. A major advantage of this method is that once a suitable thermoelectric harvester and inductor have been picked, the clock frequency can be set to achieve maximum power transfer. This is a simple elegant way to get the maximum power out, instead of using the more complex maximum power tracking loops. Also, it has the additional advantage that even when V_T moves around due to temperature variations, since Equation 5.10 is independent of V_T, the circuit will still settle itself at the maximum power point.

5.7 DC-DC Buck Converter

The final block of the thermoelectric energy harvesting system is the DC-DC buck converter. The voltage V_{STO} at the output of the storage block cannot be used to power circuits directly because it is unregulated and can vary with change in input and output power. To provide a clean regulated supply to the load circuits, a DC-DC converter is necessary. The architecture of the DC-DC buck converter is shown in Figure 5-17. The design is similar to that of the DC-DC buck converter employed in the piezoelectric energy harvester but for a few key differences. This buck converter is a more conventional one and is used to regulate the output voltage V_L as opposed to the piezoelectric buck converter which regulated its input voltage V_{RECT}. The second difference is that the thermoelectric buck converter employs a closed-loop control technique to do zero-current switching of the inductor current. The buck
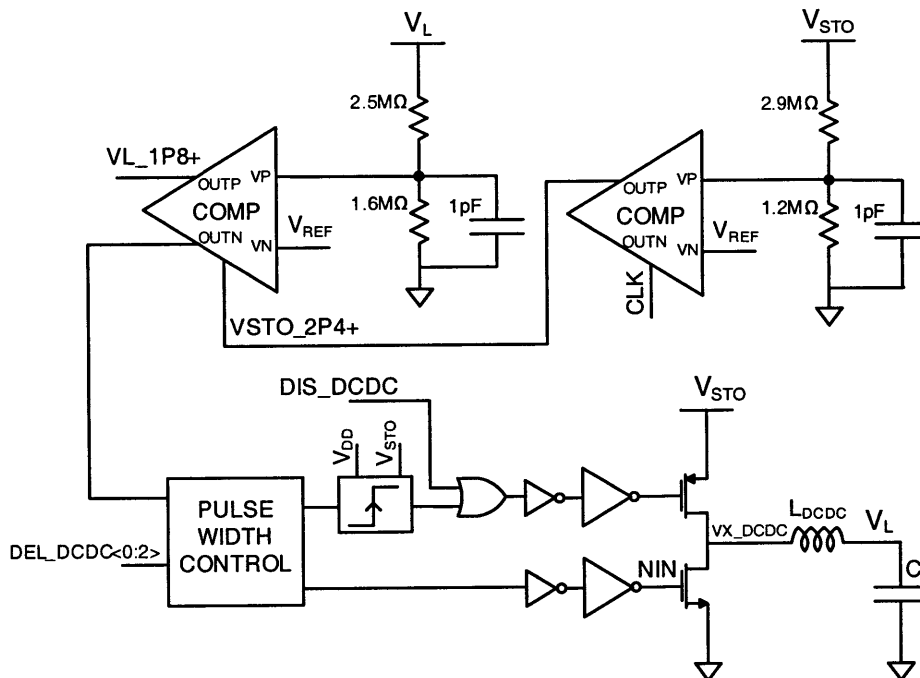
Figure 5-17: Architecture of the DC-DC Converter.

converter employs pulse-frequency modulation mode of control to regulate V_L. There are two comparators in Figure 5-17. Both the comparator's are clocked and are similar to the one described in Section 5.5. The first comparator's output feeds the clock to the second comparator. The DC-DC converter is designed to be activated only when V_{STO} is above 2.4V. The first comparator does this function by comparing a suitably divided version of V_{STO} with the reference voltage V_{REF}. Only when V_{STO} goes above 2.4V does the signal $VSTO\_2P4+$ get activated. This essentially gates the clock to the second comparator when V_{STO} is less than 2.4V thereby disabling the DC-DC buck converter. The overhead of using multiple comparators is not too large. The area occupied by the comparator itself is minuscule. Also, the power consumed by them is much less than $1\mu W$. The only disadvantage is the use of large resistors to get the voltages to be compared close to the reference voltage. These resistors need to be large as they consume quiescent current.

The second comparator is used to regulate V_L to 1.8V. The value of the output voltage is set to 1.8V in this design, but this can be easily changed by changing the resistances of
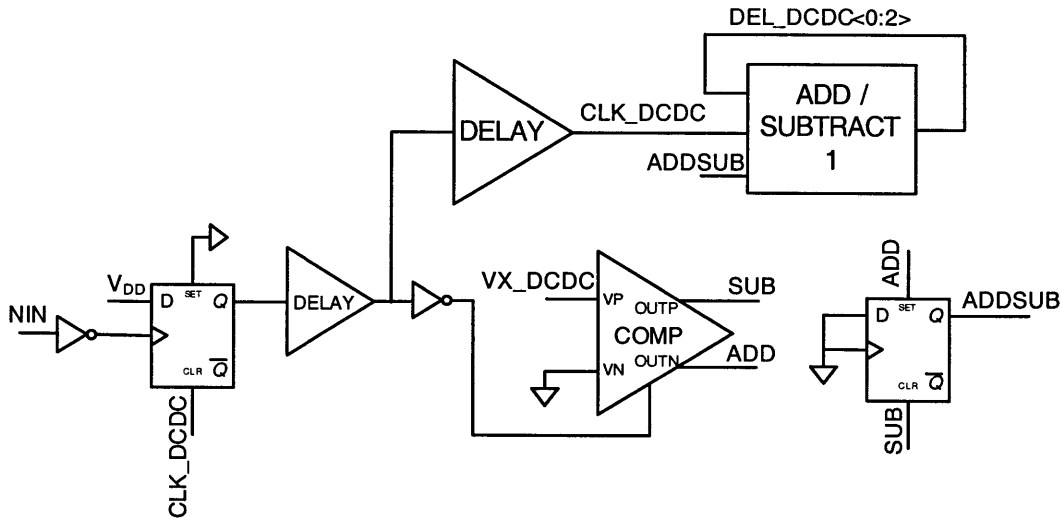
Figure 5-18: Closed-loop control block to achieve zero-current switching of the DC-DC buck converter.

the ladder network of the second comparator as was done in the buck converter design for the piezoelectric energy harvester. When V_L falls below 1.8V, the comparator sends a pulse to the pulse-width control block which turns ON the power transistors to transfer charge from V_{STO} to V_L. The pulse-width control block employs closed-loop control to achieve ZCS similar to the methodology described in Section 5.6.1. However, since the control here is for a buck converter rather than a boost converter, the ZCS block is slightly different as shown in Figure 5-18. Here, the voltage at the drain nodes of the power transistors (VX_DCDC) is compared to ground instead of VX_STO. The comparison takes place immediately after the NMOS power transistor is turned OFF. If the NMOS transistor is turned OFF too quick, the remaining inductor current in L_{STO} turns ON the parasitic diode across the NMOS transistor. This forces the voltage at VX_DCDC to fall to a diode drop below ground. On the other hand, if the NMOS transistor is turned OFF too late, the inductor current reverses direction and hence the parasitic diode across the PMOS transistor turns ON after the parasitic capacitance at the drain node gets charged to V_{STO}. This forces the voltage VX_DCDC to go above V_{STO}. Thus, by comparing VX_DCDC with ground, we can determine whether the NMOS pulse-width is larger or smaller than necessary. This is

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precisely what the comparator in Figure 5-18 detects. The comparison takes place a fixed delay after the falling edge of NIN. Depending on whether VX_DCDC is higher or lower than ground, either the SUB or ADD pulse goes high. Based on this, the 3-bit delay signal $DEL\_DCDC < 0 : 2 >$ is either incremented or decremented by 1.
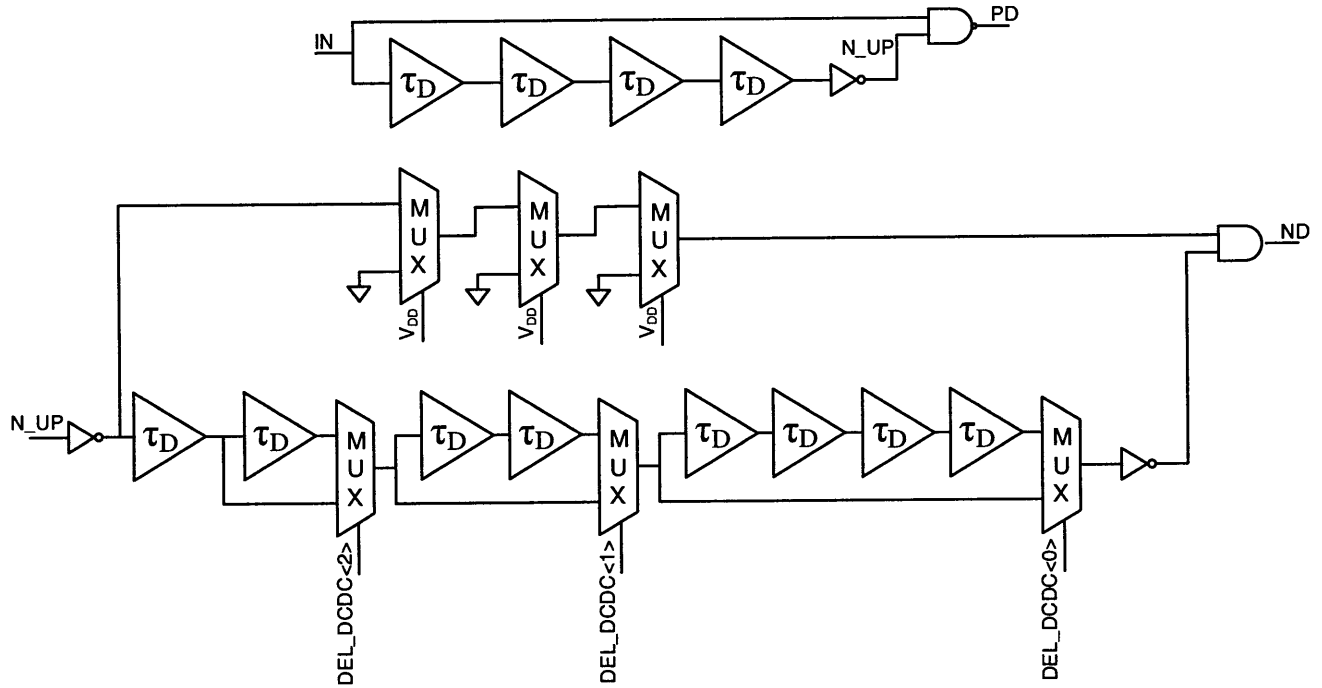
Figure 5-19: Pulse generator used to turn on the synchronous switch in the storage block.

This 3-bit delay signal controls a pulse generator block which provides the drive signals for the PMOS and NMOS power transistors. The PMOS ON-time is set to a fixed value. The rising edge of the PMOS pulse triggers the NMOS pulse generator. The width of the NMOS pulse is controlled by the 3-bit signal $DEL\_DCDC < 0 : 2 >$ to achieve ZCS. Once V_{DD} reaches 1.8V, the VL_1P8+ signal shown in Figure 5-17 goes high. This is used to short the capacitors C_L and C_{DD} as shown in Figure 5-20. This is done because once V_{DD} and V_L are shorted, the power to V_{DD} flows through the storage block and not directly from the thermal harvester. Hence, the time sharing of the thermal input between the start and storage blocks can be avoided. This happens because once V_L and V_{DD} are just above 1.8V, the CHG_VDD signal in Figure 5-8 never gets triggered. This helps to keep the storage

circuit active all the time instead of time-sharing it with the start circuit. Also, since now the storage circuit will switch at a constant frequency determined by the maximum power transfer considerations described in Section 5.6.2, optimal operation of the thermoelectric energy harvester circuit is possible. This also helps in the overall efficiency of the system because transferring power to V_{DD} through the startup block is inefficient owing to using a free-wheeling diode. The shorting is disabled once the voltage V_{DD} falls below 1.6V.
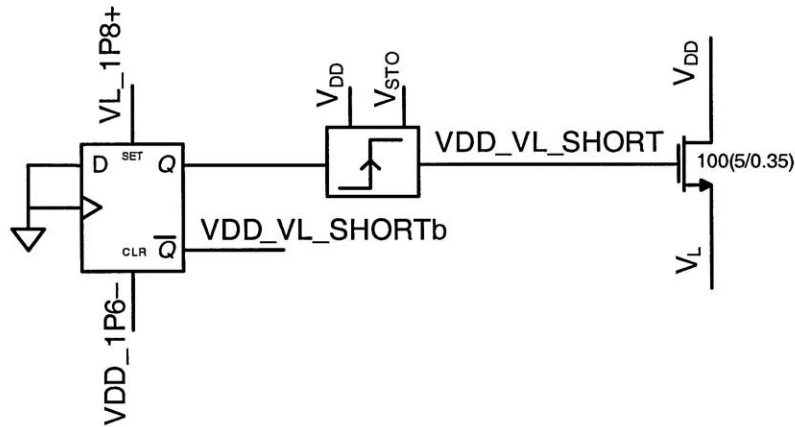
Figure 5-20: Circuit used to short V_{DD} and V_L.
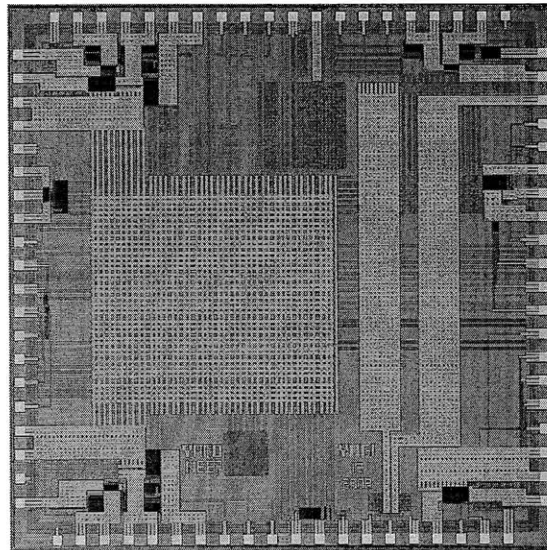
Figure 5-21: Die photo of the thermoelectric energy harvesting chip.

5.8 Measurement Results

The thermoelectric energy harvester interface circuit was implemented in a $0.35\mu m$ CMOS process. Figure 5-21 shows the die photo of the test chip. The active area of the startup and storage circuitry together with the DC-DC converter is 0.84 mm^2. The majority of this area is occupied by the resistors of the various reference ladders employed in this design.
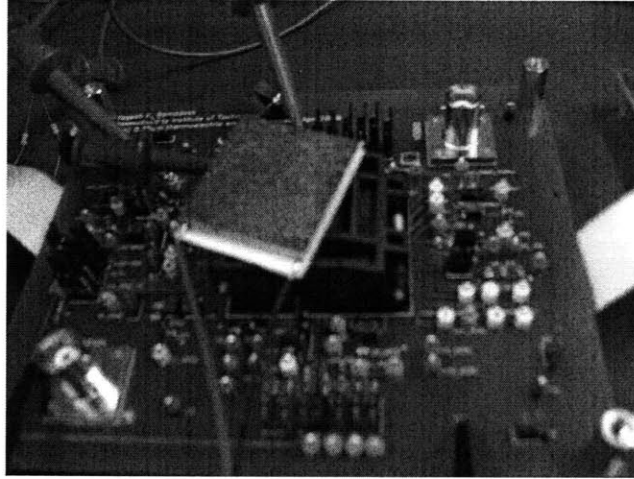
Figure 5-22: Experimental setup of the thermoelectric energy harvester.

A commercially available thermoelectric device (model G1-1.0-127-1.27) [76] from Tellurex was used to perform certain measurements reported in this section. For other measurements a voltage source with a series resistance was used as the equivalent to replace the thermoelectric harvester (see Figure 5-2). The experimental setup is shown in Figure 5-22.

The values of the various off-chip passives used in the design are listed in Table 5.1. Figure 5-23 shows the measured output of the reference voltage generator and how it compares to simulated values. The simple structure used for generating the reference voltage (see Figure 5-9(a)) does a good job of keeping the reference voltage almost constant with change in V_{DD}. However, the variations in diode strength leads to a lower V_{REF} (660mV) compared to simulated values. The difference in reference voltages leads the comparator to trip when the voltages being compared are 95% of their intended values. Thus, V_{DD} and V_L settle down to 1.7V instead of 1.8V. A more complex bandgap reference circuit [75] would be necessary

Table 5.1: Component values used in the thermoelectric energy harvester circuit

Component	Value
C_T	10μF
C_{DD}	470pF
C_{STO}	100nF
C_L	100nF
L_{START}	22μH
L_{STO}	22μH
L_{DCDC}	4.7μH
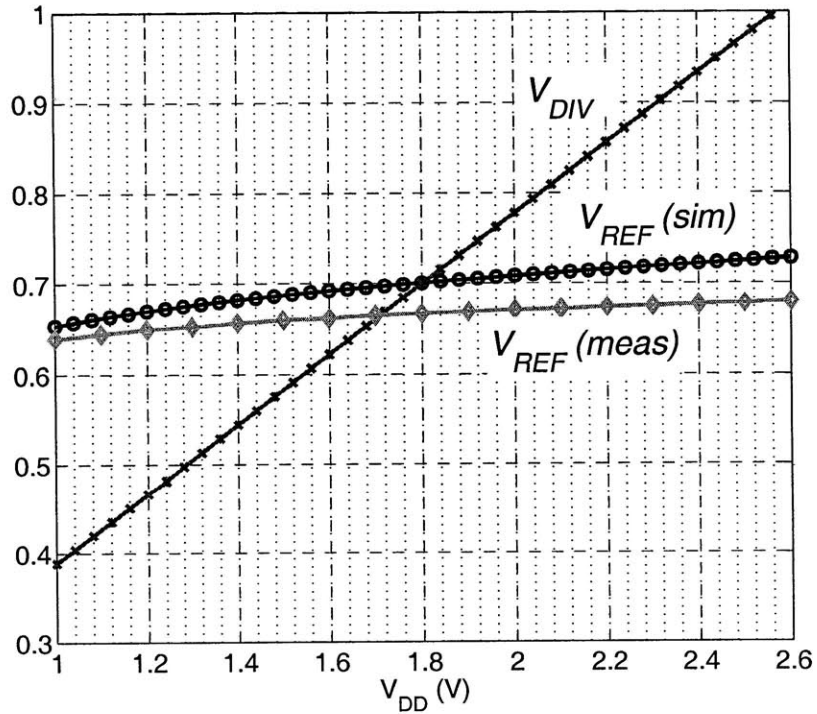
Figure 5-23: Comparison of the simulated and measured outputs of the reference voltage generator.

to keep V_{REF} independent of process variations and temperature changes.

Figure 5-24 shows oscilloscope waveforms of the different voltages in the thermoelectric

Figure 5-24: Measured waveforms of the different voltages of the thermoelectric energy harvesting circuit during startup for (a) 100mV input voltage (b) 50mV input voltage.

energy harvesting circuit for 2 different values of the input open-circuit voltage. This measurement was done with a voltage source in series with a 5Ω resistance. No external clocks or voltage references were used for the measurements. All these were internally generated on-chip using techniques described earlier in the chapter. For the 100mV input case shown in Figure 5-24(a), the mechanically assisted startup provides close to 1V which then turns ON the start block to boost up V_{DD} to above 1.7V. Once V_{DD} goes above 1.7V, the storage block is enabled as seen by the rise in V_{STO}. The start block keep V_{DD} close to 1.7V while powering up the storage block. Only after V_{STO} reaches 2.3V is the DC-DC buck converter block enabled to power V_L. While V_L is getting powered, the voltage V_{STO} stays almost constant at 2.3V. Once V_L reaches 1.7V, the capacitors C_L and C_{DD} are shorted together. From this point on, both V_{DD} and V_L have overlapping waveforms. The V_{DD} and V_L waveforms are staggered a bit vertically in the oscilloscope plot to let the reader see both the waveforms. Else, they lie on top of each other. After V_L reaches 1.7V, V_{STO} begins to rise further till the input power just matches the power consumed by the start and DC-DC blocks. The ripple voltage on V_{DD} is very high initially due to the small value of C_{DD}. The ripple is much reduced once V_L reaches 1.7V at which point V_{DD} and V_L are shorted. With the 50mV

input, the startup and other processes are similar. The circuit takes a longer time to settle down due to the smaller amount of power available from the thermal harvester. This is also why V_{STO} settles to a lower voltage with the 50mV input.

(a)   (b)
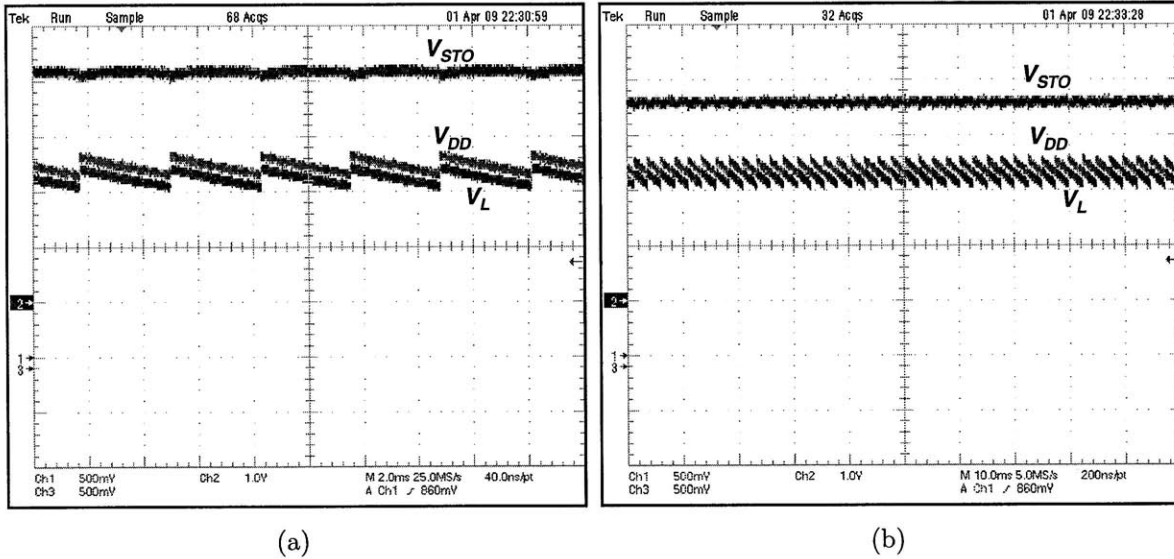
Figure 5-25: Measured waveforms of the different voltages of the thermoelectric energy harvesting circuit during steady state operation for (a) 100mV input voltage (b) 50mV input voltage.

Figure 5-25 shows the waveforms of the different voltages in the thermal harvester circuit at steady state. It can be seen that V_{DD} and V_L each have the same voltage since they are shorted internally. The waveforms for V_{DD} and V_L are typical of pulse frequency modulated, discontinuous conduction mode control. V_{STO} for the 50mV input case settles at a lower value compared to the 100mV input case.

Figure 5-26 shows oscilloscope waveforms of the different voltages in the thermoelectric energy harvesting circuit when powered through the thermoelectric generator attached to the wrist of a person. A temperature difference of 3K was observed between the 2 sides of the thermoelectric harvester when this measurement was performed.

Figure 5-27 (a) shows the measured power obtained at the output of the DC-DC converter as the input voltage of the thermoelectric harvester is changed. This measurement was done with a 5Ω thermal resistance. The only external components used are the inductors and

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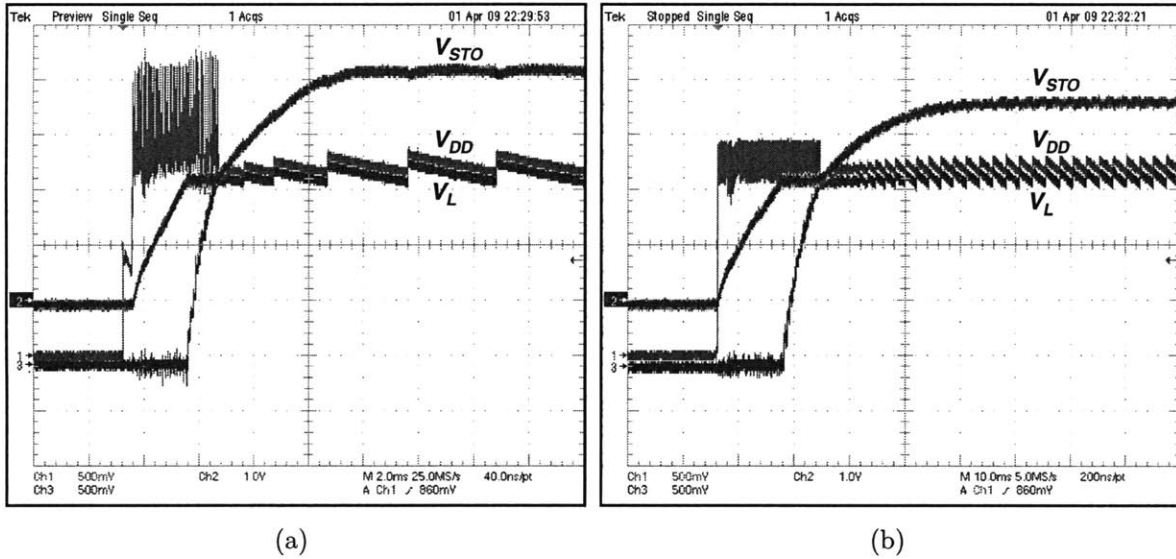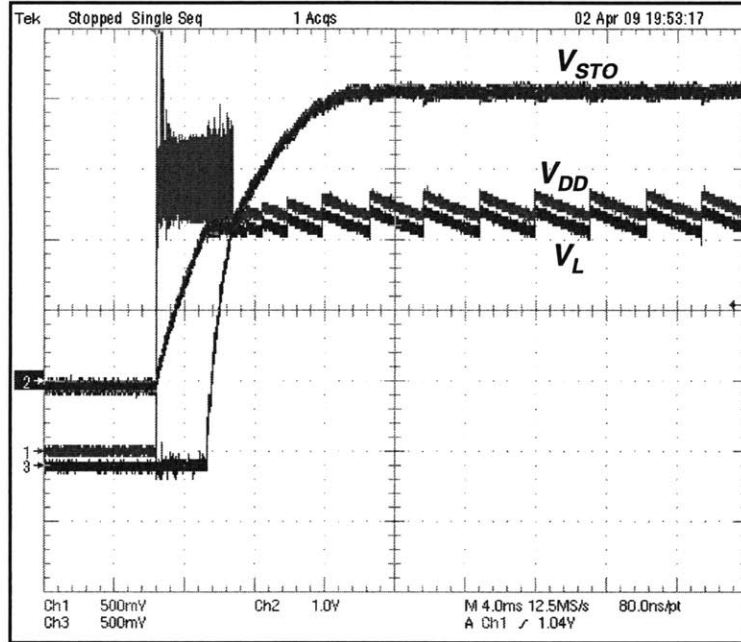Figure 5-26: Measured waveforms of the different voltages of the thermoelectric energy harvesting circuit during startup when powered by human heat harvested using a Tellurex thermoelectric generator.
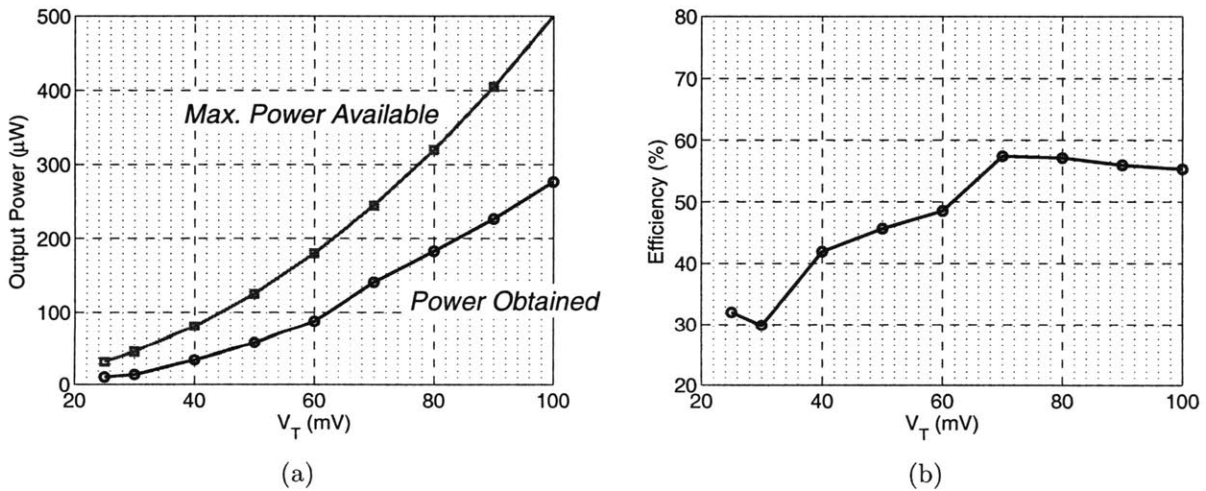
Figure 5-27: (a) Measured electrical power output by the thermoelectric energy harvester with change in input voltage, (b) Overall end-to-end efficiency of the energy transfer.

capacitors of the start, storage and DC-DC blocks along with the thermoelectric harvester. The clock and reference voltage generation was done internally. The output power shown

in Figure 5-27 (a) takes into account the power required to generate the clock and the reference voltages. It is the electrical power available out of the V_{DD} supply. The energy harvesting circuit can output electrical power from input voltages as low as 25mV. This means that the whole circuit once started can extract power from a thermal harvester with only 1K temperature difference across its sides. The startup voltage required is 35mV which corresponds to 1.5K of temperature difference. The output power obtained is 55.4% of the maximum power theoretically available from the thermoelectric harvester with a 100mV input. The majority of the loss is in the storage block where the high voltage transformation ratios lead to significant conduction loss in the switches. The energy harvesting circuit is able to output 10μW of electrical power with 25mV input voltage.

The output power obtained using the thermal harvesting circuit and the overall end-to-end electrical efficiency compares favorably with published work on thermal energy harvesting interface circuits. The work presented in [74] achieves a conversion efficiency of 60 - 70 % in the DC-DC converter with a startup voltage of 600mV. The circuit presented works of a battery voltage of 2V. The work presented in [23] uses a 1V thermal input voltage and achieves a DC-DC converter efficiency of 5 - 50% depending on the input current. Both the efficiency numbers quoted above are of the DC-DC converter and not the end-to-end efficiency taking into account the maximum output power possible.

Figure 5-28 shows the electric power obtained at the output of the storage block with change in the voltage V_{STO} for two different input voltages. The closed loop zero-current switching block described in Section 5.6.1 helps to keep the output power obtained almost constant with change in V_{STO}. At 100mV input, the maximum power available from the thermal harvester is 500μW. The storage block obtains an efficiency of close to 60% in this case. With a 50mV input, the storage block obtains a maximum efficiency of 52%.

Figure 5-29(a) shows the output voltage regulation of the DC-DC buck converter with change in the load current I_L. The buck converter with the help of pulse frequency modulation mode of control maintains a tight regulation of V_L. The change in V_L as I_L changes is due to the reduction in the ripple voltage which reduces the overall average voltage obtained.
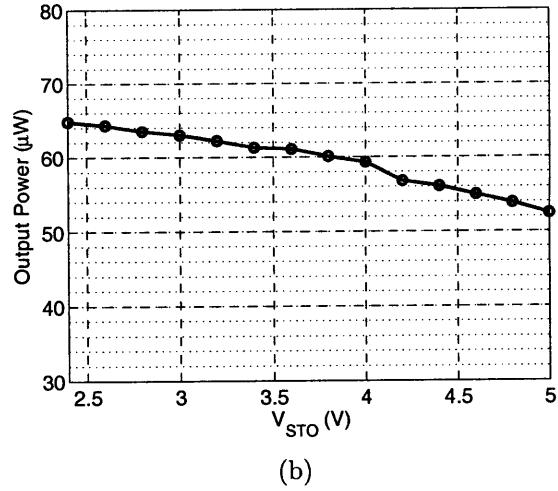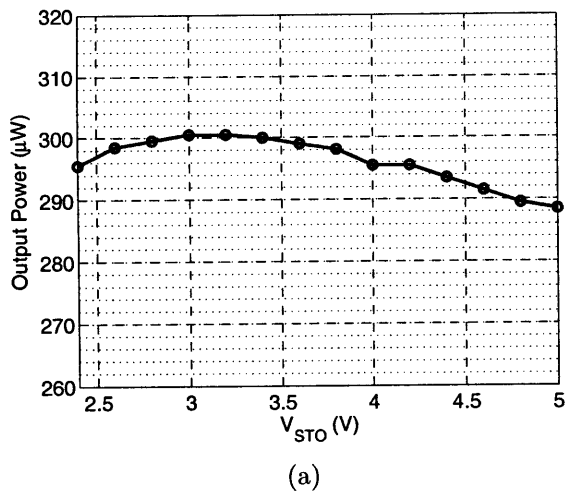
Figure 5-28: Measured power output by the storage block with change in V_{STO} for (a) 100mV thermal input and (b) 50mV thermal input.
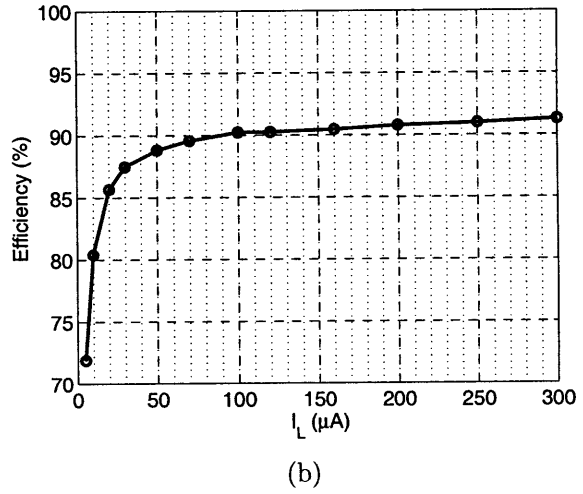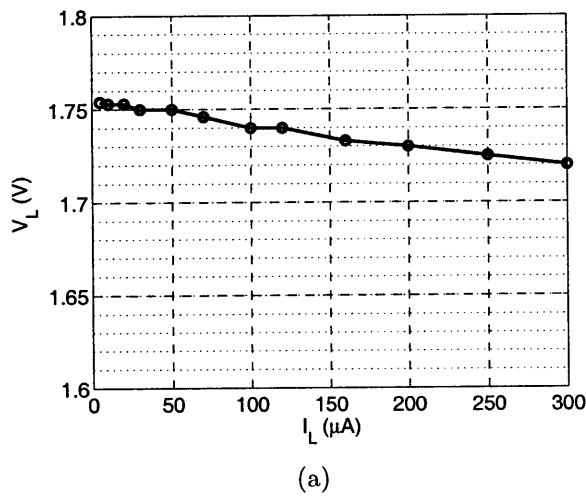
Figure 5-29: Measured values of (a) Regulated output voltage (b) Efficiency of the DC-DC converter with change in the output load current I_L.

Figure 5-29(b) shows the measured efficiency of the buck converter with change in I_L with 2.5V at V_{STO}. The converter is able to achieve an efficiency greater than 90% over majority of its operating range. The quiescent current consumed by the reference voltage ladders bring down the efficiency at low load current levels.

5.9 Summary and Conclusions

Thermoelectric elements can be used to harvest thermal energy present in everyday surroundings like on the human body to provide usable electrical power. The voltage output by the thermoelectric elements are proportional to the temperature difference across them. This is of concern while using thermal harvesters in body-worn applications as the voltage output by the harvester is only 25-50mV in most cases. Techniques have been provided in this chapter that allow circuits to interface directly with and extract power out of thermoelectric generators. This enables load circuits like processors and radios to operate directly of the thermoelectric generator without the aid of a battery. A complete power management solution was provided that could extract electrical power efficiently from the harvester independent of the input voltage conditions. Also, the availability of a regulated output voltage makes it easier to interface to load circuits on the other end. With the help of closed-loop control techniques, the energy processing circuit is able to maintain efficiency over a wide range of load voltage and process variations. The power management solution provided is ideal for low-power applications.

Chapter 6

Conclusions

Energy efficiency of integrated circuits continues to be a major factor in determining the size, weight and cost of portable electronic systems. Sophisticated battery operated electronic systems and self-powered devices have found diverse applications recently. In most of these applications, larger battery life-time or perpetual operation using scavenged energy is a key requirement. Most of these applications are in the low-power space where the currents drawn from the battery or the energy harvesters is less than 10mA. Accordingly, in battery powered systems, the power management unit needs to be highly efficient. Also, the energy processing circuits that interface to the energy harvesters have to be optimized depending on the specific harvester in use, to extract the maximum available power from it. This thesis has focused on the energy processing circuits, making them more efficient in terms of power obtained, components used and overall cost of the final solution. The specific contributions made are listed below.

6.1   Summary of Contributions

Switched Capacitor DC-DC Converter

- A different way to look at the various efficiency loss mechanisms in a switched capacitor DC-DC converter. The approach is more suitable for low current on-chip converters.

- Analysis of the current handling capability of switched capacitor converters taking into account the efficiency of the converter. Insights are given on how to pick the region of operation of the converter to maximize load current handling capabilities and efficiency.

- Three different designs of switched capacitor DC-DC converters with on-chip charge transfer capacitors. The converters are all implemented in plain vanilla digital CMOS processes.

- Demonstration of voltage scalable switched capacitor DC-DC converters that can provide >75% efficiency over a wide range of load voltages from 0.3V to 1.15V.

- Multiple gain setting architectures to mitigate conduction loss.

- New approaches employing divide-by-3 switching and charge recycling to mitigate bottom-plate losses.

- All digital control that helps the converters provide a regulated user-defined output voltage. The control is extremely simple thereby enabling high efficiencies at micro-watt power levels. The control techniques employed also enable the DC-DC converters to maintain a constant efficiency over a wide range of load voltage and orders of magnitude change in load current.

- Embedded switched capacitor DC-DC converter design that acts as the power delivery unit in a subthreshold microcontroller system. The converter occupies only a small fraction of the total area of the system and enables the microcontroller to operate at subthreshold voltages at >75% efficiency.

- Demonstration of the feasibility of using switched capacitor DC-DC converters as a high efficiency alternative to linear regulators and as a low cost alternative to inductor based switching regulators.

Piezoelectric Energy Harvesting Interface Circuit

- Identification of problems with commonly used interface circuits for piezoelectric energy harvesters.

- A switch-only rectifier circuit that can improve the power extraction capability by 2X with the help of just a CMOS transistor.

- A bias-flip rectifier circuit that enables greater than 4X improvement in power extraction capability.

- An equivalent circuit approach to arrive at the circuits for power extraction improvements.

- A complete power management solution in digital CMOS that enables the piezoelectric energy harvester to recharge a storage capacitor.

- Inductor sharing scheme that helps to keep the off-chip components to a minimum.

- High efficiency inductor-based DC-DC converters that achieve greater than 85% efficiency at micro-watt power levels.

Thermoelectric Energy Harvesting Interface Circuit

- A mechanically assisted startup circuit that enables digital CMOS circuits to operate from as low as 35mV input voltage.

- A complete power management solution that starts of from a low voltage, efficiently transfers power from the thermoelectric harvester and provides a regulated output voltage for proper operation of load circuits. The entire solution operates directly from the thermoelectric harvester without needing a battery, external clock and voltage references.

- A maximum power extraction methodology that allows the power management solution to extract the maximum available power from the thermoelectric harvester independent of the voltage output by the harvester.

- Closed loop control techniques to do automatic zero current switching of the inductor current in buck and boost regulators.

6.2 Open Problems

- This thesis has demonstrated the feasibility of switched capacitor DC-DC converters as on-chip power supplies for low-power applications. However, there are many open problems related to this area that can lead to a much improved power management solution. One of the areas that can be explored is the possibility of high frequency switching. This would help reduce the area occupied by the charge-transfer capacitors for a given load current handling capability. One of the main problems with high frequency switching is the increased switching losses which severely brings down efficiency. New techniques need to be explored for on-chip switched capacitor converters that can keep the switching losses small. This may involve new gain setting architectures, recycling of the gate charge etc.

Reducing the output ripple voltage is another major concern if the load capacitor also needs to be integrated. Interleaving techniques need to be explored in this regard to help minimize the amount of load capacitance required. Interleaving brings in problems related to overhead, generating multiple phase shifted clocks etc. These can be studied in depth.

Novel ways of incorporating on-chip inductors into switched capacitor designs is another area which holds much promise. This thesis introduced the possibility of using an on-chip inductor to reduce bottom-plate losses. This technique can be furthered to mitigate gate-switching losses too. Further, the inductor can be introduced into the charge transfer path leading to a hybrid converter which can combine the benefits of

inductor-based and switched capacitor DC-DC converters.

- The chapter on piezoelectric energy harvesting presented new rectifier techniques to improve power obtained from the harvester. It was noted that the power obtained varies with the voltage set at the output of the rectifier. While this voltage was regulated, the maximum power point was not automatically tracked in this thesis. This can be an interesting circuit that can be designed. The circuit should be able to track the optimum output voltage as the frequency and amplitude of the input vibration changes.

  Techniques can also be developed to help the interface circuit to start off without the aid of an initial voltage source. This would require some kind of a bootstrap circuit that does not employ the bias-flip rectifier to begin with, and once the voltage builds up on the output, the entire control can be activated.

  Further studies related to the mechanical aspects of the design need to be undertaken to better understand the interface between the electrical and mechanical parts of the piezoelectric harvester. This will also lead to understanding the overall efficiency of the harvester from the mechanical input to the electrical output.

- The thermoelectric energy harvester system presented made use of a mechanically assisted startup circuit to extract power from the very low voltages output by the harvester. While this circuit is applicable in situations where ambient vibration is available as in a human body, it does not work in situations where no ambient vibrations exist. A completely electronic startup circuit would be an interesting problem to tackle. Also, starting up from voltages below 30mV can be explored.

  One of the main problems with thermal harvesters is in the mechanical design of the heat transfer arrangement. It is essential to dissipate the unused heat on the cold side of the harvester. More work needs to be done in making this thermal design compact and efficient.

- An energy processor design that can simultaneously handle energy inputs from a variety of sources will be a key component in future portable electronic systems. The energy

processor needs to handle energy from not only the battery but also needs to be able to recharge the battery when energy is available from vibration, thermal or light harvesting sources. New techniques are required to combine the energy from the sources efficiently and when limited resources are available, to prioritize the energy input such that the source with the most instantaneous power input is chosen.

Appendix A

Second order RLC circuit
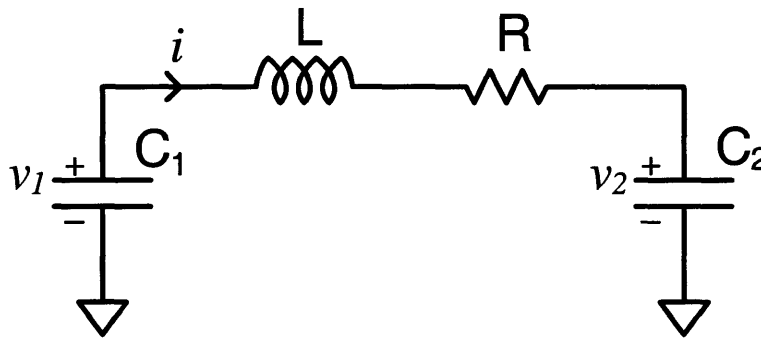
Figure A-1: A general R, L, C circuit.

Consider the second order RLC circuit shown in Figure A-1. We can write the equation for the current flowing through the elements as

$$i = C_2 \frac{dv_2}{dt} = -C_1 \frac{dv_1}{dt} \qquad (A.1)$$

Applying Kirchoff's voltage law across the loop, the voltages can be expressed as

$$v_1 = L \frac{di}{dt} + Ri + v_2 \qquad (A.2)$$

Taking the derivative of Equation A.2 with respect to time, we get

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$$\frac{dv_1}{dt} = L\frac{d^2i}{dt^2} + R\frac{di}{dt} + \frac{dv_2}{dt} \tag{A.3}$$

Rearranging the above equation and substituting values from Equation A.1, we get

$$L\frac{d^2i}{dt^2} + R\frac{di}{dt} + i(\frac{1}{C_1} + \frac{1}{C_2}) = 0 \tag{A.4}$$

Using C_S as the series combination of the capacitors C_1 and C_2, we get

$$LC_S\frac{d^2i}{dt^2} + RC_S\frac{di}{dt} + i = 0 \tag{A.5}$$

This is a homogeneous second-order differential equation with constant coefficients and can be solved easily to get the following generalized solution

$$i = Ae^{-\beta t}\cos\omega t + Be^{-\beta t}\sin\omega t \tag{A.6}$$

where $\beta = R/2L$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/\sqrt{LC_S}$.

Setting the following initial conditions, $i(0)=0$ and $v_1(0)=V_i$, we can solve for A and B. The initial conditions result in

$$A = 0, B = \frac{V_i}{\omega L} \tag{A.7}$$

This gives the equation for current i as

$$i = \frac{V_i}{\omega L}e^{-\beta t}\sin\omega t \tag{A.8}$$

From Equation A.1, we can write

$$v_2 = \frac{-C_2}{C_1}v_1 + V_{cons} \tag{A.9}$$

where V_{cons} is a constant of integration. By applying the initial conditions $v_1(0)=V_i$ and $v_2(0)=0$, we can obtain V_{cons} as

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$$V_{cons} = \frac{C_1 V_i}{C_2} \tag{A.10}$$

We can now plug Equation A.8 and Equation A.9 into Equation A.2 to get

$$v_1\left(1 + \frac{C_1}{C_2}\right) = V_i e^{-\beta t}\cos \omega t \ - \frac{\beta V_i}{\omega}e^{-\beta t}\sin \omega t \ + \frac{RV_i}{\omega L}e^{-\beta t}\sin \omega t \ + \frac{C_1}{C_2}V_i \tag{A.11}$$

Rearranging the above equation, we get

$$v_1 = \frac{C_1}{C_1 + C_2}V_i + \frac{C_2 V_i}{C_1 + C_2}e^{-\beta t}\cos \omega t \ + \frac{RV_i}{2\omega L}e^{-\beta t}\sin \omega t \tag{A.12}$$

The sine and cosine terms can be clubbed to obtain

$$v_1 = \frac{C_1 V_i}{C_1 + C_2} + \frac{C_2 V_i}{C_1 + C_2} \cdot \frac{\omega_o}{\omega}e^{-\beta t}\cos(\omega t - \phi) \tag{A.13}$$

where $\phi = \tan^{-1}(\beta/\omega)$. This gives the expression for voltage across C_1. Plugging this into Equation A.9, we can get an expression for v_2 as

$$v_2 = \frac{C_1 V_i}{C_1 + C_2} - \frac{C_1 V_i}{C_1 + C_2} \cdot \frac{\omega_o}{\omega}e^{-\beta t}\cos(\omega t - \phi) \tag{A.14}$$

The voltage across the capacitors C_1 and C_2 at the end of one half-cycle can be given by

$$v_1(\pi/\omega) = \frac{C_1 V_i}{C_1 + C_2} - \frac{C_2 V_i}{C_1 + C_2}e^{\frac{-\pi\beta}{\omega}} \tag{A.15}$$

$$v_2(\pi/\omega) = \frac{C_1 V_i}{C_1 + C_2} + \frac{C_1 V_i}{C_1 + C_2}e^{\frac{-\pi\beta}{\omega}} \tag{A.16}$$

Once the expressions for voltage and current have been obtained for the general RLC circuit, it can be extended to the circuit shown in Figure A-2 which has only one capacitor. Instead of deriving the equations again, the current and voltage relations can be obtained by substituting ∞ for the value of C_2 in the above equations. The current through the circuit
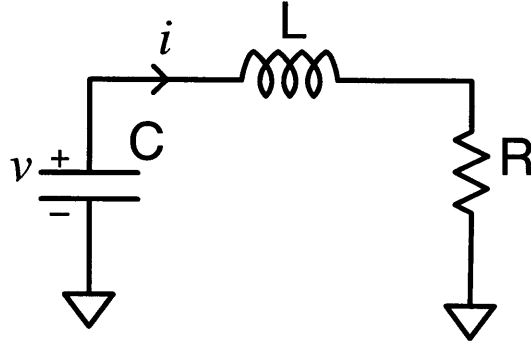
Figure A-2: A simplified R, L, C circuit with only one capacitor.

can be given by

$$i = \frac{V_i}{\omega L} e^{-\beta t} \sin \omega t \qquad (A.17)$$

where $\beta = R/2L$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/\sqrt{LC}$. Assuming the same initial conditions of $i(0)=0$ and $v(0)=V_i$, the voltage across capacitor C can be given by

$$v = \frac{V_i \omega_o}{\omega} e^{-\beta t} \cos(\omega t - \phi) \qquad (A.18)$$

where $\phi = \tan^{-1}(\beta/\omega)$. The voltage across C at the end of one half-cycle can be given by

$$v(\pi/\omega) = -V_i e^{\frac{-\pi \beta}{\omega}} \qquad (A.19)$$

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Appendix B

Power extraction from a piezoelectric energy harvester in the presence of source resistance
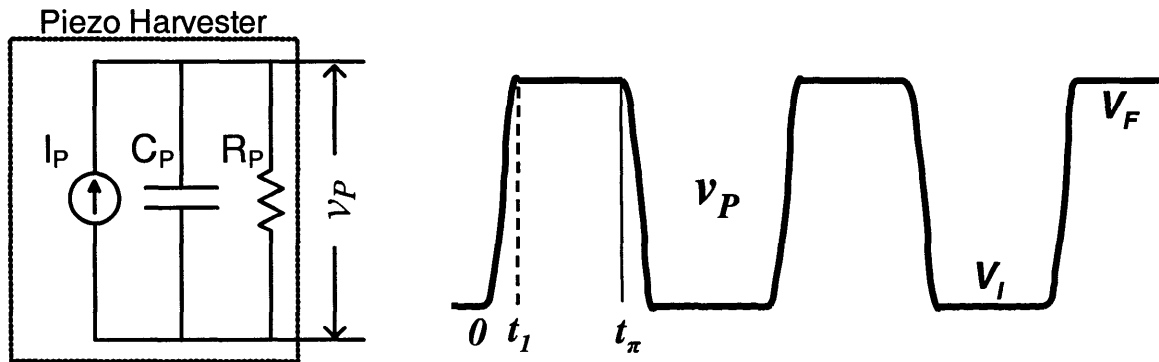
Figure B-1: Generalized waveform of the voltage across a piezoelectric energy harvester when connected to a rectifier

This section presents the derivation for the power obtained at the output of a rectifier connected to a piezoelectric energy harvester in the presence of source resistance R_P. This section builds on the discourse presented in Section 4.2 and Section 4.3. The reader is requested to read these sections to understand certain terms provided in this appendix. The

analysis of the charge not delivered to the output will be performed over a half-cycle from $t = 0$ to $t = t_\pi$. v_P is the voltage across the piezoelectric harvester.

At the beginning of the half-cycle, let $v_P = V_I$. The piezoelectric current i_P needs to charge the capacitor C_P up to V_F before the diodes can conduct and current can start to flow to the output. The charge lost over a half-cycle can be split into two major components:

1. Charge lost in charging/discharging C_P

2. Charge lost due to current flow in R_P

The charge lost due to C_P every half-cycle can be given by

$$Q_{lost,C_P} = C_P(V_F - V_I) \tag{B.1}$$

The charge lost in R_P can be derived by breaking down the half-cycle into two time periods - the first one from 0 to t_1 and the second one from t_1 to t_π.

Assuming that Q_P is fairly large (>7), the voltage v_P can be given approximately by

$$v_P \approx V_I + \frac{1}{C_P} \int_0^t I_P \sin \omega_P t \, dt = V_I + V_P(1 - \cos \omega_P t) \tag{B.2}$$

where $V_P = I_P/\omega_P C_P$ is the amplitude of the open-circuit voltage output by the piezoelectric harvester. The time t_1 taken for v_P to reach V_F is then given by

$$\omega_P t_1 = \cos^{-1}\left(1 - \frac{V_F - V_I}{V_P}\right) \tag{B.3}$$

Given t_1, the charge lost due to R_P in the interval between 0 and t_1 is

$$Q1_{lost,R_P} = \frac{1}{R_P} \int_0^{t_1} v_P \, dt = \frac{V_I + V_P}{R_P} t_1 - \frac{V_P \sin \omega_P t_1}{\omega_P R_P} \tag{B.4}$$

In the time-period from t_1 to t_π, the current through R_P is constant at V_F/R_P. Hence the charge lost due to R_P in the interval between t_1 and t_π can be given by

$$Q2_{lost,R_P} = \frac{V_F(t_\pi - t_1)}{R_P} \tag{B.5}$$

In deriving the above equation, it has been assumed that the rectifier diodes are ON till the end of the half-cycle. In reality the diodes stop conducting once i_P goes below V_F/R_P. This time is small enough that the resultant error is not large. The total charge lost in R_P over the entire half-cycle is

$$Q_{lost,R_P} = Q1_{lost,R_P} + Q2_{lost,R_P} = \frac{(V_I + V_P)t_1}{R_P} - \frac{V_P \sin \omega_P t_1}{\omega_P R_P} + \frac{V_F(t_\pi - t_1)}{R_P} \qquad (B.6)$$

The loss in R_P can be thought of as a result of a constant current V_F/R_P flowing through it for a fraction k of the half-cycle. Hence,

$$\frac{kV_F}{R_P}t_\pi = \frac{(V_I + V_P)t_1}{R_P} - \frac{V_P \sin \omega_P t_1}{\omega_P R_P} + \frac{V_F(t_\pi - t_1)}{R_P} \qquad (B.7)$$

Multiplying by ω_P on both sides and plugging in $\omega_P t_\pi = \pi$, the value of k is given by

$$k = \frac{(V_I + V_P)\omega_P t_1}{\pi V_F} - \frac{V_P \sin \omega_P t_1}{\pi V_F} + \frac{\pi - \omega_P t_1}{\pi} \qquad (B.8)$$

The total charge lost over a half-cycle is given by

$$Q_{lost} = Q_{lost,C_P} + Q_{lost,R_P} = C_P(V_F - V_I) + \frac{\pi k V_F}{\omega_P R_P} \qquad (B.9)$$

The charge available from the harvester over one half-cycle is

$$Q_{av} = \frac{2I_P}{\omega_P} = 2C_P V_P \qquad (B.10)$$

Hence, the charge delivered to the output of the rectifier every half-cycle can be given by

$$Q_{RECT} = Q_{av} - Q_{lost} = 2C_P V_P - C_P(V_F - V_I) - \frac{\pi k V_F}{\omega_P R_P} \qquad (B.11)$$

For the full-bridge, switch-only and bias-flip rectifiers, the same amount of charge delivery happens every half-cycle. For the voltage doubler, charge is delivered only in one half-cycle. Hence, for the full-bridge, switch-only and bias-flip rectifiers, the power delivered can be

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obtained by multiplying Equation B.11 by $2f_P V_{RECT}$.

$$P_{RECT} = 2C_P V_{RECT} f_P \left(2V_P - (V_F - V_I) - \frac{\pi k V_F}{Q_P} \right) \tag{B.12}$$

where $Q_P = \omega_P C_P R_P$ is the Q-factor of the piezoelectric harvester. For the voltage doubler, the output power is given by

$$P_{RECT,VD} = C_P V_{RECT} f_P \left(2V_P - (V_F - V_I) - \frac{\pi k V_F}{Q_P} \right) \tag{B.13}$$

B.1 Full-bridge Rectifier

For the full-bridge rectifier, $V_I = -(V_{RECT} + 2V_D)$ and $V_F = V_{RECT} + 2V_D$. Hence, the power output by the full-bridge rectifier can be given by

$$P_{RECT,FB} = 2C_P V_{RECT} f_P \left(2V_P - 2(V_{RECT} + 2V_D) - \frac{\pi k_{FB}(V_{RECT} + 2V_D)}{Q_P} \right) \tag{B.14}$$

where

$$k_{FB} = \frac{(V_P - V_{RECT} - 2V_D)\omega_P t_1}{\pi(V_{RECT} + 2V_D)} - \frac{V_P \sin \omega_P t_1}{\pi(V_{RECT} + 2V_D)} + \frac{\pi - \omega_P t_1}{\pi} \tag{B.15}$$

and

$$\omega_P t_1 = \cos^{-1} \left(1 - \frac{2(V_{RECT} + 2V_D)}{V_P} \right) \tag{B.16}$$

B.2 Voltage Doubler

For the voltage doubler, $V_I = -V_D$ and $V_F = V_{RECT} + V_D$. Hence, the power output by the voltage doubler can be given by

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$$P_{RECT,VD} = C_P V_{RECT} f_P \left(2V_P - (V_{RECT} + 2V_D) - \frac{\pi k_{VD}(V_{RECT} + V_D)}{Q_P} \right) \tag{B.17}$$

where

$$k_{VD} = \frac{(V_P - V_D)\omega_P t_1}{\pi(V_{RECT} + V_D)} - \frac{V_P \sin \omega_P t_1}{\pi(V_{RECT} + V_D)} + \frac{\pi - \omega_P t_1}{\pi} \tag{B.18}$$

and

$$\omega_P t_1 = \cos^{-1} \left(1 - \frac{V_{RECT} + 2V_D}{V_P} \right) \tag{B.19}$$

B.3 Switch-only Rectifier

For the switch-only rectifier, $V_I = 0$ and $V_F = V_{RECT} + 2V_D$. Hence, the power output by the switch-only rectifier can be given by

$$P_{RECT,SO} = 2C_P V_{RECT} f_P \left(2V_P - (V_{RECT} + 2V_D) - \frac{\pi k_{SO}(V_{RECT} + 2V_D)}{Q_P} \right) \tag{B.20}$$

where

$$k_{SO} = \frac{(V_P)\omega_P t_1}{\pi(V_{RECT} + 2V_D)} - \frac{V_P \sin \omega_P t_1}{\pi(V_{RECT} + 2V_D)} + \frac{\pi - \omega_P t_1}{\pi} \tag{B.21}$$

and

$$\omega_P t_1 = \cos^{-1} \left(1 - \frac{V_{RECT} + 2V_D}{V_P} \right) \tag{B.22}$$

B.4   Bias-flip Rectifier

For the bias-flip rectifier, $V_I = (V_{RECT} + 2V_D)e^{-\tau}$ and $V_F = V_{RECT} + 2V_D$ where $\tau = \pi\beta/\omega$, $\beta = R_{BF}/2L_{BF}$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/\sqrt{L_{BF}C_P}$. Please see Section 4.3.2 for a description of these terms. The power output by the bias-flip rectifier can be given by

$$P_{RECT,BF} = 2C_P V_{RECT} f_P \left(2V_P - (V_{RECT} + 2V_D)(1 - e^{-\tau}) - \frac{\pi k_{BF}(V_{RECT} + 2V_D)}{Q_P} \right)$$

(B.23)

where

$$k_{BF} = \frac{(V_P + (V_{RECT} + 2V_D)e^{-\tau})\omega_P t_1}{\pi(V_{RECT} + 2V_D)} - \frac{V_P \sin \omega_P t_1}{\pi(V_{RECT} + 2V_D)} + \frac{\pi - \omega_P t_1}{\pi}$$

(B.24)

and

$$\omega_P t_1 = \cos^{-1}\left(1 - \frac{(V_{RECT} + 2V_D)(1 - e^{-\tau})}{V_P} \right)$$

(B.25)

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