A Batteryless Single-Inductor Boost Converter With 190 mV Self-Startup Voltage for Thermal Energy Harvesting Over a Wide Temperature Range

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Abstract—In this brief, a batteryless boost converter for thermal energy harvesting is presented. Only single off-chip inductor is employed through inductor sharing technique. A stepping-up architecture consisting of a startup converter and a main converter is adopted. The startup converter activates the chip with an input voltage as low as 190 mV. With zero-current switching and maximum power point tracking techniques, the main converter achieves a peak efficiency of 60% and outputs a maximum power of 400 μW. The converter is capable of maintaining its operation under a minimum input voltage of 50 mV over a wide temperature range from −30 °C to 80 °C. The proposed design has been fabricated with 180 nm CMOS process and been demonstrated with thermal energy harvesting.

Index Terms—Boost converter, maximum power point tracking (MPPT), self-startup, single inductor, thermal energy harvesting.

I. INTRODUCTION

HARVESTING energy from ambient sources is a key technology for energy autonomous systems. The ambient energy sources can be solar [1], [2], vibration [3], [4], electromagnetic [5], [6], and RF energy [7], [8], etc. As one of the most eco-friendly energy sources, the thermal energy can be converted into electric energy via Seebeck effect. With recent advances, miniaturized thermoelectric generator (TEG) devices have been successfully fabricated and promoted in small-scale thermal energy harvesting applications [9]–[18].

However, due to the physical dimension and temperature gradient limitations, the induced voltage level from a TEG device could be quite low in Internet-of-Things (IoT) sensor applications. The small dimension limits its effective temperature coefficient (from 50mV/K to 100mV/K), whereas the restricted thickness limits the temperature gradient across the device (from 0.5K to 2K) [17]. Thus the resulting output voltage level could be as low as tens of millivolts, which is not suitable to directly power the electronic devices. A boost converter with low startup voltage and low operating

voltage is needed in TEG applications. To build a compact and low-cost system, it is also necessary to avoid the built-in batteries as well as to reduce the number of bulky off-chip components. Existing works have achieved low startup or operating voltage at high system complexity, such as utilizing a pre-charge or an external battery [9], [10], mechanical switches [11], off-chip transformers [12], an LC oscillator [13]. Other implementations [14]–[17] have minimized the system complexity with only one or no off-chip inductor, but either require high startup voltage [14], [15] or have relative low efficiency or output power [16], [17].

Therefore, in this brief, we proposed a stepping-up boost converter, which consists of a startup converter and a main converter. After initially activated by the startup converter, the chip automatically steps up to the main converter with higher conversion efficiency. In contrast to [13], the proposed switched branches enable inductor sharing between the startup converter and the main converter, thus leading to a batteryless boost converter that employs single off-chip inductor (which was first presented in [19]). Different from other single-inductor converters [14], [15], the startup converter utilizes a redundant inverter based ring oscillator [20] which achieves self-startup at 190mV without the need for RF kickstart. Thanks to the zero-current switching (ZCS) [21] and the proposed maximum power point tracking (MPPT) techniques, the main converter achieves a peak efficiency of 60% and outputs a maximum power of 400μW. In addition, after startup, the chip can sustain operation at 50mV over a wide temperature range (from −30°C to 80°C), which could be an attractive feature for thermal energy harvesting applications under extreme conditions.

The rest of this brief is organized as follows: Section II describes the overall architecture. Section III presents the circuit implementations. The measurement results are shown and compared with state-of-the-arts in Section IV. Section V draws conclusions.

II. THE PROPOSED ARCHITECTURE

The top-level architecture of the proposed boost converter is shown in Fig. 1(a). The chip integrates a startup converter, a main converter, a MPPT block, voltage monitors, and switched branches with associated control logic. It can self-startup from the input (V_I) and provide a regulated voltage supply rail (V_O) to power the loading circuits, using single off-chip inductor. With a stepping-up architecture, the chip operates under two modes: 1) startup boost mode when the internal voltage (V_S) is low; 2) main boost mode when V_S is sufficiently high to maintain high conversion efficiency.
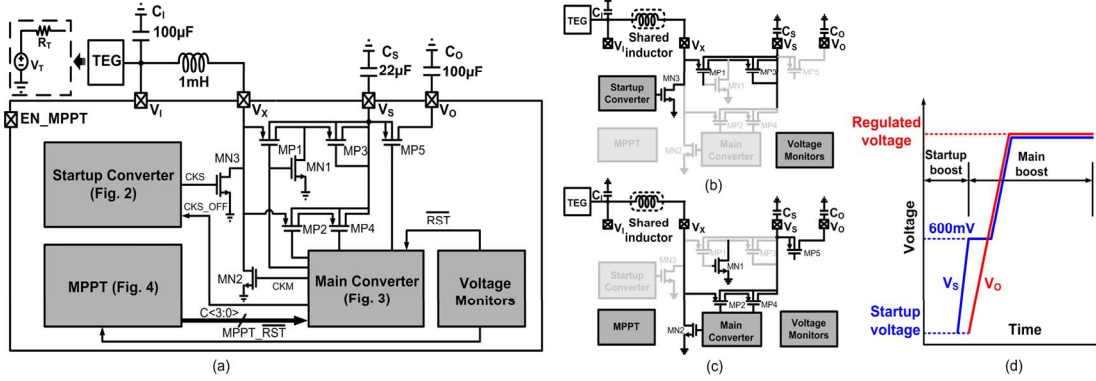
Fig. 1. (a) Top-level architecture; (b) Startup boost mode; (c) Main boost mode; (d) Transition from startup to main boost mode.
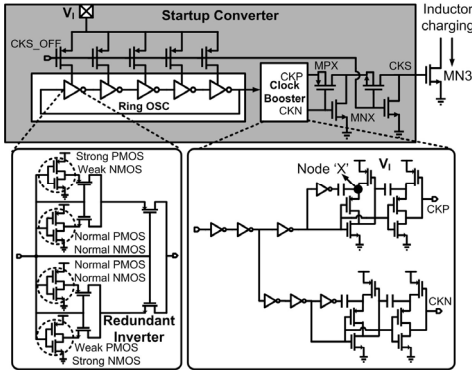

Fig. 2. Schematic of the startup converter.

The transition from the two modes is implemented by the switched branches with associated control logic. Fig. 1 (b)-(d) show the details. It works as follows: When V_I reaches the startup voltage, the startup converter and the branch switch (MP1) is turned on. The clock signal (CKS) turns on/off the NMOS switch (MN3) and charges V_S via MP1 and a diode-connected PMOS (MP3). When V_S reaches around 600mV, the voltage monitor releases a signal ($\overline{RST}$) to activate the main converter and simultaneously disable the startup converter. In this mode, by turning on branch switches (MP2 and MP5), the converter charges the node of V_O through MP2, MP4, and MP5. Since the switches can be fully turned on, less conduction loss occurs during this mode. To further improve the efficiency, the main converter works under ZCS conditions (detailed in Section III-B) and automatically tracks the maximum power point (detailed in Section III-C). The switched branches enable sharing of single inductor between two converters, allowing for energy transfer from the harvester to either V_S or V_O.

III. CIRCUIT IMPLEMENTATION

A. Startup Converter

Fig. 2 shows the schematic of the startup converter. It consists of a ring oscillator, followed by a clock booster, which generates the driving clock (CKS) for MN3. To enable oscillation at very low supply voltage, a redundant inverter [20], consisting of four inverters and two stages of multiplexers, is utilized as the basic cell for the ring oscillator. The main concept is to make both stronger pull-up and pull-down paths through larger PMOS/NMOS sizing, respectively. As shown in the bottom left of Fig. 2. The top inverter has a strong PMOS and a weak NMOS, which can output strong '1' and weak

'0'. The bottom inverter, on the opposite, has a strong NMOS and a weak PMOS. The output of the redundant inverter is multiplexed according to the input, with both strong '1' and strong '0'. In this way, the internal node of the ring oscillator can have both stronger pull-up and pull-down paths, which enables the oscillation at very low supply voltage at the expense of lower switching speed. When the oscillation begins, the multiplexers and other inverters function well with normal threshold transistor, even under very low supply voltage. Simulation shows that even using transistors in 180nm CMOS process with threshold voltage as high as 650mV, it is still able to oscillate at 150mV. However, the output swing of ring oscillator is still not sufficient to fully switch on/off MN3 directly and therefore a clock booster is designed, as shown in the bottom right of Fig. 2. It works as follows: When the input clock is '0', the node 'X' is pre-charged to V_I. After the rising edge of the input clock, the node 'X' is boosted to $2V_I$. Therefore by cascading two such stages, the maximum voltage level is tripled by the clock booster. In order to obtain a clock swing of $3V_I$, two more transistors (MPX and MNX) are inserted. Thus CKS has a voltage level of $3V_I$ when CKP is high, whereas it is pulled down to ground when CKN is high.

The startup converter has two phases. During the charging phase (when CKS is high), the current flows through MN3, charging the inductor. During the discharging phase (when CKS is low), charge is delivered to C_S through the branch switch MP1 and the diode-connected MP3. Thus the converter works in the discontinuous conduction mode (DCM) and has a high boost ratio (BR), which can be expressed in (1) [20].

$$\text{BR} = \frac{V_S}{V_I} = 1 + \frac{V_I D^2 T_S}{2 L I_O} \tag{1}$$

where T_S and D is the period and duty cycle of CKS respectively. I_O is the loading current. To activate the main converter, V_S is required to be boosted to around 600mV, which determines BR and hence the maximum value of the inductance L.

The startup converter controls the charging of the intermediate node of V_S, with a high BR at the cost of low efficiency. To improve the overall efficiency, when V_S reaches 600mV, the branch switching logic generates a CKS_OFF signal, turning off the startup converter and stepping up to the main converter.

B. Main Converter

In low-power applications, the continuous conduction mode (CCM) operation is not efficient because the
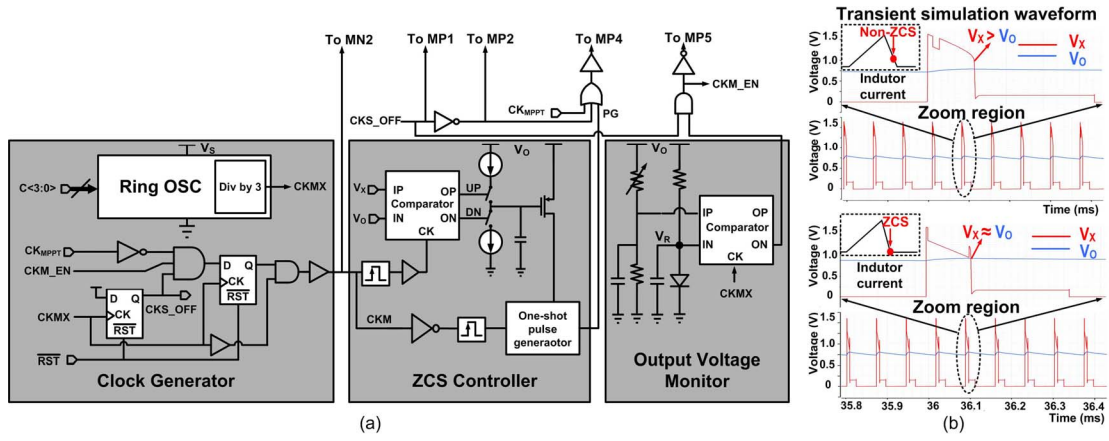
Fig. 3. Main converter (a) Schematic of the main converter; (b) Transient simulation waveform of the ZCS controller.

negative-flowing inductor current cannot be used for power transfer into the converter output. Therefore, the DCM operation which prevents the inductor current from flowing negative is adopted in this design. Since the turn-on time of the low-side (LS) switch (MN2 in Fig. 1) is preserved during charging transient, the technique that turns off the high-side (HS) switch (MP4 in Fig. 1) once the inductor current crosses zero is very important to enhance the overall efficiency, which is the basic concept of the ZCS control [13], [14], [21].

Fig. 3 (a) shows the schematic of the main converter. It includes a clock generator, a ZCS controller [21] and an output voltage monitor. To ensure ZCS condition and maximize the conversion efficiency, the on-time t_p of the HS switch MP4 requires to be dynamically adjusted in a feedback loop according to the fixed on-time of the LS switch MN2, so that MP4 could be turned off once the inductor current crosses zero. It works as follows: When V_S is sufficiently high, the clock generator begins to work. The first rising edge of the clock CKMX sets CKS_OFF to '1' and turns off the startup converter. The HS switch MP4 is driven by the buffered PG signal from the ZCS controller and its on-time t_p is initially set nearly to zero. At the moment when MP4 is turned on, V_X is compared to V_O. If V_X is larger than V_O, the comparator in ZCS controller generates a UP signal, decreasing the charging current for the on-shot pulse generator (the block which generates a pulse signal with variable time width) so that t_p is increased. On the opposite, if V_X is smaller than V_O, t_p is decreased. Fig. 3 (b) shows the simulation waveforms of the ZCS controller. The waveform on the top shows MP4 is turned off prematurely ($V_X > V_O$) with non-zero inductor current ('Non-ZCS' condition). The waveform on the bottom shows with the dynamic feedback loop, finally MP4 is turned off when V_X reaches very close to V_O with zero inductor current ('ZCS' condition). The output voltage monitor, by cutting off the main converter when V_O reaches V_R, regulates the output in the range of 1V-1.6V.

Since the ZCS condition ($V_X \approx V_O$) is achieved via a feedback loop, it has an intrinsic robustness over wide temperature range. Assume the temperature changes, although the switching frequency as well as the on-time of the LS switch may change, the ZCS condition could always be achieved by comparing V_X to V_O and adjusting t_p in the feedback loop.

C. MPPT

According to the power delivery theory, the available power to the load can be maximized only if the equivalent load
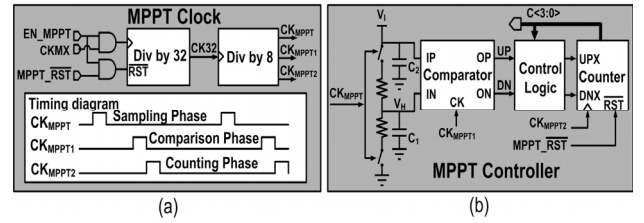

Fig. 4. Schematic of the MPPT circuit (a) MPPT clock; (b) MPPT controller.

impedance R_{EQ} matches the source impedance R_T. The conventional approach for MPPT in thermal energy harvesting uses a switching frequency that is calculated from R_T [11]. However, since R_T varies in different environmental conditions, such as temperature, pressure, or humidity, the optimum switching frequency cannot always be exactly calculated. An improved way of MPPT is to adaptively track the maximum power point in a feedback loop. Since R_{EQ} is in proportion to the switching frequency f_S of the main converter's clock [11], as expressed by (2).

$$R_{EQ} = \frac{2Lf_S}{D1^2} \qquad (2)$$

where L is the inductance and $D1$ is the fixed duty-cycle of the clock (CKM), thus by adaptively controlling f_S in a feedback loop, R_{EQ} could be dynamically adjusted to match R_T, which leads to a variation-tolerant MPPT. In this way, even if R_T varies over wide temperature range, the loop could still guarantee MPPT.

Fig. 4 shows the proposed MPPT circuit. The main purpose is to fix the average value of V_I at one half of V_T (the target value when $R_{EQ} = R_T$) by controlling f_S. It works as follows: The clock of the main converter (CKMX) is divided by 32 (determined by the frequency of MPPT execution) to CK32. Then, CK_{MPPT}, CK_{MPPT1}, and CK_{MPPT2} are generated from CK32 to control the timing of MPPT in three consecutive phases. In the sampling phase, MN2 and MP4 in the main converter are both turned-off, disconnecting the load from the source. One half of the open circuit source voltage (V_H in MPPT Controller) is sampled to C_1. In the comparison phase, the load is re-connected and the comparator compares the average value of the input voltage V_I to V_H. As V_I has ripples, its average value is obtained via a filtering capacitor C_2. In the counting phase, the UP/DN counter increases or decreases its output C<3:0> according to the comparison results. If V_I is lower than V_H, C<3:0> is down countered and vice versa.
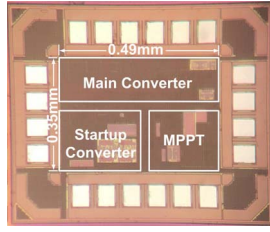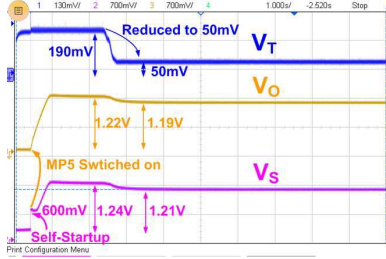
Fig. 5. Die photograph.

Fig. 7. Measured MPPT waveform.

Fig. 6. Measured transient waveform.

Fig. 8. (a) Measured efficiency and output power curve; (b) Simulated power consumption break-up (V_T = 120mV).

Fig. 9. (a) Measured self-startup voltage and minimum operating voltage; (b) Measured line regulation and load regulation.

The preceding control logic to the counter holds the value of C<3:0> when it reaches the maximum or the minimum value. C<3:0> is used to control the loading capacitance of the ring oscillator in the main converter (see Fig. 3 (a)), and thus the switching frequency f_S. The range of R_T determines the required tuning range of f_S, whereas the tacking accuracy determines its tuning resolution. In this design, 4-bits capacitor array together with a fixed capacitor obtains a frequency tuning range over 6 times with a tuning resolution of around 30%.

IV. MEASUREMENT RESULTS

Fig. 5 shows the die photograph of the chip, fabricated in 180nm CMOS process, occupying a core area of 0.17mm^2.

Fig. 6 shows the measured transient waveform of the converter, with an input voltage from 50mV to 300mV with 30Ω series resistance. The chip can self-startup at 190mV, charging V_S to 600mV. The main converter then starts to boost the output voltage to around 1.2V, showing the effectiveness of the stepping-up architecture as well as the inductor sharing. After the output has been regulated to the target value, we deliberately reduce V_T. The measurement shows that the chip can sustain operation at a minimum input of 50mV.

Fig. 7 shows the measurements of MPPT. The voltage of V_I is maintained to around half of V_T, showing an effective tracking of the maximum power point.

Fig. 8 (a) shows the efficiency versus V_T in the full design range. The efficiency is expressed in (3) [20].

$$\text{Efficiency} = \frac{P_{OUT}|_{V_O=1.2V}}{P_{IN}|_{V_I=V_T/2}} = \frac{P_{OUT\_max}}{P_{IN\_max}} \quad (3)$$

The peak efficiency of the proposed converter is 60%, with an input voltage of 120mV, proving an output power of 66μW. With MPPT, the peak efficiency is improved by around 10%.

Fig. 8 (b) shows the simulated power consumption break-up in the main boost mode. Power loss mainly comes from four dominant sources: MP2/MP4 (27.4%, including parasitic resistance), inductor loss (26.5%), MN2 (20.9%, including parasitic resistance), and clock generator (19.3%).

While most of the previous work [10], [13]–[15] reported the converter's performance over narrow temperature range close to room temperature. In this brief, we measured the
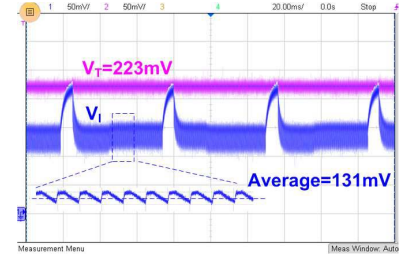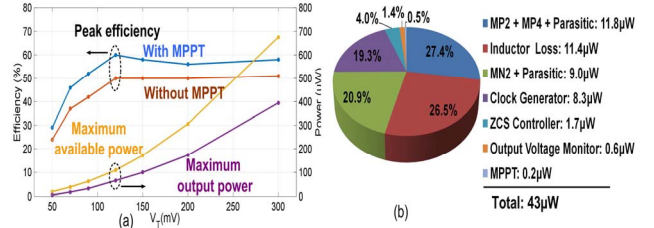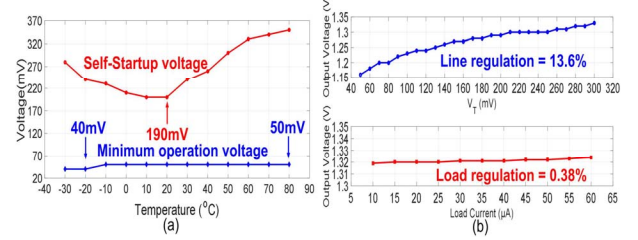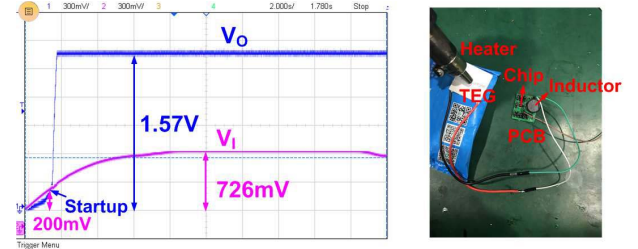

Fig. 10. Measured output waveform with a TEG as an input.

minimum startup and operating voltage over wide temperature range, as shown in Fig. 9 (a). The converter is capable of startup at less than 200mV voltage in room temperature. The startup voltage increases at lower or higher temperature. Thanks to the closed- loop ZCS and MPPT, the converter is capable of maintaining its operation at a minimum input voltage of 50mV over a wide temperature range from −30°C to 80°C, with the lowest of 40mV at temperature of −20°C, which could be an attractive feature for thermal energy harvesting applications under extreme conditions. Fig. 9 (b) shows the measured line regulation and load regulation of the converter, 13.6% and 0.38% in the operation range, respectively. The line regulation could be improved by adopting a low dropout regulator, at the cost of reducing efficiency.

Fig. 10 shows the measured output voltage with a TEG as an input. In the measurement, a heater is adopted to maintain the temperature difference between the two plates with a fixed temperature at the bottom plate, thus generating V_I for the

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

	[10]	[13]	[14]	[15]	[16]	[17]	**This work**
Startup Method	external battery	LC oscillator	cold-start/RF kick-start	cold-start/RF kick-start	self-startup	self-startup	**self-startup**
Startup Voltage	20mV	50mV	220mV	260mV	100mV	70mV	**190mV**
# of Off-chip Inductor	1	3	1	1	0	1	**1**
Minimum Input Voltage	20mV	30mV	10mV	12mV	N.A.	70mV	**50mV**
Output Voltage	1.2V	1.2V	1.1V	0.9V-1.3V	0.76V	1.25V	**1V-1.6V**
Output Power	40μW	1.25mW	N.A.	6.48mW	6.6μW	17μW	**400μW**
Peak Efficiency	70%	73%	53%-83%	60%-90.8%	33%	58%	**60%**
Temperature Range*	R.T.	R.T.+2℃ to 8℃	20℃ to 60℃	0.6℃ to 19℃	N.A.	N.A.	**-30℃ to 80℃**
MPPT	Yes	No	Yes	Yes	No	No	**Yes**
Die Area	9mm^2	1mm^2	0.12 mm^2	0.48 mm^2	2.18 mm^2	0.6mm^2	**0.17mm^2**
Process	65nm	65nm	130nm	180nm	65nm	130nm	**180nm**

* R.T stands for room temperature.

converter. The chip begins to startup when the input reaches around 200mV and the output voltage is regulated to around 1.6V. The measurement demonstrates the chip in real-scenario thermal energy harvesting.

Table I shows the performance comparison with state-of-the-art. The batteryless converter uses single off-chip inductor with a peak efficiency higher or comparable with the previous work. Although the startup voltage is larger than [16], [17], the output power as well as the peak efficiency are higher. It is noteworthy if fabricated in more advanced process (65nm or beyond), lower startup voltage could be probably achieved with a similar architecture due to the available transistors with lower threshold voltage and smaller gate capacitance. In addition, the proposed converter is measured and validated over a wider temperature range compared with previous works, which could be an attractive feature for thermal energy harvesting applications under extreme conditions.

V. CONCLUSION

This brief presents a batteryless boost converter for thermal energy harvesting fabricated in 180nm CMOS process. Thanks to the stepping-up architecture and inductor sharing techniques, the chip uses single off-chip inductor. With the ZCS control and the proposed MPPT techniques, the converter has a peak efficiency of 60% with a self-startup voltage of 190mV, and is capable of maintaining its operation under a minimum input voltage of 50mV over a wide temperature range from -30°C to 80°C, targeting for low-cost thermal energy harvesting applications under extreme conditions.

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