Project Name	Duration (days)	Start Date	End Date
LCD Screen Expansion	27	12/1/2018	12/28/2018

Task ID	Task Name	Duration	Start Date	End Date	Completed %
1	**Study Nasa Guidelines**	**18**	**12/1/2018**	**12/18/2018**	**100%**
1.1	Style Guide	**18**	**12/1/2018**	**12/18/2018**	**100%**
1.2	Defensive Programming	**16**	**12/3/2018**	**12/18/2018**	**100%**
2	**Communication Protocols**	**5**	**12/3/2018**	**12/7/2018**	**100%**
2.1	Study both SPI and I2C	**1**	**12/3/2018**	**12/3/2018**	**100%**
2.2	Implement SPI communication library	**3**	**12/3/2018**	**12/5/2018**	**100%**
2.3	Implement I2C communication library	**4**	**12/3/2018**	**12/6/2018**	**100%**
2.4	Testing both libraries	**1**	**12/7/2018**	**12/7/2018**	**100%**
3	**Screen Library**	**6**	**12/8/2018**	**12/13/2018**	**100%**
3.1	SPI Implementation	**3**	**12/8/2018**	**12/10/2018**	**100%**
3.2	I2C Implementation	**4**	**12/8/2018**	**12/11/2018**	**100%**
3.2	Integration of both protocols	**1**	**12/12/2018**	**12/12/2018**	**100%**
3.3	Integration testing	**1**	**12/13/2018**	**12/13/2018**	**100%**
4	**Expansion Algorithm**	**3**	**12/12/2018**	**12/14/2018**	**100%**
4.1	Development of the expansion algorithm	**2**	**12/12/2018**	**12/13/2018**	**100%**
4.2	Testing of the algorithm	**1**	**12/13/2018**	**12/13/2018**	**100%**
5	**Lab Prototype Design**	**2**	**12/15/2018**	**12/16/2018**	**100%**
5.1	Integrating both screens with one MCU	**1**	**12/15/2018**	**12/15/2018**	**100%**
5.2	Integration testing	**1**	**12/16/2018**	**12/16/2018**	**100%**
6	**Memory Tests**	**9**	**12/10/2018**	**12/18/2018**	**100%**
6.1	Study Flash, RAM and EEPROM tests	**3**	**12/10/2018**	**12/12/2018**	**100%**
6.2	Implement Flash test	**5**	**12/13/2018**	**12/17/2018**	**100%**
6.3	Implement RAM test	**4**	**12/13/2018**	**12/16/2018**	**100%**
6.4	Implement EEPROM test	**4**	**12/13/2018**	**12/16/2018**	**100%**
6.5	Verify memory tests	**2**	**12/17/2018**	**12/18/2018**	**100%**
7	**PCB Design**	**3**	**12/18/2018**	**12/20/2018**	**100%**
7.1	Schematic design	**1**	**12/18/2018**	**12/18/2018**	**100%**
7.2	Board design	**1**	**12/19/2018**	**12/19/2018**	**100%**
7.3	Preliminary routing tests	**1**	**12/20/2018**	**12/20/2018**	**100%**
7.4	Final routing and compliance tests	**1**	**12/20/2018**	**12/20/2018**	**100%**
8	**Documentation**	**28**	**12/1/2018**	**12/28/2018**	**100%**
8.1	Gantt chart	**28**	**12/1/2018**	**12/28/2018**	**100%**
8.2	Final report	**8**	**12/21/2018**	**12/28/2018**	**100%**