Experiment 1 – Clock and Periodic Signal Generation

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***Abstract*—In this document we are using 74 series ,LM555 and some other ICs to build Ring Oscillator, Schmitt Trigger Oscillator, Frequency Divider and T Flip-Flop and analyze their beahavier.**

***Keywords*—Clock Generation, 74 Series Basic Logic Gates, Ring Oscillator, LM555, Schmitt Trigger Oscillator, Frequency Divider, Counter, T Flip-Flop, D Flip-Flop**

I. Introduction

In this document we will discuss about clock signals and see how to program them with Basic Logic Gates like 74 series and try to bulid different clock generation and analyze the circuit with different resistance and see how it responds.

II. Clock Generation Using IC's and Analog Components

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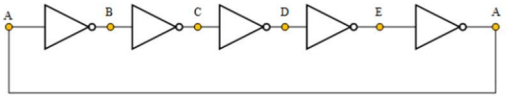
A. Ring Oscillator



The picture above is the circuit of Ring Oscillator. We connected pins of 74HCT04 like the figure below. We applied VCC to pin 14 and GND to pin 7. at last we connected oscilloscope to pin 2.

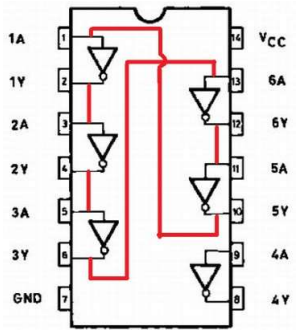


Figure 1 LM555 timer pin-out

Fig.2 Output of Ring Oscillator

1. As we know propagation delay is the time from the 50% point of input to the 50% point of output. In the picture above the propagation delay of the chain is equal to the time that the output is more than 50% of its maximum value. Thus, the propagation delay of the chain is equal to 23 ns.
The time period of the output signal is 1/f and the frequency of signal is 21.74 MHz. Therefore, the time period of the output signal is equal to 45.9 ns.

So we can say the propagation delay of the chain is approximately equal to half of The Time period of the output signal.

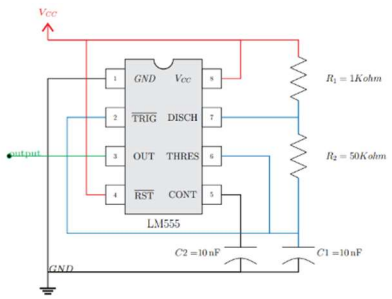
45.9/2 = 22.95 ns ≈ 23 ns

2.

$$T = \frac{1}{f} = \frac{1}{21.73\ MHz} = 45.9\ ns$$
$$T = 2N \times Delay_{inv}$$
$$45.9\ ns = 10 \times Delay_{inv}$$
$$Delay_{inv} \approx 4.6\ ns$$

B. LM555 Timer

First, we connected the circuit below.



1. Here is our output waveform of the following circuit with R2 = 50kΩ.

$$Clock\ Frequency = 1.267\ KHz$$

$$Duty\ cycle = \frac{T_{on}}{T_{total}} \times 100 = \frac{4}{8} \times 100 = 50\%$$

$$Clock\ Frequency(formula) = \frac{1}{0.693 \times (R1 + 2R_2) \times C_1}$$
$$= 1.42\ KHz$$

$$Duty\ cycle(formula) = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$
$$= \frac{51}{101} \times 100 = 50.5\%$$

Figure 2 R=50k

R2 = 1kΩ:

$$Clock\ Frequency = 36.08\ KHz$$

$$Duty\ cycle = \frac{T_{on}}{T_{total}} \times 100 = \frac{1.8}{2.9} \times 100 = 65.5\%$$

$$Clock\ Frequency(formula) = \frac{1}{0.693 \times (R1 + 2R_2) \times C_1}$$
$$= 48.1\ KHz$$

$$Duty\ cycle(formula) = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$
$$= \frac{2}{3} \times 100 = 66.6\%$$

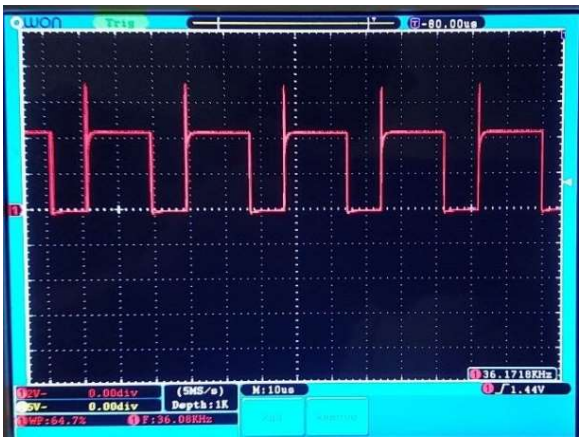


Fig. 3 R2 =1k

R2 = 10kΩ:

$$Clock\ Frequency = 5.755\ KHz$$

$$Duty\ cycle = \frac{T_{on}}{T_{total}} \times 100 = \frac{1.8}{3.4} \times 100 = 52\%$$

$$Clock\ Frequency(formula) = \frac{1}{0.693 \times (R1 + 2R_2) \times C_1}$$

$$= 6.87\ KHz$$

$$Duty\ cycle(formula) = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$

$$= \frac{11}{21} \times 100 = 52.4\%$$

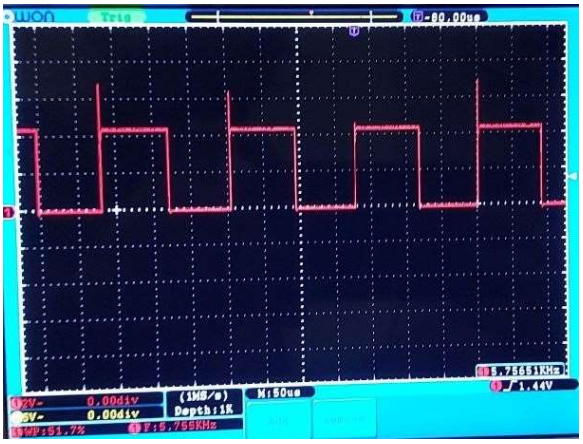


Fig. 1 R2 = 10k

R2 = 100kΩ:

$$Clock\ Frequency = 614.4\ Hz$$

$$Duty\ cycle = \frac{T_{on}}{T_{total}} \times 100 = \frac{1.6}{3.2} \times 100 = 50\%$$

$$Clock\ Frequency(formula) = \frac{1}{0.693 \times (R1 + 2R_2) \times C_1}$$

$$= 717.91\ Hz$$

$$Duty\ cycle(formula) = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100$$

$$= \frac{101}{201} \times 100 = 50.2\%$$

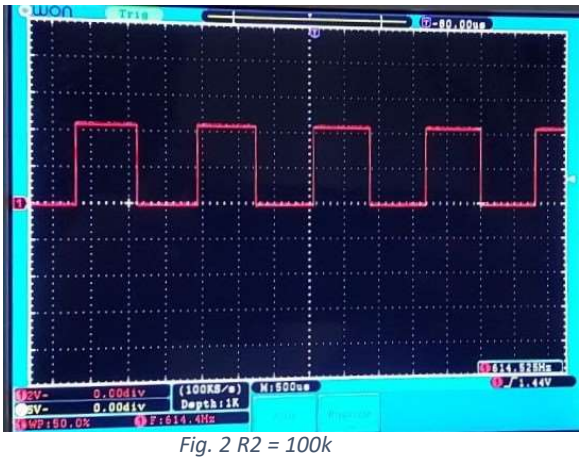


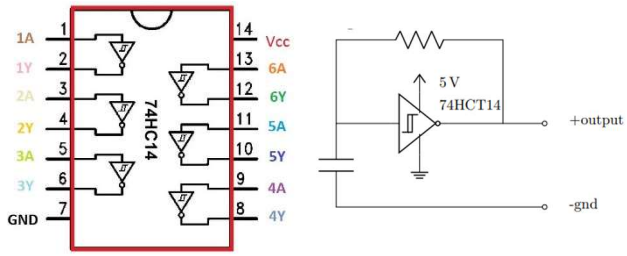
Fig. 2 R2 = 100k

R2	Clock Frequency (Real)	Clock Frequency (formula)	Duty cycle (Real)	Duty cycle (formula)
50K	1.267 KHz	1.42 KHz	50%	50.5%
1K	36.08 KHz	48.1 KHz	65.5%	66.6%
10K	5.755 KHz	6.87 KHz	52%	52.4%
100K	614.4 Hz	614.4 Hz	50%	50.2%

Table 1.

C. Schmitt Trigger Oscillator

First, we selected inverter between pin1 and pin2 and then we connected the circuit below.



R = 470Ω, C = 10nF

$$Frequency = 280.5\ KHz$$

$$\alpha = f \times R \times C$$

$$\alpha = 1.32$$

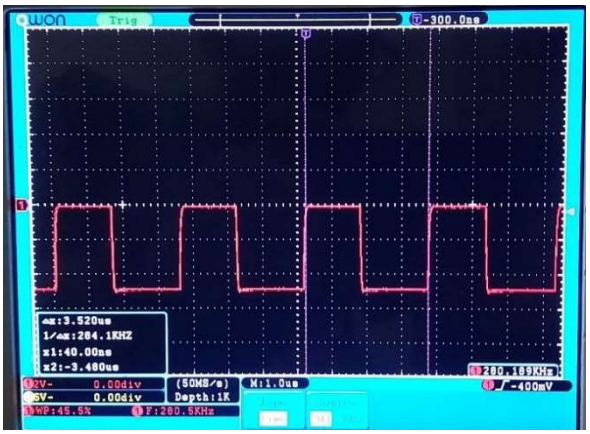


Fig. 3 Part C: R=470

R = 1000Ω, C = 10nF

$$Frequency = 138.9\ KHz$$
$$\alpha = f \times R \times C$$
$$\alpha = 1.38$$

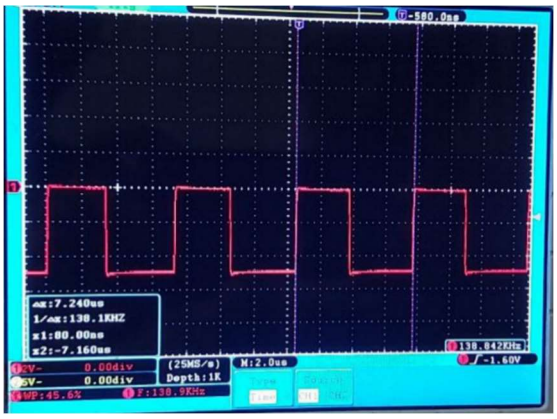


Fig. 5 Part C: R=1k

R = 2200Ω, C = 10nF

$$Frequency = 67.39\ KHz$$
$$\alpha = f \times R \times C$$
$$\alpha = 1.48$$

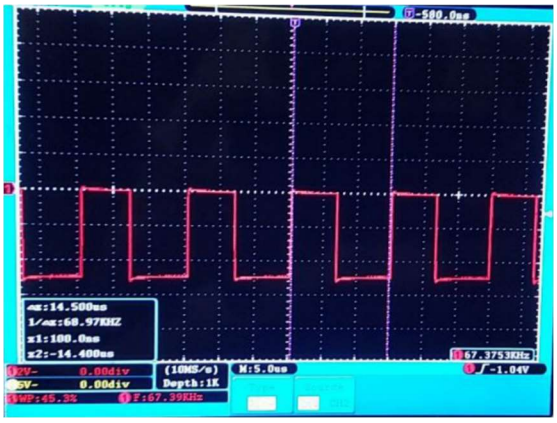


Fig. 4 Part C: R=2.2k

R	**α**
470 Ω	1.32
1000 Ω	1.38
2200 Ω	1.48

Table 2

D. Synchronous Counter as a Frequency Divider

In this part we want to make a divide by 200 synchronous up-counter using two 74LS193 (4-bit up/down counter) ICs and 74HC008 IC and the ring oscillator that we made in part 1.

For making a divide by 200 synchronous up-counter we need to cascade two 4-bit up/down counters. The counting range of this 8-bit counter is 0 to 255. So to make a divide by 200 synchronous up-counter we have to load 56 to two cascaded ICs like the figure below.

initial value = Maximum value – Modulus

256-200 = 56

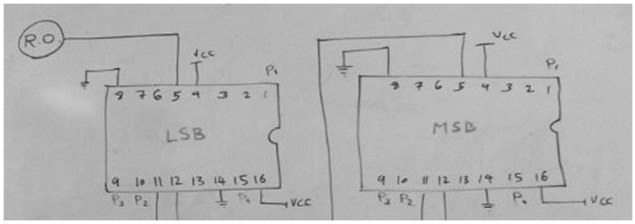


Fig. 6 Frequency divider using 74

56 in binary is 00111000 so we need to load 0011 to MSB and 1000 to LSB.

We connected pin5 of LSB to our ring oscillator.

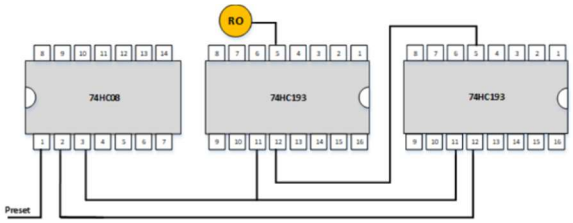


Fig. 7 Frequency divider

We use Preset to initialize the counter to 0 so first, we connect it to GND, and then we switch it to VCC, and then the counter will start counting.

We connect the preset to pin1 of 74HC008 because this IC can behave like an AND gate.

pin1 & pin2 = pin3

if pin 1(preset) is 0 then the output will be 0

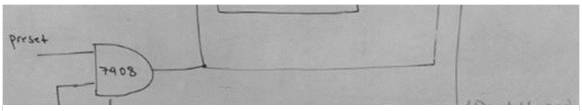


Fig. 8 how to use 74HC08

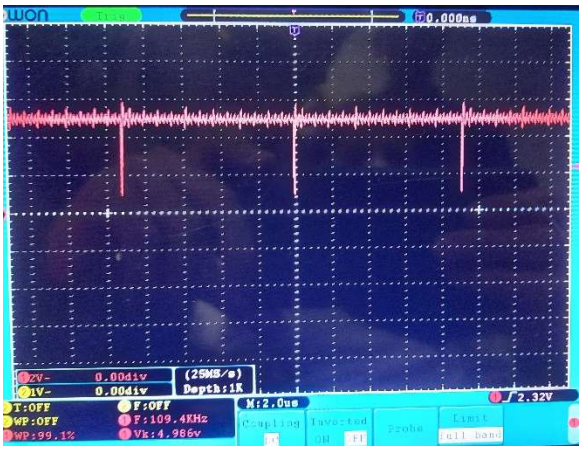


Fig. 9 part D: result Frequency divider

Fig. 10 Part E: resulte

We can see the frequency of ring oscillator in part1(21.74 MHz) is approximately divided by 200.

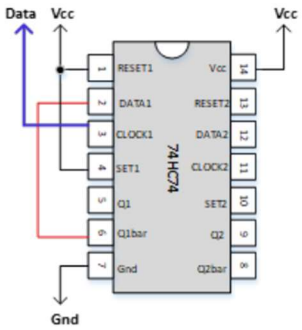
$$\frac{21.7\ MHz}{109.4\ KHz} = 198.7 \approx 200$$

E. T Flip-Flop

In this part we use a T Flip-Flop after counter to produce a 50 percent duty cycle signal.

We use a D Flip-Flop (74HC74 IC) for this purpose, so we have to convert it to T Flip-Flop like the circuit below.

The Data pin is connected to carry-out of the divide by 200 synchronous up-counter.



As we can see the frequency of the divide by 200 synchronous up-counter that we made in part D is approximately halved.

$$\frac{109.4\ KHz}{54.57\ KHz} \approx 2$$

Also we can see duty cycle of this signal is 50%.

As we know the output frequency of a T Flip-Flop is one-half of the clock frequency and this is the reason that why the frequency of divider was halved.

III. Conclusion

Well, in this experiment we've learned how to use 74 series ICs and LM555, and learned how to generate different method of clock signal and create Frequency Divider and T Flip-Flop with thies ICs.