



B. TECH - CE - V - 2012
DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [Computer Engineering]
SUBJECT: (CE-502) Microprocessor Fundamentals and Programming

Examination : External
Date : 03/12/2012
Time : 2.00 to 5.00 PM

Seat No : _____
Day : Monday
Max. Marks : 60

INSTRUCTIONS:

1. Answer each section in separate answer book.
2. Figures to the right indicate maximum marks for that question.
3. The symbols used carry their usual meanings.
4. Assume suitable data, if required & mention them clearly.
5. Draw neat sketches wherever necessary.

SECTION - I

Q.1 Do as directed.

- (a) What is radix of the number? Why hexadecimal numbers are more compact than binary number? Explain with an example [10]
[2]
- (b) Do the instruction encoding for the following [2]
1. MOV AX, [BP]+4101H
2. MOV CL, CH
- (c) Define a control word for 8255A for the following [2]
• Port B as input in mode 1, port A as output in mode 2, port C(lower) as input and port C(upper) as output.
Explain single-handshake I/O and double-handshake data transfer. [2]
- (d) Explain below instructions with an example [2]
1. ROR
2. XCHG
3. TEST
4. SCASB
- (e) Why 8086 memory bank is divided into two different banks. Explain with a neat and clean diagram. [2]

Q.2 Attempt Any TWO from the following questions.

- (a) Draw neat and clean diagram for the write machine cycle for 8086 with two continuous wait states. [10]
[5]
- (b) Write an assembly language program to print the **Fibonacci Series**. Implement a procedure called **fibProc** and pass the parameter to the procedure **through stack**. [5]
(e.g No=6, Ans: 0, 1, 1, 2, 3, 5)
- (c) Write an assembly language program to check whether the string is palindrome or not without using any temporary variable or array. [5]

Q.3 Answer the followings.

- (a) Explain working of DMA in detail with neat and clean diagram. Also explain the HRQ and HLDA pin of DMA. [10]
[5]
- (b) I. What are the differences between 8253 and 8254 programmable timer? [3]
Explain the Control Word register of 8254 in detail.
II. Write an assembly language program to find out the square root of the number. [2]

OR

Q.3 Answer the followings.

- (a) Explain the architecture of 8086 with neat and clean diagram. [10]
[5]
- (b) Write an assembly language program for the following. [5]
• Input string : The world is very **worst** with the **worst** people.
• Output string: the world is very **good** with the **good** people.
Use string operation instructions. Also print the string.

SECTION - II

Q.4 Do as directed.

- (a) What is the difference between the CPU and the Microprocessor? Can a CPU contain several processors or a processor contains several CPUs? [2]
- (b) Assume AX=F000H, BX=9015H, DX=0000H [2]
1. IMUL BX, find out the content of AX,DX
 2. IDIV BL, find out the content of AX
- (c) Identify the condition under which the content of AX would remain unchanged after execution of the instruction of that follows [2]
- MOV CL,04H
SHL AX,CL
SHR AX,CL
- (d) What is IVT? What are the interrupt vector addresses of the following interrupts in the 8086 Interrupt Vector Table? [2]
1. INTO
 2. INT 20H
- (e) Explain the use of 8251A. [2]

Q.5 Attempt *Any TWO* from the following questions.

- (a) I. Differentiate Microprocessor and MicroController. [2]
- II. **State TRUE or FALSE and Justify:** - The Microcontroller design uses multi-byte instruction compared to Microprocessor. [1]
- III. Explain type of interrupts in 8051 controller. [2]
- (b) I. Write an assembly language program (8051) for initializing timer 1 in mode 1 and check the overflow flag of timer 1 after 1/30 second elapsed. [3]
- II. Relate the following frequencies: [2]
- Crystal Freq
 - Oscilli. Freq
 - Peripheral Freq
- (c) I. Explain the Internal RAM organization in 8051 Microcontroller [3]
- II. Predict the output of AX, status of CF and AF for following code fragments. [2]
- Explain ASCII adjustment instruction in each case:-
- | | |
|--|--|
| <ul style="list-style-type: none"> • MOV AL,31h MOV BL,39h SUB AL,BL AAS | <ul style="list-style-type: none"> • MOV AL,31h MOV BL,39h ADD AL,BL AAA |
|--|--|

Q.6 Answer the followings.

- (a) Write an assembly language program to implement modulo operator (%) without using DIV instruction. Implement a procedure named **findModulo** by using register passing. [5]
- e.g Enter Dividend: 5
Enter Divisor: 2
Reminder is: 1
- (b) I. Write a program for addition of two 3x3 matrices. The matrices are stored in the form of lists(ROW MAJOR ORDER). Store the result of addition in third list. [3]
- II. Explain SEGMENT directive in details. [2]

OR

Q.6 Answer the followings.

- (a) What is interrupt vector number for interrupt which comes on INTR pin? Explain the procedure for calculating ISR address for it in details. [5]
- (b) I. Write an assembly language program for any arithmetic operation on Two numbers and also **handle overflow interrupt** (Type 4). [4]
- II. Differentiate procedure and interrupt. [1]



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
EXTERNAL EXAMINATION
SUBJECT: (CT) DESIGN & ANALYSIS OF ALGORITHM

Examination : B.TECH - Semester - V(CE/IT) Seat No. :
Date : 04/12/12 Day : Tuesday
Time : 02.00 to 05.00 Max. Marks : 60

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

SECTION-I

Q.1 Answer the following questions

[10]

- a) What is an algorithm? What are the characteristics of an algorithm?
- b) On what kind of input does the Quick sort algorithm exhibit its worst-case behavior? Why?
- c) "Dynamic programming avoid calculating the same stuff twice thus better than divide and conquer"-Justify
- d) Justify : Exhaustive search is not a good method to solve any problem
- e) What is complexity of bubble sort in Best case and worst case ?.

Q.2

[10]

- a) Write a divide & Conquer algorithm for finding Maximum and Minimum of n numbers.
- b) Solve the following recurrence using recurrence Tree method
 $T(n) = 1$ if $n=1$
 $T(n) = 7T(n/2) + 18(n/2)^2$ Otherwise

OR

Q.2

[10]

- a) Table given below shows jobs with their profit and deadlines. Using greedy approach, find optimum profit.

Job	1	2	3	4
Profit	50	10	15	30
Dead Line	2	1	2	1

- b) Solve the following recurrence

$$a_n = 6a_{n-1} - 9a_{n-2}$$

Initial Conditions : $a_0 = 1, a_1 = 6$

Q.3

[10]

- a) Write a Dynamic Programming algorithm for Making a Change Problem and find time and space complexity of algorithm
- b) Solve the given instance of Fractional knapsack problem using Greedy Method. Capacity of Knapsack is 10

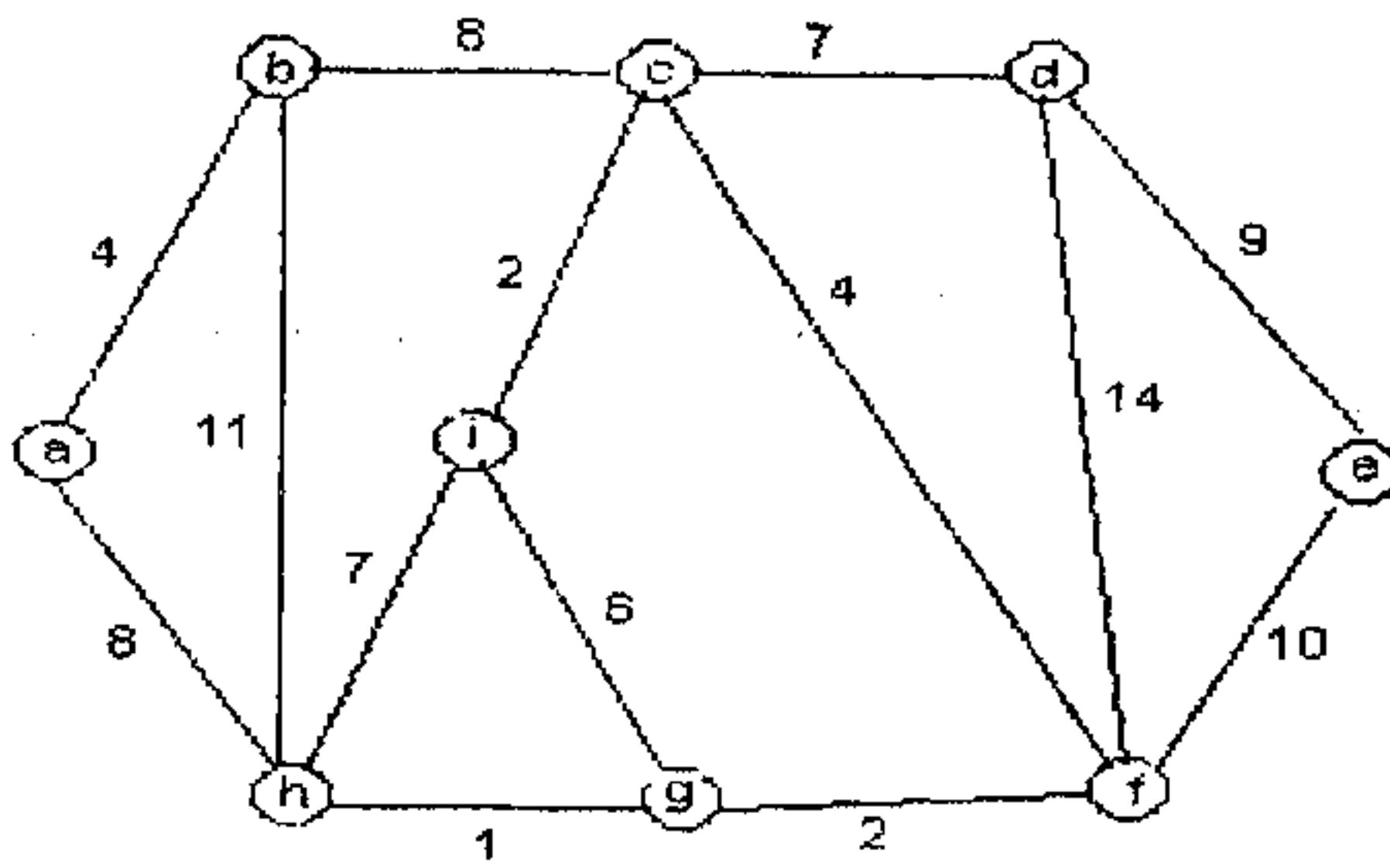
Item	Weight	Value	Value/Weight
1	4	40	10
2	7	42	6
3	5	25	5
4	3	12	4

OR

Q.3

[10]

- a) Find Longest Common Subsequence of two sequences
X: abcdace Y: badcabe
- b) Write Prim's algorithm for Minimum Spanning Tree (MST) and also find MST for given graph



SECTION -II

Q.4 Answer the following questions

[10]

- What are the issues that govern or influence the choice of either adjacency matrix or an adjacency list for storage of graphs?
- For which value of n , n -queen problem has no solution?
- Mention implicit and explicit constraints for graph coloring problem.
- Number of ways to multiply 6 matrices is _____ and Minimum number of multiplication required to find M^6 is _____ where size of M is 4×4
- Show relationship between P, NP, NP-Hard and NP-Complete

Q.5

[10]

- Write an algorithm for "Sum of Subset Problem" using Backtracking
- Find lower-bound through reduction for the given problem.
"Finding maximum and minimum element among n distinct element"

6

4

OR

Q.5

[10]

- Write a branch and bound algorithm for 0/1 knapsack problem
- Compare Deterministic & Non-Deterministic Algorithm

6

4

Q.6

[10]

- Solve 4-queen problem using backtracking
- Solve the following 15-puzzle

5

5

Initial Position			
1	3	4	15
2		5	12
7	6	11	14
8	9	10	13

Goal Position			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	

OR

Q.6

- Allocate RED, GREEN, BLUE and YELLOW colors to the squares in the following figure such that no two adjacent squares (vertical, diagonal and horizontal) contain same color *using backtracking.*

[10]

5



Use branch and bound to solve the assignment problem (Minimization) with the following cost matrices.

5

Job	1	2	3	4
Person a	94	1	54	68
Person b	74	10	88	82
Person c	62	88	8	76
Person d	11	74	81	21



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [COMPUTER ENGINEERING]
SUBJECT: (CE615) ADVANCED JAVA TECHNOLOGY

Examination : External
Date : 05/12/12
Time : 02 to 05

Seat No :
Day : Wednesday
Max. Marks : 60

INSTRUCTIONS:

1. Answer each section in separate answer book.
2. Figures to the right indicate maximum marks for that question.
3. The symbols used carry their usual meanings.
4. Assume suitable data, if required & mention them clearly.
5. Draw neat sketches wherever necessary.

SECTION - I

Q.1 Do as directed. [10]

- (a) State the usefulness of Remote interface in RMI.
- (b) Represent categorized view of J2EE Technologies.
- (c) How servlets are different from applets?
- (d) What is the difference between ServletContext and PageContext?
- (e) State comparison between RMI and JMS.

Q.2 Attempt Any TWO from the following questions. [10]

- (a) Explain life cycle of servlet with its architecture diagram.
- (b) State the difference between session cookie and persistent cookie. Also define common code which differentiates both properly.
- (c) State any six methods and its description to read HTTP Header.

- Q.3**
- (a) Write an Internationalization program where you can provide country code and the language code on the command line. And according to that code respectively it will print the message. [5]
 - (b) Write a servlet that takes student id and password as input, finds result of authenticated student from table STUDENT and calculate percentage online. This calculated percentage should be displayed to user. [5]

OR

- Q.3**
- (a) Write a servlet program for any shopping website by using cookie utility which maintains the shopping cart of user by adding the items in it from the different pages of the same site. And also it should identify the existing user, if the user has already visited once. [5]
 - (b) Write a RMI client-server application, where server enter the two values and client displays the multiplication of that two numbers. [5]

SECTION - II

Q.4 Do as directed. [10]

- (a) The term Internationalization is often abbreviated as i20n since there are 20 letters in the word "Internationalization". State TRUE/FALSE. Justify your answer.
- (b) List the various implicit objects available in a JSP.
- (c) What is the difference between include standard action and include directive?
- (d) What is the difference between `${ myBean["property"] }` and `$ {myBean[property]}` ?
- (e) State the procedure when web server is started, after declaring a custom tag library.

Q.5 Attempt Any TWO from the following questions.

[10]

- (a) Explain the life cycle of Simple Custom Tag.
- (b) Give example code for explaining each feature of Spring framework.
- (c) Explain the execution of Struts application by showing its diagram.

Q.6 (a) Write an application(jsp file,tag handler and tld file) for creating a custom tag which [5]
prints the Fibonacci series for any given number.

- (b) Implement a scriptless JSP to test whether the id and password are valid or not. [5]**
Compare provided id and password with id and password set as init parameter for that JSP. Also implement an error page for null pointer exception.

OR

Q.6 (a) Implement a tag file named paint having attributes color and text. When the tag is [5]
invoked, it displays the passed text in mentioned color. Implement all supporting components for the tag file.

- (b) Implement a web application in which one filter is provided to check for username and [5]**
password. If username and password match with context init param, unname and pwd then display servlet with user information and "Greeting message" otherwise display "Sorry message".



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [C.E.]
SUBJECT: (CE 616) ADVANCED VISUAL TECHNOLOGY

Examination : Regular
Date : 05/12/12
Time : 02 to 05

Seat No : _____
Day : Wednesday
Max. Marks : 60

INSTRUCTIONS:

1. Answer each section in separate answer book.
2. Figures to the right indicate maximum marks for that question.
3. The symbols used carry their usual meanings.
4. Assume suitable data, if required & mention them clearly.
5. Draw neat sketches wherever necessary.

SECTION - I

Q.1 Do as directed.

[10]

- (a) List the benefits of using ADO.NET in framework 4.0.
- (b) How to place comment between ASP.NET Tags?
- (c) How to check if a Textbox contains a valid date?
- (d) List the uses of Appsetting section in Web.config file.
- (e) What is Absolute and Sliding Expiration in .NET?

Q.2 Attempt *Any TWO* from the following questions.

[10]

- (a) Write a code along with proper explanation which displays visitor count on header of web page.
- (b) What is cross-page posting? Write a code to explain the concept.
- (c) Explain the different ways to use unmanaged code in managed code

- Q.3** (a) Explain in detail about constituent of .NET platform. [5]
(b) What is application-level event? List and Describes them. [5]

OR

- Q.3** (a) "*A strict relationship doesn't exist between assemblies and namespaces.*" Elaborate the statement with proper example. [5]
(b) Describe different Authorization Rules. [5]

SECTION - II

Q.4 Do as directed.

[10]

- (a) What is the use of Trim function in C#? List different variants of it
- (b) List the benefit of using *param* keyword in C# and show how to use it programmatically.
- (c) Define: Anonymous Methods. Describe the use of it programmatically.
- (d) What is smart array? How to use it?
- (e) List the difference between Abstract Class and Interface

Q.5 Attempt *Any TWO* from the following questions.

[10]

- (a) Explain component based programming along with three tier design approach
- (b) Explain the concept of custom exception along with necessary code.
- (c) Explain the use of partial keyword along with necessary code.

- Q.6** (a) Explain common type system architecture. [5]

- (b) "*The great majority of ASP.NET web applications use the Dataset to store data but not to make updates*" Elaborate the statement with proper reasoning. [5]

OR

- Q.6** (a) Explain simple databinding with properties with appropriate example [5]
(b) Explain in detail about working of post-back event [5]



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V (COMPUTER ENGINEERING)
SUBJECT: (CE-505) Computer Organization

Examination : Regular
Date : 08/12/12
Time : 02:00 to 05:00

Seat No. : _____
Day : Thursday
Max. Marks : 60

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

SECTION - I

- Q.1** Do as directed [10]
- a List the instruction set of the IAS computer. [1]
 - b What are microcontrollers? [1]
 - c Write the machine code for the instruction mov H,A , if the opcode $= 01_2$, the register code for $H=100_2$, and the register code for $A=111_2$. [1]
 - d What is RAW hazard? [1]
 - e Show how to design a 4×16 decoder using the 2×4 decoder as your sole building block. [2]
 - f List the advantages and disadvantages of hardwired control unit over micro programmed control unit. [2]
 - g What is precise interrupt? How it can be met? [2]
- Q-2** Attempt *Any TWO* from the following questions. [10]
- a i. Design a 4 bit comparator using 4-bit parallel adders. [3]
ii. What are vectored interrupts? How can vectored interrupts implemented? [2]
 - b Implement a control unit for GCD processor using classical method. [5]
 - c i. What are the various bus arbitration techniques? Explain them in brief. [3]
ii. Compare and contrast the CSMA/CD and token passing network techniques. [2]
- Q.3** a Consider the pipelined multiply and add instructions. Suppose that the number of execution stages of multiply are six and the number of execution stages of add are two. Consider execution of the following three instruction code segment. [3]
- $R1=R4 * R0;$
 $R2=R4 + R6;$
 $R3=R2 * R5;$
- i. What is the minimum number of cycles to process this code with out-of-order completion allowed?
 - ii. What is the minimum number of cycles to process this code with in-order completion? Draw the space timing diagram for both the conditions?
- b. Implement a program control unit for the accumulator based processor using one hot method. [7]
- OR**
- Q.3** a Write short note on DMA and interrupts [5]
- b What is nanoprogramming? Show how nanoprogramming reduces the control memory space of the control unit. [3]
- c A 128MB RAM is to be designed from $2M \times 4$ - bit RAM ICs. Assume that 1 out of 2^k decoder ICs are also available for $k \leq 3$, as well as ICs containing standard logic gates. Show the necessary connections. [2]
- SECTION - II**
- Q.4** Do as directed. [10]
- (a) System A has stored 4 bytes data "UNIX" as two shorts and when system B tries to read it, it find as "NUXI". Why so happen? Explain. [2]

- (b) DDU R&D dept. has implemented 8-bit adder composed of 4-bit adders linked by carry look-ahead, explain the carry generation logic for the given input values by propagating proper values into stages. $X[7:0]=[10010101]$, $Y[7:0]=[01111010]$ [2]
- (c) Why are there separate L1 caches for instruction and data? [2]
- (d) Client is sending data to server. Received data at server is "01101110" and the syndrome word computed at server is 1000. So, is there any error in the data received at server? If, yes then write down the corrected data. [2]
- (e) What is the effective memory access time if the cache access time is 15nsec, main memory access time is 10 times of cache access time, cache hit ratio is 90%? [2]

Q.5 Attempt *Any TWO* from the following questions. [10]

- (a) i. An instruction is stored at location 300 with its address field at location 301, the address field has value 400, register R1 contains the number 200, evaluate the effective address for following addressing modes. Direct 2. Immediate 3. Relative 4. Register Indirect 5. Index(R1 is index Register). [3]
- ii. How many minimum number of RISC instruction set instruction are required to perform addition? Specify the instruction as well [2]
- (b) Consider the following page address trace generated by a two level cache- main memory scheme that uses demand paging and has a cache capacity of three pages. [5]
pages: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1
Which of the page replacement policies FIFO or LRU or OPT is more suitable in this case? Show your calculations, and give a short intuitive justification of your answer
- (c) Suppose, you are appointed as a system architect of research division in your company. Design the proper processor based on the following requirements of your System. Specify the processor component which you are using. Justify your design perspective in terms the usage of particular processor component. [5]
Requirements:
i] Space for higher level memory is very much larger irrespective of low level memory.
ii] Address mapping must be quick.
iii] System is having shared environment.
iv] Data transfer between memory levels must be simplified.
v] Higher priority application can preempt the execution of lower priority application.

- Q.6 (a) Differentiate Paging and Segmentation and explain the working of TLB. [5]
- (b) i. Convert floating point decimal 12.375 into binary using IEEE 754 format. [4]
- ii. What is the disadvantage of using TAG? [1]

OR

- Q.6 (a) i. What is meant by locality of reference? [1]
- ii. Advantage of combination ALU over the sequential ALU [2]
- iii. Match the following. [2]

Control Unit	Controllers
ALU	Transistors
Disk	Adders
Memory	Decoders

- (b) Derive the equation for the access efficiency (e) of the two level memory. [3]
- (c) Derive the equation for finding the optimum space utilization and optimum page size. [2]



DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER V [CE]

Examination : External

Date : 07/12/2012

Time : 2:00 to 5:00

Seat No : _____

Day : Friday

Max. Marks : 60

SUBJECT: (CE-407) DATABASE SYSTEMS

INSTRUCTIONS:

1. Answer each section in separate answer book.
2. Figures to the right indicate maximum marks for that question.
3. The symbols used carry their usual meanings.
4. Assume suitable data, if required & mention them clearly.
5. Draw neat sketches wherever necessary.

SECTION - I

Q.1 Do as directed.

[10]

- (a) Let Relation schema $R=(A,B,C,D,E)$. The set of functional dependencies is $\{ AB \rightarrow C, CD \rightarrow E \}$. Using Armstrong's Axioms Prove that ABD is a key. [2]
- (b) Explain the difference between physical and logical data independence. [1]
- (c) Differentiate these terms: [4]
 - 1) Generalization and Specialization
 - 2) Deferred and Immediate database modification
 - 3) Strong and Weak Entity Set
 - 4) Serial schedule and Serializable schedule
- (d) Since every conflict-serializable schedule is view serializable, why do we emphasize conflict serializability rather than view serializability? [1]
- (e) Who is DBA? State the function of DBA. [2]

Q.2 Attempt Any TWO from the following questions.

[10]

- (a) What is a recoverable schedule? Why is recoverability of schedules desirable? Are there any circumstances under which it would be desirable to allow non-recoverable schedules? Explain your answer.
- (b) Explain the purpose of the checkpoint mechanism. How often should checkpoints be performed? How does the frequency of checkpoints affect
 - 1) System performance when no failure occurs
 - 2) The time it takes to recover from a system crash
 - 3) The time it takes to recover from a disk crash
- (c) Compare the shadow-paging recovery scheme with the log-based recovery schemes in terms of ease of implementation and overhead cost.

Q.3 (a) Create an ER diagram, complete with attributes, keys and constraints, for the following description of albums: [6]

Each musician has a name, address and phone number. Each instrument that is used in songs has a name (e.g. flute, guitar). Each Album has a title, a copyright date, a format (e.g. CD or MC) and an album identifier. Each song has a title and an author. Each musician may play several instruments and a given instrument may be played by several musicians. Each album has a several songs on it but no song can appear on more than one album. Each song is performed by one or more musicians and a musician may perform a number of songs.

- (b) Let Relation schema $R=(A,B,C,D)$. The set of functional dependencies is $\{ A \rightarrow B, B \rightarrow C \}$ and the decomposition of R: $R_1 = (A, C, D), R_2 = (A, B)$. [4]
 - 1) Decompose R into a set of Boyce-Codd relations which constitute a lossless join decomposition.
 - 2) Is the decomposition dependency preserving? Justify.