3E1203

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B.Tech. III-Sem. (Main/Back) Examination, January - 2025

Artificial Intelligence and Data Science

3AID3-04 Digital Electronics

AID, CAI, CS, IT

Time : 3 Hours **Maximum Marks : 70**

Instructions to Candidates:

Attempt all Ten questions from Part A, Five questions Out of seven questions from Part B and three questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

PART - A

(Answer should be given upto 25 words only)

All questions are compulsory.

1. State and prove De Morgan's theorem. **(10×2=20)**
2. Convert the following.
   a) $(BC)_{16} = (\ )_{10}$
   b) $(1000011)_2 = (\ )_{10}$
3. Perform the following (a) Subtraction using 9's complement for the given.
   54321 - 41245
4. Convert the following to binary and then to gray code. $(1111)_{16}$
5. Explain the Binary Codes.
6. Mention the types of counter
7. What is a flip-flop?
8. Write about Gray to the binary convertor.
9. Explain briefly about the S-R flip-flop
10. Write a comparison of various logic families.

PART-B

(Analytical/Problem solving questions)

Attempt any Five questions. **(5×4=20)**

1. Explain the:
   a) Encoder -Decoders
   b) BCD to 7 segment decoder.
2. What do you mean by digital system? Explain the characteristics of digital systems.
3. Explain half adder? Implement the full adder using two half adders.
4. Explain the working of Master Slave flip flop and discuss the Race around problem.
5. Implement the following Boolean function using 8:1 multiplexer $F(A,B,C,D) = \Sigma m$ (0,1,2,5,7,8,9,14,15)
6. Discuss the following concerns with Logic Families and Semiconductor Memories:
   a) Noise margin
   b) Propagation delay
   c) Fan-in, Fan-out.
7. Draw and explain the 4-bit Universal shift register.

PART-C **(3×10=30)**

(Desriptive/Analytical/Problem Solving/ Design question)

Attempt any Three questions.

1. Discuss the Quine Mccluskey (Tabulation) method using suitable example.
2. Simplify the Boolean expression using K-map and implement using NAND gates $F(A,B,C,D) = \Sigma m(0,2,3,8,10,11,12,14)$
3. Design a Mod-10 Asynchronous counter using J-K FFs.
4. Draw and explain the following using truth table and logic diagrams
   a) J-K Flip flop
   b) D- Flip Flop
   c) T- Flip flop
5. Write a short note on:
   a) TTL Logic
   b) ECL
   c) CMOS Digital logic families.