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CS 472 HW 3

(3.1) Why is the program counter a *pointer* and not a *counter*?

- If the program counter was a *counter*, the instructions would have to be sequential. Since the program counter is a *pointer*, the instructions can be located in any order since the PC simply gets the next address, enabling branching.

(3.2) Explain the function of the following registers in a CPU:

- PC (program counter): The PC holds the address of the *next* instruction to be fetched from memory
- MAR (memory address register): the MAR holds the address of the memory location that is being accessed for reading/writing during the current execute cycle
- MBR (memory buffer register): the MBR holds the data that was read from or is about to be written to the location pointed to by the address in the MAR
- IR (instruction register): the IR holds the instruction being currently executed

(3.3) For each of the following 6-bit operations, calculate the values of the C, Z, V, and N flags.

(3.10) Why does the ARM provide a reverse subtract instruction *RSB r0, r1, r2* that implements *[r0] = [r2] - [r1]* when the normal subtraction instruction *SUB r0, r2, r1* will do exactly the same job?

- Both operations only allow the last operand to be a flexible value. Flexible operands can be constants or registers with applied shifts, instead of just registers. In this example, SUB allows r1 to be flexible, while RSB allows r2 to be flexible.

(3.17) ARM instructions have a 12-bit literal. Instead of permitting a word in the range 0 to 2^{12}-1, the ARM uses an 8-bit format for the integer and a 4-bit alignment field that allows the integer to be shifted in steps of 2. What are the advantages and disadvantages of this mechanism in comparison with a straight 12-bit integer?

- The advantage is that the form is $(8 - bit) \times 2^{4-bit}$ allows for numbers larger than 2^{12}-1. The disadvantage is that not all numbers between 255 and 255×2^{15} cannot be represented because not all numbers are multiples of this form.