Name: **CS/ECE 472/572 Midterm 2**

ID#:

1. (10 points) 9.23 When a CPU writes to the cache, both the item in the cache and the corresponding item in the memory must be updated. If data is not in the cache, it must be fetched from memory and loaded in the cache. If t_1 is the time taken to reload the cache on a miss, show that the effective average access time of the memory system is given by
   $t_{ave} = ht_c + (1-h)t_m + (1-h)t_1$

- Assuming the cache does not have to be reloaded, the average access time is equal to
  $t_{ave} = ht_c + (1-h)t_m$
  In this case, the cache does take time to reload. For a single access, the time taken to reload the cache must be added to the no-miss access time. Since we are concerned about the average time, the cache reload time multiplied by the cache miss ratio must be added to the prior equation. This gives us
  $t_{ave} = ht_c + (1-h)t_m + (1-h)t_1$
  which is the hit ratio multiplied by the cache access time plus the miss ratio multiplied the memory access time plus the miss ratio multiplied by cache reload time.

2. (10 points) 9.26 A system has a level 1 cache and a level 2 cache. The hit rate of the level 1 cache is 90%, and the hit rate of the level 2 cache is 80%. An access to level 1 cache requires one cycle, an access to level 2 cache requires four cycles, and an access to main memory requires 50 cycles. What is the average access time?

- The average access time can be expressed as a sum of the various access times multiplied by their respective occurrence rates:
  $t_{avg} = h_1 t_{c1} + (1-h_1)h_2 t_{c2} + (1-h_1)(1-h_2)t_m$ where h_1 is the l1 cache hit rate, h_2 is the l2 cache hit rate, t_{c1} is the l1 cache access time, t_{c2} is the l2 cache access time, and t_m is the main memory access time. On average, the l1 cache access occurs as frequently as the l1 hit rate, the l2 cache access occurs as frequently as the l1 miss rate, and the main memory access occurs as frequently as the l2 miss rate and the l1 miss rate. Plugging in values gives:
  $t_{avg} = .9 \times 1 + .1 \times .8 \times 4 + .1 \times .2 \times 50 =$ **2.22 cycles**

3. (10 points) 9.35

4. (10 points) Assume a 64-bit virtual address and a 64-bit physical address. The page size is 4KB. How many total entries are there in the page table? Express your answer in powers of 2.

5. (10 points) 7.16

6. (10 points) 9.12

7. (10 points) 7.18

8. (10 points) 6.13

9. (15 points) 7.35

10. (15 points) 7.38