ECE411 MP3 CP3 Report

Group: ZerotoOne

TA meeting:
We met our TA, Ahmed, during this checkpoint period. The following are some of the useful advice and design recommendations that we received:

1. Put the branch resolver unit in the ALU/EX stage
2. Pipeline the L2-arbiter unit
3. Recommend the size of the victim buffer to be 4-cache-line and put it between L2 and pmem
4. Build the performance buffer that counts
    a. Number of stalls
    b. Number of cache miss in 3 caches
    c. Number of miss predictions
    d. Conflict arbiter
    e. Number of miss cycles/number of memory access cycles

    And make this unit a memory mapped unit. Map this performance buffer to the biggest address memory location.
5. Build our own test code:
    a. Use loops to check branch prediction
    b. Access memory in various patterns to check prefetch/cache replacement policy/eviction buffer

Progress Report:
By checkpoint 3, we successfully add the L2 cache into cache hierarchy. This addition decrease the maximum frequency by a considerable degree. We decide to pipeline the L2 cache to burst the frequency. We also complete the branch resolver and the forwarding unit. We test its functionality through the given test code.

Besides the implemented functionalities, the design of the following parts are completed and ready to be implemented:

1. Performance unit
2. Branch predictor
3. Eviction buffer

Contribution:
Haichuan Xu: L2 unified cache implementation and debugging
Haiyang Zhang: complete forwarding unit and debugging
Yuan Ma: complete the branch resolver and debugging

Roadmap:
By checkpoint 4, we expect:

1. Finishing the design of some advanced cache features: eviction buffer and victim cache
2. Add performance unit to the system.

3. Pipeline the L2 cache to improve the max frequency.
4. Add the performance unit.