**CS-320 – Fall 2018   
Homework Assignment 5 – Due: Tuesday, March 30th at the beginning of the lab**

The goal of this assignment is to trace the execution of the following code fragment through an out-of-order processor pipeline on a cycle-by-cycle basis. During each cycle of execution, you need to show the state of the key processor structures used to support out-of-order execution according to the instructions given below. PLEASE TYPE YOUR ANSWERS AND USE THE ANSWER FORMAT PROVIDED BELOW. WE WILL NOT ACCEPT HAND-WRITTEN ANSWERS FOR THIS ASSIGNMENT.

Code fragment:

I1: DIV R1, R2, R3

I2: STUR R4, R5, #50

I3: ADD R7, R1, R5

I4: OR R1, R5, R2

I5: LDUR R4, R6, #25

I6: SUB R3, R1, R4

Assume that two execution units (ALUs) are available: one to execute the DIV instruction, and one to execute all other instructions. Assume that the execution latency of DIV instruction is 7 cycles, and that the execution latency of all other instructions is 1 cycle. Assume that all memory accesses take a single cycle and that *the LOAD instruction (I5) loads from the same address that the STORE instruction (I2) writes into*. Further assume that this code is executed on an out-of-order pipeline with register renaming and the following pipeline stages are used: fetch, decode, renaming, scheduling, execution (one or more cycles), memory access, writeback and commit. Assume that all registers are maintained inside a physical register file and that commit-time rename table is used to detect which physical registers represent the mapping of each ISA register at each instruction’s commit.

Assume that the initial state of the front-end rename table is such that logical register R0 maps to physical register P0, R1 maps to P1, R2 maps to P2, … R31 maps to P31 for all logical registers. Assume that 40 physical registers are available and that registers 32 to 40 are in the free list.

Trace the execution of the above code through this pipeline on a cycle-by-cycle basis and determine how many cycles are required to execute this code fragment. For each cycle, show the state of the front-end rename table, the commit-time-rename table, the instruction queue, the reorder buffer, the load/store queue, and the free list of registers. Also indicate what pipeline stage each instruction is in at every cycle. Explicitly show how the physical registers are deallocated!

Example for the first cycle is given below. You can simply replicate it for the subsequent cycles and fill in the structures with the new values. Please provide your answers such that each cycle is shown on a separate page. If nothing changes in a given cycle from the previous cycle, you can skip that cycle in your answer. (Yes, there will be quite a few pages in your submission).

**Cycle 1:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I1 |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail |  |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | head  tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P32 | P33 | P34 | P35 | P36 | P37 | P38 | P39 | P40 |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 2:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I2 |
| Decode | I1: DIV R1, R2, R3 |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail |  |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | head  tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P32 | P33 | P34 | P35 | P36 | P37 | P38 | P39 | P40 |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 3:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I3 |
| Decode | I2: STUR R4, R5, #50 |
| Rename | I1: DIV P32, P2, P3 |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail |  |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | head  tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P33 | P34 | P35 | P36 | P37 | P38 | P39 | P40 |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 4:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I4: |
| Decode | I3: ADD R7, R1, R5 |
| Rename | I2: STUR P4, P5, #50 |
| Scheduling | I1: DIV P32, P2, P3 |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I1 |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Head/Tail |  |  |  |  |  |  |  |  |
| Instruction | I1 |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | head  tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P33 | P34 | P35 | P36 | P37 | P38 | P39 | P40 |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 5:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I5: |
| Decode | I4: OR R1, R5, R2 |
| Rename | I3: ADD P33, P32, P5 |
| Scheduling | I2: STUR P4, P5, #50 |
| Execution | I1: DIV P32, P2, P3…cycle 1 |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I2 |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail | Head |  |  |  |  |  |  |  |
| Instruction | I2 | I1 |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I2 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P34 | P35 | P36 | P37 | P38 | P39 | P40 |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 6:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | I6: |
| Decode | I5: LDUR R4, R6, #25 |
| Rename | I4: OR P34, P5, P2 |
| Scheduling | I3: ADD P33, P32, P5 |
| Execution | **I2:** STUR P4, P5, #50 & **I1**: DIV P32, P2, P3…cycle 2 |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I3 |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  | Head |  |  |  |  |  |  |
| Instruction | I3 | I2 | I1 |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I2 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P35 | P36 | P37 | P38 | P39 | P40 |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 7:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | I6: SUB, R3, R1, R4 |
| Rename | I5: LDUR P35, P6, #25 |
| Scheduling | **I4:** OR P34, P5, P2 & **I3**: ADD P33, P32, P5 |
| Execution | I1: DIV P32, P2, P3…cycle 3 |
| Memory Access | I2:STUR P4, P5, #50 |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P3 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I4 | I3 |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  | Head |  |  |  |  |  |
| Instruction | I4 | I3 | I2 | I1 |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I2 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P36 | P37 | P38 | P39 | P40 |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 8:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | I6: SUB, P36, P34, P35 |
| Scheduling | **I5:** LDUR P35, P6, #25 & **I3**: ADD P33, P32, P5 |
| Execution | **I4:** OR P34, P5, P2 & **I1:** DIV P32, P2, P3…cycle 4 |
| Memory Access | Empty |
| Writeback | I2:STUR P4, P5, #50 |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I5 | I3 |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  | Head |  |  |  |  |
| Instruction | I5 | I4 | I3 | I2 | I1 |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I5 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 9:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | I6: SUB, P36, P34, P35 & **I3**: ADD P33, P32, P5 |
| Execution | **I5:** LDUR P35, P6, #25 & **I1:** DIV P32, P2, P3…cycle 5 |
| Memory Access | I4: OR P34, P5, P2 |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I6 | I3 |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I5 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 10:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | **I6:** SUB, P36, P34, P35 & **I3**: ADD P33, P32, P5 |
| Execution | I1: DIV P32, P2, P3…cycle 6 |
| Memory Access | I5: LDUR P35, P6, #25 |
| Writeback | I4: OR P34, P5, P2 |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I6 | I3 |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction | I5 |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 11:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | **I6:** SUB, P36, P34, P35 & **I3**: ADD P33, P32, P5 |
| Execution | I1: DIV P32, P2, P3…cycle 7 |
| Memory Access | Empty |
| Writeback | I5: LDUR P35, P6, #25 |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I6 | I3 |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 12:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | I3: ADD P33, P32, P5 |
| Execution | I6: SUB, P36, P34, P35 |
| Memory Access | I1: DIV P32, P2, P3 |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | I3 |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 13:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | I3: ADD P33, P32, P5 |
| Memory Access | I6: SUB, P36, P34, P35 |
| Writeback | I1: DIV P32, P2, P3 |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P1 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 |  |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None this cycle

**Cycle 14:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | I3: ADD P33, P32, P5 |
| Writeback | I6: SUB, P36, P34, P35 |
| Commit | I1: DIV P32, P2, P3 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  |  | Head |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 | I1 |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* P1

**Cycle 15:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | I3: ADD P33, P32, P5 |
| Commit | I2: STUR P4, P5, #50 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P7 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  |  | Head |  |  |  |  |
| Instruction | I6 | I5 | I4 | I3 | I2 |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 |  |  |  |  |  |  |

Registers De-allocated this Cycle:

* None

**Cycle 16:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | I3: ADD P33, P32, P5 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P32 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  |  | Head |  |  |  |  |  |
| Instruction | I6 | I5 | I4 | I3 |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 | P7 |  |  |  |  |  |

Registers De-allocated this Cycle:

* P7

**Cycle 17:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | I4: OR P34, P5, P2 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P3 |
| R4 | P4 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail |  | Head |  |  |  |  |  |  |
| Instruction | I6 | I5 | I4 |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 | P7 | P32 |  |  |  |  |

Registers De-allocated this Cycle:

* P32

**Cycle 18:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | I5: LDUR P35, P6, #25 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P3 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Tail | Head |  |  |  |  |  |  |  |
| Instruction | I6 | I5 |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 | P7 | P32 | P4 |  |  |  |

Registers De-allocated this Cycle:

* P4

**Cycle 19:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | I6: SUB P36, P34, P35 |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Head /Tail |  |  |  |  |  |  |  |  |
| Instruction | I6 |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 | P7 | P32 | P4 | P3 |  |  |

Registers De-allocated this Cycle:

* P3

**Cycle 20:**

Pipeline Stages (and instructions in them):

|  |  |
| --- | --- |
| Pipeline Stage | Instructions in this Stage |
| Fetch | Empty |
| Decode | Empty |
| Rename | Empty |
| Scheduling | Empty |
| Execution | Empty |
| Memory Access | Empty |
| Writeback | Empty |
| Commit | Empty |

Front End Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Commit Time Rename Table:

|  |  |
| --- | --- |
| Logical Register | Physical Register |
| R0 | P0 |
| R1 | P34 |
| R2 | P2 |
| R3 | P36 |
| R4 | P35 |
| R5 | P5 |
| R6 | P6 |
| R7 | P33 |

Instruction Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction |  |  |  |  |  |  |  |  |  |

Reorder Buffer:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Head /Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Load/Store Queue:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Head/Tail | Head/  Tail |  |  |  |  |  |  |  |  |
| Instruction |  |  |  |  |  |  |  |  |  |

Free List of Registers:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |
| Physical Register | P37 | P38 | P39 | P40 | P1 | P7 | P32 | P4 | P3 |  |  |

Registers De-allocated this Cycle:

* None