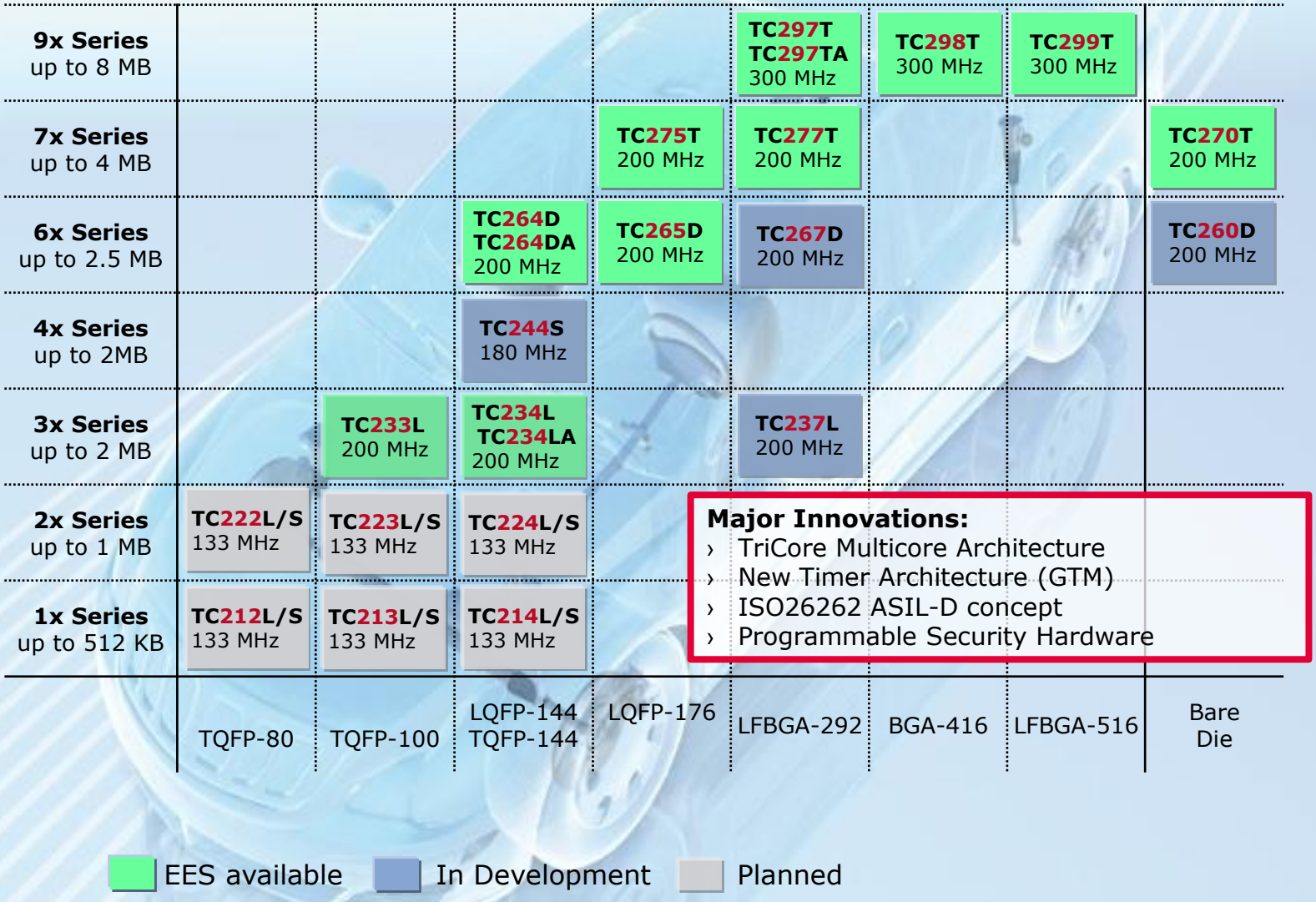
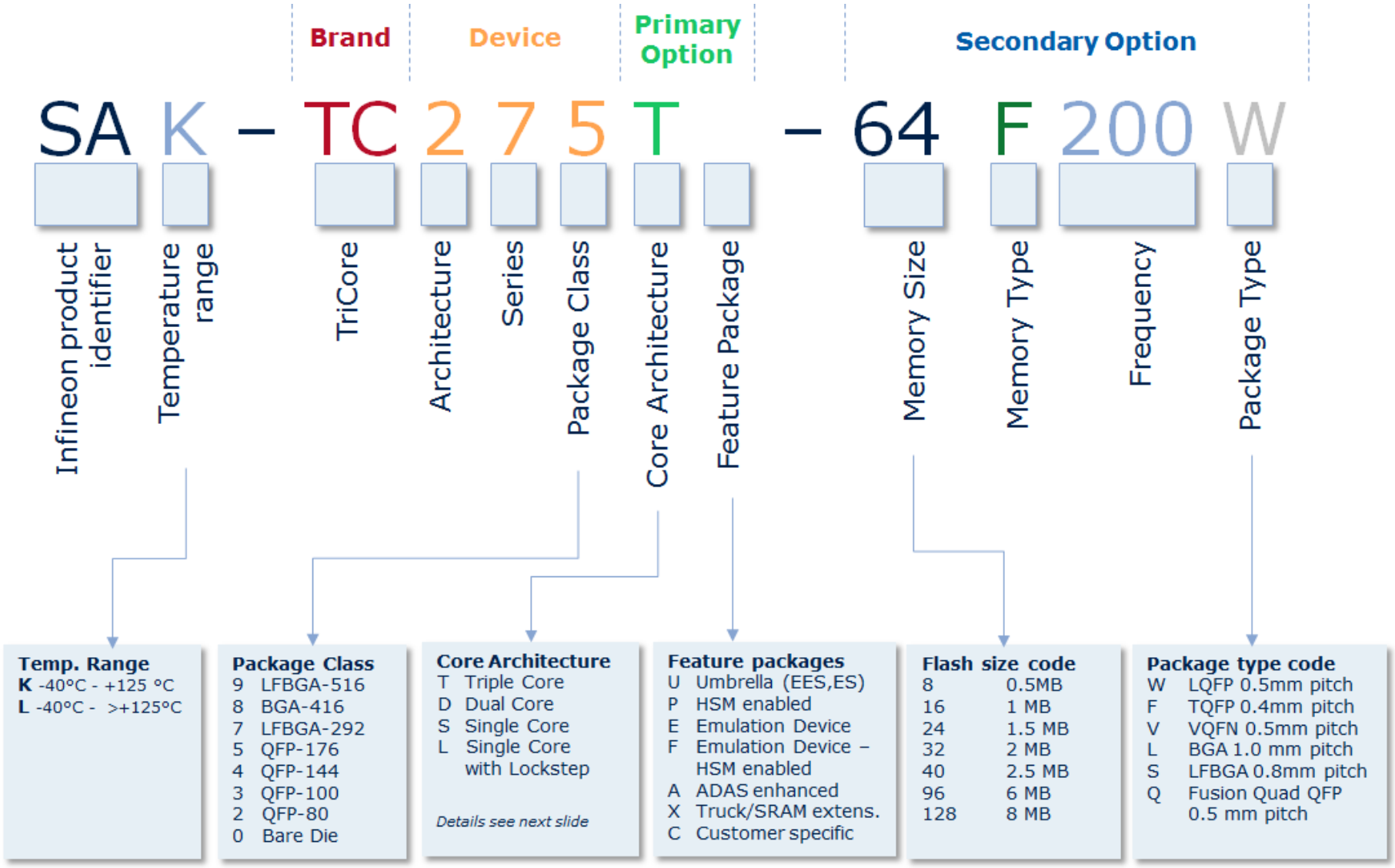
Infineon AURIX Microcontroller description

Infineon Technologies Korea

AURIX Family Overview
from low cost to high performance

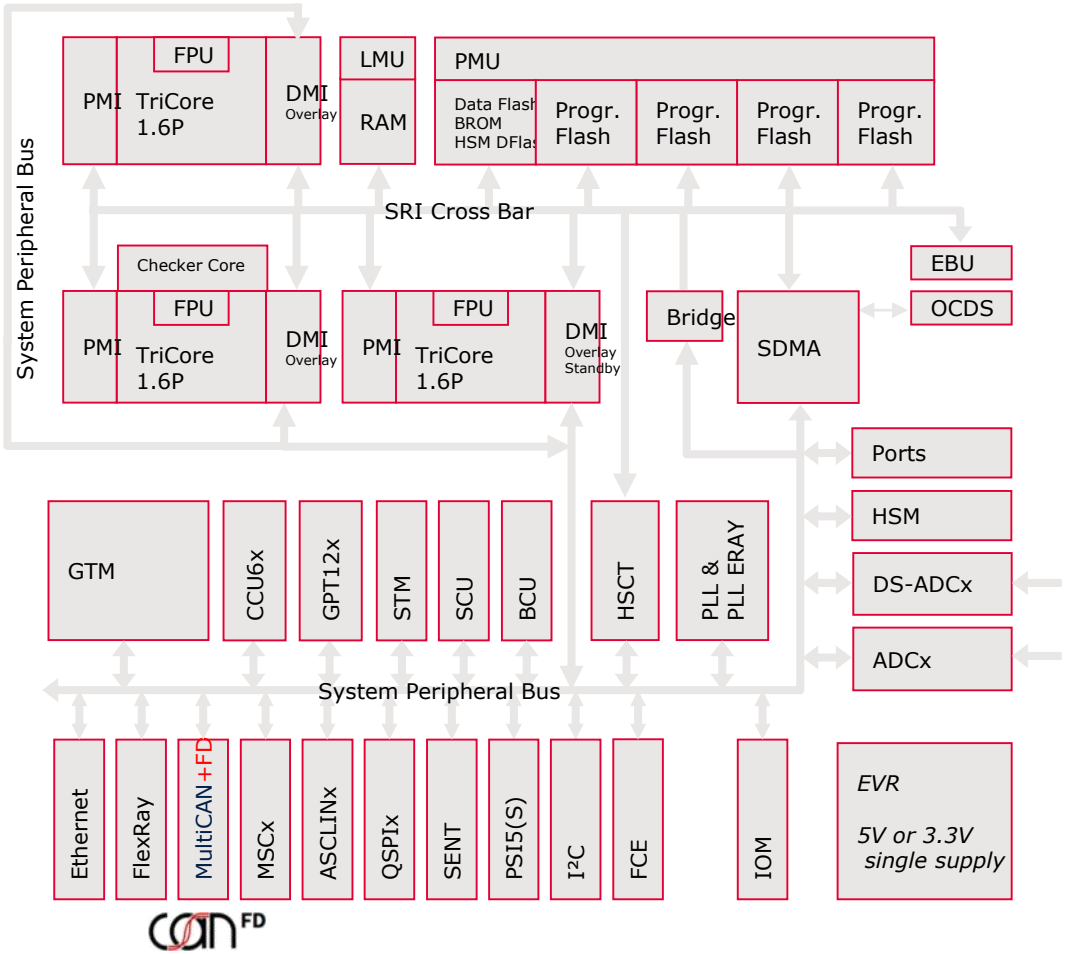


AURIX Product Naming



9x Series – Umbrella Device SAK-TC29xTP-128F300

Feature Set		9x Series
TriCore 1.6P	# Cores / Checker	3 / 1
	Frequency [2]	2x300 / 1x200 MHz
Flash	Program Flash	8 MB
	EEProm @ w/e cycles	128 KB @ 500k
SRAM	Total (DMI , PMI, LMU)	728 KB
DMA	Channels	128
ADC	Modules 12bit / DS	11 / 10
	Channels 12bit / DS	84 / 10 diff
Timer	GTM Input / Output	48 / 152 channels
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	2 / 4
	CAN-FD (nodes/obj)	6 / 384
	QSPI / ASCLIN / I2C	6 / 4 / 2
	SENT / PSI5 / PSI5S	15 / 5 / 1
	HSCT / MSC / EBU	1 / 3 diff LVDS / 1
	Other	Ethernet MAC
Safety	SIL Level	ASIL-D
Security	HSM	Yes
Power	EVR	Yes
	Standby Control Unit	Support



Package Variants

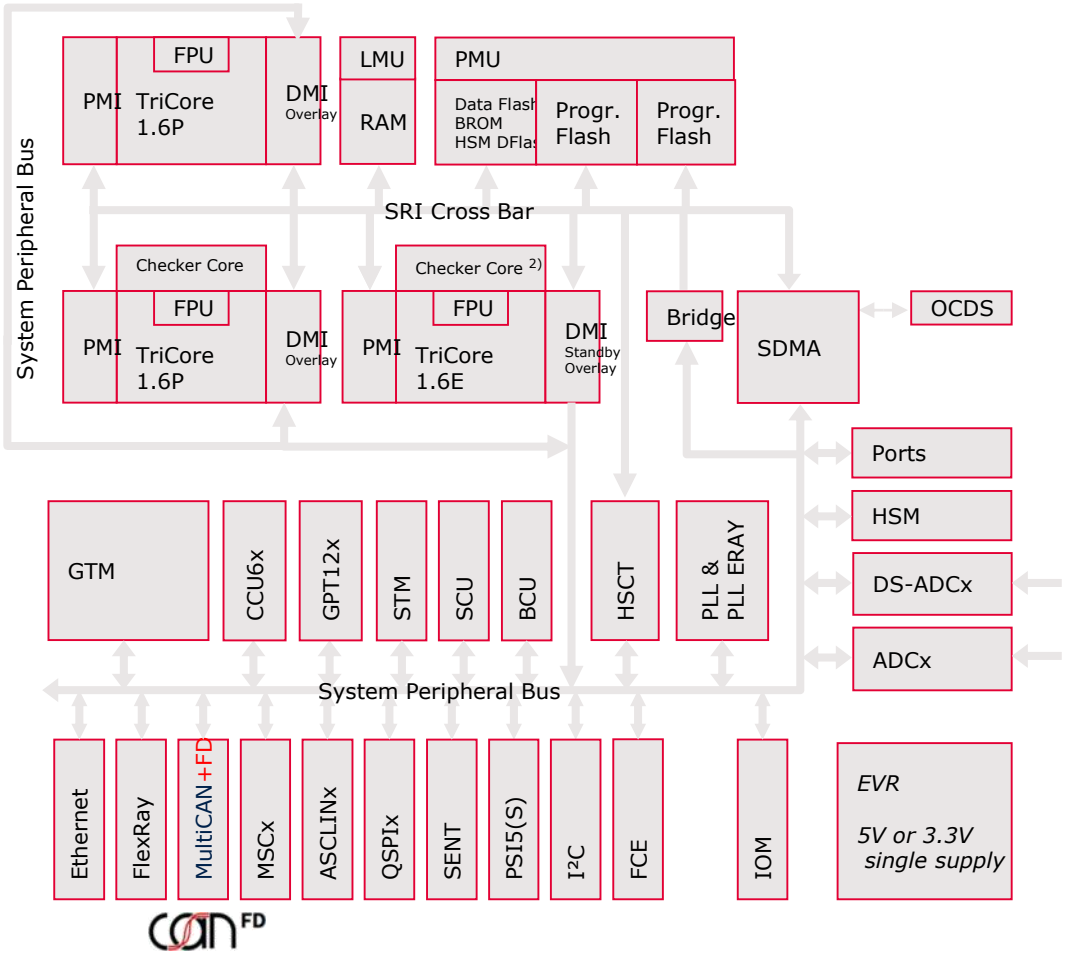
LFBGA-516	BGA-416	LFBGA-292	Bare Die
0.8mm	1.0mm	0.8mm	
-40°C to +125°C, 84 ADC inputs	-40°C to +125°C [1] 60 ADC inputs	-40°C to +125°C [1] 60 ADC inputs	Tjmax 170°C, 84 ADC inputs

1) *HOT option available on request with limited functionality >Ta=125°C*
2) *High performance version with 3x300MHz on request with specific limitations*
3) *CAN-FD in B-Step*

7x Series – Umbrella Device SAK-TC27xTP-64F200

Feature Set		7x Series
TriCore 1.6P	# Cores / Checker	2 / 1
	Frequency	200 MHz
TriCore 1.6E	# Cores / Checker	1 / 1 2)
	Frequency	200 MHz
Flash	Program Flash	4 MB
	EEProm @ w/e cycles	64 KB @ 500k
SRAM	Total (DMI , PMI)	472 KB
DMA	Channels	64
ADC	Modules 12bit / DS	8 / 6
	Channels 12bit / DS	60 / 6 diff
Timer	GTM Input / Output	32 / 88 channels
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	1 / 2
	CAN-FD (nodes/obj)	4 / 256
	QSPI / ASCLIN / I2C	4 / 4 / 1
	SENT / PSI5 / PSI5S	10 / 3 / 1
	HSCT / MSC / EBU	1 / 2 diff LVDS / -
	Other	Ethernet MAC
Safety	SIL Level	ASIL-D
Security	HSM	Yes
Power	EVR	Yes
	Standby Control Unit	Support

1) *HOT option available with limited functionality >Ta=125°C*
2) *not available on TC29x/TC26x – to be considered in SW family concept*
3) *CAN-FD in C-Step*



Package Variants

LFBGA-292
0.8mm
-40°C to +125°C
60 ADC inputs

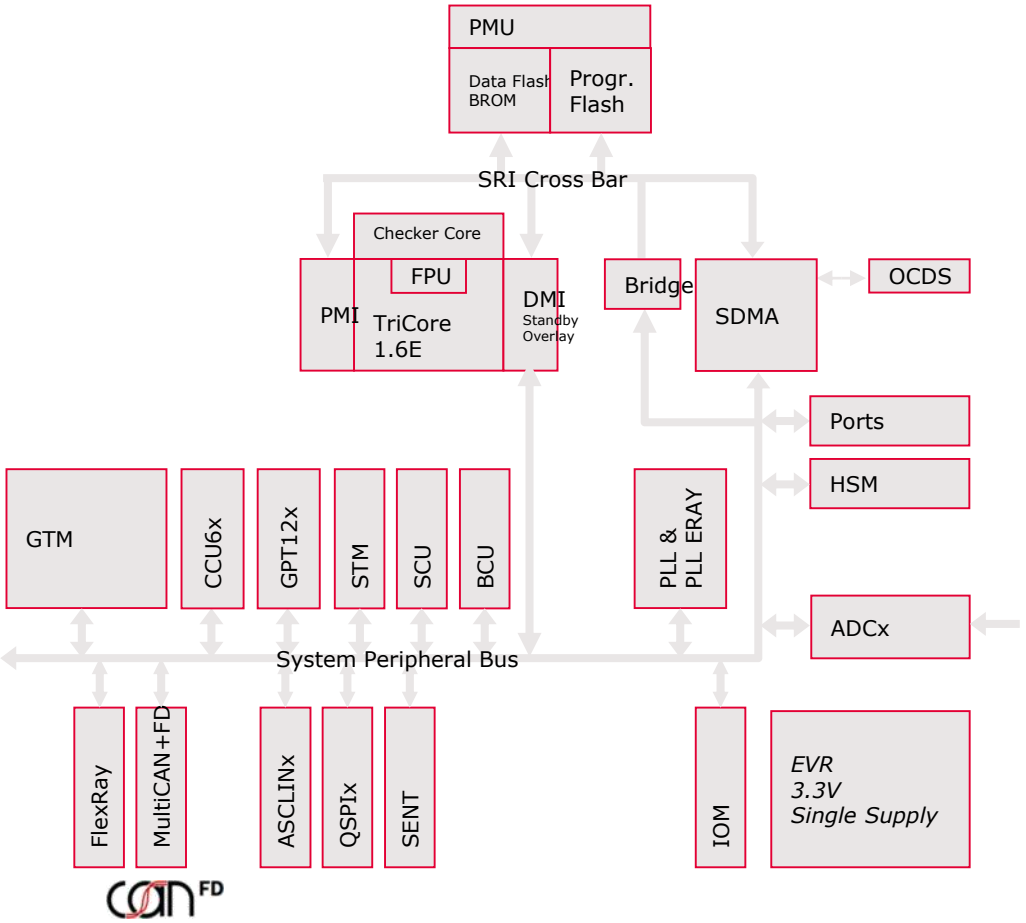
LQFP-176
0.5mm
-40°C to +125°C 1)
48 ADC inputs

Bare Die
Tjmax 170°C
60 ADC inputs

3x Series – Umbrella Device SAK-TC23xLP-32F200

		3x Series
TriCore 1.6P	# Cores / Checker	- / -
	Frequency	-
TriCore 1.6E	# Cores / Checker	1 / 1
	Frequency	200 MHz
Flash	Program Flash	2 MB
	Data Flash	128k , 125 k cycles
SRAM	Total (DMI, PMI)	192 KB
DMA	Channels	16
ADC	Modules 12bit / DS	2 / -
	Channels 12bit / DS	24 / -
Timer	GTM Input / Output	8 / 32
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	1 / 2
	CAN-FD (nodes/obj)	6 / 256
	QSPI / ASCLIN / I2C	4 / 2 / -
	SENT / PSI5	4 / -
	HSCT/ MSC / EBU	- / - / -
	Other	-
Safety	SIL Level	ASIL-D
Security	HSM	Yes
Power	EVR	Yes
	Standby Control Unit	WUT + SRAM

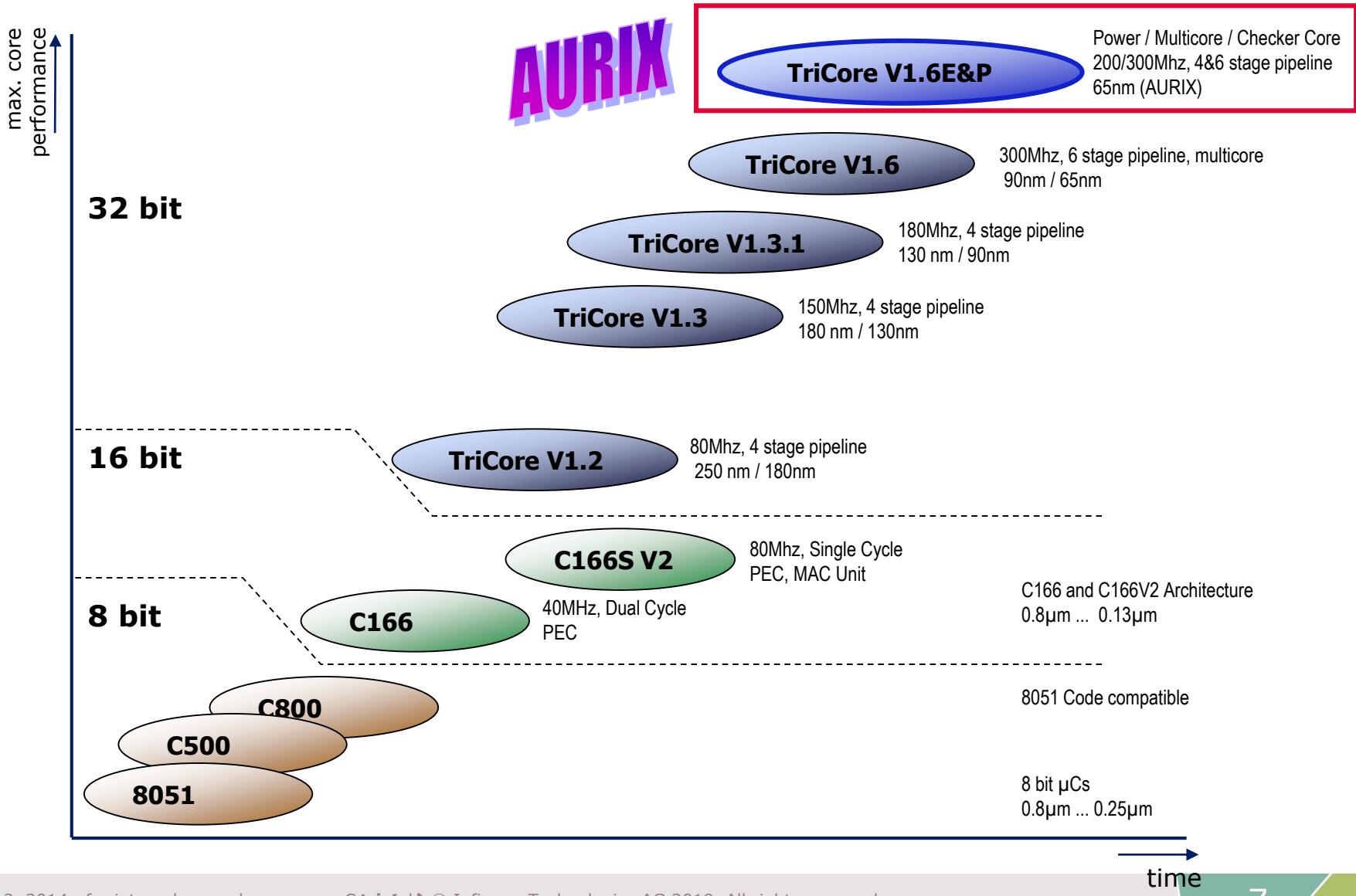
1) *HOT option available on request with limited functionality >Ta=125°C*



Package Variants

TQFP-144	TQFP-100	LFBGA-292
0.4mm	**0.4mm**	**0.8mm**
-40°C to +125°C [1)]	-40°C to +125°C [1)]	-40°C to +125°C [1)]
24 ADC inputs	24 ADC inputs	24 ADC inputs

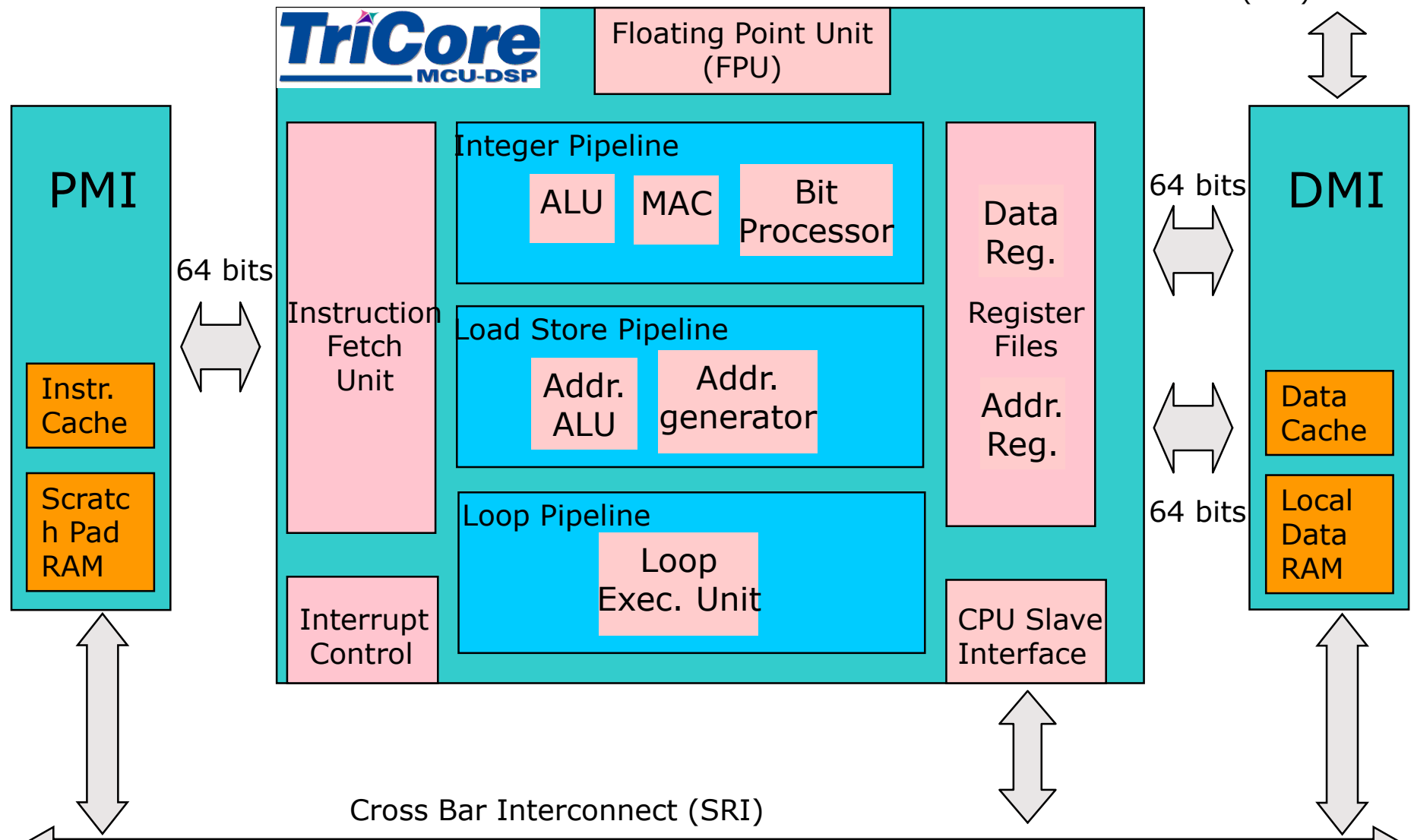
Infineon Technologies Microcontroller Core Roadmap



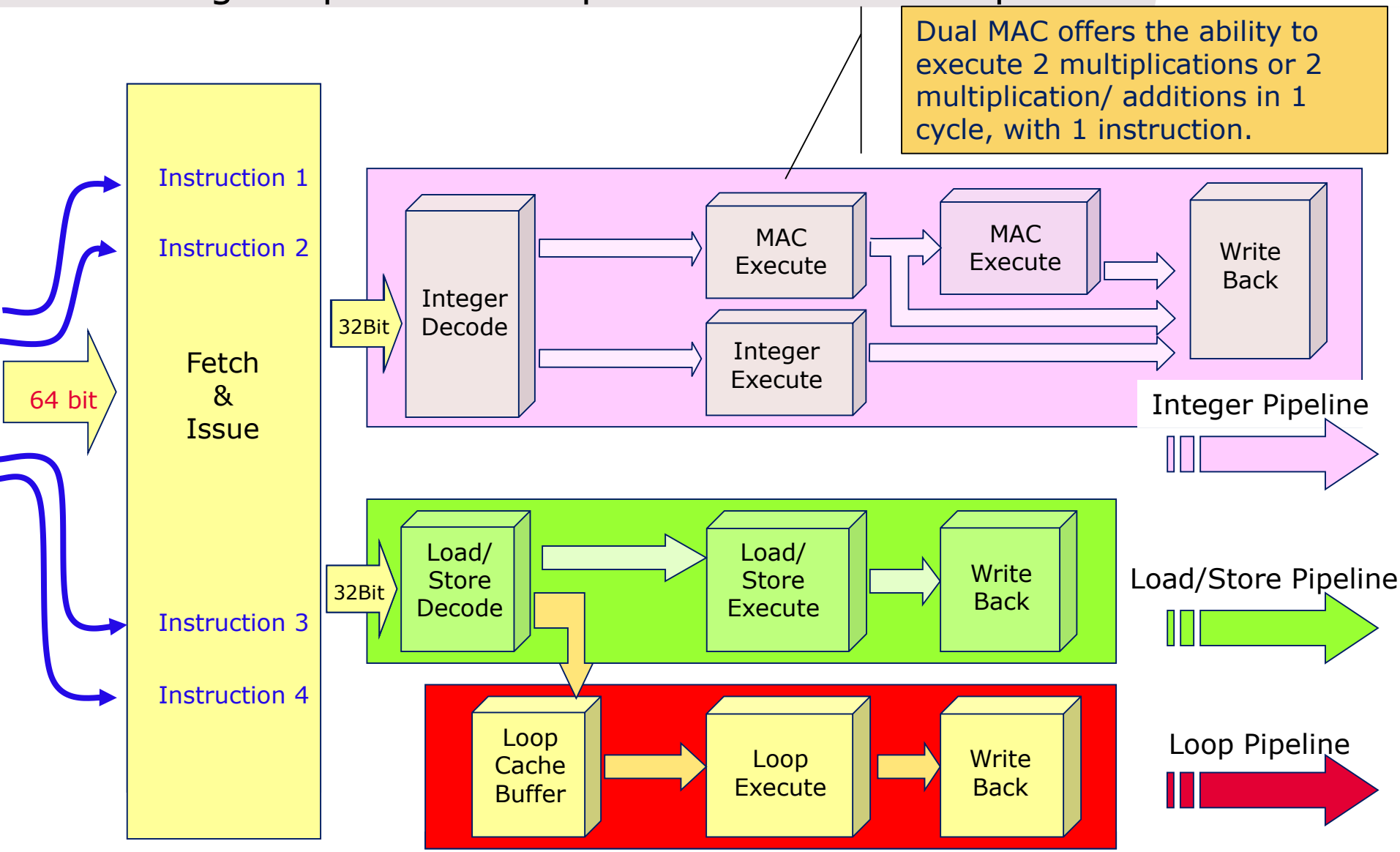
Key Features

- 32 bit Harvard architecture
- RISC architecture
- Superscalar architecture
- Little-endian byte ordering
- 4 GByte address space
- 16 & 32 bit instructions
- Most instruction executed in 1 cycle
- Bit handling
- Flexible interrupt prioritization scheme
- Low interrupt latency
- Fast context switching
- Dual MAC unit
- Zero Overhead Loop
- FPU

Core Subsystem



General Pipeline Overview
Four-Stage Super-Scalar triple issue TriCore™ Pipeline



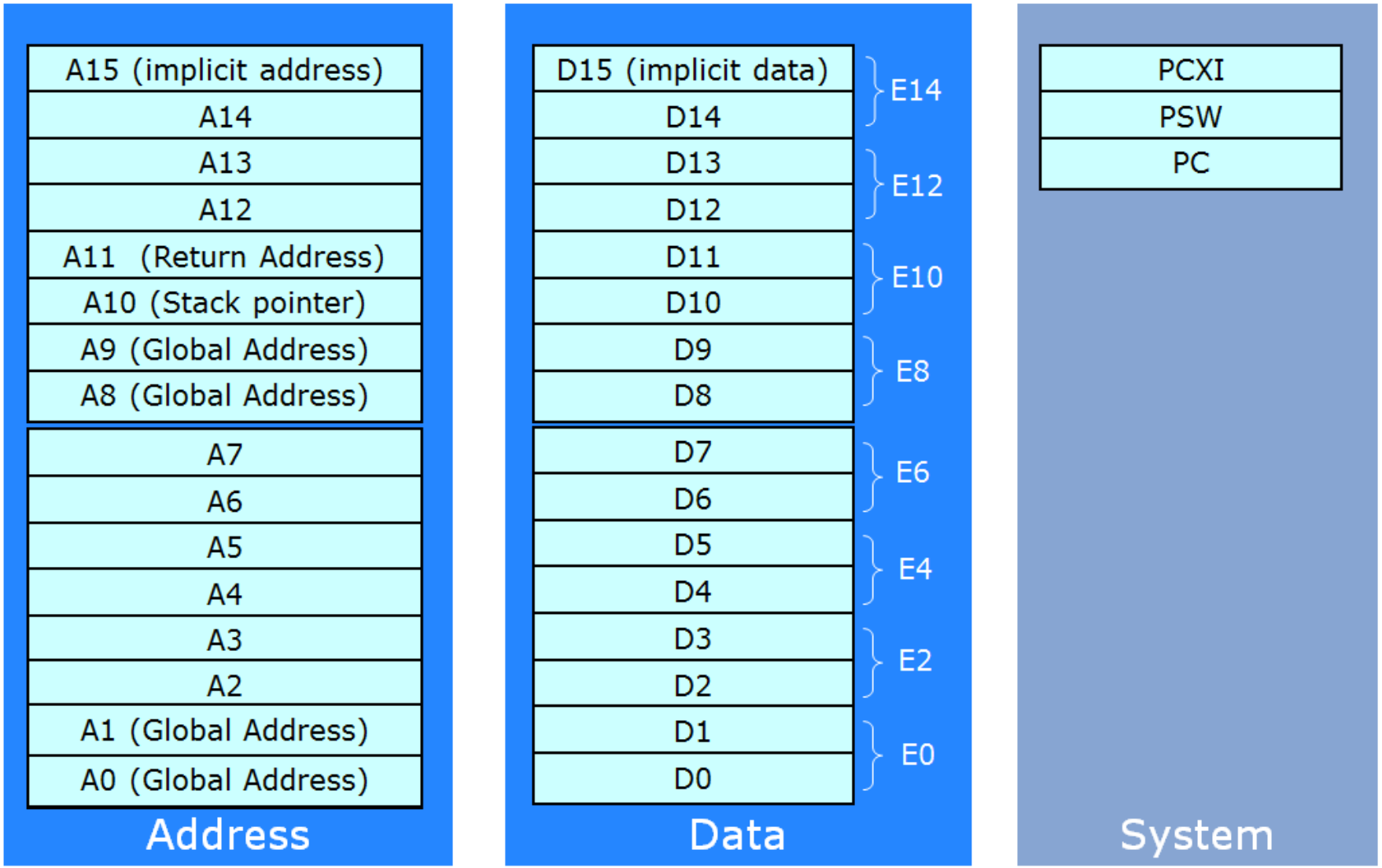
Pipeline - General

- Integer pipeline:
  - Integer arithmetic and logic instructions.
  - Bit operations.
  - Divide and MAC instructions.
  - Etc.

- Load /Store pipeline:
  - Load / Store instructions.
  - Context operations.
  - Address arithmetic instructions.
  - Etc.

- Loop pipeline:
  - Loop instructions.

Architectural Registers



Core Registers

General Purpose Registers	
D0 – D15	Data Registers.
A0 – A15	Address Registers.

System Registers	
PC	Program Counter
PSW	Program Status Word
SYSCON	System Control Registers
PCXI	Previous Context Information.

Context Management	
FCX	Free CSA List Head Pointer
LCX	Free CSA List Limit Pointer

CPU Interrupt and Trap Control	
ICR	Interrupt Control Reg.
BIV	Base Address of Interrupt Vect. Table.
BTV	Base Address of Trap Vect. Table.

Memory Protection	
DPRx_L DPRx_H	Data Lower and Upper Address Range
CPRx_L, CPRx_U	Code Lower and Upper Address Range
CPRXE_n	Code Execute Permission
DPRE_n	Data Read Permission
DPWE_n	Data Write Permission

Stack management	
ISP	Interrupt Stack Pointer

Core Special Function Registers (CSFRs) can only be accessed by special read/write instructions:
→ MTCR: move to core special function register (write access, supervisor mode only)
→ MFCR: move from core special function register (read access)

What is a context?

- In an embedded real time system, independent tasks switching occur frequently (in response to an interrupt, RTOS management, etc).
- The task's context represents the state of this task.
- Basically, the context is everything the µC needs to know in order to start (or re-start) a task.

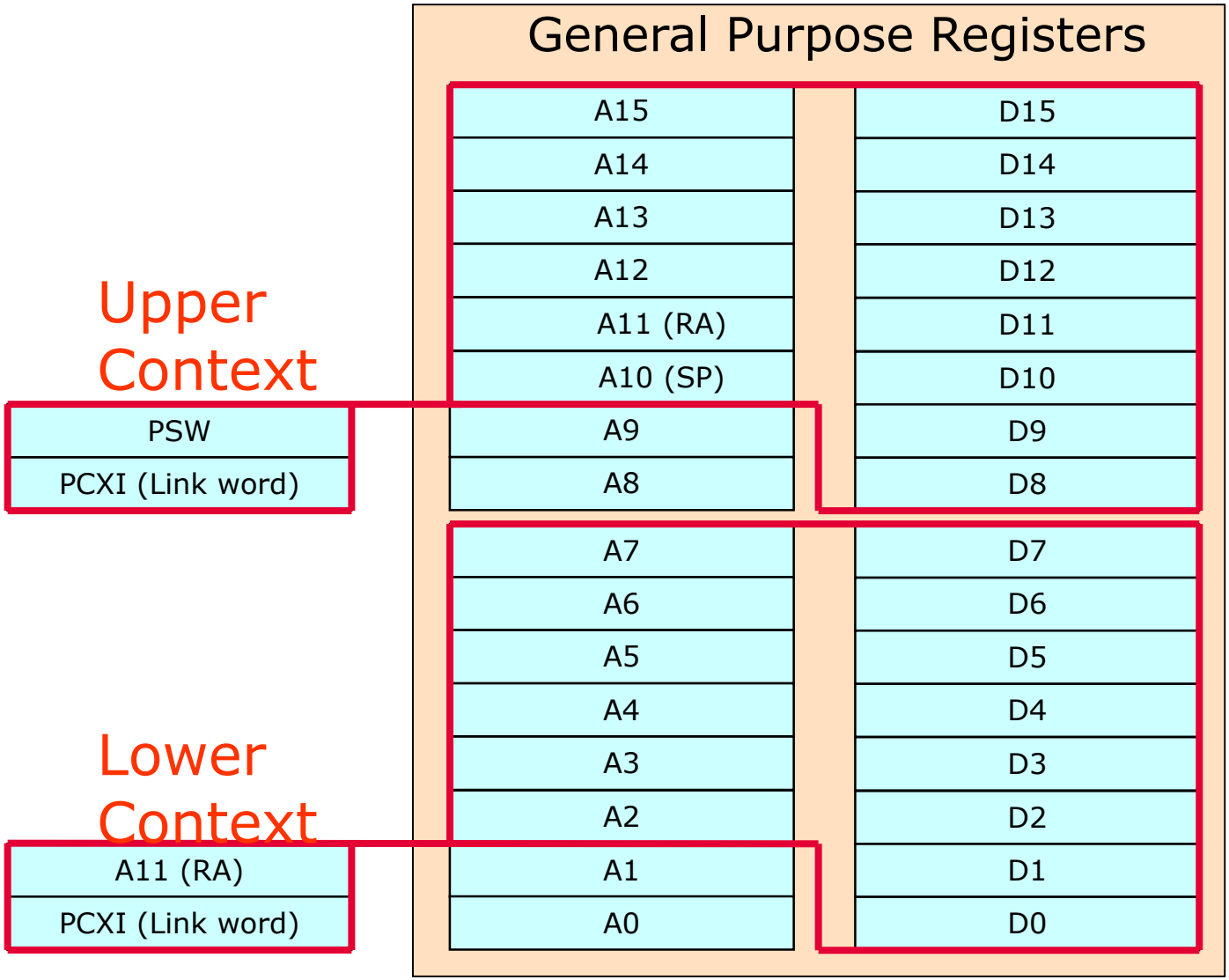
Upper and Lower context

- TriCore defines two contexts:
  - The upper context (task specific)
  - The lower context (for parameter passing).

- The upper context is automatically saved on call, interrupt or trap.

- The lower context has to be saved explicitly with an instruction.

Upper and Lower Contexts



Context Saving and restoring

Automatically saved / restored

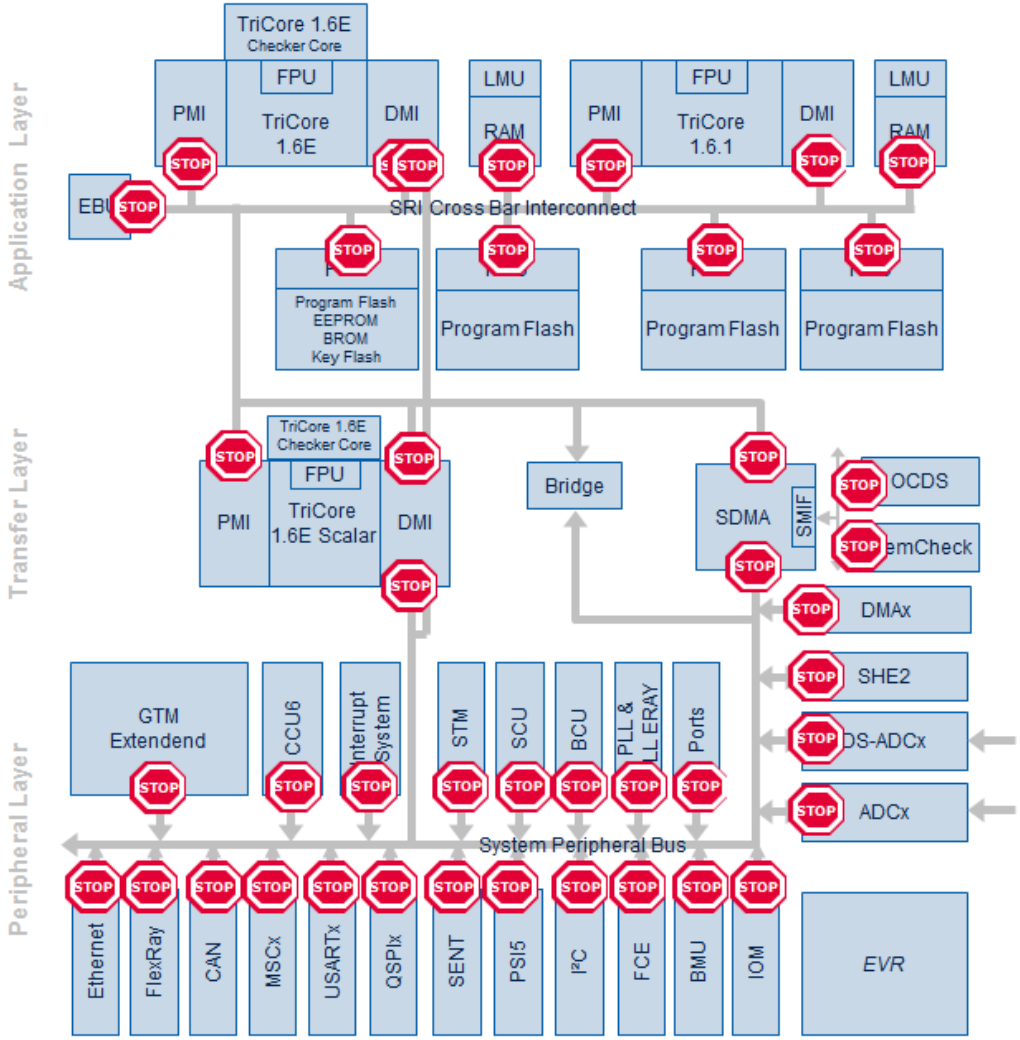
Save		Restore	
Event / Instruction	**Saved context**	**Event / Instruction**	**Restored Context**
Interrupt	Upper	RFE	Upper
Trap	Upper	RFE	Upper
CALL	Upper	RET	Upper
BISR	Lower	RSLCX	Lower
SVLCX	Lower	RSLCX	Lower
STLCX	Lower	LDLCX	Lower
STUCX	Upper	LDUCX	Upper

Saving to CSA

Saving to Absolute Address

Ability to Host Multiple Applications on One Device

- Common accesses protection based on Master ID (TriCores / DMAs)
- Each DMI (Data Access) has 2 IDs
  - 'Safe' ID
  - 'Non-Safe ID'
- Each Slave has write permissions based on ID
  - Permission register Safety Endinit protected
- Address range based protection pages for SRAMs



Aurix Peripherals: Access Enable Protection

New method for write access protection from On Chip Bus to Slave modules

- Endinit Protected (E)
- Safety Endinit Protected (SE -> New)
- TAG ID protected (P -> New)
- User / Supervisor Mode (U / SV)

Register Short Name	Register Long Name	Offset Address	Access Mode	
			Read	Write
Pn_OUT	Port n Output Register	0000_H	U, SV	U, SV, P
Pn_OMR	Port n Output Modification Register	0004_H	U, SV	U, SV, P
Pn_IOCR0	Port n Input/Output Control Register 0	0010_H	U, SV	U, SV, P
Pn_IOCR4	Port n Input/Output Control Register 4	0014_H	U, SV	U, SV, P
Pn_IOCR8	Port n Input/Output Control Register 8	0018_H	U, SV	U, SV, P
Pn_IOCR12	Port n Input/Output Control Register 12	$001C_H$	U, SV	U, SV, P
Pn_ ACCEN1	Port n Access Enable Register 1	$00F8_H$	U, SV	SV, SE
Pn_ ACCEN0	Port n Access Enable Register 0	$00FC_H$	U, SV	SV, SE

Aurix Peripherals: Access Enable Registers

- Each On Chip Bus transaction includes a Master TAG ID
- Master TAG ID is used for the write access protection
- After reset: per default no restriction

All On Chip Bus TAG IDs are unique and hardwired

- Each CPU.DMI with two TAG Ids (safe/non-safe)

Each On Chip Slave Module (E.g SPI, GTM)

- At least one set of ACCEN0/1 registers
- Some Slave Modules with multiple ACCEN0/1 sets
  - (e.g. SDMA, SCU)
- Interrupt Router with different ACCEN0/1 sets for
  - SRC[31:16]/SRC[15:0]
- SRAMs with additional range protection registers
  - each CPU with 8 ranges for PSRP/DSPR, LMU with 8 ranges

Masters on Bus

Access protection violations and bus errors are reported to the Safety Management Unit (SMU)

INT_ACCEN00
Access Enable Register 0 **($0F4_H$)** **Reset Value: FFFF FFFF$_H$**
INT_ACCEN10
Kernel 1 Access Enable Register 0 **($0FC_H$)** **Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN 31	EN 30	EN 29	EN 28	EN 27	EN 26	EN 25	EN 24	EN 23	EN 22	EN 21	EN 20	EN 19	EN 18	EN 17	EN 16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN 15	EN 14	EN 13	EN 12	EN 11	EN 10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

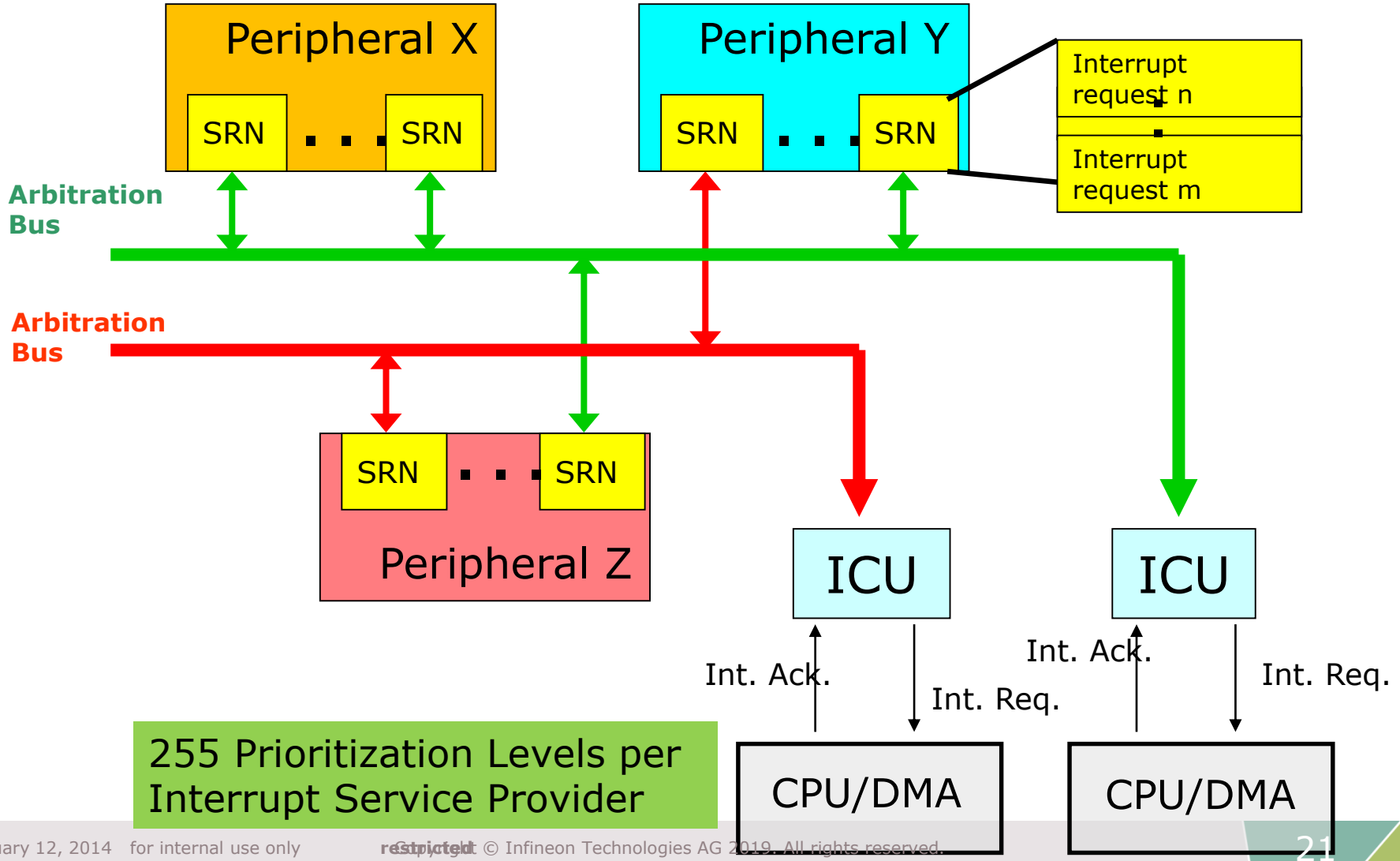
Table 3-15 On Chip Bus Master TAG Assignments

TAG-Number	Module	Location	Description
000000_B	CPU0	SRI/SPB	DMI.NonSafe TAG ID
000001_B	CPU0	SRI/SPB	DMI.Safe TAG ID
000010_B	CPU1	SRI/SPB	DMI.NonSafe TAG ID
000011_B	CPU1	SRI/SPB	DMI.Safe TAG ID
000100_B	CPU2	SRI/SPB	DMI.NonSafe TAG ID
000101_B	CPU2	SRI/SPB	DMI.Safe TAG ID
000110_B	SDMA	SRI/SPB	Move Engine 0 (SDMA.ME0)
000111_B	SDMA	SRI/SPB	Move Engine 1(SDMA.ME1)
001000_B	SDMA	SRI/SPB	Cerberus
001001_B	DMA	SRI/SPB	Move Engine 0 (DMA.ME0)
001010_B	DMA	SRI/SPB	Move Engine 1 (DMA.ME1)
001011_B	HSSL	SRI	High Speed Serial Link
001100_B	Ethernet	SPB	Ethernet
001101_B	HSM	SPB	HSMCMI, HSMRMI[1)]
001110_B	-	-	Reserved
001111_B	-	-	Reserved
010000_B	CPU0	SRI	PMI
010001_B	CPU1	SRI	PMI
010010_B	CPU2	SRI	PMI
011000_B	DAM	SRI	DAM
111000_B	IOC32	BBB	Cerberus on Back Bone Bus (ED)
111001_B	CIF	BBB	CIF Master on Back Bone Bus (ED)
110000_B	LMU	BBB	LMU Master on Back Bone Bus (ED)
Others		-	Reserved

1) Both HSM FPI Master Interfaces (HSMCMI, HSMRMI) are using the sam TAG ID

Interrupt System Overview

- Independent Interrupt Systems per Interrupt Service Provider (CPUs, DMA, SDMA)



255 Prioritization Levels per Interrupt Service Provider

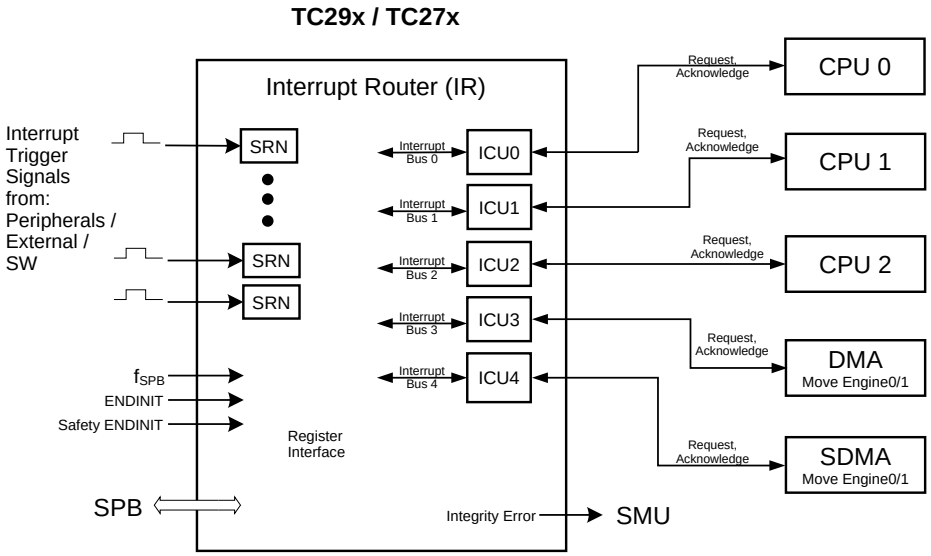
Aurix Interrupt System: Introduction

- An interrupt request is serviced by CPU/DMA, called **Service Provider**
- Interrupt requests are called **Service Requests**. Each interrupt request source must connect to a Service Request Node (**SRN**). An interrupting device can have more than one SRN.
- Interrupt service requests are serviced by an **Interrupt Control Unit (ICU)** that handles the priority arbitration and the communication with the CPU.
- Each SRN contains a **Service Request Control Register (SRC)** and the necessary logic to communicate with the requesting source and the interrupt arbitration bus

Aurix Interrupt System: Feature Set Overview

Central Interrupt Router Module (IR)

- Interrupt Trigger Signals from Peripherals
- Result from last Arbitration Round to Service Provider
- Acknowledge from Service Provider when Service Request taken
- One Service Request Node (SRN) per Interrupt Trigger signal
- Each SRN with own Service Request Control register (SRC)



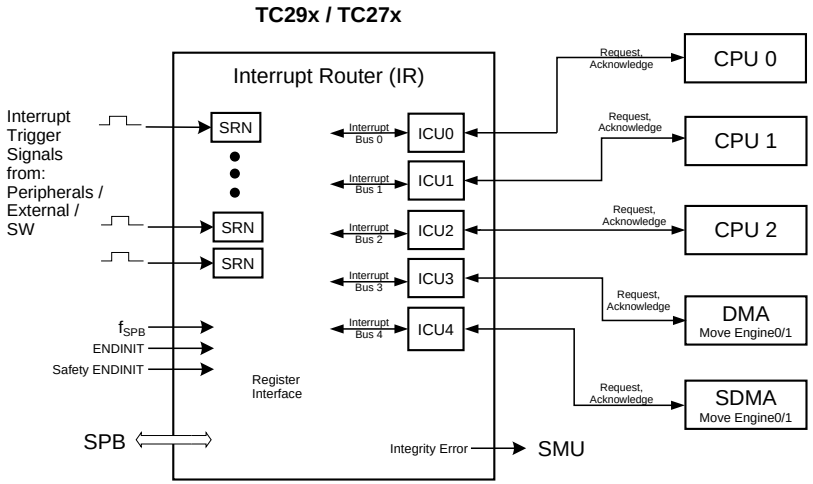
Feature Set Overview:

- Supports up to 1024 Service Requests
- Support of up to 255 service request priority level per ICU / Service Provider
- One Interrupt Control Unit (ICU) per Interrupt Service Provider
- ICUs with independent arbitration

Aurix Interrupt System: Feature Set Overview

Feature Set Overview (cont´d):

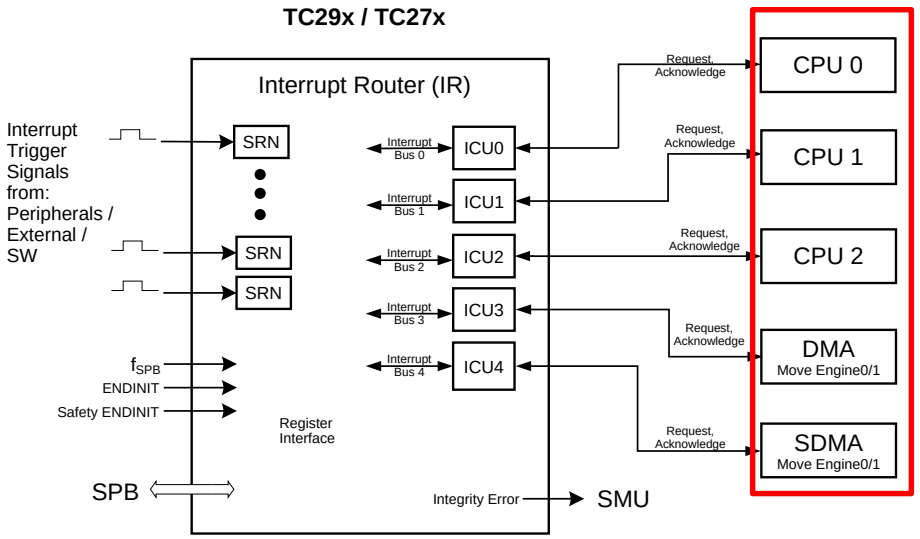
- Each Interrupt with dedicated Service Request Node (SRN)
- Each SRN with a programmable 8-bit priority vector
- Each SRN can be mapped to one of the ICUs (Service Providers: CPUs or DMA)
- Interrupt System Integrity support (ECC based)
- Four General Purpose Interrupts per CPU that are not assigned to peripherals or external interrupts (-> to be used as SW Interrupt)
- Mechanism to signal Software Interrupts simultaneously to multiple Service Providers
- Interrupt Overflow mechanism (new service request was triggered while the SRN has still an pending service request)



Aurix Interrupt System: TC27x

Interrupt Router (IR) for TC27x:

- 5 Interrupt Service Provider (Interrupt Targets)
- 479 Interrupt Nodes
- Main Interrupt Contributor Modules:
  - GTM: 159
  - DMA/SDMA: 68
  - ADC/VADC: 52
  - QSPI: 30
  - HSSL/DigRF: 18
  - MultiCAN: 16
  - CCU6: 16
  - SW/GP: 15
  - Sent: 10
  - ...



Aurix Interrupt System: SRC

- Service Request Priority Number (SRPN)
  - priority increasing with number
  - CPU: SRPN=0 not allowed
  - DMA/SDMA: only available channel numbers
- Service Request Enable (SRE)
- Type Of Service Control (TOS)
  - 0->CPU0
  - 1->CPU1
  - 2->CPU2
  - 3->SDMA
  - 4->DMA

- ECC
  - Updated with any write to SRC[15:0]
- Set / Clear (SETR/CLRR)
- SRR (Service Request Pending)
- Interrupt Overflow Bit (IOV/IOVCLR)
- Software Sticky Bit (SWS/SWSCLR)
- Busy Bit (BUSY)
  - To be used by SW sequence when re-configuring SRNs during runtime

ECC is checked when the SRN with an pending service request was accepted by the service provider as next service request to be processed

set when the SRR bit has been set via SETR

To prevent a missmatch between the acknowledged TOS/SRPN value (using the old value) and the new values. This will result in ECC error.

SRC
Service Request Control Register (xx_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BUSY	SWSCLR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0		ECC					
rh	w	rh	w	rh	w	w	rh	r		rwh					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	TOS				SRE	0		SRPN							
r	rw				rw	r		rw							

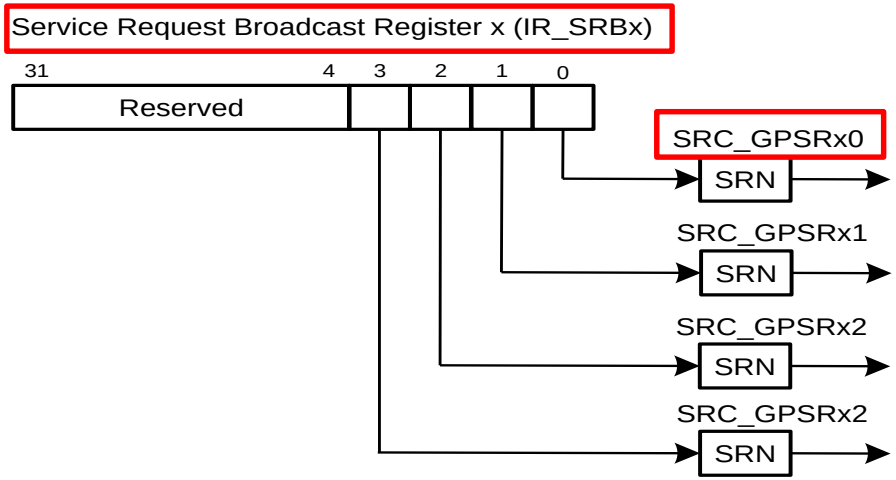
Aurix Interrupt System: SW Interrupts and Broadcast

General Purpose Service Request Nodes (GPSR):

- not assigned to HW interrupt triggers
- can only be used as SW interrupts
- GPSR group: 4 Service Request Nodes
- One GPSR group per TriCore CPU implemented

Parallel service requests to multiple Service Provider:

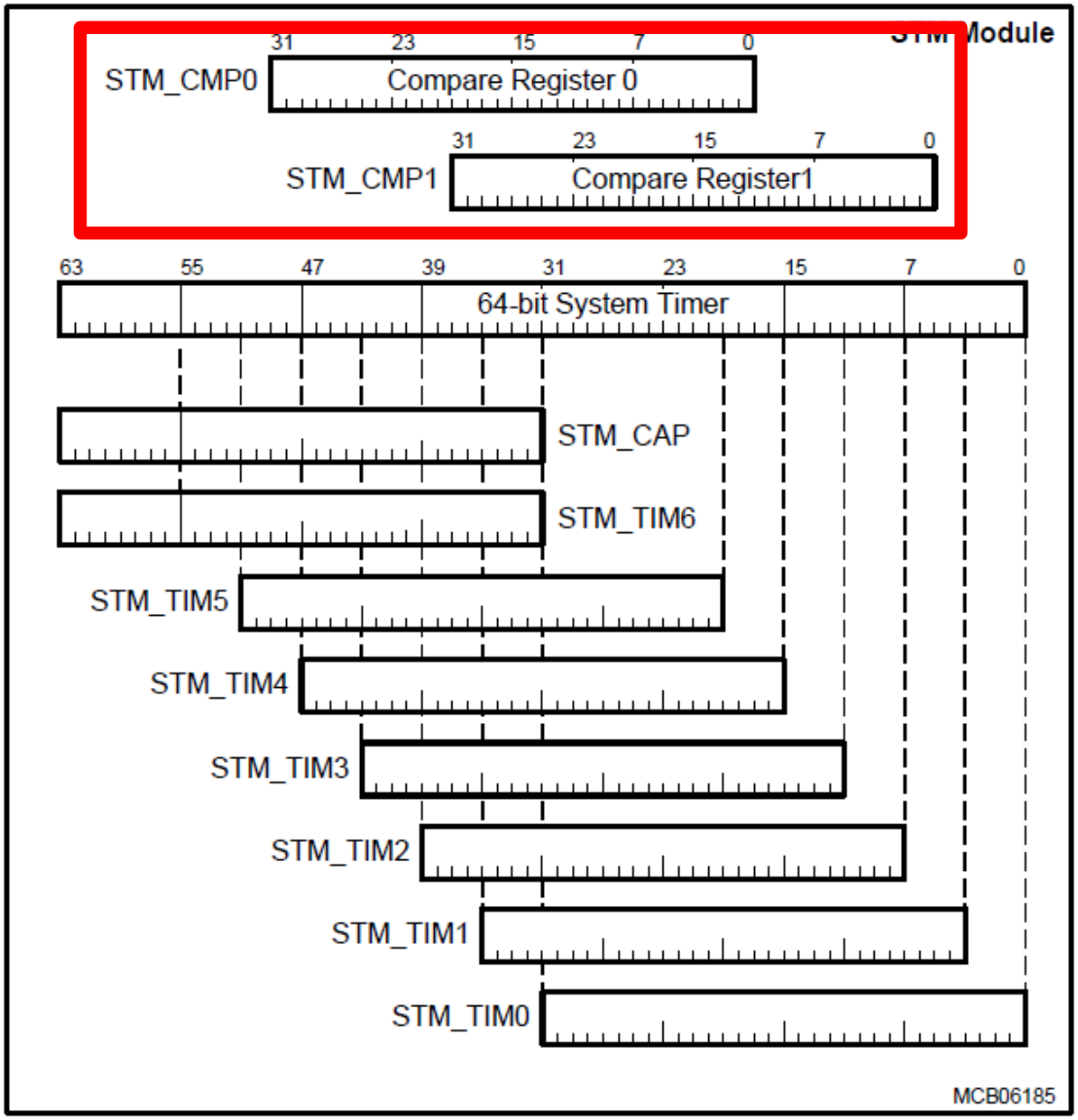
- Each GPSR group with a dedicated Broadcast register
- Broadcast register allows to trigger multiple GPSR



A GPSR Request xy can be triggered by
1) writing ´1´ to the related SRC_GPSRxy.SETR bit or
2) by writing a ´1´to the related Service Request Broadcast register bit SRBx[y]

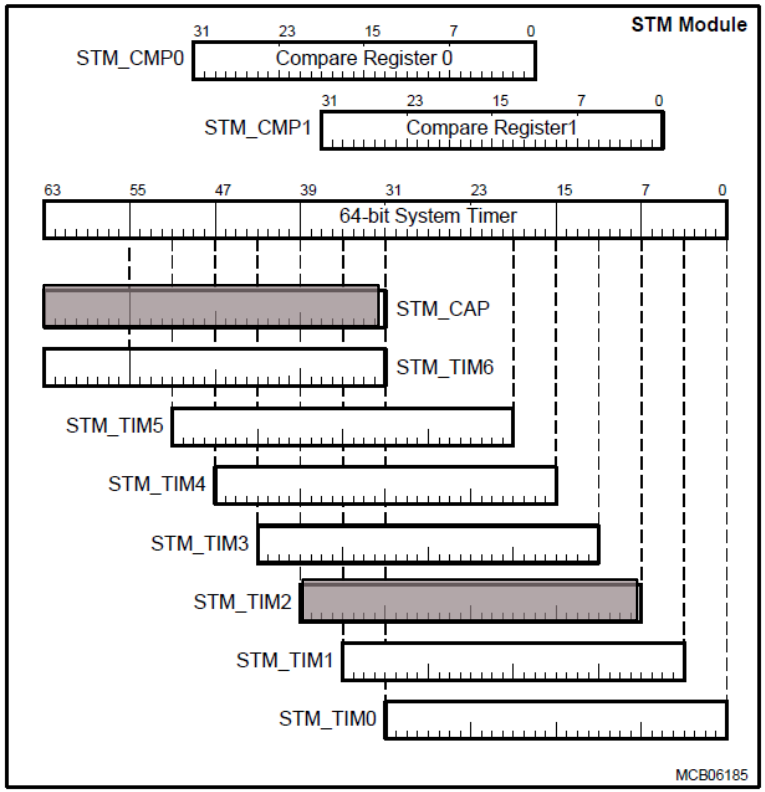
** x refers to CPU0, CPU1 or CPU2
** y refers to the 4 SW interrupts per CPU

STM (System Timer) - Block Diagram

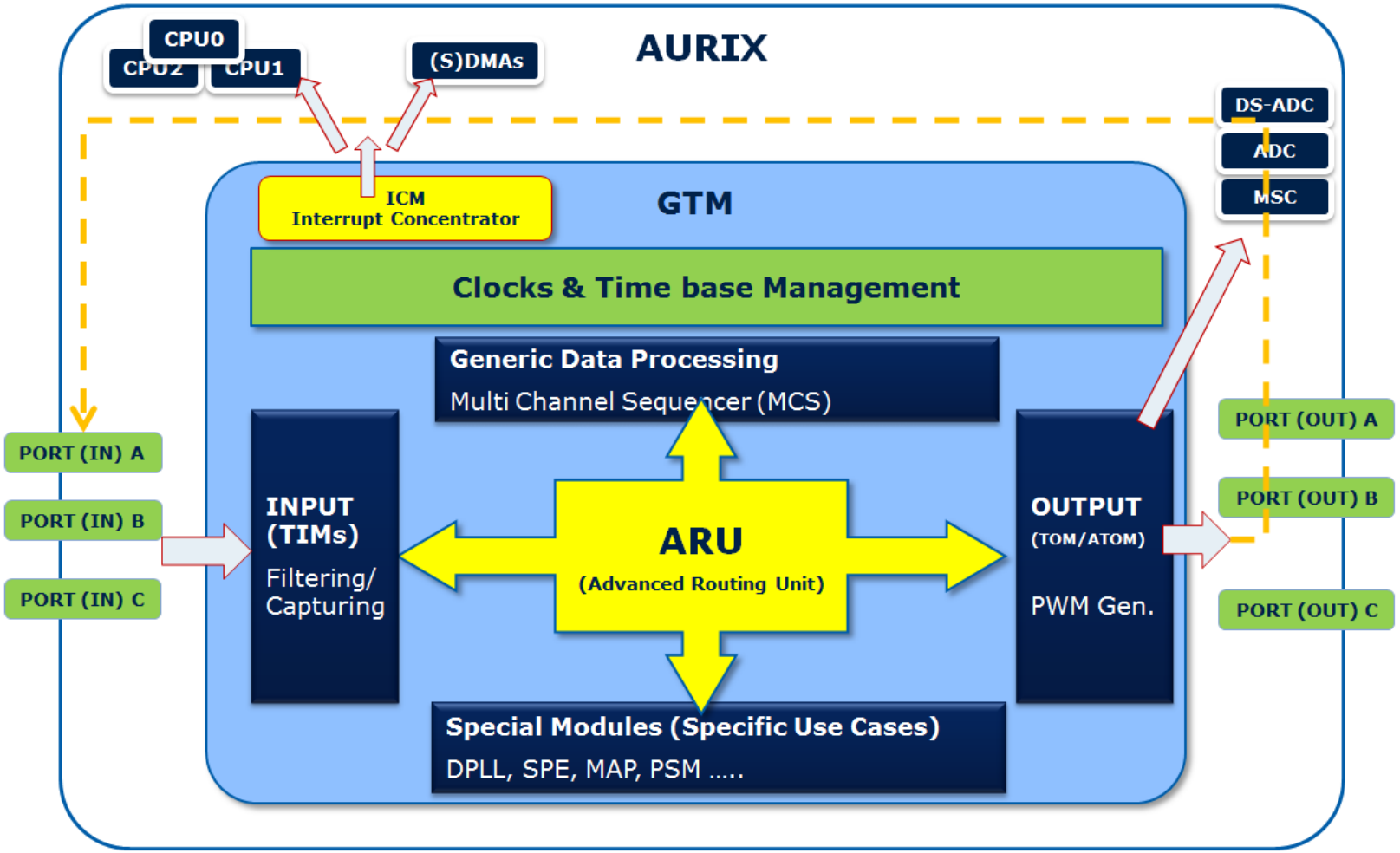


System Timer: How to read >32 bits synchronously

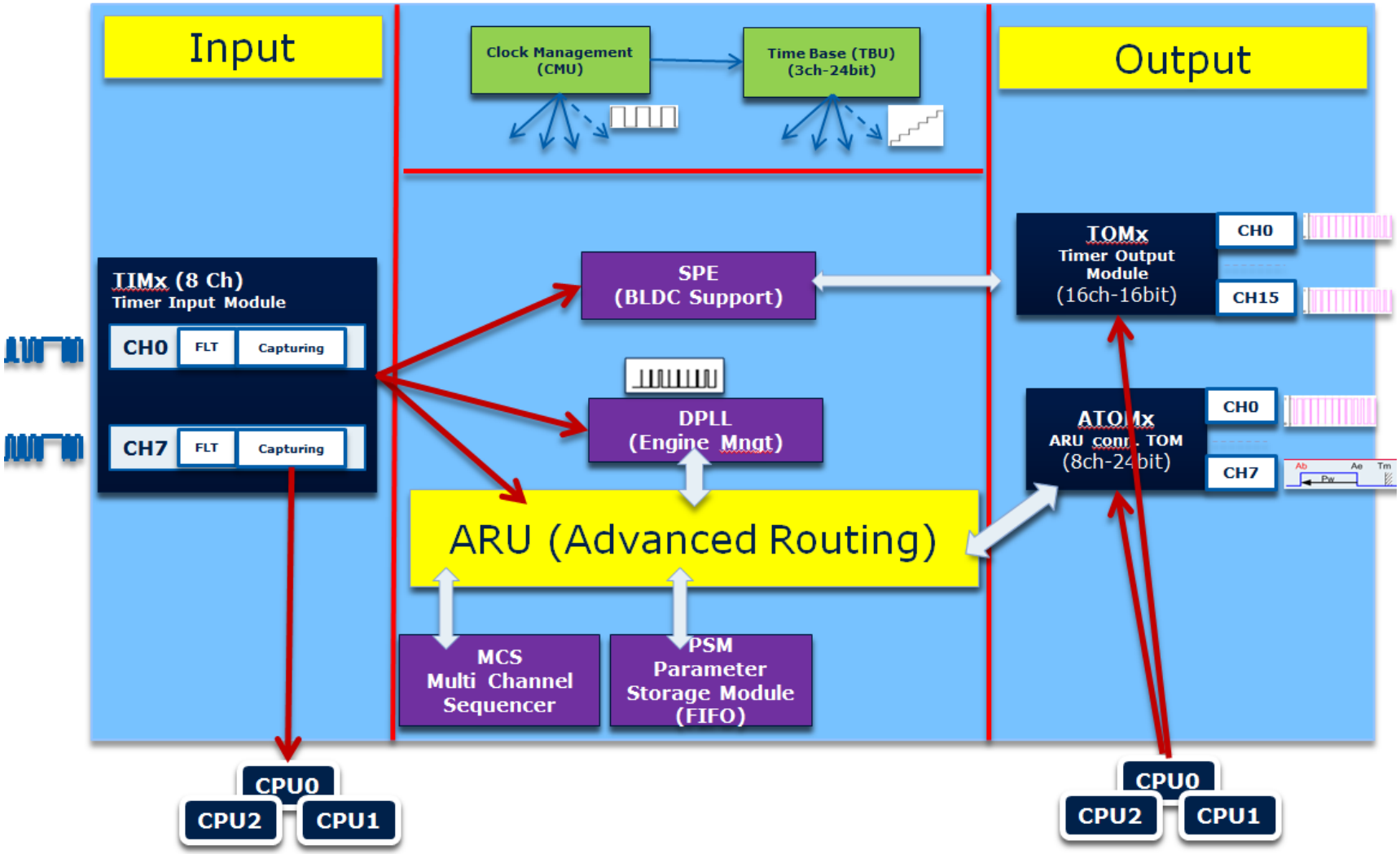
- STM is a free running 64 bit upward counter
- TriCore can only do max 32 bit read operations
- Could get roll over between reading lower and upper bits
- Therefore bits 32 to 63 are cap[illegible]me registers TIM0-5 are read



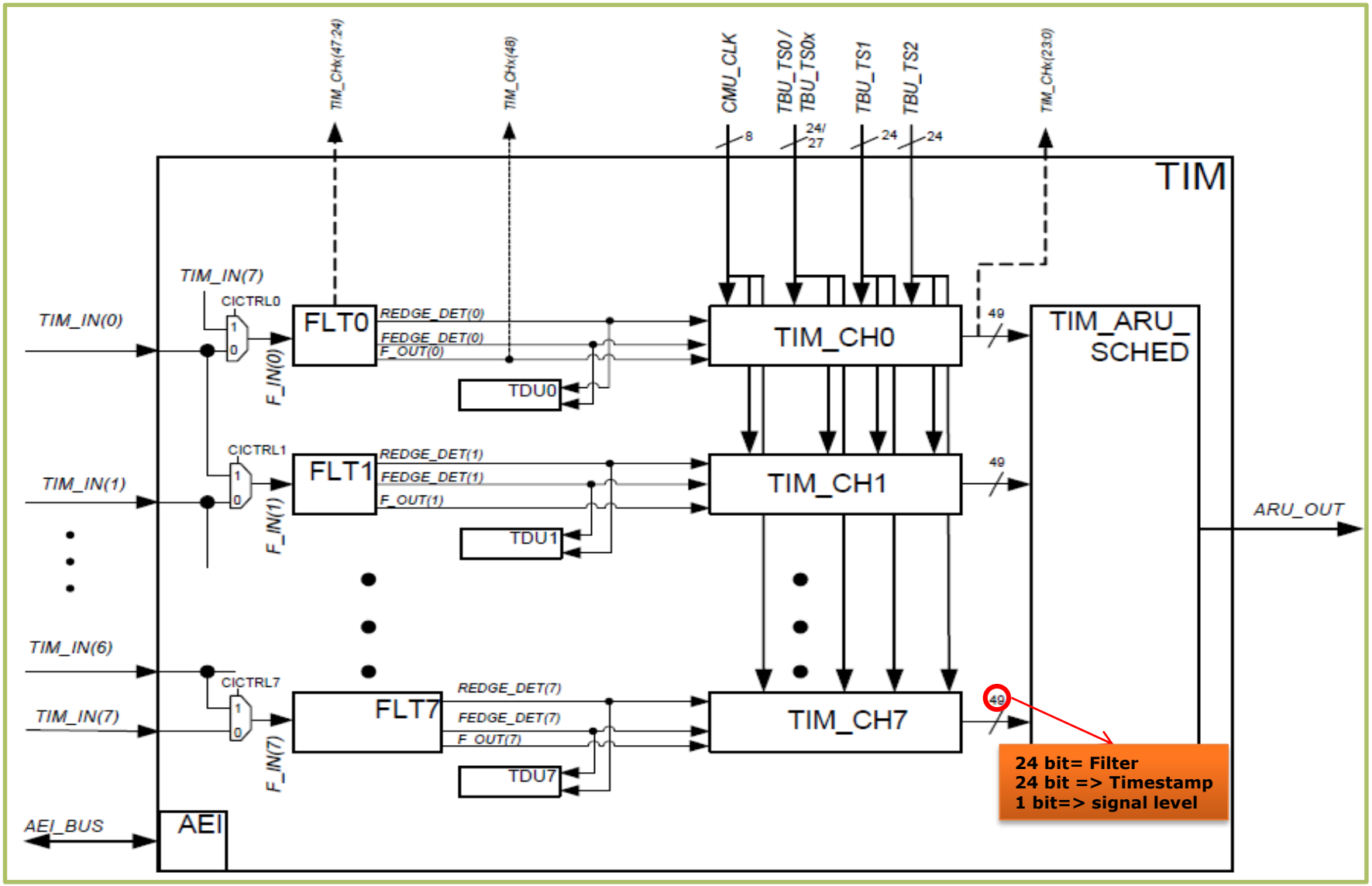
GTM - Generic Timer Module System Overview 1/2



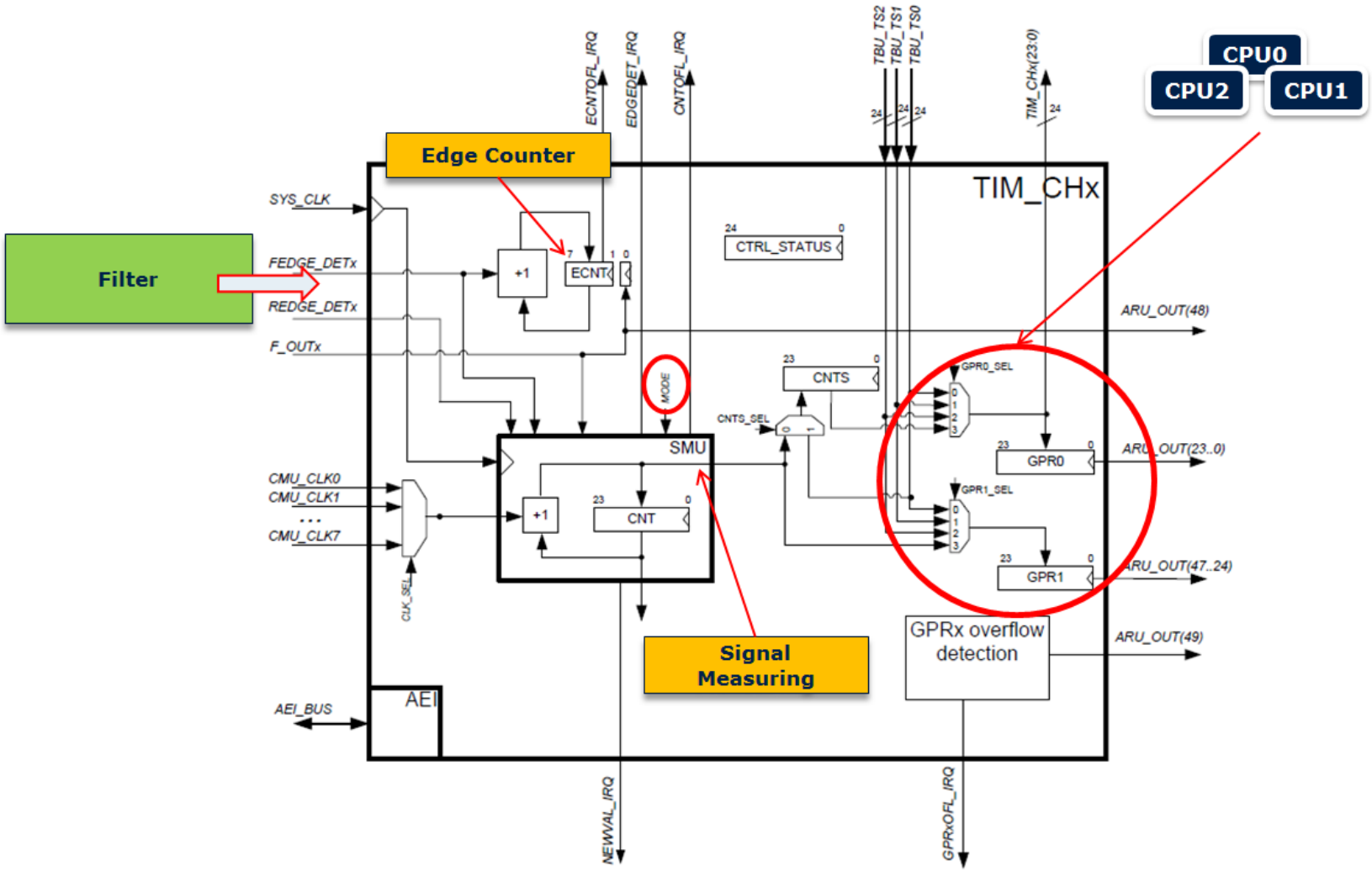
GTM - Generic Timer Module System Overview 2/2



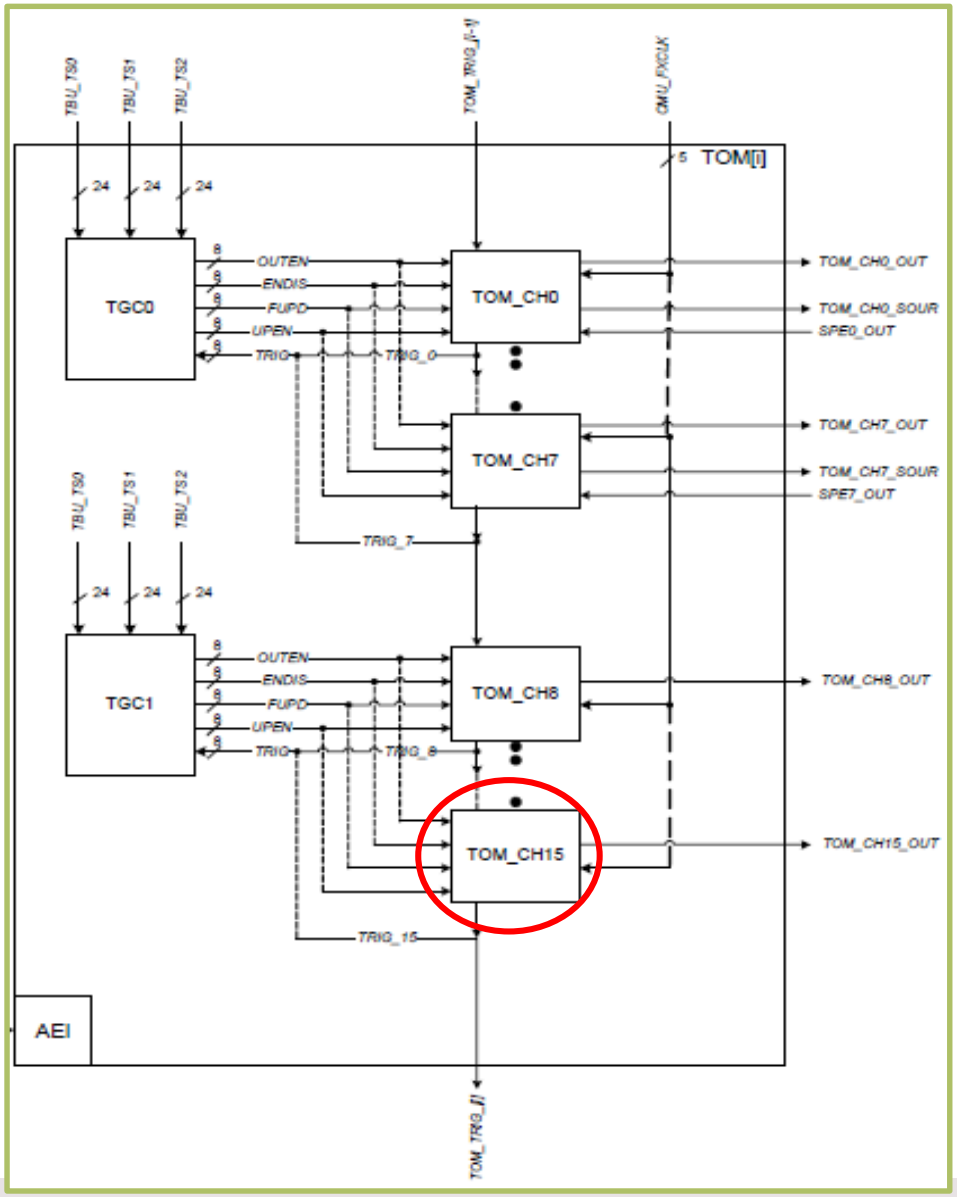
GTM (Generic Timer Module)
TIM – Timer Input Module



GTM (Generic Timer Module)
TIM - TIM_CHx – Timer Channel Architecture



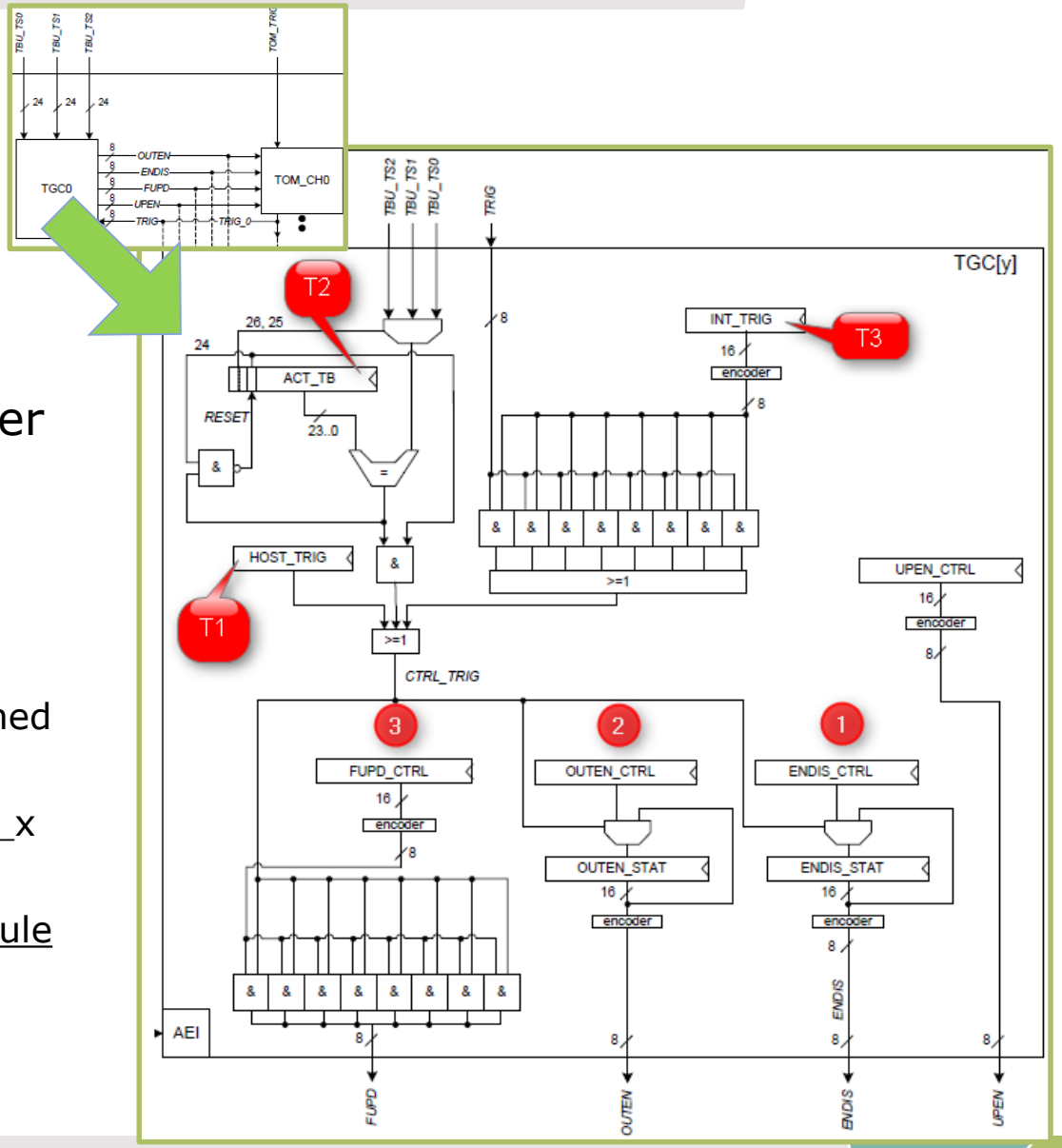
GTM (Generic Timer Module)
TOM – Timer Output Module - Overview



- 16 independent channels (**TOM_CH0…15**) for simple PWM generation
  - 2 groups of 8 channel
  - TOM_OUT(15) moreover offers a PCM (Pulse Count Modulated) signal
  - 16 bits counter
- **TGC0** & **TGC1** are **global channel control** units to drive TOM channels **synchronously** by external or internal events.
  - control enabling/disabling of the channels
  - Output Enable
  - Force update
- 5 dedicated clock line inputs **CMU_FXCLKx** are providing clocks (PWM resolution)

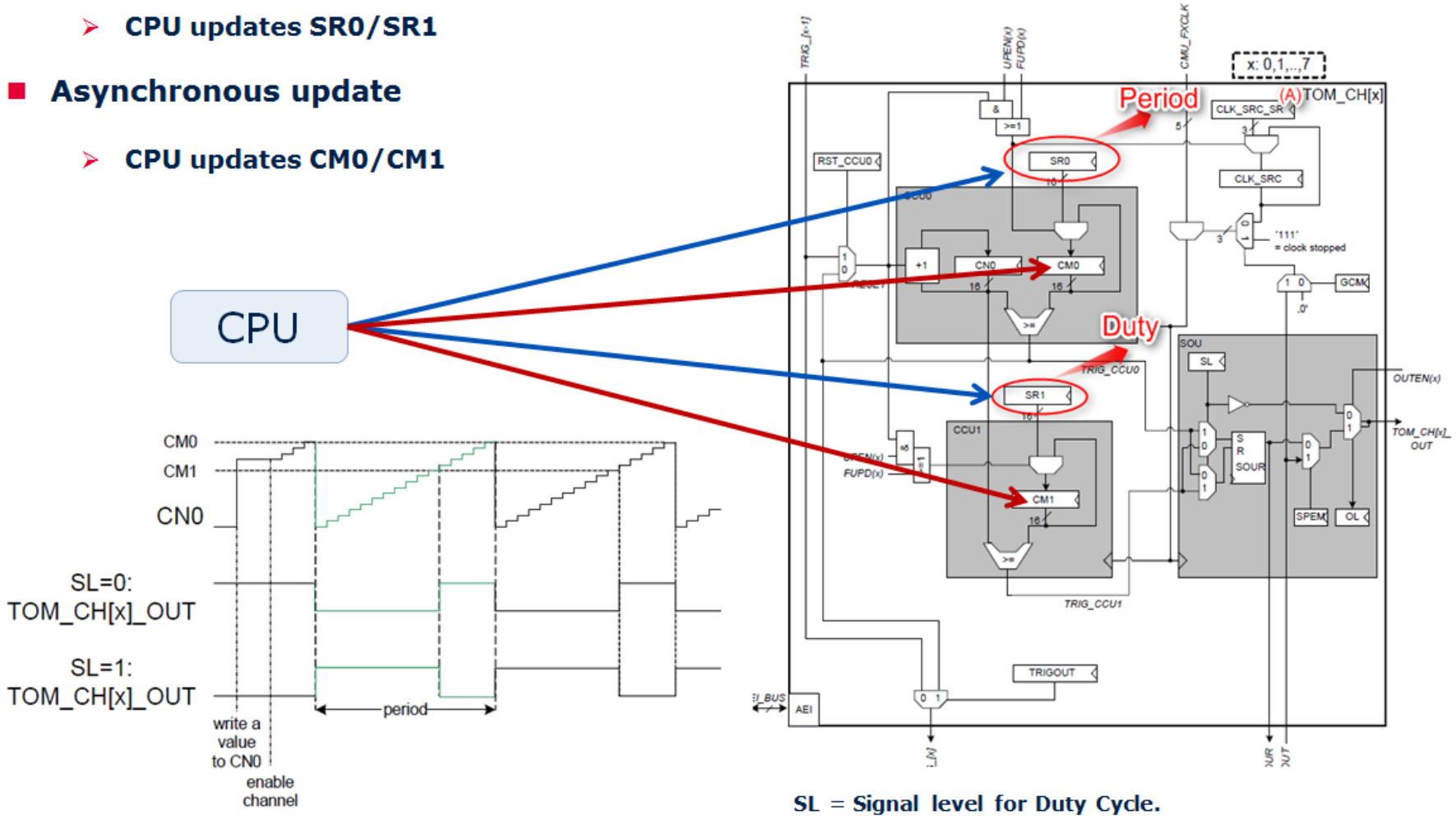
GTM (Generic Timer Module)
TOM – TGCx - Global Channel Control - Overview

- 3 individual mechanisms supported
  - control enabling/disabling of the channels (1)
  - Output Enable (2)
  - Force update (3)
- Above mechanisms by 3 trigger sources
  - **T1**: SW (via SFR **HOST_TRG**)
  - **T2**: TBU time stamp based on selected TBU_TSx time base
    - TBU time stamp can be defined by SFR **ACT_TB**
  - **T3**: Internal trigger signal TRIG_x
    - signal TRIG_x coming from channel x within a TOM module can be masked by SFR **INT_TRIG**



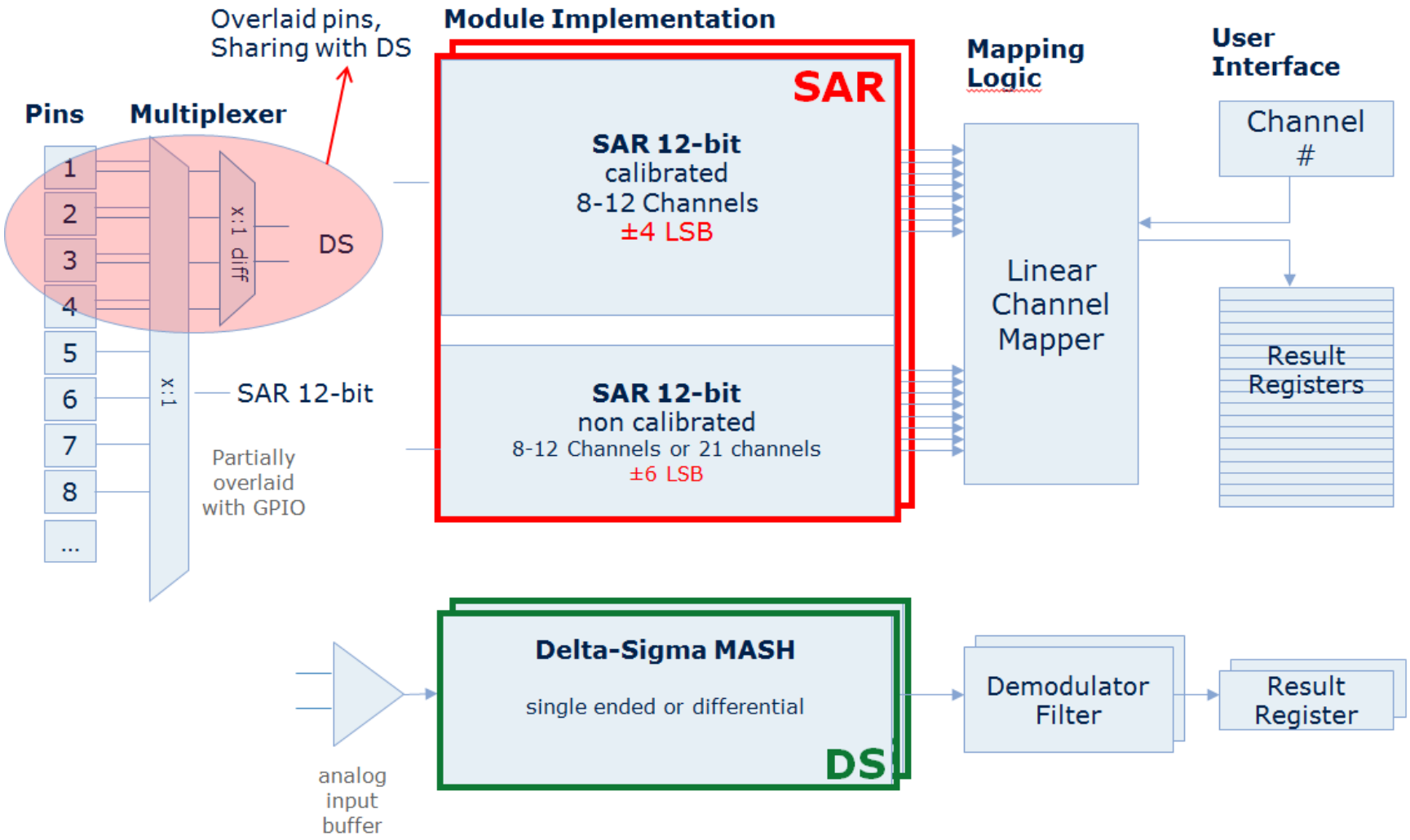
GTM (Generic Timer Module)
TOM – PWM Generation (1)

- **Synchronous update**
  - **CPU updates SR0/SR1**
- **Asynchronous update**
  - **CPU updates CM0/CM1**



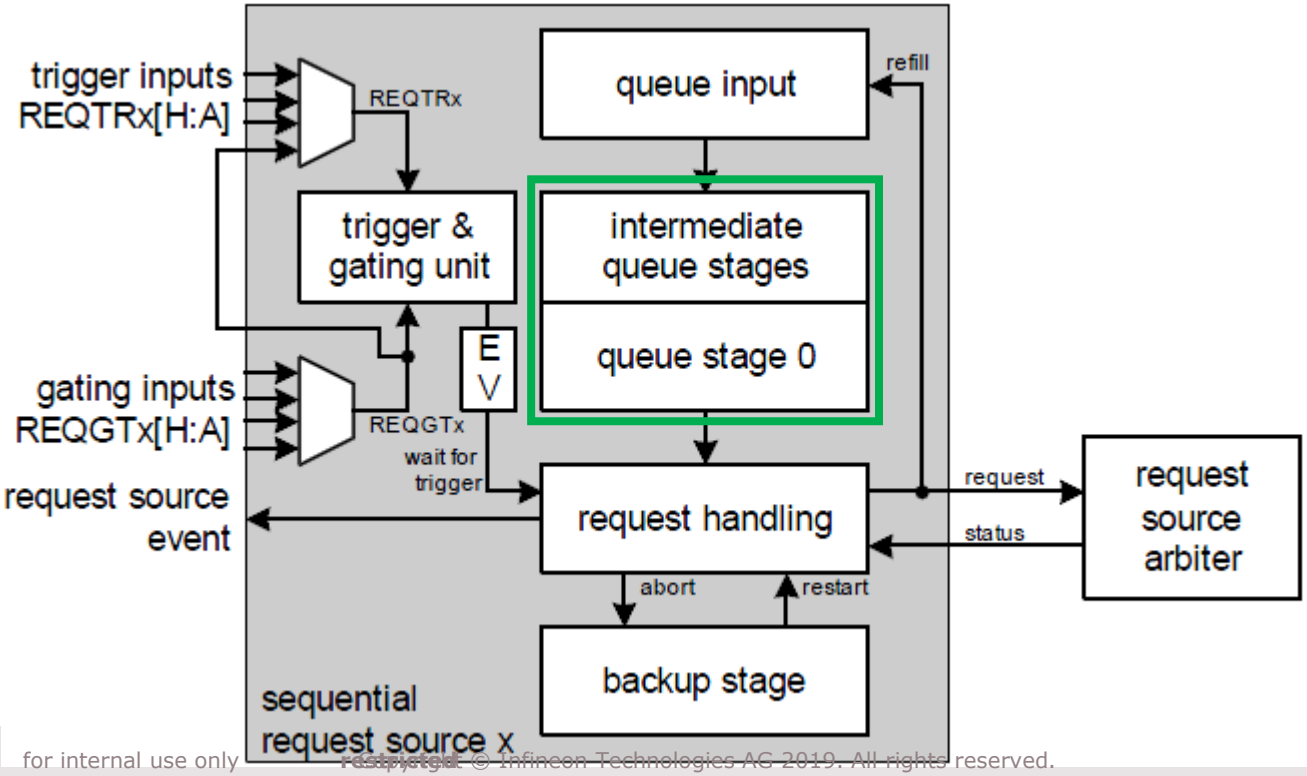
SL = Signal level for Duty Cycle.

ADC/DS Implementation Concept



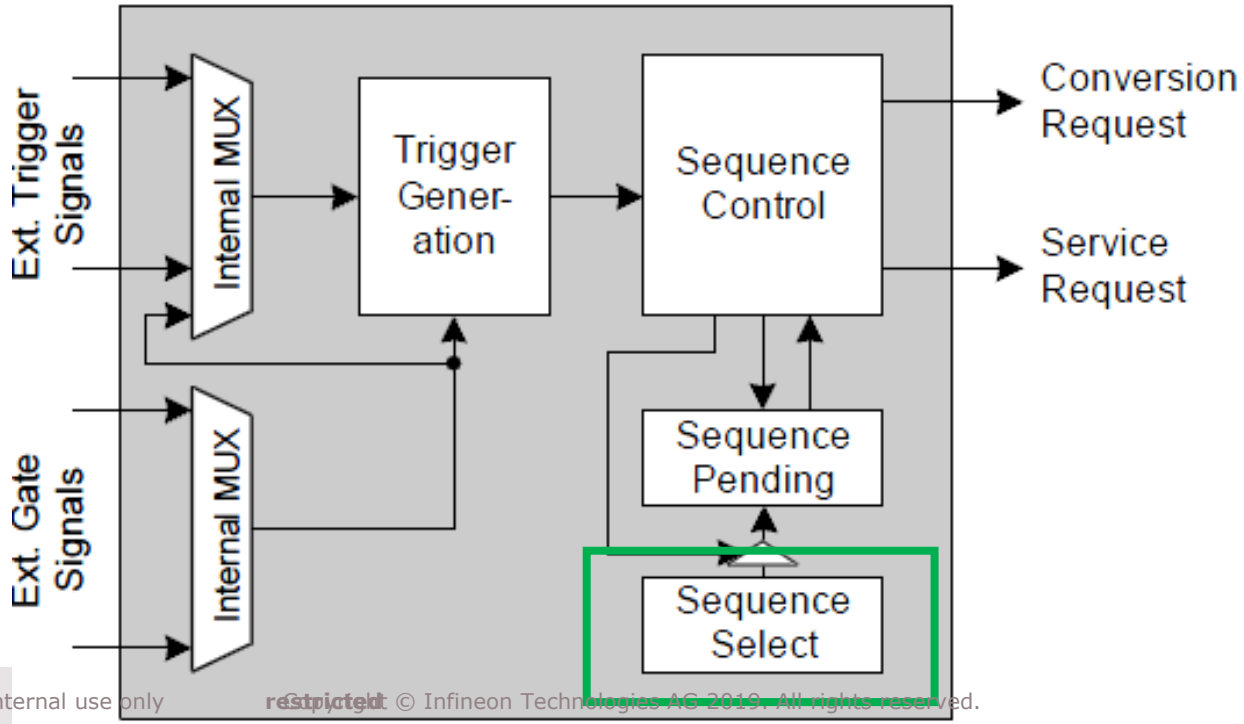
Queued Request Source

- **The Queued Request Source** of group x can select up to 8 channels that are subsequently converted in a sequence
- These channels can be arranged in an arbitrary order
- Each entry can be refilled into the buffer to be repeated automatically
- Conversion sequences can be started either via software or via a selectable trigger signal from on-chip and external sources



Scan Request Source

- **The Scan Request Source** of group x can schedule a linear sequence of conversions for the associated converter
- Each channel of group x can be included or excluded from a sequence
- A sequence can be repeated automatically
- Conversion sequences can be started either via software or via a selectable trigger signal from on-chip and external sources



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