

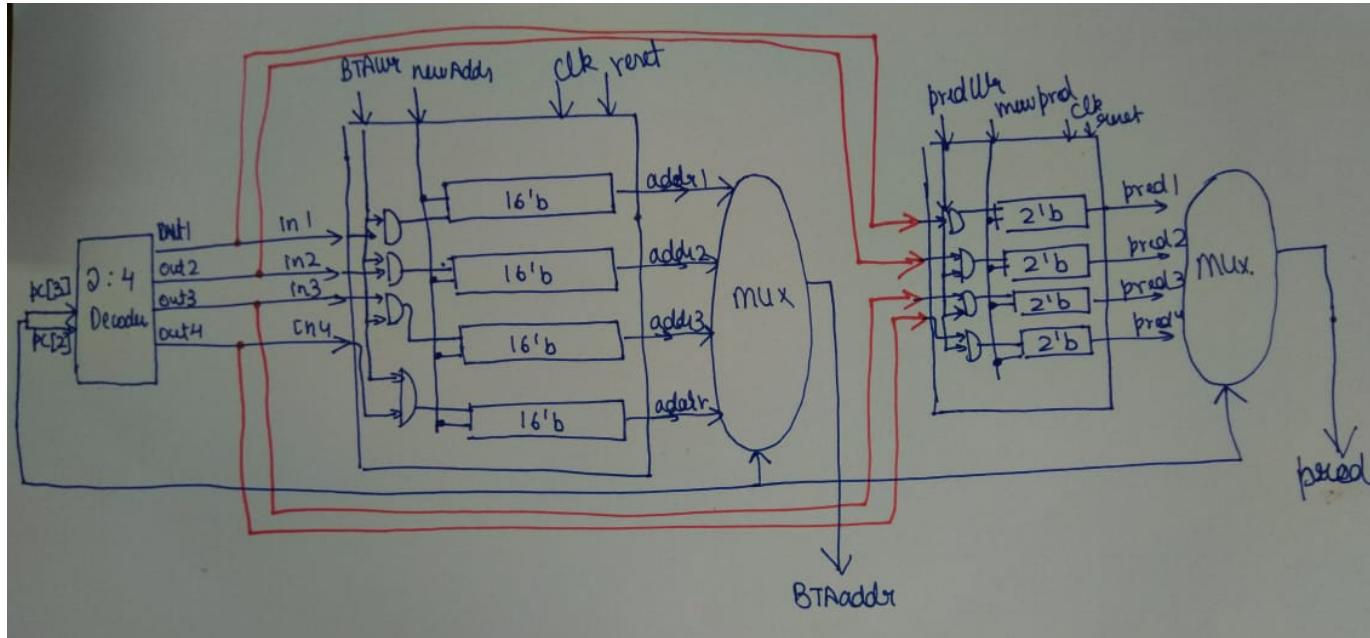
Advance Computer Architecture Assignment-3

Branch Prediction Buffer

Submitted By-
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2018H1030041G

Verilog Platform Used: iverilog
Waveform Viewer: Scansion
Operating System: MacOS Sierra 10.13

Architecture

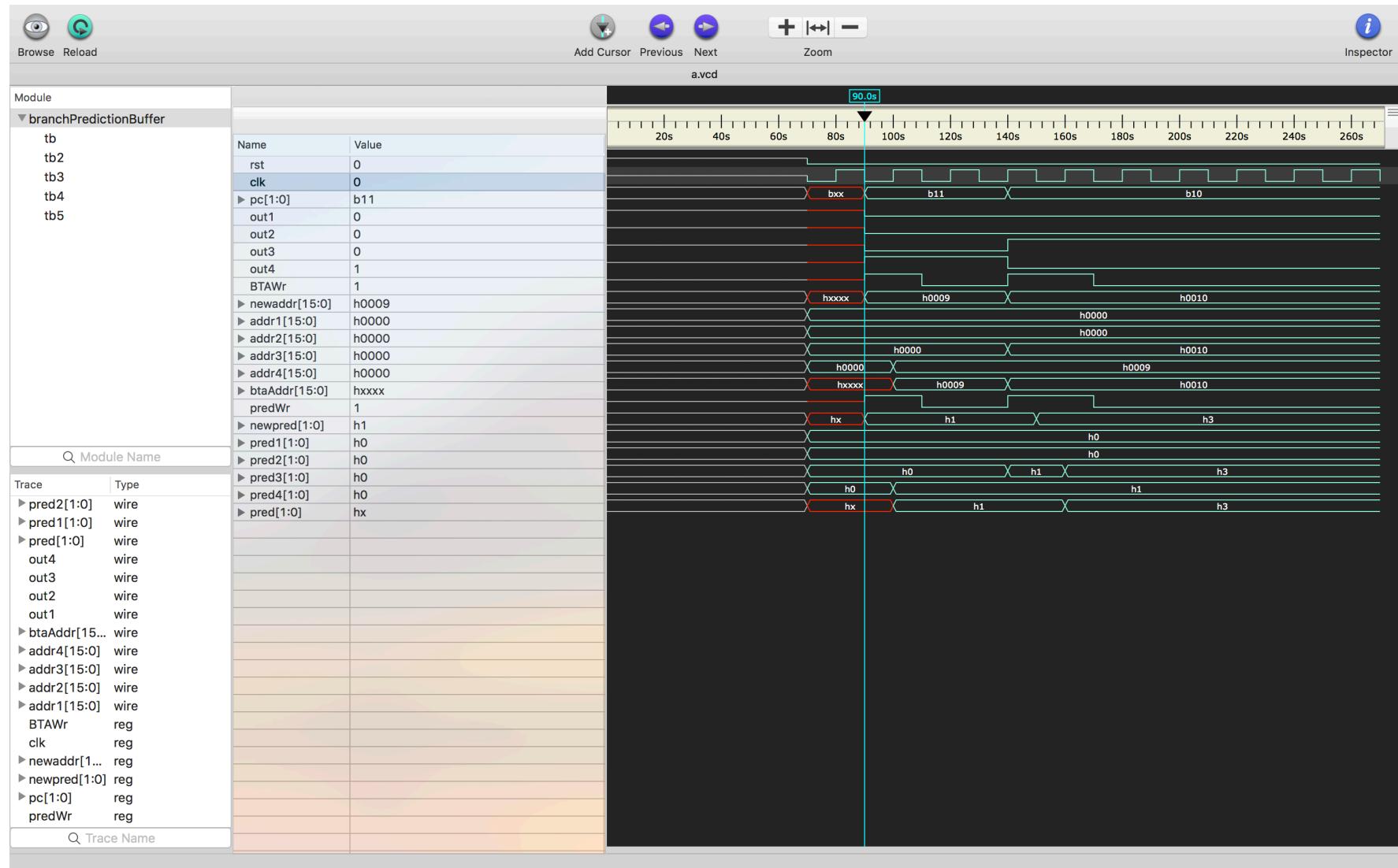


Design Constraints:

- (A) Branch completes in ID stage. Branch prediction circuit with 2-bit dynamic prediction is used to reduce branch penalty. The Branch prediction buffer can store details of 4 branches. Hardware should update branch prediction buffer entries.
- Design Branch prediction buffer.
 - What is the storage of Branch prediction buffer if PC is 16bits.

- According to the given question , PC is considered of size 16 bits , hence BTA registers size = 16 bits.
- Input to Decoder is 2 and 3 bits of PC. In Implementation of above hardware I have named variable **pc** which denotes PC[3:2] bits.

Output as Waveforms



Here input to decoder1 represented by pc variable is set to 2'b11.

BTAWr control signal is set to 1.

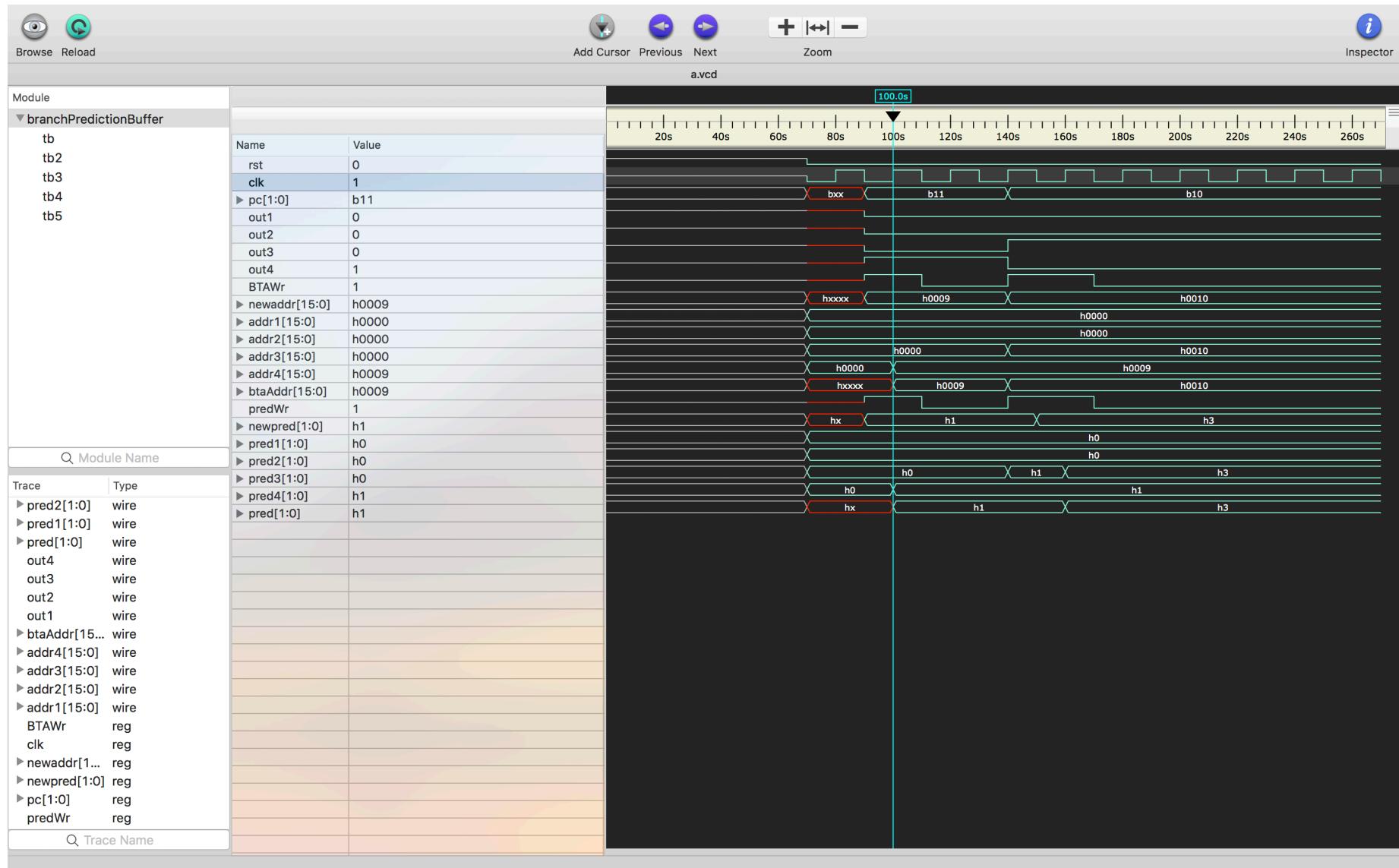
newAddr i.e. new BTA to be written is set to 16'd9.

predWr is 1 and newpred is 2'b01.

In next positive edge of clock , addr4 is updated to 16'd9 and pred4 is updated to 2'b01.

corresponding prediction is read i.e pred= pred4

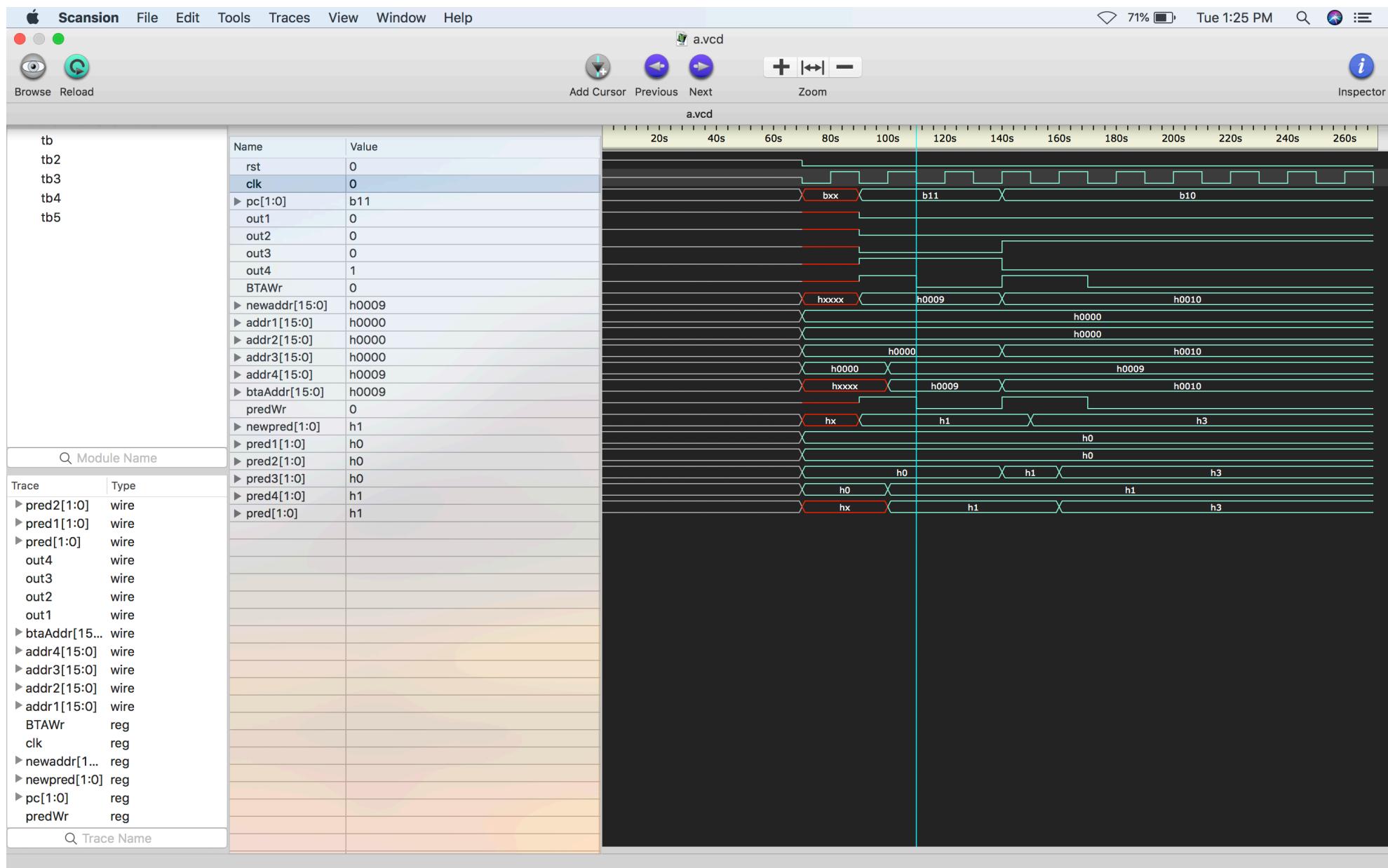
corresponding BTAaddr is read i.e. btaAddr = addr4.



In the case when predWr is 0 and BTAWr is 0 and pc = 2'b11.

That is the same branch occurs again.

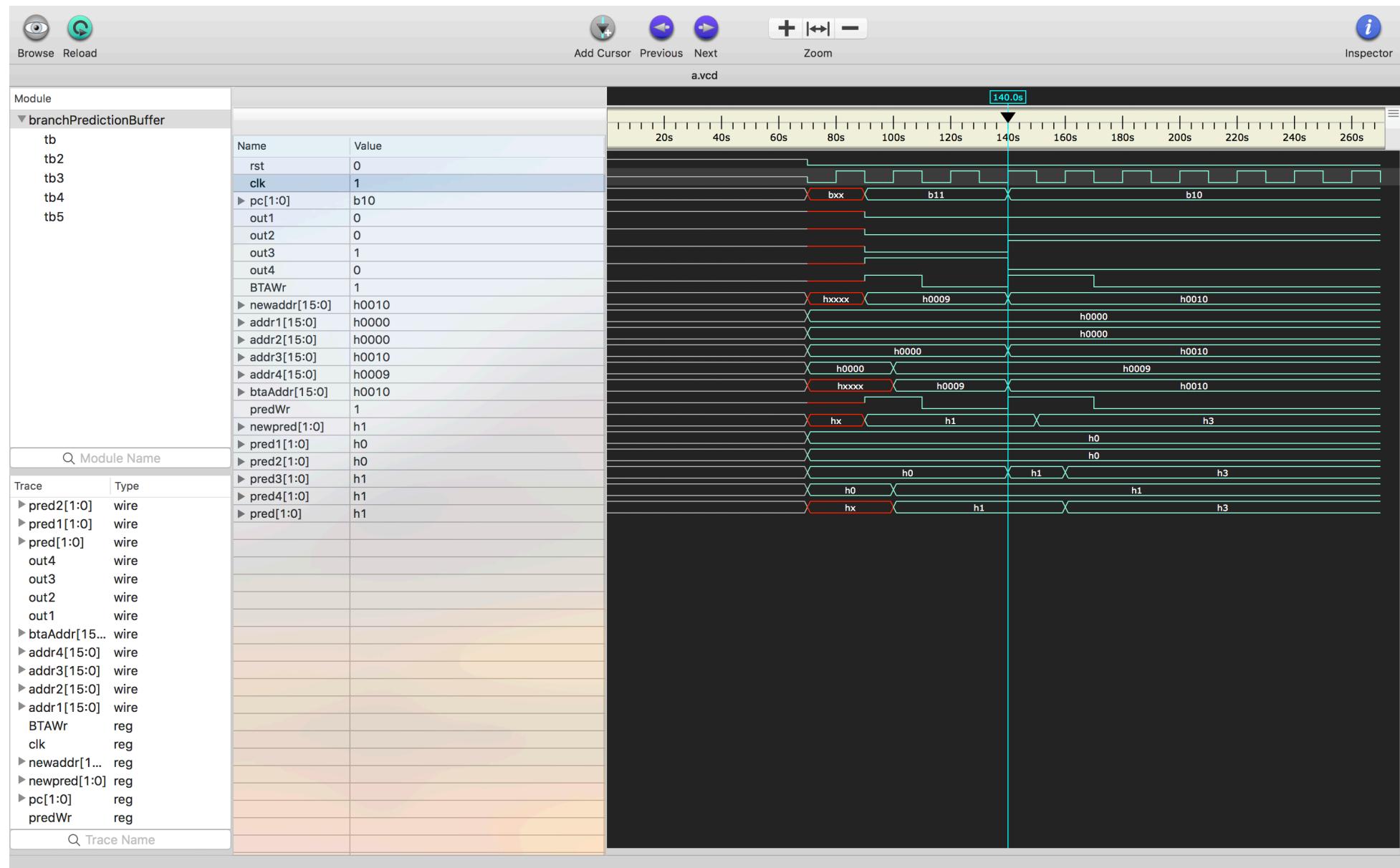
BTAaddr= addr4 and pred = pred4 is read



Same as above case , waveforms is shown for pc = 2'b10

newaddr = 15'd16.

newpred = 2'b01.

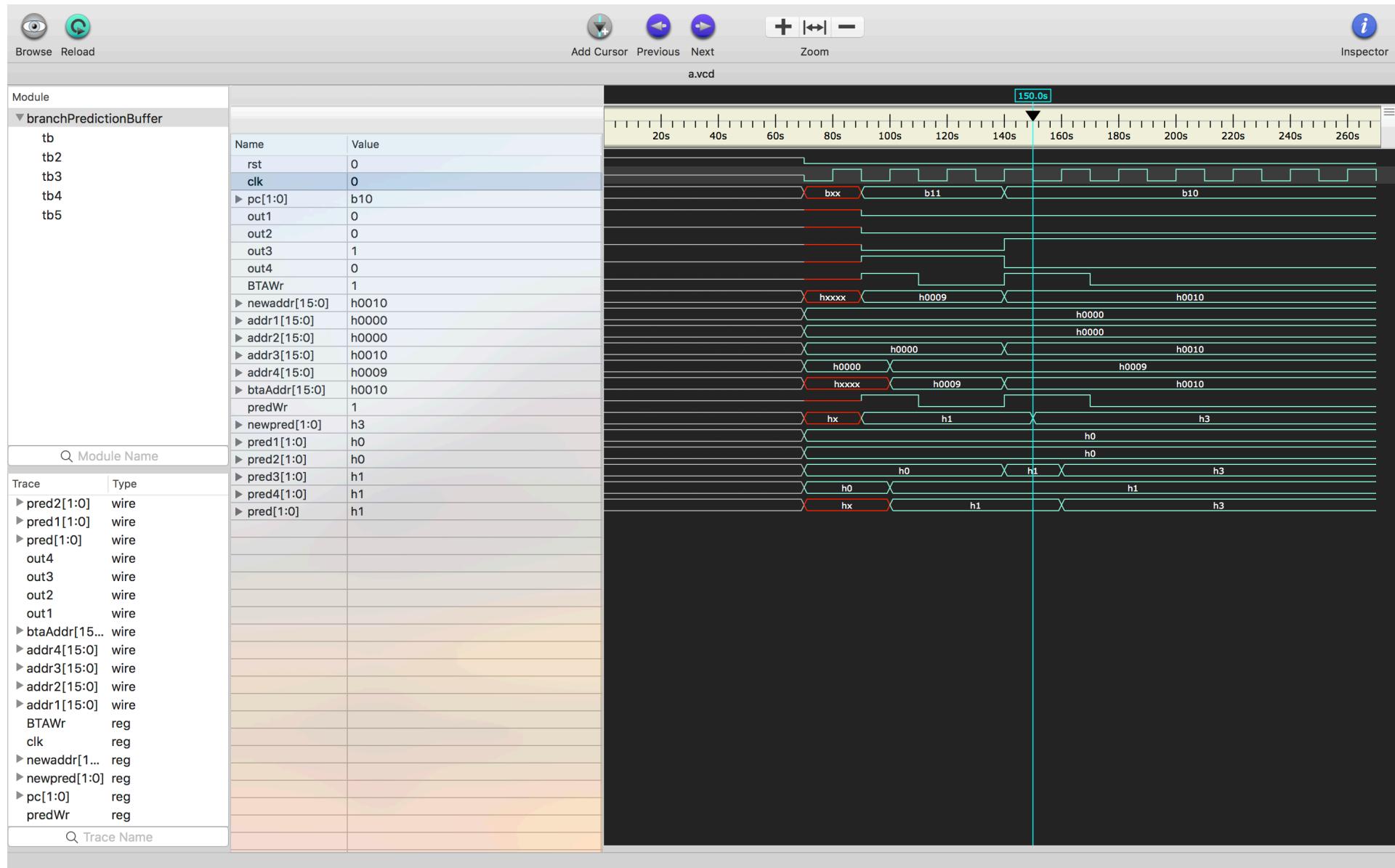


Same as above case , waveforms is shown for pc = 2'b10

newaddr = 15'd16.

newpred = 2'b11.

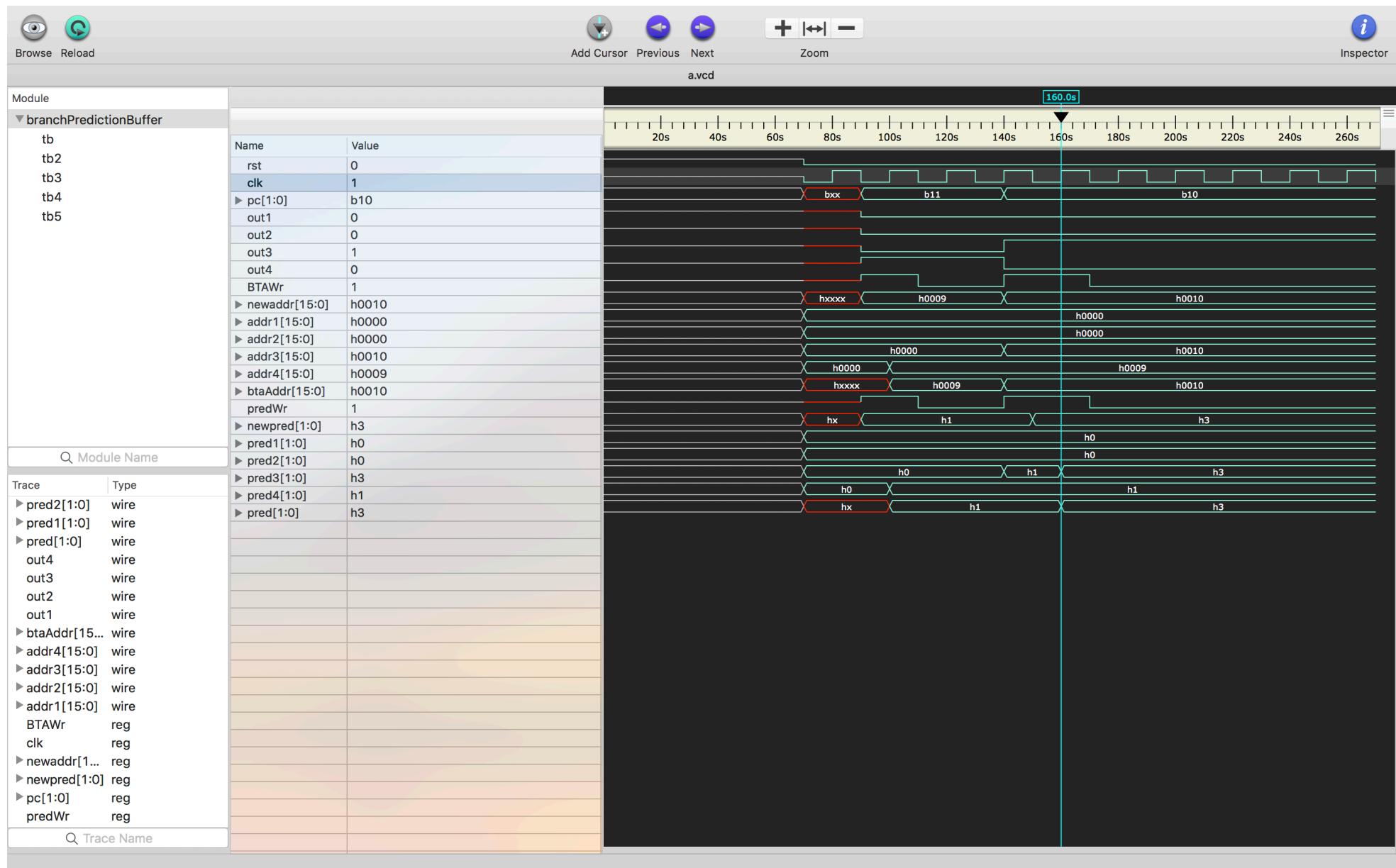
Situation occurs when prediction is wrong twice .



In next positive edge of clock , addr4 is updated to 16'd9 and pred4 is updated to 2'b01.

corresponding prediction is read i.e pred= pred3

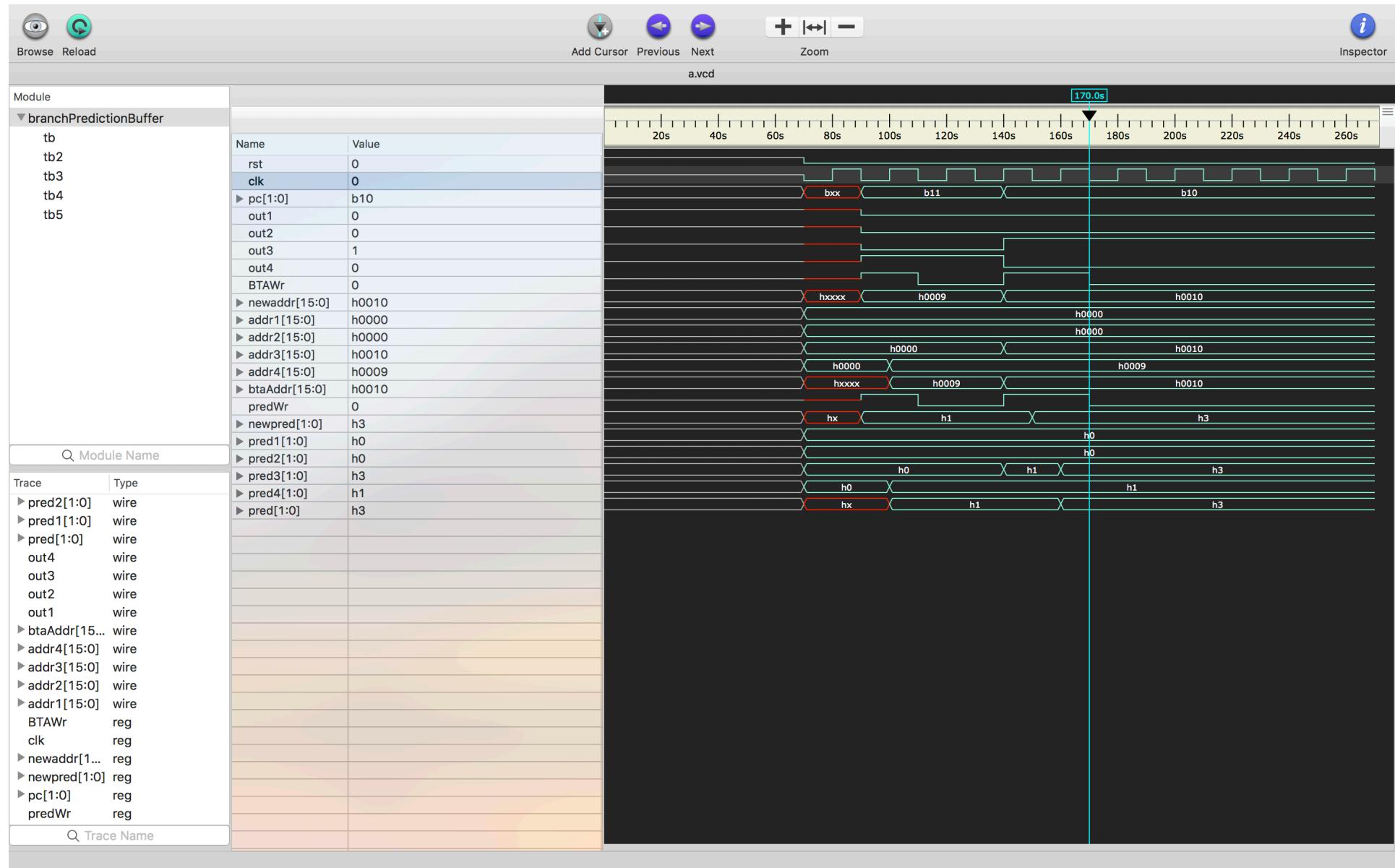
corresponding BTAaddr is read i.e. btaAddr = addr3



In the case when predWr is 0 and BTAWr is 0 and pc = 2'b10.

That is the same branch occurs again.

BTAaddr= addr3 and pred = pred3 is read.



Output on Console

The summary of above can also be shown in the following output generated on console with \$monitor command in Verilog.

```
Apples-MacBook-Pro:Desktop apple$ iverilog BTA.v
Apples-MacBook-Pro:Desktop apple$ ./a.out
VCD info: dumpfile a.vcd opened for output.
out1 = x, out2=x , out3=x, out4=x, addr1= 0 , addr2= 0 , addr3= 0, addr4= 0 , BTA_Address_Selected= x , pred1 = 0 , pred2= 0 , pred3= 0 , pred4 =0 , Prediction_Made = xx
out1 = 0, out2=0 , out3=0, out4=1, addr1= 0 , addr2= 0 , addr3= 0, addr4= 0 , BTA_Address_Selected= x , pred1 = 0 , pred2= 0 , pred3= 0 , pred4 =0 , Prediction_Made = xx
out1 = 0, out2=0 , out3=0, out4=1, addr1= 0 , addr2= 0 , addr3= 0, addr4= 9 , BTA_Address_Selected= 9 , pred1 = 0 , pred2= 0 , pred3= 0 , pred4 =1 , Prediction_Made = 01
|out1 = 0, out2=0 , out3=1, out4=0, addr1= 0 , addr2= 0 , addr3= 16, addr4= 9 , BTA_Address_Selected= 16 , pred1 = 0 , pred2= 0 , pred3= 1 , pred4 =1 , Prediction_Made = 01
out1 = 0, out2=0 , out3=1, out4=0, addr1= 0 , addr2= 0 , addr3= 16, addr4= 9 , BTA_Address_Selected= 16 , pred1 = 0 , pred2= 0 , pred3= 3 , pred4 =1 , Prediction_Made = 11
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