Dr. Ahmet Kirac
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Experienced Digital Signal Processing (DSP) Engineer with unique background in 100Gbps (per lambda) dual-polarization free space and digital coherent optical communications, 64Gbps (per lane) Gen6 PAM4 PCIe interconnect, Wi-Fi connectivity, cellular wireless, terrestrial and satellite digital audio broadcasting, solar photo-voltaic (PV) and light-emitting diode (LED) semiconductor junction efficiencies, solid-state drive (SSD) cloud data storage, and semiconductor System-on-Chip (SoC) development across multiple industries.

PhD and MS in Electrical Engineering.
California Institute of Technology, Pasadena, CA 91125 USA
Thesis Title: Optimal orthonormal sub-band coding and lattice quantization with vector dithering

Selected Skills
Multirate and Multicarrier Signal Processing · Sampling Clock and Data Recovery · Carrier Frequency and Phase Tracking · Polarization Tracking · Optical and Free Space Communications · Wireless Communications · MATLAB · Simulink · FPGA · System on a Chip (SoC) · Advanced Digital Signal and Micro Processors (TI, Tensilica, ARM)

Experience

Cadence Design Systems San Jose, CA, USA

Principal Firmware and Design Engineer Jul 2024 - Present

• PCIe Gen6 multi-protocol production firmware development and customer deployment (64Gbps/lane PAM4 modulation supporting 53Gbps ETH PAM4)

• Performance, power, and area optimization, meeting or exceeding all PCI-SIG standards, offering best in class solutions as IP and silicon.

• Linux python environment development for controlling multiple PCIe devices from one host/server, independent lane margining, SNR, jitter, and packet error measurements

• Rate dependent common clock analog PLL bandwidth optimization and calibration

• Centroid channel estimate and LMS based CTLE optimization and adaptation.

• CDR digital loop filter bandwidth optimization and adaptation

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Kirac Consulting LLC

Principal Consultant Apr 2024 - Jun 2024

References
• Intel Corporation - DARPA Space-BACN
Helped secure 21-month Phase 2 contract (undisclosed sum $) for Technical Area 2 (TA2) 100Gbps free space optical transceiver design, implementation and manufacturing.

Intel Corporation, Altera, Intel Labs Santa Clara, CA, USA
Staff DSP Algorithm Engineer/Researcher Sep 2022 – Mar 2024

DARPA – contract via Intel Federal LLC

The research and development of a reconfigurable DSP chiplet in Intel 3nm technology enabling DARPA multi-mode, 100Gb/s Space-Based Adaptive Communications Node (Space-BACN) optical terminals. (see Patents, Honors and Awards)

• Developed algorithms and complete system model in MATLAB for Space-BACN Optical Inter-Satellite Link (OISL) Communications. The system model includes:

> • DSP (Digital Signal Processing chiplet for base-band signal processing, 3nm CMOS),

> • EIC (Electronic Integrated Circuit for Electronic Current to Voltage and Analog-to-Digital (TIA and A/D) and Digital-to-Analog Electronic Drive Voltage (D/A and Driver) Conversions @50GHz),

> • PIC (Photonic Integrated Circuit for Modulation (optical interference driven by electronic voltage) and Demodulation (photo-detection to electronic current) of dual-polarization optical signals (Silicon Photonics (SiPh)) with external lasers).
> System model also includes device non-idealities and channel impairments.

• Designed novel 2nd and 3rd order robust CDR loop filters with exceptional tracking performance down to -4dB SNR
• Designed rate change filters and developed methods for their fast and efficient implementation
• Blind equalization of both amplitude and phase response for optimal coherent operation that include group delay response compensation and constant modulus algorithm
• Designed algorithms for light polarization drift compensation and tracking

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Kirac Consulting LLC NJ, USA
Owner Apr 2008 – Sep 2022

- System and Algorithm Development for Free Space Optical Communications, Wireless Cellular Radio Access, Wi-Fi Connectivity, and Digital Audio Broadcasting (See Honors and Awards)
- Research in Quantum Computing Hardware and Algorithms, 2019-2022

References:
- SiPort – A Silicon Valley start-up, acquired by Intel Corporation.
  Developed complete system model in MATLAB for implementation of HD Radio receiver System on a Chip (SoC) in CMOS using single-die for microwave radio frequency (RF), mixed signal, and DSP for base-band processing.

Yeditepe University Istanbul, Turkey
Assistant Professor Sep 2017 – Aug 2019 (2 yrs)
- Research in Wireless, DSP
- Taught courses on Wireless, Digital Signal- and Micro-Processors

GTC Solar Istanbul, Turkey
Chief Technical Officer (CTO) Apr 2015 – Aug 2017

- Design and manufacturing of high-efficiency Silicon Mono-crystal Photo-Voltaic Solar Cells and Panels. 130MW panel manufacturing capacity

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Airties Wireless Networks Istanbul, Turkey
Director of Engineering Jun 2014 – Apr 2015
- Development of Wi-Fi transceiver hardware and platform software of industry award winning advanced Wi-Fi Access Point (AP), gateway, and video streaming customer premise equipment (CPE) products for mass volume operators and retail markets.
- The hardware platform with the smallest-form factor dual-band PCB multi-antenna, and software with innovative mesh architectures (See Honors and Awards).
- Managed R&D, product platform design, and manufacturing support

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Dell EMC Hopkinton, MA, USA
Senior Software Consultant Feb 2010 – Jun 2013
Developed advanced statistical learning algorithms in enterprise and internet scale storage for optimal utilization of Solid-State Drives (SSD) and memory pools. (See Patents, Honors and Awards)

Qualcomm Bridgewater, NJ USA
Staff Engineer Jan 2007 – Feb 2009
- Design and implementation of first-generation LTE modem ICs for base stations.
- Developed peer-to-peer cooperative physical layer algorithms and protocols.

Ibiquity Digital Corporation (Xperi Inc.) Warren, NJ, USA
Principal Engineer Jun 2001 – Dec 2006

- Developed world's first HD Radio Receiver for digital audio broadcasting in USA while at iBiquity Digital Corporation, acquired by Xperi.
- Drove the cost significantly lower by developing Analog AM/FM receiver stack in the same DSP platform.
- Designed low-power and low-cost ADC mixed-signal IC with a Low-Intermediate Frequency (IF) architecture.

Lucent Technologies Bell Labs Huntington Beach, CA and Holmdel, NJ USA
Member Of Technical Staff Aug 1998 – June 2001
- Designed DSP algorithms and performed top-level VHDL RTL simulation of CMOS digital System-On-Chip (SoC) for multi-channel ADSL modems.
- Designed mixed-signal integrated chip (IC) for ADC and DAC using over-sampled Sigma-Delta and Delta-Sigma architectures with state-of-the-art resolution and sampling rates.
- Designed world's first CMOS digital ICs for satellite radio receiver chipset for Sirius Satellite Radio which later merged with XM into SiriusXM.

Patents

1. Method and apparatus for enabling access to tiered shared storage using dynamic tier partitioning 9,335,948 · Issued May 10, 2016
2. Performing data storage optimizations across multiple data storage systems US 8,935,493 · Issued Jan 13, 2015
3. Cloud capable storage system with high performance NoSQL key-value pair operating environment US 8,904,047 · Issued Dec 2, 2014
4. Techniques for automated discovery of storage devices and their performance characteristics US 8,868,797 · Issued Oct 21, 2014
5. Techniques for automated discovery and performing storage optimizations on a component external to a data storage system US 8,838,931 · Issued Sep 16, 2014
6. Data storage system modeling US 8,688,878 · Issued Apr 1, 2014
7. Coherent Reception of On/Off Keying and Pulse Position Modulation In Process
8. Methods for adaptive blind equalization and polarization tracking for waveforms used in optical intersatellite communication In Process

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Selected Publications

1. Cyclic LTI systems in digital signal processing IEEE Transactions on Signal Processing · Feb 1, 1999
2. Results on optimal biorthogonal filter banks IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing · Aug 1, 1998
3. Theory and design of optimum FIR compaction filters IEEE Transactions on Signal Processing · Apr 1, 1998
4. On the minimum phase property of prediction-error polynomials EEE Signal Processing Letters · May 1, 1997
5. Results on lattice vector quantization with dithering IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing · Dec 1, 1996

Honors & Awards

- IDP Divisional Recognition Award for work on Space-BACN project - Intel Labs Dec 2023
  For "The cross-team and cross-geo collaboration on the research and development of a reconfigurable DSP chip-let in Intel 3 technology enabling DARPA multi-mode, 100Gb/s Space-Based Adaptive Communications Node optical terminals."
- CSI Awards for Best Customer Premise Technology for Air 4920 in IBC 2015, and for Air 4820 in IBC 2014 Amsterdam, Netherlands.
  Air 4920 product is based on 802.11ac AP baseband processor IC of Broadcom and RF and mixed signal processors of Skyworks and RFMD (now Qorvo after merging with TriQuint), and it had simultaneous operations in dual band (2.4GHz and 5GHz).
  Air4820 product is based on 802.11ac AP IC of the Quantenna Communications which had the highest density of MIMO processing at the time in the industry.
- Winner of EMC Innovation Competition, November 2011, Enterprise Storage Division - Corporate CTO Office, EMC Oct 2011. The idea and proof-of-concept for cloud enabled NoSQL and Key-Value data services with PCIe Flash.
- Certificate of Reviewer, Broadband Technology Opportunities Program (BTOP) - National Telecommunications and Information Administration Dec 2009
- FCC Radio Station Authorization with Radio Service NN-3650-3700MHz and Call Sign WQKS500 - Federal Communications Commission Sep 2009. This license enables to deploy and operate regional broadband mobile network for commercial purposes with an allocated bandwidth of 50MHz. The type of the license is Common Carrier.