Chanikya Badam

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LINKS

LinkedIn: **chanikyabadam**

SKILLS

PROGRAMMING

- System Verilog
- UVM
- Verilog
- C/C++(Basics)
- Python(Basics)

DV SKILLS

- Constraint Randomization
- Assertions
- Test Plan Development
- OOPS
- Coverage - Code/Func
- AMBA - APB Protocol
- AMBA - AHB Protocol
- AMBA - AXI-Lite Protocol
- Regression
- TB Component Developments

TOOLS

- Cadence virtuoso
- Cadence IMS
- Synopsis Design Compiler
- Cadence Verdi
- VCS Synopsis

COURSEWORK

GRADUATE

Design of Digital System
Design test of Multi-core chips
Analog Electronics
Basics of Yield (AMD)
Formal verification/ SVA (NXP)
Coverage (NXP,EC)
Assertion(EC)

EDUCATION

ROCHESTER INSTITUTE OF TECHNOLOGY
MS Electrical Engineering
Focusing in Digital Design and Verification
May, 2019

GITAM , INDIA.
B.Tech in Electrical Engineering
Aug, 2015

SUMMARY

Enthusiastic Electrical Engineer specializing in Digital Verification, with hands-on experience in SystemVerilog and UVM methodology.

EXPERIENCE

DESIGN VERIFICATION ENGINEER | Efficient Computers, Austin
April 2025 - Now

- Verified data flow graph architecture for arithmetic operations, math functions, and RAM load/store functionality, ensuring correct data path.
- Created UVM sequence item classes and driver code for the AHB & APB protocol, supporting transaction-level stimulus generation and driving bus-level signal activity.
- Built a UVM verification environment from scratch (UVM skeleton) for a new project and validated DUT connectivity using Cadence Xcelium, and also assisted in setting up the Cadence Xcelium and coverage tools.
- Enhanced code and functional coverage through constrained-random testing, assertions, and coverage closure techniques.

DESIGN VERIFICATION ENGINEER | NXP Semiconductors, Austin
Feb 2022 - Feb 2025

- Developed and verified testbenches for automotive products (ASIL-B/D) using UVM, SystemVerilog, C, and industry-standard EDA tools.
- Verified and optimized DMA, LPI2C, interrupts, FIFO Tx/Rx, and safety blocks, ensuring reliable SoC/SS-level performance and compliance using an ARM core processor.
- Improved functional/code/toggle coverage across multiple peripherals using randomization, SVA, and formal verification techniques.

PROCESS INTEGRATION ENGINEER | Global Foundries, New York
Sep 2019 - Feb 2022

- Responsible for managing ASIC and MPW products for 14nm technology.
- Collaborated with cross-functional module teams (Litho, Etch, Metrology, Cleans, PC, Test Development, and Customer Engineering) to ensure wafer and test performance met specifications.
- Analysing the trend charts, work with process engineers to make sure the wafers are within the spec's.
- Gained experience verifying schematics & layouts across multiple mask layers in the manufacturing process.

CO-OP ENGINEER IN TECHNOLOGY VALIDATION TEAM | AMD, Texas
Jan 2018 - Aug 2018

- Responsible for developing an environment for creating, converting and validating patterns for 7nm FinFet technology.
- Wrote patterns for validating SoC's/IP's like JTAG/P1500/scan diagnostics in the test chip.
- Setting up a Verilog model for validating the IP's in the test chip using VCS in Verdi using Linux environment.

PROJECTS

A MULTISTAGE PIPELINE REGISTER IS DESIGNED USING PERL/PYTHON FOR GENERATING A SYNTHESIZABLE VERILOG HDL CODE | RIT

- Designed using Getopt package user can give either "-param " or "-width", "-Stages", "-Outfile" and "-reset".
- A synthesizable RTL code (2-128) stages and each stage is (1-64 bits wide) and testbench in Verilog is obtained using Perl/Python.