A Review on Various Divider Circuit Designs in VLSI

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Abstract—**In this paper we investigate Vedic divider, double precision floating point divider, Vedic divider used in RSA cryptography, Goldschmidt algorithm based floating point divider, which have been proposed by different researchers. At the point when the investigation of the different dividers have been performed, Vedic divider has less power sparing, faster and less space possessed compared to customary divider. The Goldschmidt computational calculation is actualized utilizing subtractor and floating-point multiplier. By joining Boolean rationale with ancient Vedic arithmetic, generous measure of iteration are reduced, diminishment in delay and decrease in power for most part utilized designs. The division calculation for double precision floating point has lessening in power utilization and configuration space contrast with various double precision division techniques.**

Keywords--- Vedic divider, double precision, Goldschmidt algorithm, RSA cryptography.

I. INTRODUCTION

Division operation is one of most asset expending calculation in ALU of processor. It has higher significance in equipment execution of flag handling unit which has excellent illustrations are prepared i.e. GPU. Division operation has consecutive sort of operations in this manner it was all the more exorbitant as far as computational intricacy, than other numerical operations [7, 9].

Numerous recursive procedures are proposed by various investigators to realize fast divider [1-11], like recurrence method (restoring [8], non-restoring [9, 10, 11]), division using convergence method, division by series expansion [1]. The cost regarding area and computational complexity of many-sided quality of digit recurrence calculations [8] is low, but as a result of the huge number of cycles; consequently, delay(spread deferral) turns out to be high. While, a many of the researchers depend on high radix usage of recurrence calculation method [9, 10] to diminish iterations, in this manner the latency winds up plainly enhanced reports [1-7], yet these arrangements likewise extends the hardware multifaceted (complexity) nature. Some other appealing thoughts depend on practical iterations, Goldschmidt's [1] calculation that use increase strategies alongside the multiplication development, where measure of remainder digits got per cycle is multiplied. The drawback of the above procedures is operands are institutionalized previously and used primitives increases, and the rest are not specifically acquired.

Vedic Maths is antiquated arrangement of Indian science which has an extraordinary method of estimations in view of 16 Sutras (Formulae). “Nikhilam Navatascaramam Dasatah” is Sanskrit expression designating “all from 9 and last from 10”, embraced from the Vedas; equation is experienced to execute division hardware. By utilizing Vedic technique, division is actualized by addition and multiplication, along these lines lessens the cycle, attributable to the significant decrease in propagation delay.

II. GOLDSCHMIDT ALGORITHM BASED FLOATING POINT DIVIDER ON FPGA

This paper was proposed by Naginder Singh and others [1]. The Goldschmidt algorithm is completed using subtractor and floating point multiplier of 32-bit. The striking element of this configuration is module that process mantissa in floating point multiplier of 32-bit is planned utilizing multiplication of 24-bit of Vedas (Urdhva-triyakbhyam-sutra) strategy. The multiplier is a floating point number of 32 bit, by

utilizing Vedic multiplier, higher computational speed is yielded and is utilized to expand execution of the divider. The primary target is to blend the proposed divider circuitry implementing on FPGA utilizing Verilog HDL. The proposed divider is utilized as a part of the plan of floating point divide – add fused design. This algorithm is a single precision type floating point divider.

This algorithm utilizes iterative procedure in which denominator gets scaled down to 1 to get last quotient. The iterative procedure, utilized as a part of this calculation, utilizes a few complex operations to perform division, where not just the accuracy is to be kept up for substantial interval; however exactness ought to be high for better operation. The device usage parameters were enhanced along these lines; utilization of power and Latency are lessened by 26% and 42.6% individually when contrasted with existing DAF.

III. VEDIC DIVIDER - A High Performance Computing algorithm for VLSI Applications

This paper was proposed by Soma BhanuTej[2]. Here, the Parvartya yojayet calculation is connected to build up a superior division and timing examination is performed on Vedic divider and regular divider. A practically tried 32-bit dividend / 16-bit divisor twofold Vedic divider is incorporated, has power sparing of ~109mW in contrast with ordinary divider and speed is ~7 times speedier and territory(area) involved is ~13 times less than traditional divider.

In this paper the division calculation and its design in view of antiquated Indian science. Paravartyayojayet (PYY) in terms of Sanskrit signifies "transpose and apply" is embraced from the Vedas; formula. By utilizing Vedic technique, division is actualized by addition and multiplication, accordingly lessens the no. of iterations, inferable from the generous decrease in propagation delay, space and power.

This paper demonstrates that Vedic divider is of superior computational algorithm that has brought down power utilization and space. Likewise as basic way, slack is high for Vedic divider which can work for high frequencies.

IV. VEDIC DIVIDER: ASIC for High Speed VLSI Applications

This paper was proposed by Prabir Saha, Arindam Banerjee and others [3]. Novel divider structure for rapid VLSI utilizing such old system is discussed. Delay and utilization of dynamic power for the divider hardware were limited fundamentally by evacuating superfluous recursion through Vedic mathematics. The usefulness of this architecture is execution parameters of engendering propagation delay and power utilization are computed by SPICE. The delay of 16-bit by 8-bit divisor hardware was just ~10.5ns and expended ~24μW control for area of ~10.25 mm2. By consolidating Boolean logic with old Vedic arithmetic, generous measure of iteration disposed of about ~45% decrease in delay and ~30% diminishment of power contrasted and for the most part utilized methods.

The design offered 50%, 45%, and 41% change separately as far as propagation delay contrasted and digit recurrence, Convergence and series expansion based engineering execution individually.

V. IMPLEMENTATION OF VEDIC DIVIDER ON RSA CRYPTOSYSTEM

This paper was proposed by Jyotinnyee subudhi and C.Karthick [4]. RSA cryptosystem is chief public key cryptography that is utilized for information security. A divider is key equipment hinders in many applications, for example, cryptography, advanced signal processing and other coherent calculations. Less power utilization, rapid and littler area is absolute most imperative perspectives for outlining of VLSI framework. Speed and space are typically contrary limitations. So great outline needs to set harmony amongst area and speed. It is likewise well established certainty that Divider unit shapes a necessary piece of processor plan. Because of this respect, high speed divider design turns important. This paper manages the usage of Vedic divider in calculation of RSA rather than regular divider. Vedic mathematics portrays a technique called 'Dhvajanka - On the top of flg' which is a summarized formulae in Vedic

division utilized as part of Vedic divider. Power dissipation has been diminished. Significant change has been seen as far as area usage and time delay.

VI. BINARY DIVISION ALGORITHM AND HIGH SPEED DECONVOLUTION ALGORITHM

This paper was proposed by Surabhi Jain, Mukul P, Garg, Sandeep S [5].Division is constantly thought to be cumbersome and a standout amongst the most troublesome operations in arithmetic and henceforth every one of the use of division calculations in VLSI have higher requests of timing considerations and space . Vedic Maths then again offers another all encompassing way to deal with arithmetic. Its range reaches out from the most solid estimations of numerical calculation to the most theoretical parts of the flow of knowledge.

In this work they have executed a streamlined binary division hardware utilizing sutras of Vedic Maths which are Nikhilam Sutra and Parvartya Sutra. This work talks two calculations of division and their application for ascertaining deconvolution. Both the calculations have been executed with enhanced results of time delay and with fewer complexities. Results come about for proposed Vedic divider circuit demonstrates a diminishment in area of 19 % than the traditional strategy.

VII. NOVEL BINARY DIVIDER ARCHITECTURE FOR HIGH SPEED VLSI APPLICATIONS

This paper was proposed by Ratiranjan S, Bandan Kumar Bhoi, Manoranjan P [6]. The Novel Binary divider hardware for rapid VLSI design utilizing such ancient methods is introduced here. Delay and power utilization for divider hardware was limited fundamentally by expelling pointless recursion by Vedic division approach. The usefulness of this circuit was tested and execution parameters like delay and power utilization are computed. The Propagation delay of subsequent 8-bit by 4-bit divider hardware is just ~19.9ns and expended ~34Mw control for LUTs of 23/1536. By joining Boolean logic to antiquated Vedic mathematics, considerable amount of iteration are disposed about ~46% lessens delay and ~27% diminishment of power contrasted and for the most part utilized (Repetitive subtraction method) design.

TABLE 1: Comparison of Latency time and Power of Various divider circuits

Type of Divider	Latency time	Power
Goldschmidt algorithm	75ns	0.037W
Vedic Divider	-2059.2(ps)	187nW
Conventional Divider	-13806.8(ps)	1409nW
RSA Cryptosystem	7.90ns	176.26mW

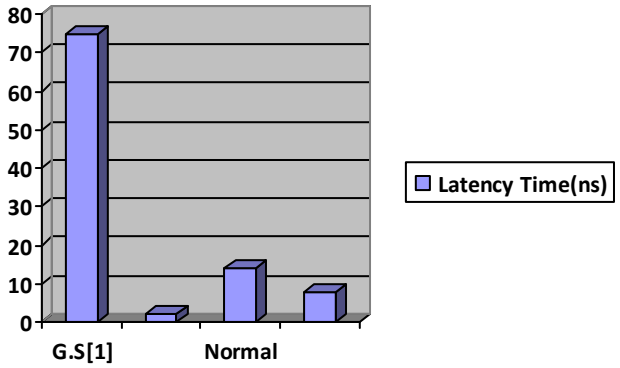

Fig 1: Latency Time (ns) calculations of various Divider circuits

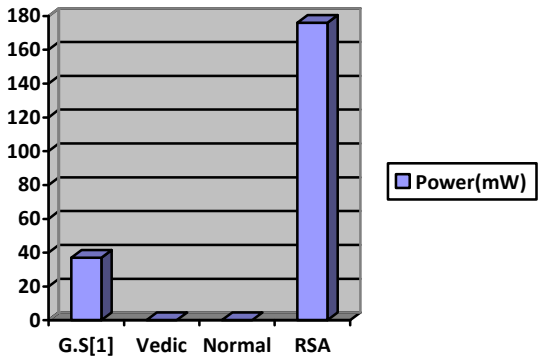

Fig 2: Power (mW) calculations of various Divider circuits

TABLE 2: Comparison of Various Division methods.

Division algorithms	Parameters			
	FPGA Device Family	**No. of Slice Registers used**	**No. of Slice LUT's**	**No. of bonded IOB's**
GOLDSCHMIDT ALGORITHM[1]	Spartan 6	3025/54576	9281/27288	161/296
VEDIC DIVIDER ON RSA CRYPTOSYSTEM[4]	Quartus II 9.0	N/A	N/A	N/A
BINARY DIVISION ALGORITHM[5]	Virtex 5	--	72/12480	22/172
NOVEL BINARY DIVIDER[6]	Spartan 3E	17/960	30/1920	13/66
Division algorithms	**Parameters**			
	Tool	**Technology**	**Frequency**	**Dynamic Power**
VEDIC DIVIDER[2]	Cadence RTL compiler	180nm and 32 nm CMOS technology	300 MHz	756405 nW
VEDIC DIVIDER: ASIC [3]	Spice spectre	90 nm CMOS technology	N/A	24.32 µW

VIII. CONCLUSION

From the study, we have realized that Vedic divider is of elite computational algorithm which has brought down power scattering and area. By using novel binary divider architecture propagation delay of 8-bit by 4- bit divider circuit is ~19.9ns and consumes ~34Mw power for LUTs of 23 out of 1536. While the relating change in power is 44 %(D.R), 35 %(Con), and 27 %(S.E) compared with Vedic divider.

IX. REFERENCES

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