LOGICALLY REVERSIBLE ARITHMETIC CIRCUIT USING PASS-TRANSISTOR

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ABSTRACT

This paper proposes novel reversible logic circuits, i.e., a reversible ExOR gate and a two-way AND gate. The gates operate in both directions and the input and output are indistinguishable. We design the circuits using dual-line pass-transistor logic. Applying the method to arithmetic circuits, we realize logically reversible arithmetic circuits. Because proposed circuits have no garbage output, the adder and multiplier operate as the subtracter and divider respectively by replacing the input with the output. We confirm the behavior of the circuits by both real experiments and SPICE simulations.

1. INTRODUCTION

Recently, reversible logic receives much attention of many researchers in quantum computing [1, 2]. As for reversible computation, Bennett studied theoretically [3], and Fredkin and Toffoli suggested reversible circuits [4]. The reversible computing is incomplete without both the reversible logic and reversible circuit. As you know, logic gates such as AND or OR are one-way logic, that is, the logic does not have inverse. Even though logic has inverse such as ExOR, the circuits of CMOS logic are one-way, that is, the direction of signal flow is fixed based on the structure and reverse signal flow is impossible.

This paper considers four operations, i.e., addition, subtraction, multiplication and division. These operations are logically reversible. For example, let us consider an equation $a + b = c$. If we give a and b, we obtain the result c. If we give b and c, we obtain $a = c - b$ by subtraction. This example shows that the addition and subtraction are reversible operations. In the same way, the multiplication and division are also reversible operations. However, if we make an arithmetic circuit using Fredkin gate, the circuit has garbage outputs which make it impossible to realize reversible arithmetic circuits [5]. To overcome this difficulty, this paper proposes a method to construct arithmetic circuits which operate reversibly by using dual-line pass-transistor logic.

First we propose a logically reversible ExOR gate and a two-way AND gate. The AND gate is not logically reversible but it allows two-way operations. Second, we also propose logically reversible adder and multiplier which operate as a subtracter and a divider by reversing the signal flow. Furthermore, we confirm the behavior with real experimental circuits.

2. REVERSIBLE LOGIC

There exist only two different truth tables with one bit input and one bit output reversible logic (see Table 1). These are the follower and the inverter.

Table 1. One bit input and one bit output reversible logic

A	B
0	0
1	1

A	B
0	1
1	0

Next, we consider two bit input and one bit output reversible logic. In this case, the "reversible" means that we can select any two terminals as input. There exist only two different truth tables which satisfy the above condition (see Table 2). These are the ExOR and the NOT of ExOR and the terminals A,B,C are symmetric.

Table 2. Two bit input and one bit output reversible logic

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

In order to extend the concept of the reversible logic to an AND gate, we introduce a two-way AND logic. The "two-way" means that we can select any terminal as input although the output is not always uniquely determined. Because the logic does not have inverse, the output has possibility not to be fixed. The truth table of the two-way AND logic is shown in Table 3. This truth table consists of three states "0", "1" and "Z". the Z means "don't care" bit. The "-" in the table means that the output can not be defined.

Table 3. Truth table of two-way AND gate. Z means "don't care" bit. "-" means that the output can not be defined. The (a), (b), (c) show the truth tables for the output C, B, A, respectively.

(a)

IN A	IN B	OUT C
Z	Z	Z
Z	0	0
Z	1	Z
0	Z	0
0	0	0
0	1	0
1	Z	Z
1	0	0
1	1	1

(b)

IN A	IN C	OUT B
Z	Z	Z
Z	0	Z
Z	1	1
0	Z	Z
0	0	Z
0	1	-
1	Z	Z
1	0	0
1	1	1

(c)

IN B	IN C	OUT A
Z	Z	Z
Z	0	Z
Z	1	1
0	Z	Z
0	0	Z
0	1	-
1	Z	Z
1	0	0
1	1	1

3. DESIGN OF REVERSIBLE CIRCUIT

We design the reversible circuit using dual-line pass-transistor logic [2] and monotone circuit. Boolean values X=1 and X=0 are denoted by $(X,\overline{X})=(1,0)$ and $(X,\overline{X})=(0,1)$, respectively. For example, an inverter is shown in Fig. 1. It consists of a metal cross-over. Because of the monotone circuit, we set all initial values $(X,\overline{X}) = (0,0)$.

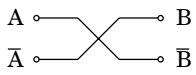

Fig. 1. Reversible inverter

For the implementation of an on-off switch, we use a CMOS transmission gate which is a two-way switch shown in Fig. 2.

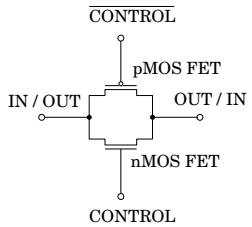

Fig. 2. CMOS transmission gate

We represent the "don't care" bit with high impedance. Figure 3 shows a method for the detection of the high impedance. In order to detect the high impedance state as (0,0), we put pull down resistors. The correspondences between the states and the output voltages are shown in Table 4. The voltage 5V corresponds to the state 1.

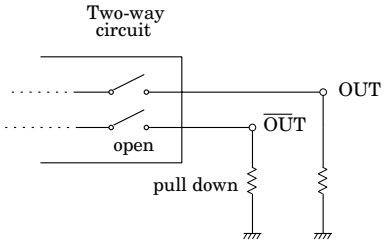

Fig. 3. Detection of high impedance

Table 4. Output voltage in 0, 1, and Z

State	Output voltage (V)	
	OUT	$\overline{\text{OUT}}$
0	0	5
1	5	0
Z	0	0

4. REVERSIBLE EXOR CIRCUIT

The reversible ExOR circuit is shown in Fig. 4. The left hand and the right hand of the dotted line show the parts of gate control and signal flow, respectively. The terminals $A, \overline{A}, B, \overline{B}, C, \overline{C}$ in gate control part are connected to the terminals $A, \overline{A}, B, \overline{B}, C, \overline{C}$ in signal flow part, respectively. The symbol of the switch is defined by Fig. 5.

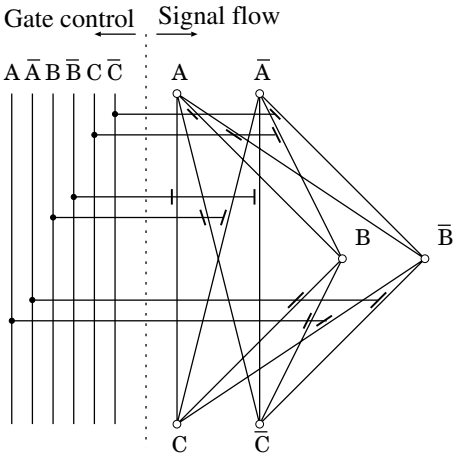

Fig. 4. Reversible ExOR gate

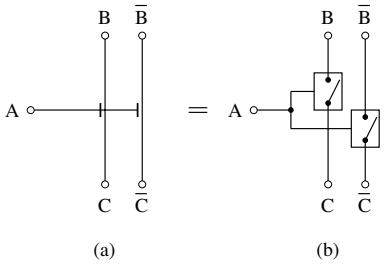

Fig. 5. Definition of the switch. : The switches are closed when A = 1

If A =1, then B and C are connected ($\overline{B}$ and $\overline{C}$ are also connected). If A=0, then B and $\overline{C}$ are connected ($\overline{B}$ and C are also connected). The structure of terminals A, B and C is symmetric.

Table 5 shows the result of a real experimental circuit. Because the circuit has symmetry, we show the case that A and B are input. We can confirm the behavior of the ExOR gate with enough accuracy.

Table 5. Experimental result of ExOR

Input[V]		Input[V]		Output[V]	
A	$\overline{A}$	B	$\overline{B}$	C	$\overline{C}$
0.00	5.03	0.00	5.03	0.00	5.02
0.00	5.03	5.03	0.00	5.02	0.00
5.03	0.00	0.00	5.03	5.02	0.00
5.03	0.00	5.03	0.00	0.00	5.02

5. TWO-WAY AND GATE

Figure 6 shows a design of the two-way AND gate. If A = 1, then B and C are connected, and if A = 0, then A and C are connected. If C=1, all terminals are connected each other. The structure of terminals A and B is symmetric.

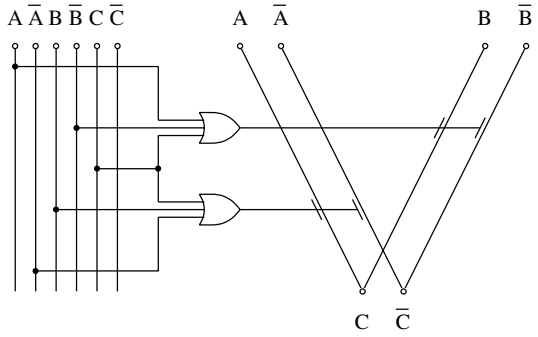

Fig. 6. Two-way AND gate

Table 6 shows the result of a real experiment. Although the table shows only one case, we confirmed that the circuit operates in all cases.

Table 6. Experimental result of AND:A and C are input

Input[V]		Input[V]		Output[V]	
A	$\overline{A}$	C	$\overline{C}$	B	$\overline{B}$
0.00	0.00	0.00	0.00	0.00	0.00
0.00	0.00	0.00	5.03	0.00	0.00
0.00	0.00	5.03	0.00	5.02	0.00
0.00	5.03	0.00	0.00	0.00	0.00
0.00	5.03	0.00	5.03	0.00	0.00
0.00	5.03	5.03	0.00	-	-
5.03	0.00	0.00	0.00	0.00	0.00
5.03	0.00	0.00	5.03	0.00	5.02
5.03	0.00	5.03	0.00	5.02	0.00

6. REVERSIBLE ADDER

A reversible full adder is shown in Fig. 7. If A, B and C are input, the output is S and C_+, and if A, C and S are input, the output is B. The line which does not need the reversible signal flow, consists of normal irreversible logic circuits. This normal logic circuits compensate voltage-level loss which is caused by on-resistances of pass-transistors. Experimental results of the full adder is shown in Table 7. Although the table shows only one case, we confirmed that the circuit successfully operates in all cases.

The circuit of *n*-bit adder is shown in Fig. 8. Because the carry bit consists of active normal gates, the number of serial stages of pass-transistors is always less than three and the voltage-level loss does not increase. We successfully confirmed the behavior of 4-bit reversible adder using SPICE.

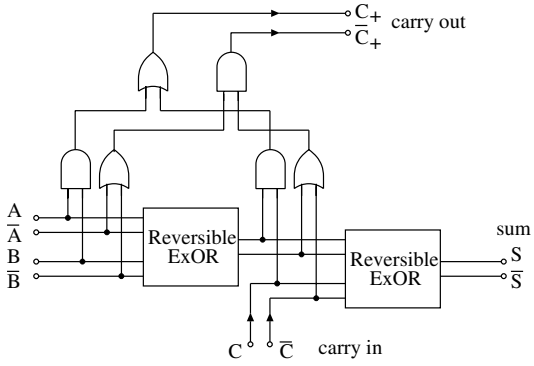

Fig. 7. Reversible full adder

Table 7. Experimental results of reversible full adder: A, C and S are input.

Input[V]			Output[V]		Output[V]	
A	C	S	B	C_+	$\overline{B}$	$\overline{C}_+$
0.00	0.00	0.00	0.00	0.00	5.02	5.03
0.00	0.00	5.03	5.02	0.00	0.00	5.03
0.00	5.03	0.00	5.02	5.03	0.00	0.00
0.00	5.03	5.03	0.00	0.00	5.02	5.03
5.03	0.00	0.00	5.02	5.03	0.00	0.00
5.03	0.00	5.03	0.00	0.00	5.02	5.03
5.03	5.03	0.00	0.00	5.03	5.02	0.00
5.03	5.03	5.03	5.02	5.03	0.00	0.00

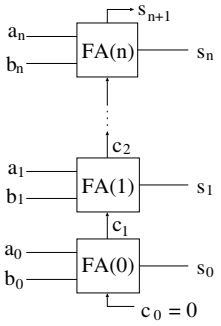

Fig. 8. *n*-bit reversible Adder

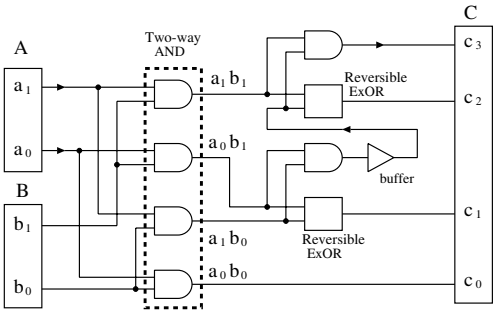

Fig. 9. 2×2 bit reversible multiplier. Only the positive-logic is shown.

7. REVERSIBLE MULTIPLIER

A reversible 2×2 bit multiplier is shown in Fig. 9. This figure shows only the positive-logic. In the same way as the reversible adder, the line which does not need the reversible signal flow, consists of normal irreversible logic circuits. If we give A and B, then we obtain the output on C. If we give A and C, then we obtain the output on B. In the operation as divider, we have to give consistent data to the product C.

The result of a real experimental circuit is shown in Table 8. Although this table shows only the operation as divider, we successfully confirm the operation as multiplier. Further, we successfully confirmed the behavior of 4×4 bit reversible multiplier using SPICE.

Table 8. An experimental result of 2×2 bit reversible multiplier: operations as divider.

Input[V]		Input[V]				Output[V]		Output[V]	
a_1	a_0	c_3	c_2	c_1	c_0	b_1	b_0	$\overline{b_1}$	$\overline{b_0}$
0.00	0.00	0.00	0.00	0.00	0.00	0.02	0.02	0.02	0.02
0.00	5.03	0.00	0.00	0.00	0.00	0.00	0.00	5.01	5.02
0.00	5.03	0.00	0.00	0.00	5.03	0.00	5.02	5.01	0.00
0.00	5.03	0.00	0.00	5.03	0.00	5.01	0.00	0.00	5.02
0.00	5.03	0.00	0.00	5.03	5.03	5.01	5.02	0.00	0.00
5.03	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.01	5.01
5.03	0.00	0.00	0.00	5.03	0.00	0.00	5.01	5.01	0.00
5.03	0.00	0.00	5.03	0.00	0.00	5.01	0.00	0.00	5.01
5.03	0.00	0.00	5.03	5.03	0.00	5.01	5.01	0.00	0.00
5.03	5.03	0.00	0.00	0.00	0.00	0.00	0.00	5.02	5.02
5.03	5.03	0.00	0.00	5.03	5.03	0.00	5.02	5.02	0.00
5.03	5.03	0.00	5.03	5.03	0.00	5.02	0.00	0.00	5.02
5.03	5.03	5.03	0.00	0.00	5.03	5.02	5.02	0.00	0.00

8. CONCLUSION

We proposed the logically reversible and two-way logic gates using dual-line pass-transistor logic and monotone circuits. Further, we applied the gate to the logically reversible arithmetic circuits. We confirmed the behavior of the reversible circuits using both real experiments and SPICE simulations.

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9. REFERENCES

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