EC- 310 Testing and Diagnosis of Digital System Design

BIST implementation of BCD 16-Bit adder Using Verilog

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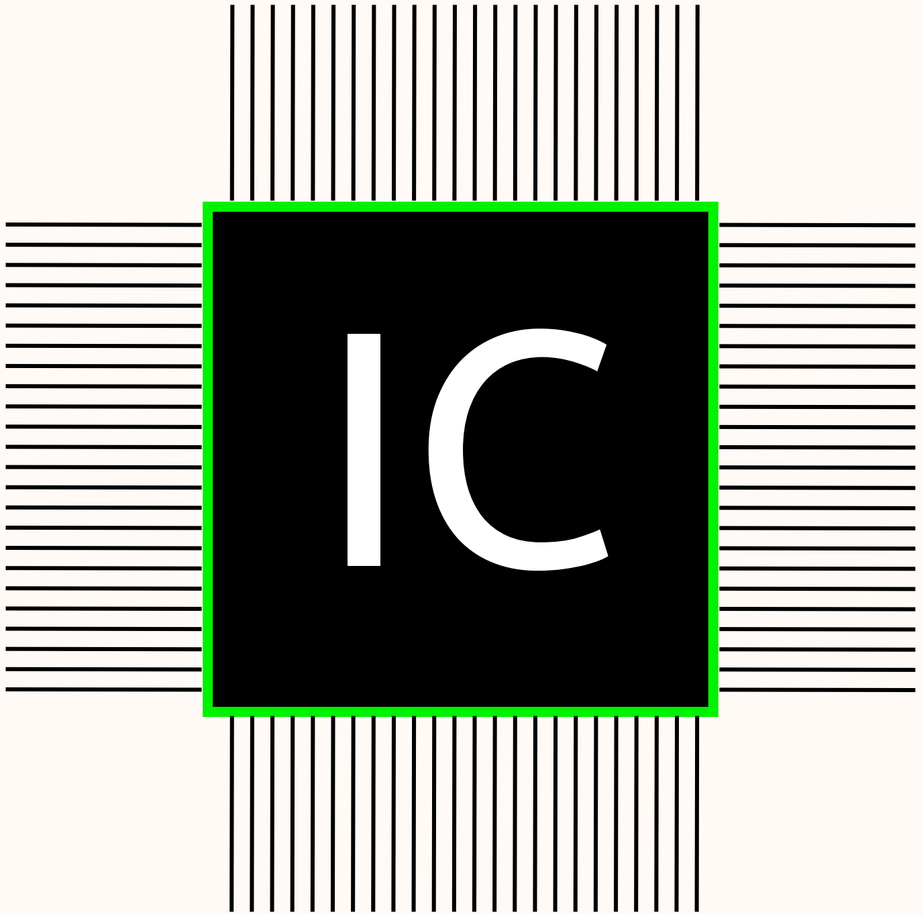
INTRODUCTION

ELECTRONIC DEVICES and their development are rapidly progressing and thus, thorough testing and verification of their components, such as for example digital circuits, is crucial. Moreover, testing with guaranteed fault coverage (100% fault detection) is extremely important for digital circuits that are used in critical systems.

New testing methods are needed for the next generation of electronic equipment.

Some of the techniques now becoming popular include design for testability **(DFT)**, built-in self-test **(BIST)**, and automatic test vector generation **(ATVG).**



Advantages of implementing BIST include:

1) Lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated

2) Better fault coverage, since special test structures can be incorporated onto the chips

3) Shorter test times if the BIST can be designed to test more structures in parallel

4) Capability to perform tests outside the production electrical testing environment, actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

Brief Description

In this project for designing Built In Self Test(BIST) we have designed

- Cellular Automata for generating pseudo random test patterns(in which the cells are following rule 150 and rule 90 alternatively)
- 16 bit BCD adder as the Circuit Under Test(CUT)
- Multiple Input Signature Register(MISR) for analysing and compacting the response of the circuit under test which provides output when the TPG provides inputs to the bcd adder.
- Finally we have created a controller to connect all the sub modules so as to synchronize the three circuits

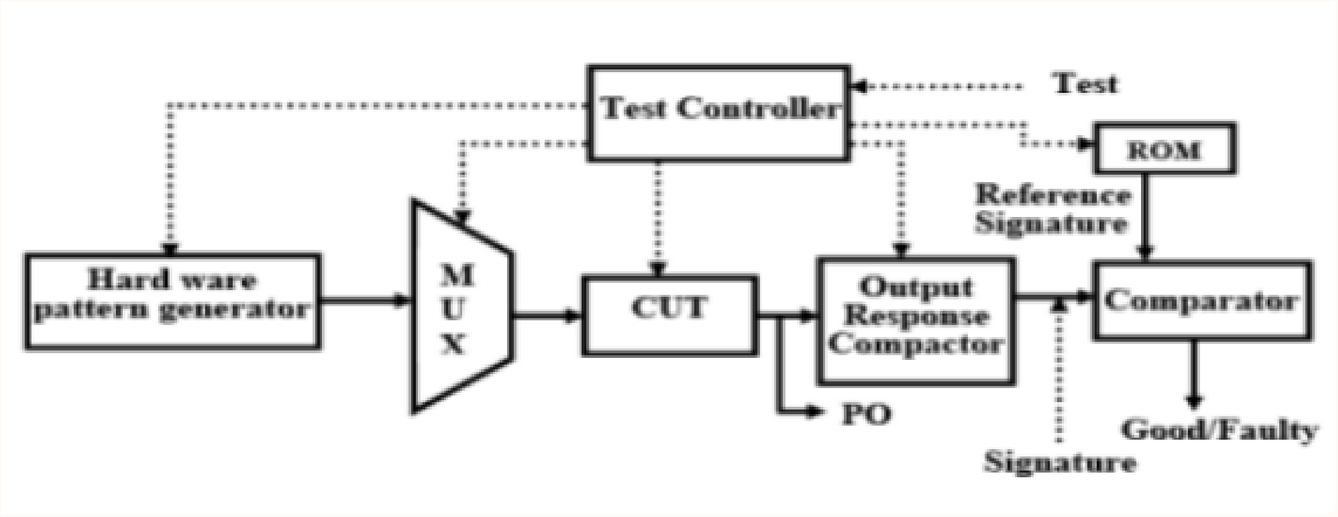
BIST

Built-in Self Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing

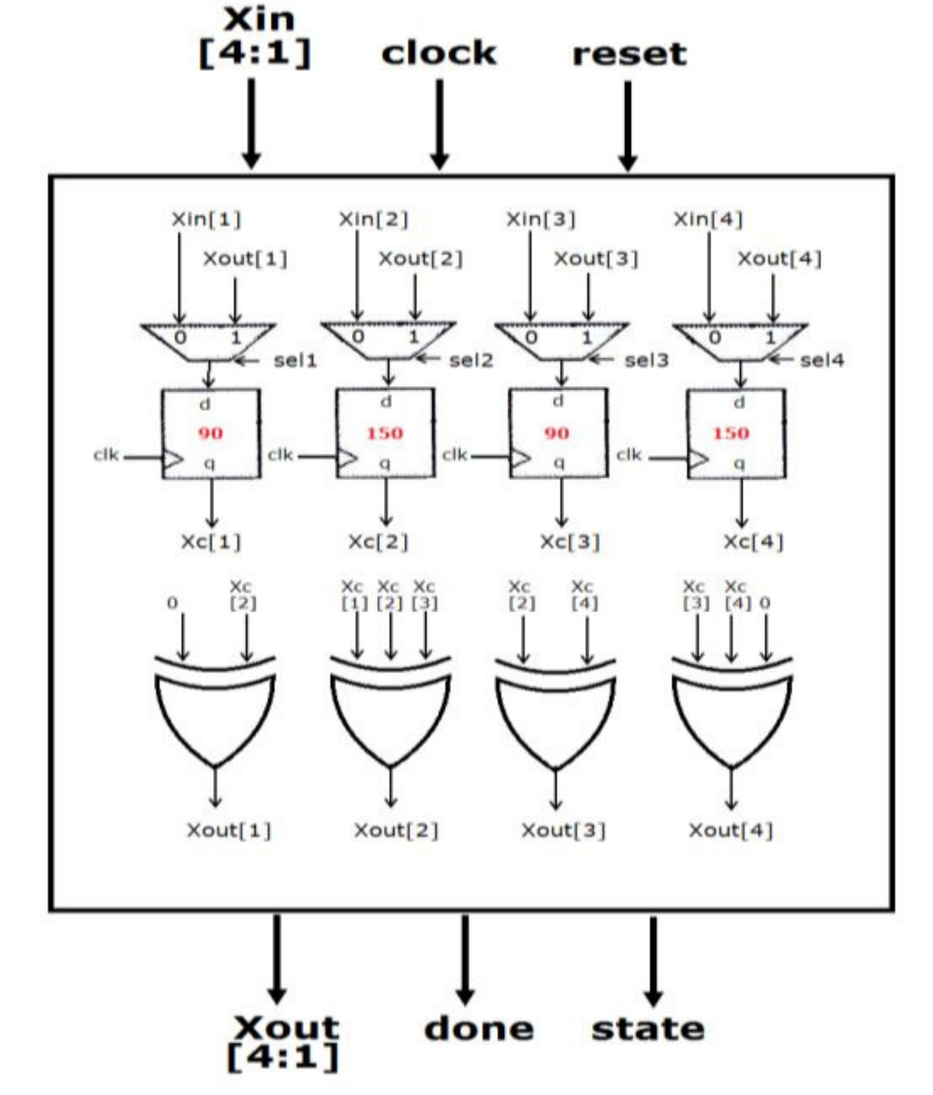
IT is a **Design-for-Testability** (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly.

The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary widely.

Here, we are using BIST to detect the fault in BCD adder .The BIST controller is there which helps to control or act as the processing unit for the three components:
a)Test pattern generator
b)Circuit under test
c) Output analyzer



CELLULAR AUTOMATA (TPG)



To implement Rule 150

$$y_i(t+1) = y_{i-1}(t) \oplus y_{i+1}(t),$$

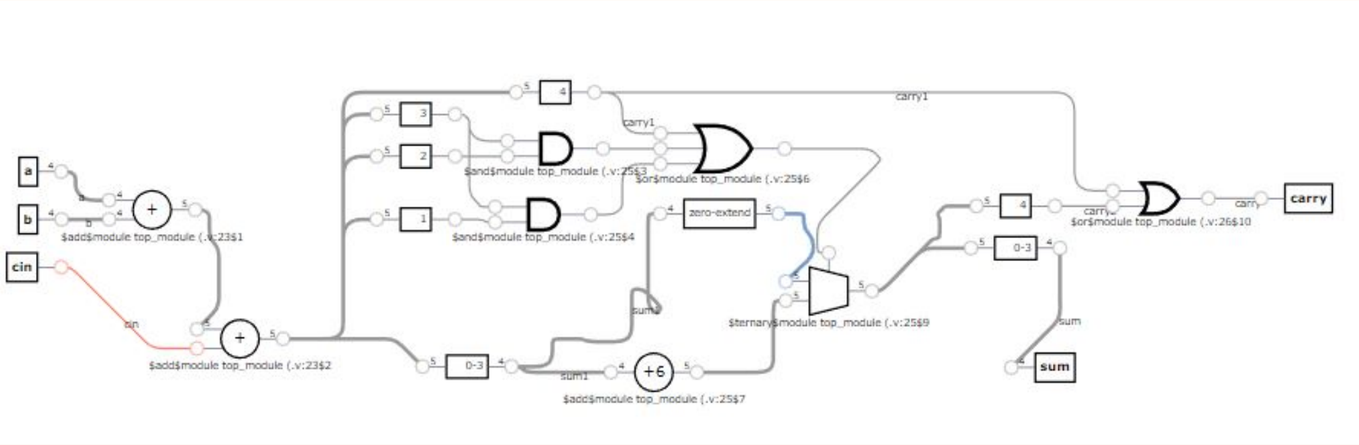
To implement Rule 90

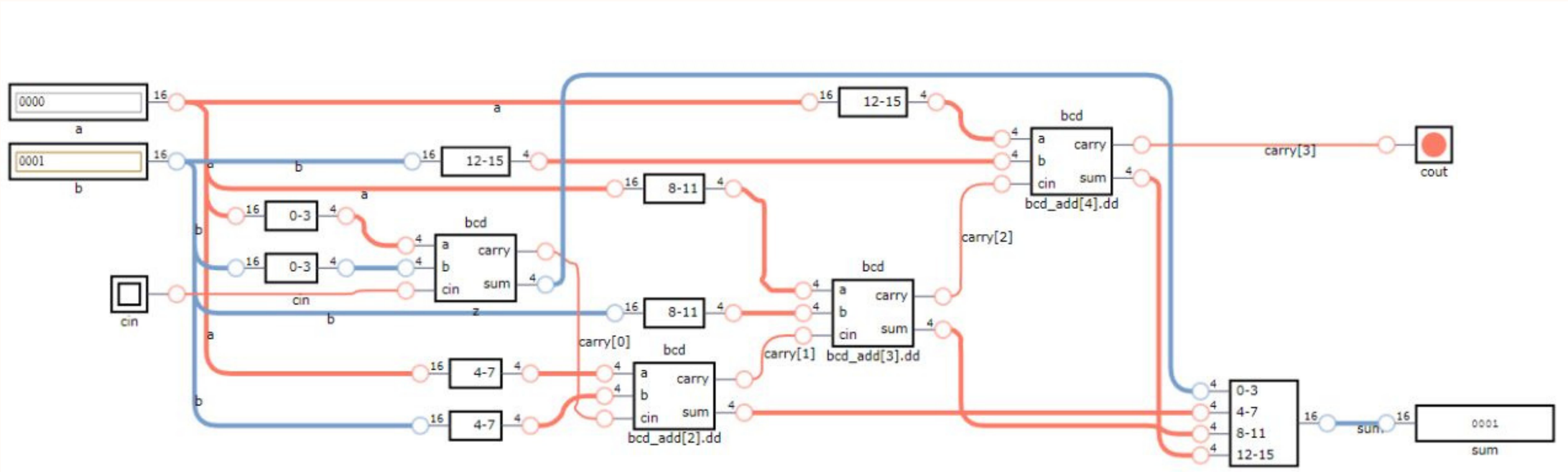
$$y_i(t+1) = y_{i-1}(t) \oplus y_i(t) \oplus y_{i+1}(t),$$

where yi(t) denotes the state of cell **i** at time **t**.

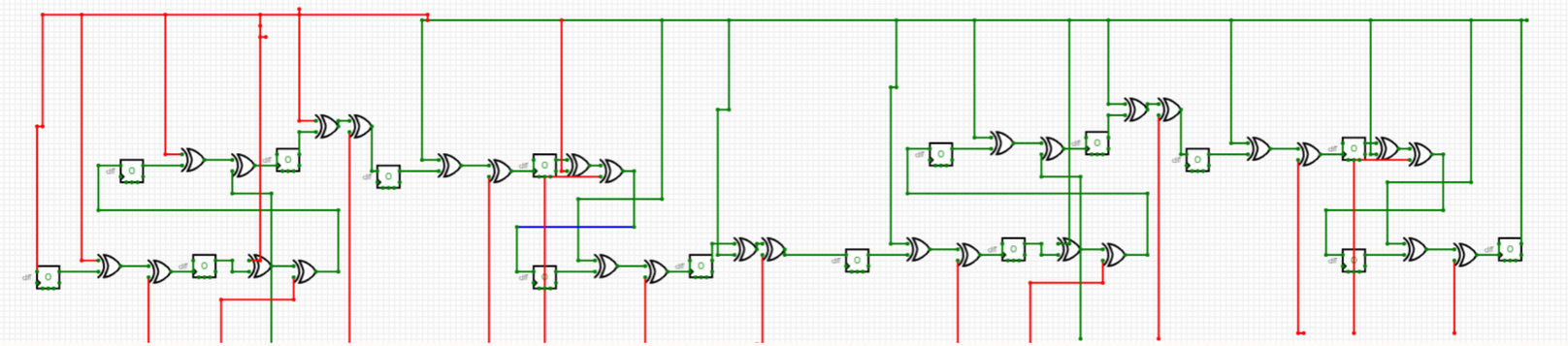
BCD ADDER (CUT)

Circuit under test is 16 bit BCD adder . We have implemented BCD (binary-coded decimal) that adds two BCD digits and carry-in, and produces a sum and carry-out. We have instantiated 4 copies to create a 4-digit BCD ripple-carry adder.





MISR(ORA)



- MISR is the multiple inputs signature register
- It used to compact the multiple bit output responses into the distinct bit response and to analyze its signature which helps in quicken the methodology to test the circuit.

- Here, we are taking the 16 bit input from the result of CUT ,ie. SUM and giving each bit to sixteen D-flip FLop. Then at every clock cycle the TPG will create a test pattern through which MISR will give some values.

- When the pattern will start repeating , at that clock cycle the output of the MISR will give us the signature.

OUTPUT(without fault)

```
Running Icarus Verilog simulator...
VCD info: dumping is suppressed.
MACHINE IN TEST MODE
 SIGNATUER 17431 =17431
MACHINE IS NOT FAULTY
Hint: Total mismatched samples is 0 out of 0 samples
Simulation finished at 20480 ps
Mismatches: 0 in 0 samples
```

From here we can conclude that the final signature is **good** signature

OUTPUT (with fault)

```
Running Icarus Verilog simulator...
VCD info: dumping is suppressed.
MACHINE IN TEST MODE
OUTPUT RESPONSE 00821 !=17431
MACHINE IS FAULTY
Hint: Total mismatched samples is 0 out of 0 samples
Simulation finished at 20480 ps
Mismatches: 0 in 0 samples
```

As we can see that the final signature is not equal to the **ideal** signature. Therefore the we can conclude that the machine is faulty.