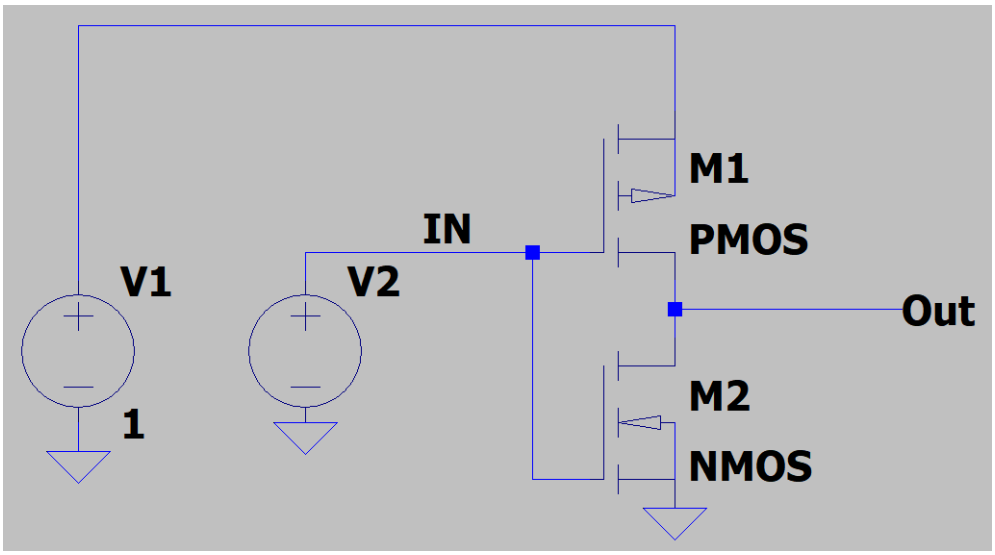
Aim:

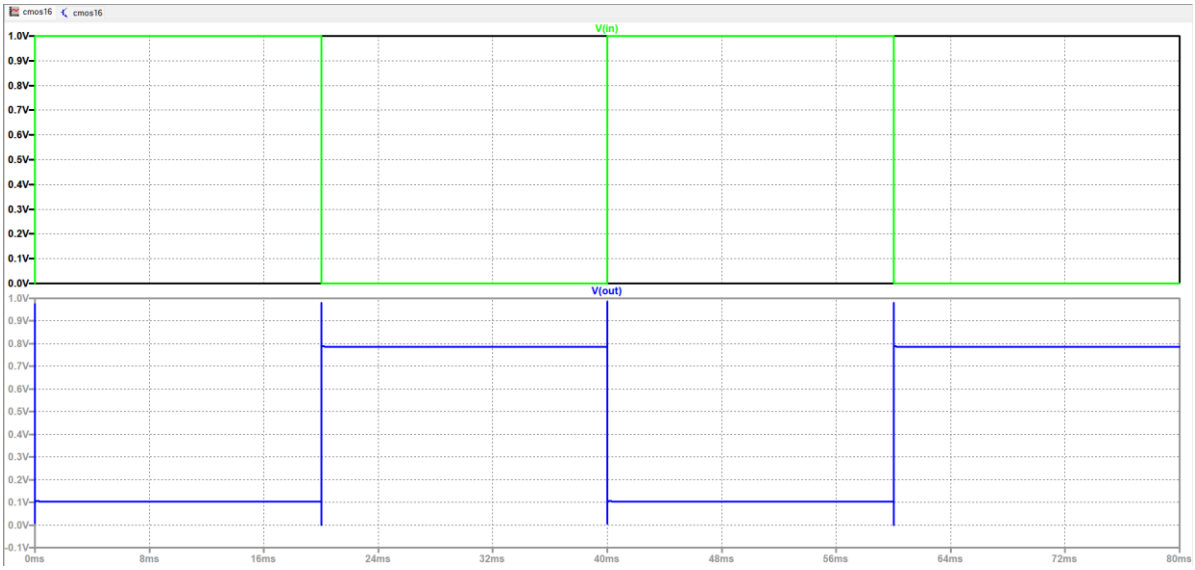
To study CMOS inverter characteristics and calculate power dissipation and output delay for different technology.

Schematic:

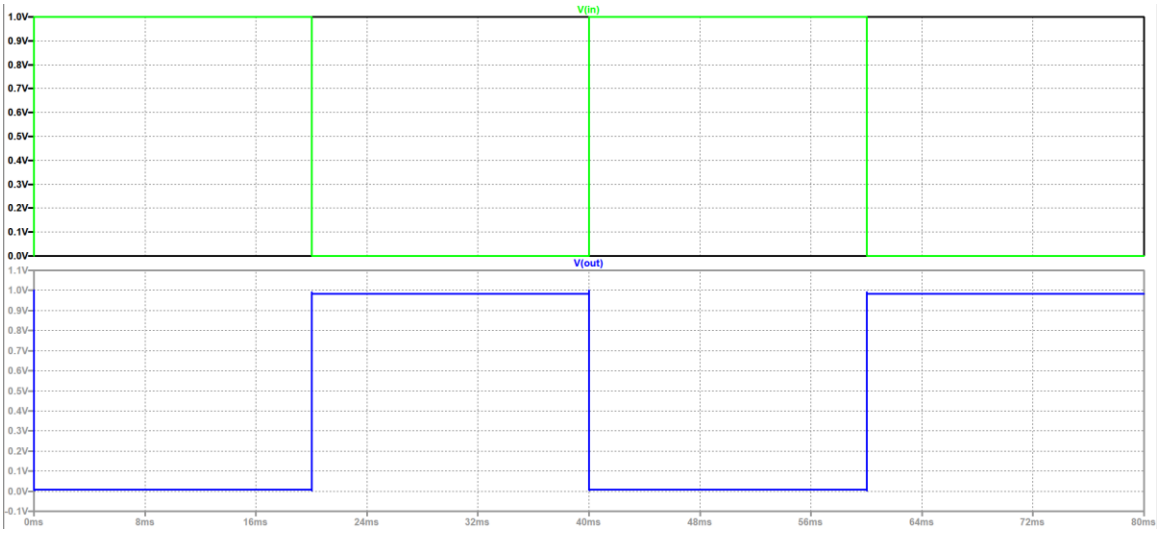


Outputs and Graphs:

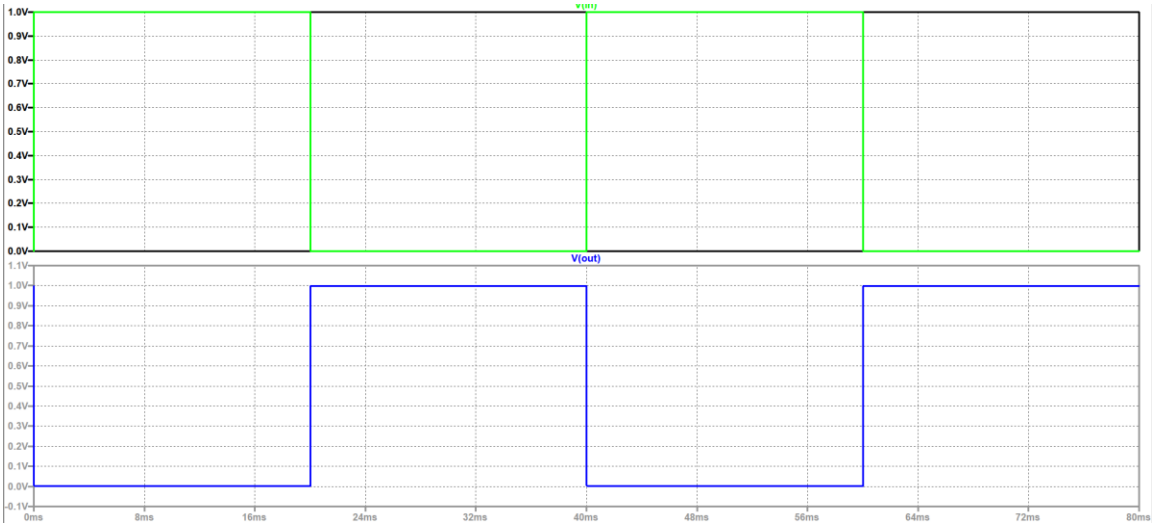
- 16nm Technology



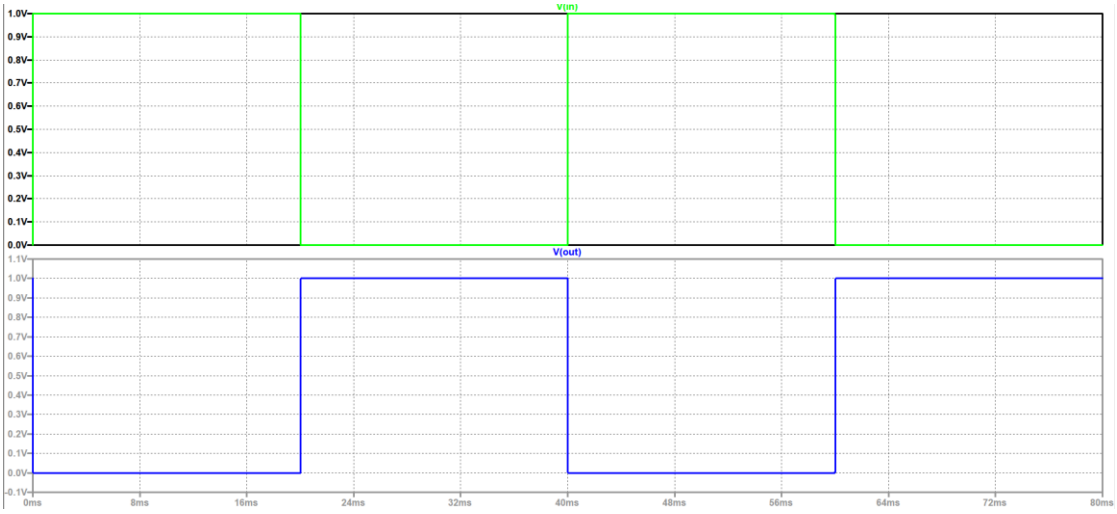
- 22nm Technology



- 32nm Technology



- 45nm Technology



Observations and Calculations:

Formulas Used:

- Output Delay= (Tlh + Thl) / 2
- Power Dissipation= Vdd * $I_{D(avg)}$

Vdd=1 V for all technologies

16 nm Technology

Tlh=42.537068ns
Thl=326.48425ns
Output Delay= 184.514ns
$I_{D(avg)}$= 2.7062µA
Power Dissipation= 2.7062µW

22 nm Technology

Tlh=218.64909ns
Thl=94.179023ns
Output Delay= 156.414ns
$I_{D(avg)}$= 473.05nA
Power Dissipation= 473.05nW

32 nm Technology

Tlh= 41.120264ns
Thl= 237.59473ns
Output Delay= 139.357ns
$I_{D(avg)}$= 48.012nA
Power Dissipation= 48.012nW

45 nm Technology

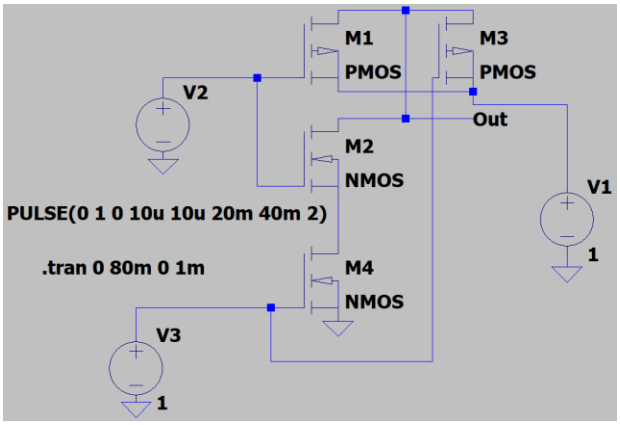
Tlh= 34.173056ns
Thl= 328.94157ns
Output Delay= 181.55 ns
$I_{D(avg)}$= 4.9063nA
Power Dissipation= 4.9063nW

Aim:

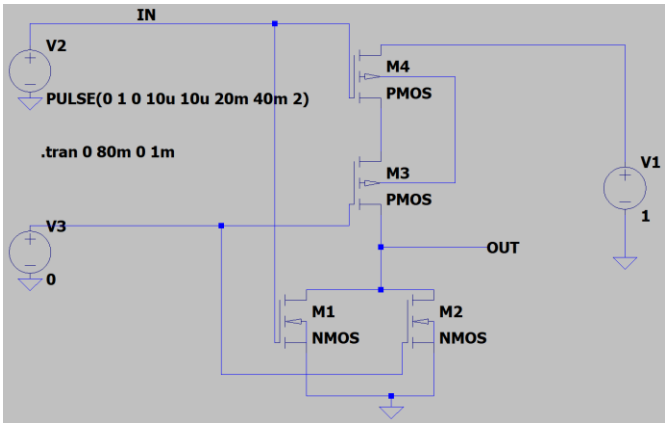
Realization of NAND and NOR gates using PMOS and NMOS transistors.
And calculation of output delay.

Schematic:

NAND



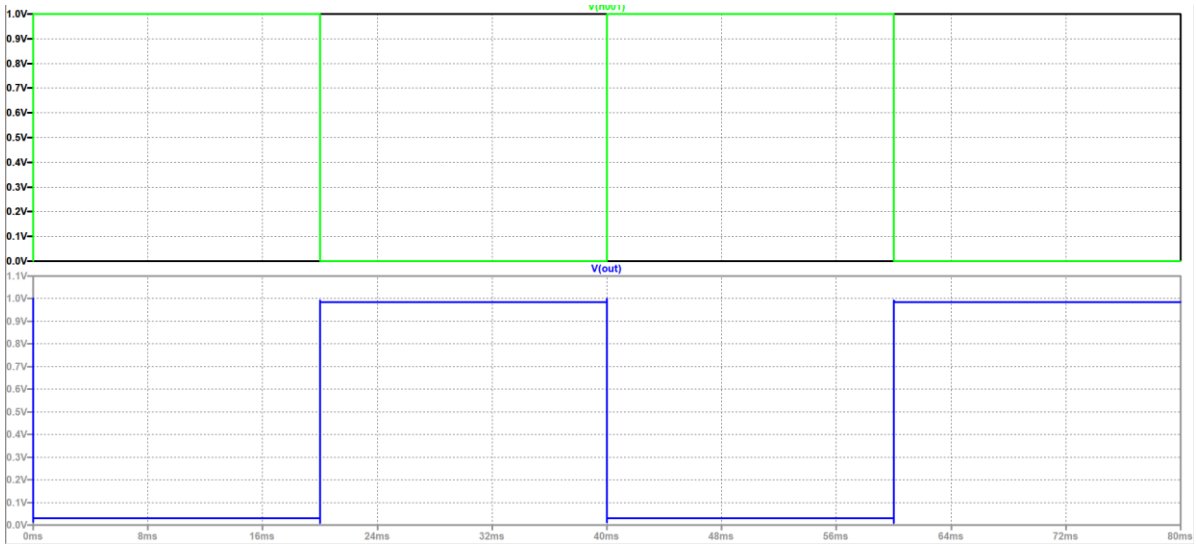
NOR



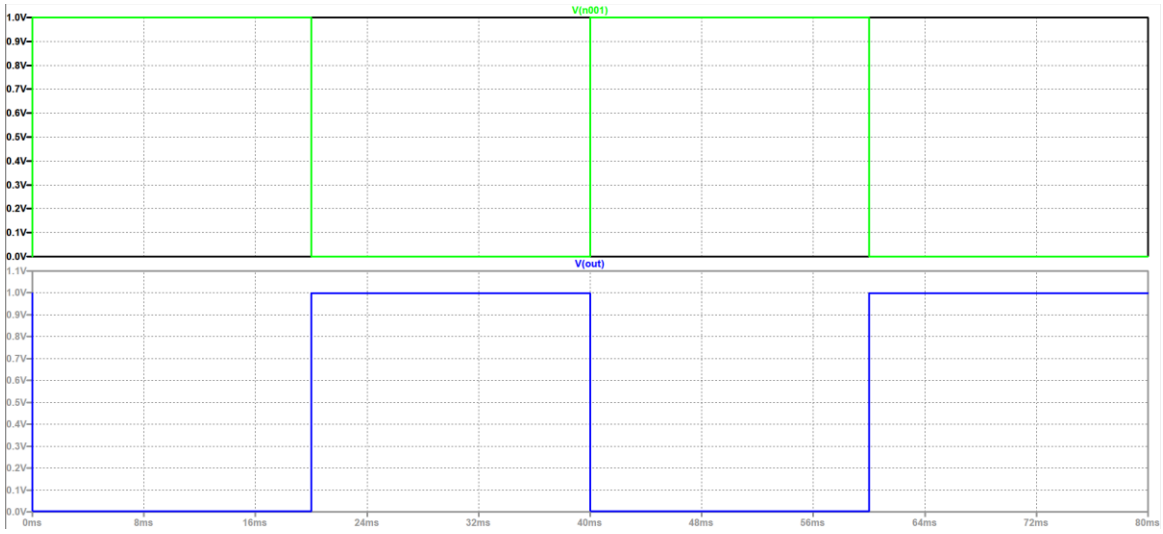
Outputs and Graphs:

NAND

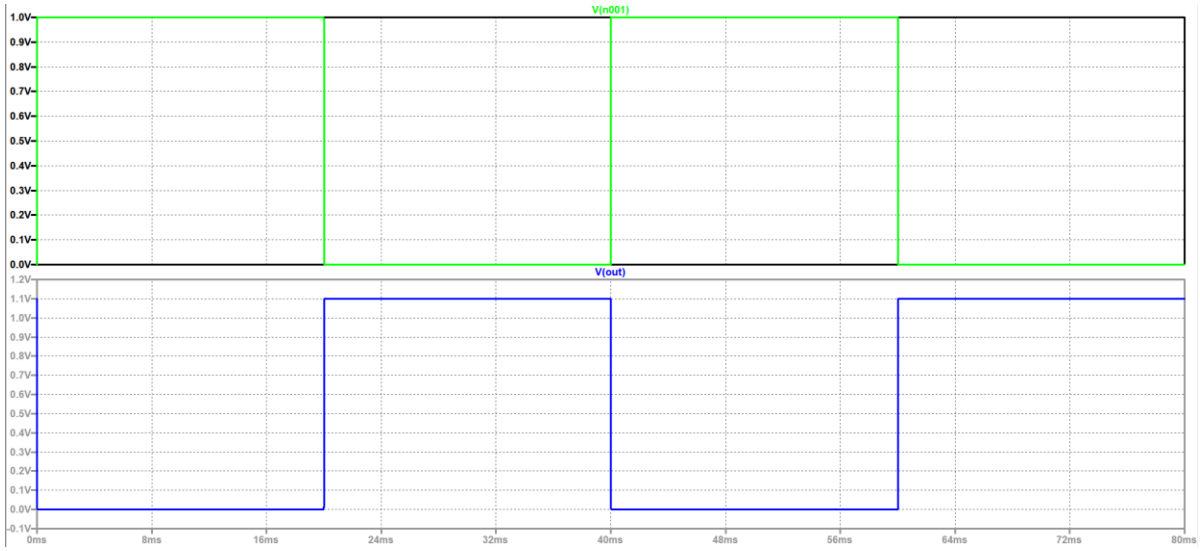
- 22nm Technology



- 32nm Technology



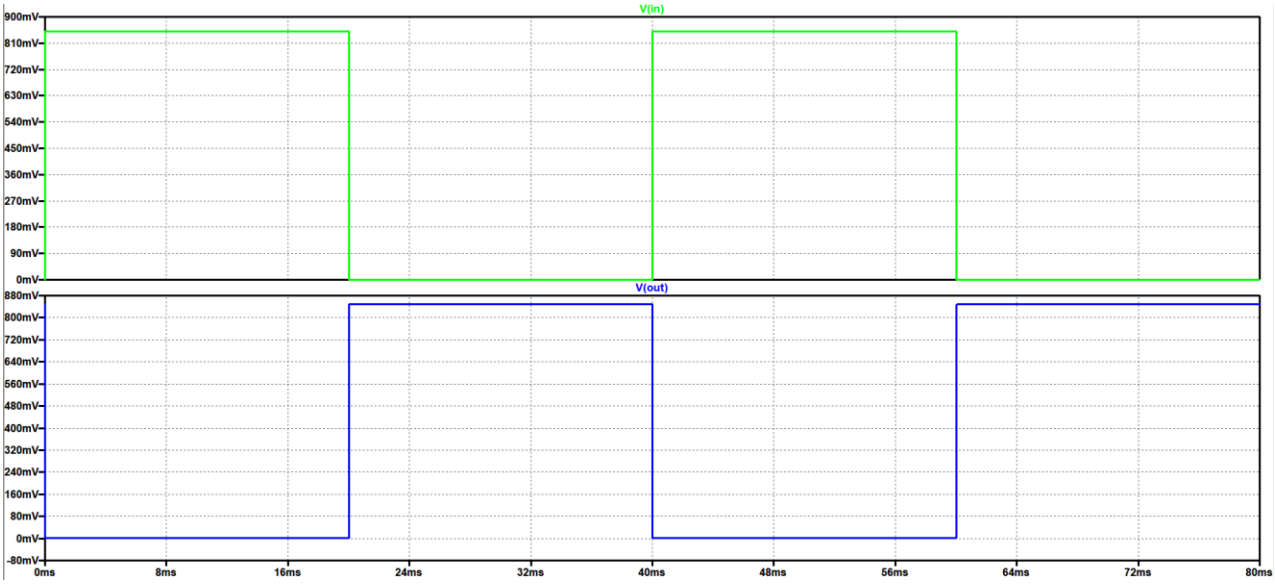
- 45nm Technology



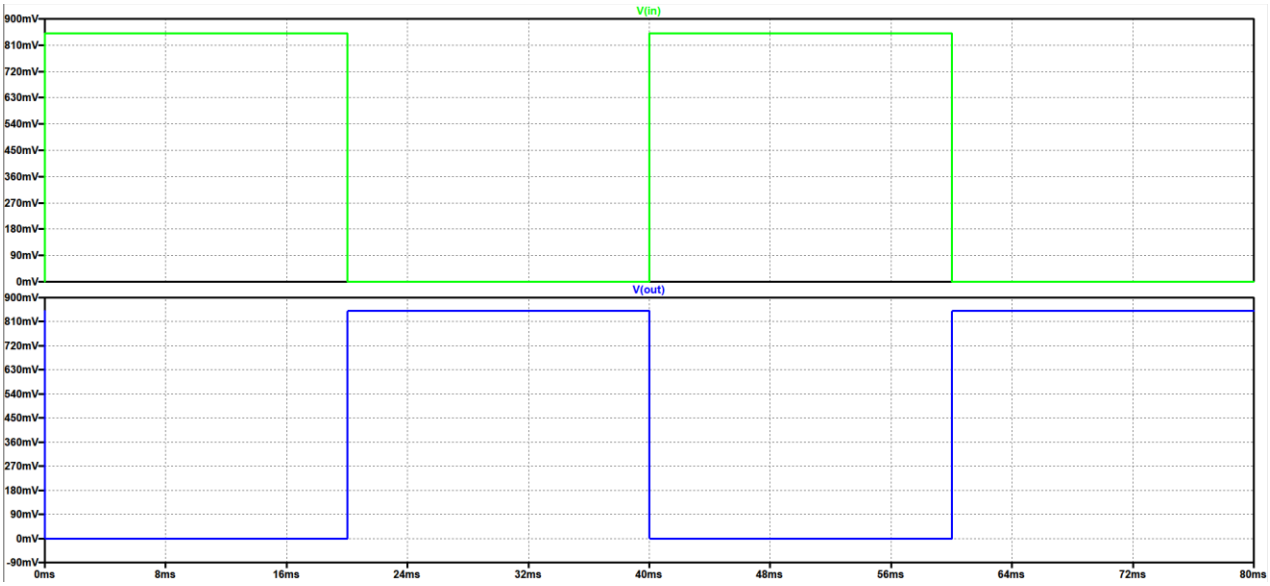
NOR

- 22nm Technology

- 32nm Technology



- 45nm Technology



Observations and Calculations:

Formulas Used:

- Output Delay= (Tlh + Thl) / 2
- Power Dissipation= Vdd * $I_{D(avg)}$

Vdd=1 V for all technologies

NAND

Technology	Tlh	Thl	Output Delay	$I_{D(avg)}$	Power Dissipation
22 nm	88.291874ns	40.120087ns	64.2059805ns	473.65nA	473.65nW
32 nm	54.649123ns	1.5113573ns	28.08024015ns	48.031nA	48.031nW
45 nm	6.2516376ns	3.65781ns	4.9547238ns	297.19pA	297.19pW

NOR

Technology	Tlh	Thl	Output Delay	$I_{D(avg)}$	Power Dissipation
22 nm	108.32566 ns	47.0145 ns	77.67008 ns	470.6nA	470.6nW
32 nm	82.2584 ns	29.9875 ns	56.12295 ns	147.96nA	147.96nW
45 nm	33.41985 ns	17.568 ns	25.493925 ns	27.047nA	27.047nW