

# Electronic Component Zero Orientation For CAD Library Construction

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# 1 INTRODUCTION

## 1.1 Scope

To establish a consistent technique for the description of electronic component orientation, and their land pattern geometries, that facilitates and encourages a common data capture and transfer methodology amongst and between global trading partners.

## 1.2 Purpose

IPC, in conjunction with the International Electrotechnical Commission (IEC), have established several standards that are in the process of being coordinated. One of the standards is on the design of land patterns geometries (IPC-7351/IEC 61188-5-1); the other set is on electronic description for data transfer between design and manufacturing (IPC-2581/IEC 61182-2). In order to maintain a consistent method where these two important standards describe the component mechanical outlines, and their respective mounting platforms, a single concept must be developed that takes into account various factors within the global community.

One of these factors is that of establishing a CAD component description and land pattern standard that adopts a fixed Zero Component Orientation so that all CAD images are built with the same rotation for the purpose of assembly machine automation.

The land pattern standards clearly define all the properties necessary for standardization and acceptability of a "One World CAD Library". The main objective in defining a one world CAD library is to achieve the highest level of "Electronic Product Development Automation". This encompasses all the processes involved from engineering to PCB layout to fabrication, assembly and test. The data format standards need this type of consistency in order to meet the efficiency that electronic data transfer can bring to the industry.

Many large firms have spent millions of dollars creating and implementing their own unique standards for their own "Electronic Product Development Automation". These standards are proprietary to each firm and are not openly shared with the rest of the industry. This has resulted in massive duplication of effort costing the industry millions of man hours in waste and creating industry chaos and global non-standardization.

The industry associations responsible for component descriptions and tape and reel orientation have tried valiantly to influence the industry by making good standards that describe the component outlines and how they should be positioned in the delivery system to the equipment on the manufacturing floor.

Suppliers of parts have either not adhered to the recommendations or have misunderstood the intent and provided their products in different orientations.

The Land pattern standards (both IPC-7351 and IEC 61188-5-1) put an end to the "Proprietary Intellectual Property" and introduce a world standard so every electronics firm can benefit from Electronic Product Development Automation. The data format standards (IPC-2581 and IEC 61182-2) are an open database XML software code that is neutral to all the various CAD ASCII formats. For true machine automation to exist, the world desperately needs a neutral CAD database format that all PCB manufacturing machines can read.

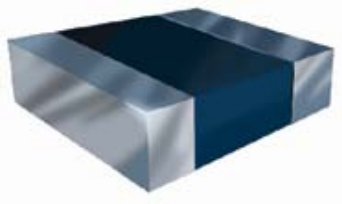
The main purpose of creating the land pattern standards is to achieve reliable solder joint formation platforms; the reason for developing the data transfer structure is to improve the efficiency with which engineering intelligence is converted to manufacturing reality. Even if the neutral CAD format can drive all the manufacturing machines, it would be meaningless unless the component description standard for CAD land patterns was implemented with some consistency. Zero Component Orientation has a key role in machine automation.

The obvious choice for global standardization for EE hardware engineering, PCB design layout, manufacturing, assembly and testing processes is to incorporate the standard land pattern conventions. Any other option continues the confusion and additional manual hours of intervention in order to achieve the goals of automation. In addition, the ease of having one system export a file so that another system can accomplish the work may require unnecessary manipulation of the neutral format in order to meet the object of clear, unambiguous software code.

The design of any assembly will continue to permit arrangement and orientation of components at any orientation consistent with design standards. Starting from a commonly understood data capture concept will benefit the entire supply chain.

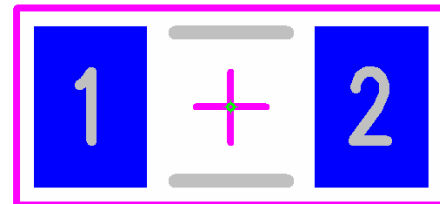
## 2 CHIP COMPONENTS

### 2.1 Chip Capacitor



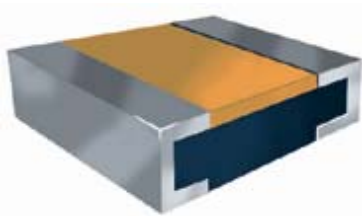
Component

Pin 1 on Left Side



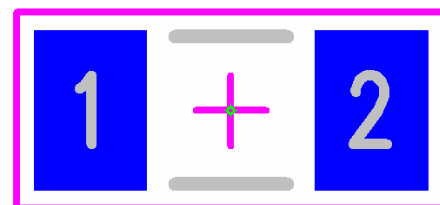
Land Pattern

### 2.2 Chip Resistor



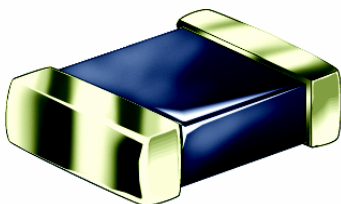
Component

Pin 1 on Left Side



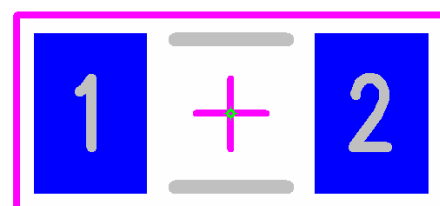
Land Pattern

### 2.3 Chip Inductor



Component

Pin 1 on Left Side



Land Pattern

Note: Pin 1 is always the “Positive” pin

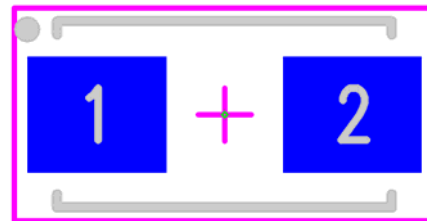
### 3 MOLDED COMPONENTS

#### 3.1 Molded Capacitors



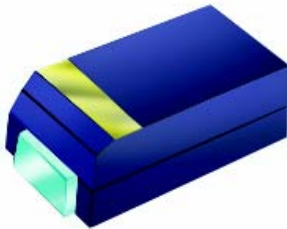
Component

Pin 1 on Left Side



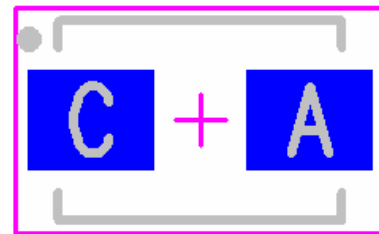
Land Pattern

#### 3.2 Molded Diodes



Component

Pin 1 on Left Side (Cathode)



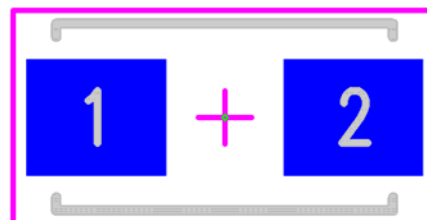
Land Pattern

#### 3.3 Molded Inductors



Component

Pin 1 on Left Side

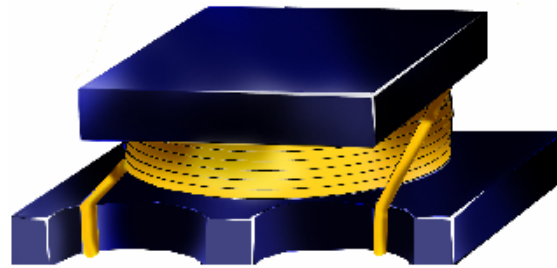


Land Pattern

Note: Pin 1 is always the “Positive” pin

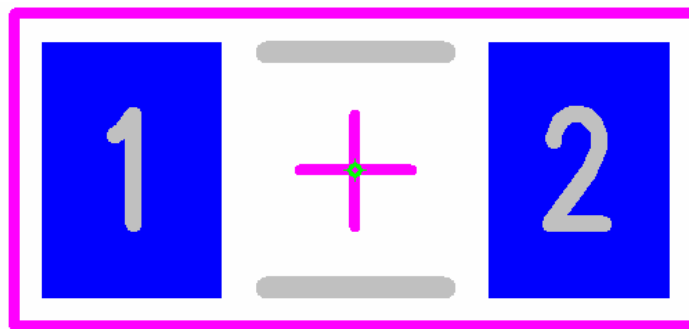
## 4 PRECISION WIRE-WOUND

### 4.1 Precision Wire Wound Components



**Component**

**Pin 1 on Left Side**



**Land Pattern**

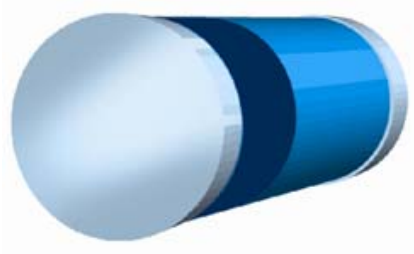
**Note: Pin 1 is always the “Positive” pin**



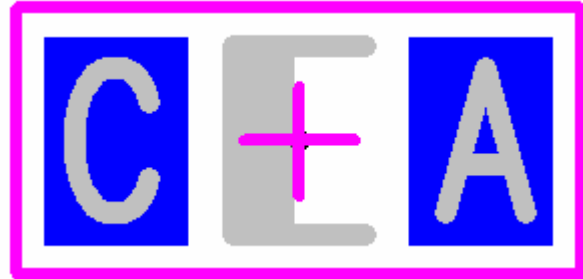
## 5 MELF COMPONENTS

### 5.1 MELF Diodes

Pin 1 on Left Side (Cathode)



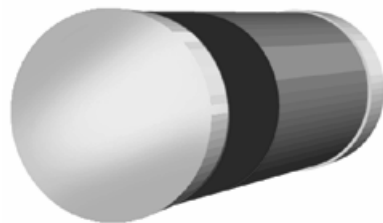
Component



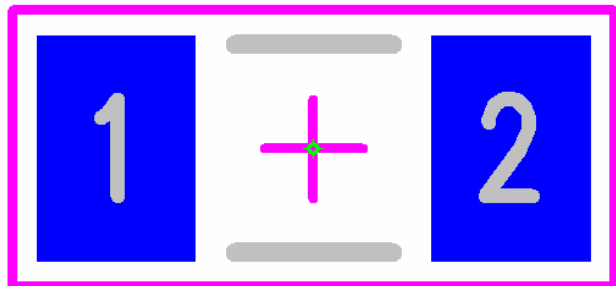
Land Pattern

### 5.2 MELF Resistors

Pin 1 on Left Side



Component

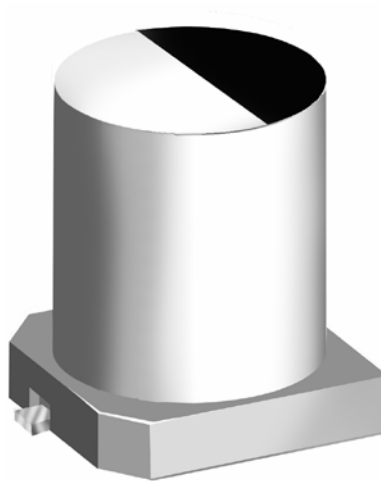


Land Pattern

**Note:** Pin 1 is always the “Polarity Mark” pin or Cathode

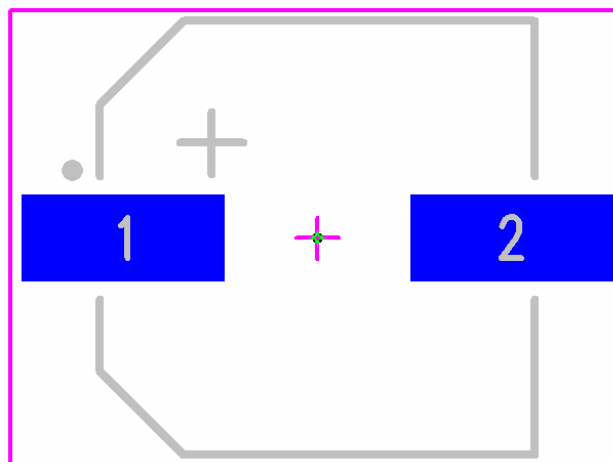
## 6 ALUMINUM ELECTROLYTIC CAPACITORS

### 6.1 Aluminum Electrolytic Capacitors



**Component**

**Pin 1 on Left Side**



**Land Pattern**

**Note: Pin 1 is always the “Positive” pin**

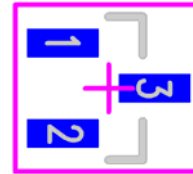
## 7 SOT COMPONENTS

### 7.1 SOT23-3



Component

Pin 1 on Upper Left



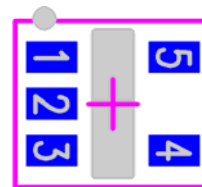
Land Pattern

### 7.2 SOT23-5



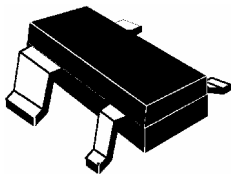
Component

Pin 1 on Upper Left



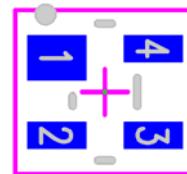
Land Pattern

### 7.3 SOT343



Component

Pin 1 on Upper Left



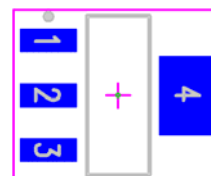
Land Pattern

### 7.4 SOT223



Component

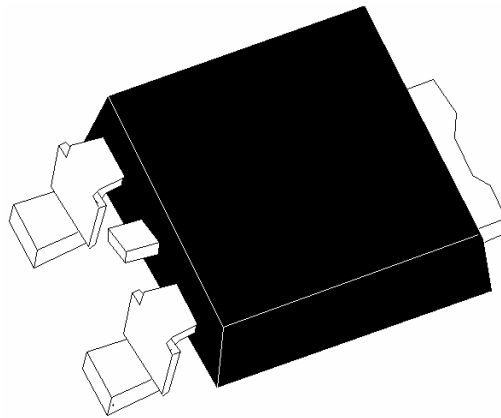
Pin 1 on Upper Left



Land Pattern

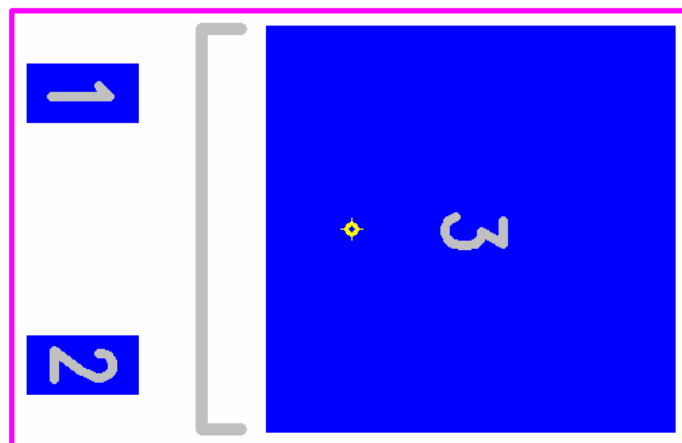
## 8 TO COMPONENTS

### 8.1 TO252 (DPAK)



**Component**

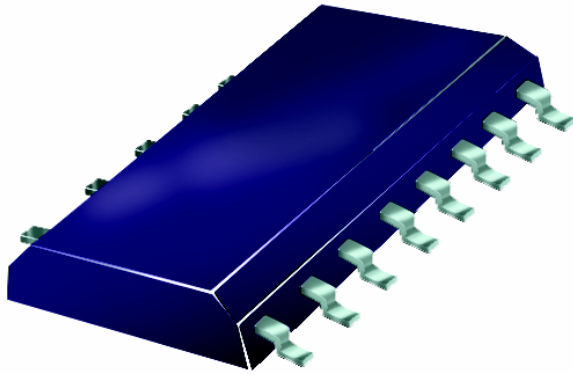
**Pin 1 on Upper Left**



**Land Pattern**

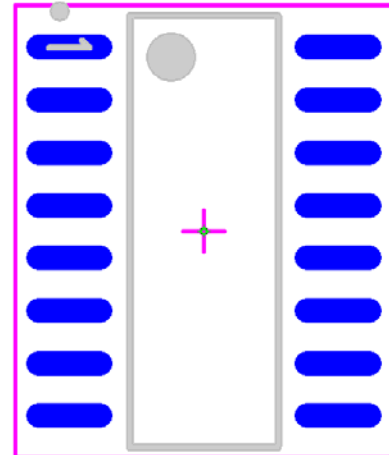
## 9 SMALL OUTLINE GULLWING COMPONENT

### 9.1 SOIC, SOP & SSOP



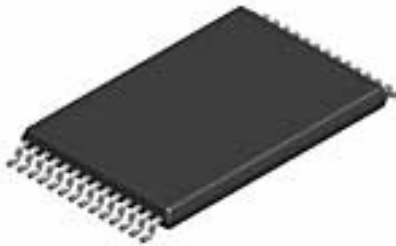
Component

Pin 1 on Upper Left



Land Pattern

### 9.2 TSSOP



Component

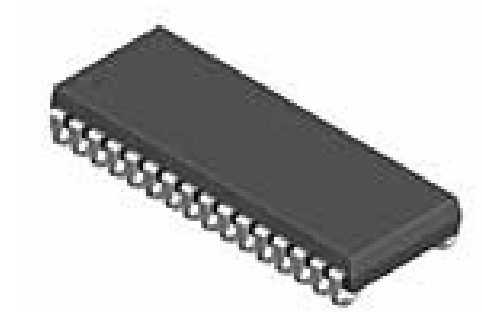
Pin 1 on Upper Left



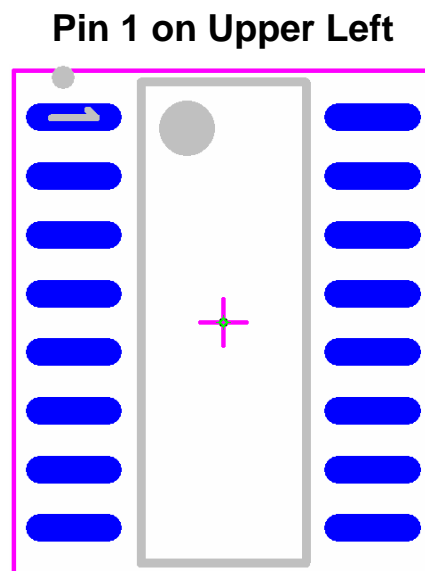
Land Pattern

## 10 SMALL OUTLINE J-LEAD COMPONENTS

### 10.1 SOIC J-Lead



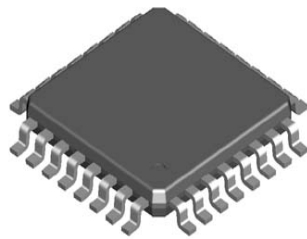
Component



Land Pattern

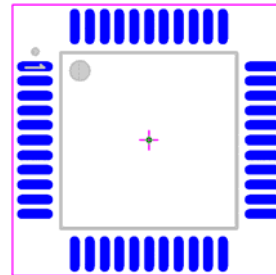
## 11 QUAD FLAT PACKAGE

### 11.1 Square QFP Pin 1 on Side



Component

Pin 1 on Upper Left



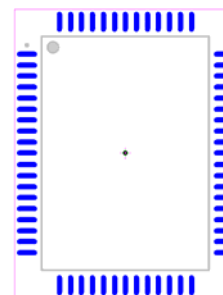
Land Pattern

### 11.2 Rectangle QFP Pin 1 on Side



Component

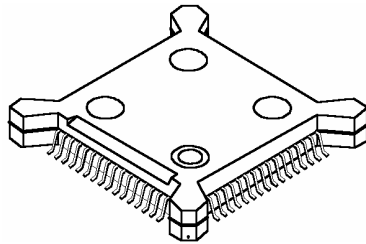
Pin 1 on Upper Left



Land Pattern

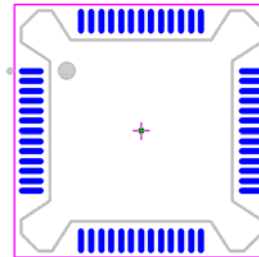
## 12 BUMPER QUAD FLAT PACKAGE

### 12.1 Bump QFP Pin 1 on Side



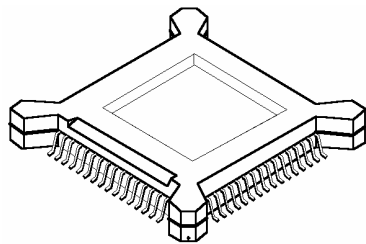
Component

Pin 1 on Upper Left



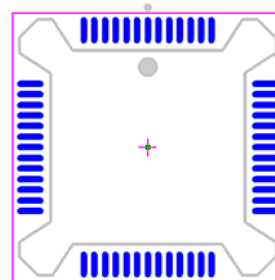
Land Pattern

### 12.2 Bump QFP Pin 1 in Center



Component

Pin 1 on Top Center

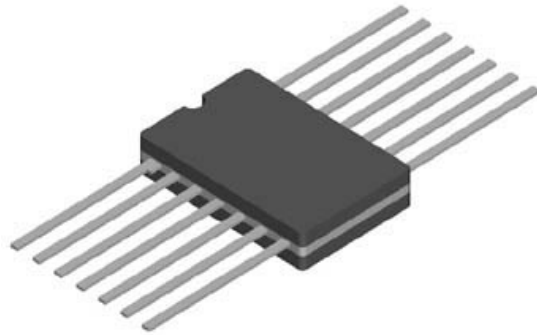


Land Pattern



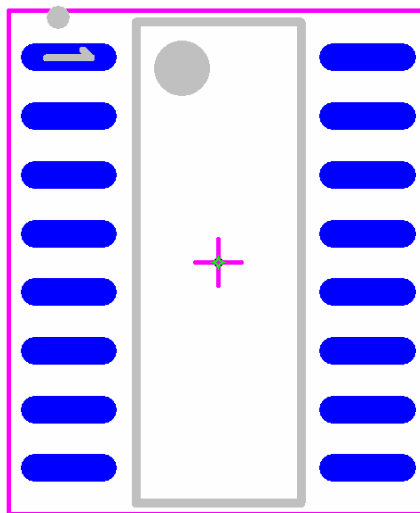
## 13 CERAMIC FLAT PACKAGE

### 13.1 Ceramic Flat Package



**Component**

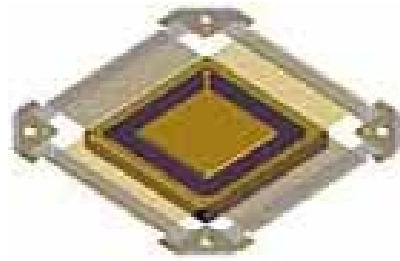
**Pin 1 on Upper Left**



**Land Pattern**

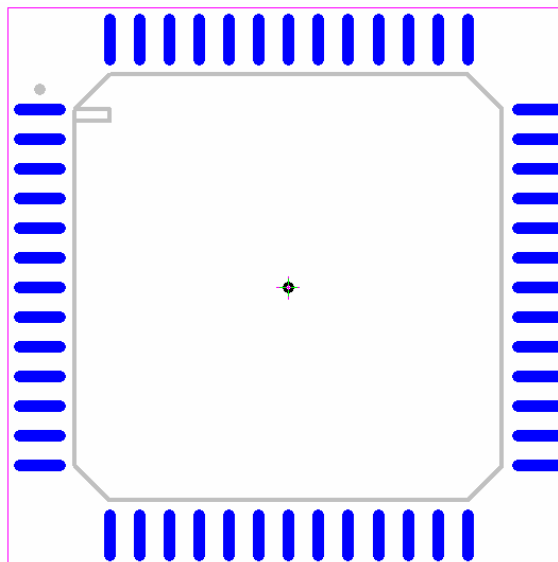
## 14 CERAMIC QUAD FLAT PACKAGE

### 14.1 CQFP (Ceramic Quad Flat Package)



Component

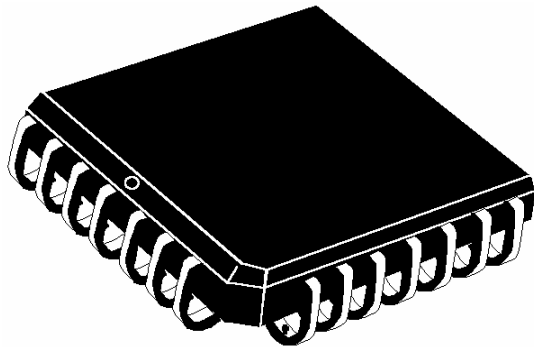
Pin 1 on Upper Left



Land Pattern

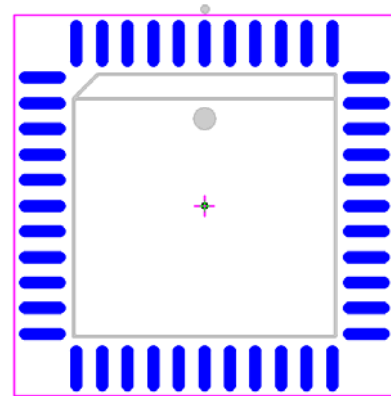
## 15 PLASTIC LEADED CHIP CARRIERS

### 15.1 PLCC Square



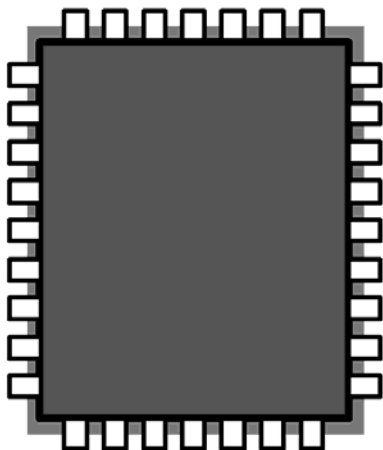
Component

Pin 1 on Top Center



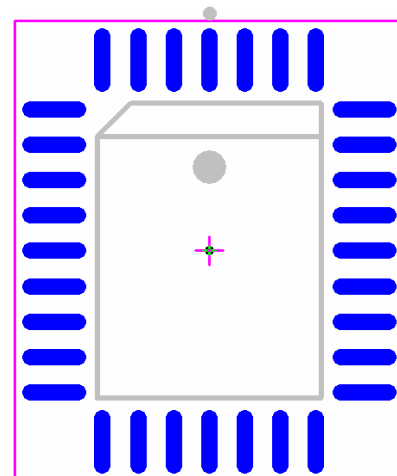
Land Pattern

### 15.2 PLCC Rectangular



Component

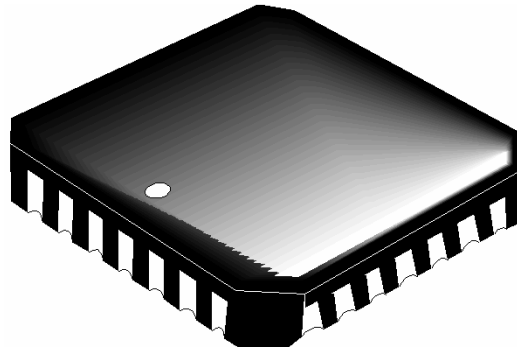
Pin 1 on Top Center



Land Pattern

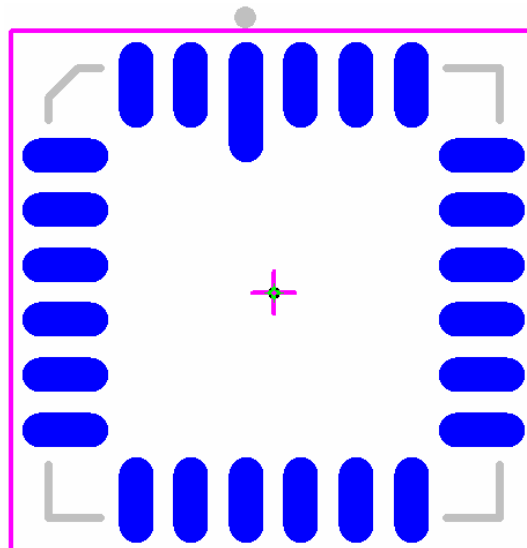
## 16 LEADLESS CHIP CARRIERS

### 16.1 LCC Square



Component

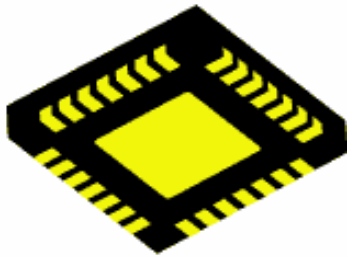
Pin 1 on Top Center



Land Pattern

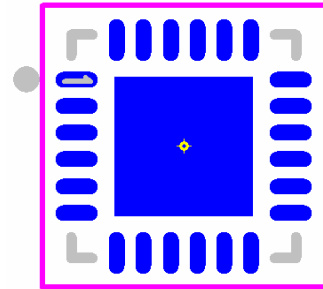
## 17 QUAD FLAT NO-LEAD

### 17.1 QFN Square



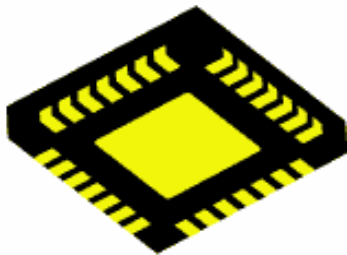
Component (Bottom View)

Pin 1 on Upper Left



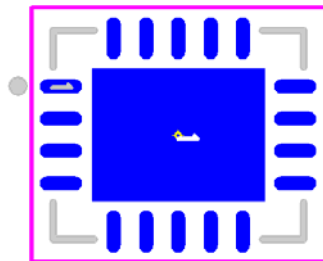
Land Pattern

### 17.2 QFN Rectangular Vertical



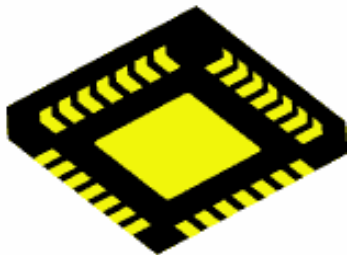
Component (Bottom View)

Pin 1 on Upper Left



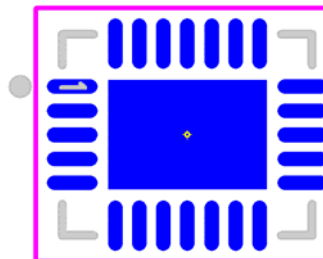
Land Pattern

### 17.3 QFN Rectangular Horizontal



Component (Bottom View)

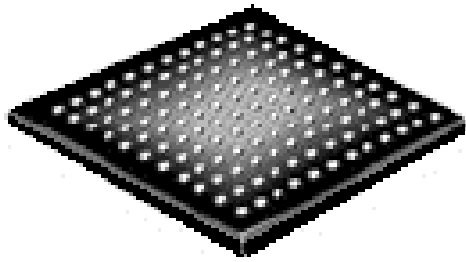
Pin 1 on Upper Left



Land Pattern

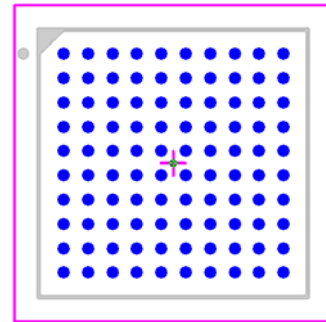
## 18 BALL GRID ARRAY

### 18.1 BGA Square



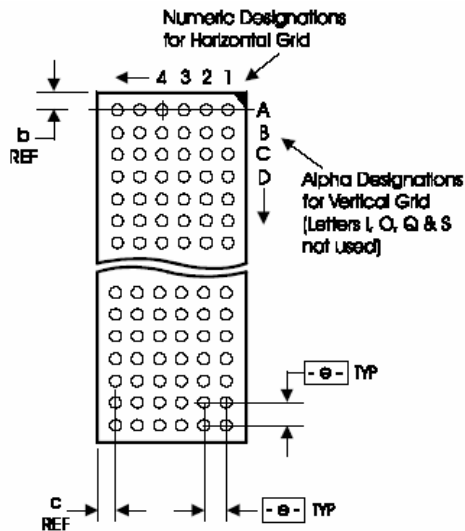
Component (Bottom View)

Pin A1 in Upper Left



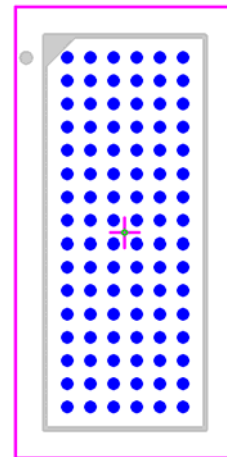
Land Pattern

### 18.2 BGA Rectangular



Component (Bottom View)

Pin A1 in Upper Left



Land Pattern

# 19 COMPONENT ZERO ORIENTATIONS

## 19.1 Summary

### Surface Mount Land Patterns

#### IPC-735\* Component Family Breakdown:

**IPC-7351** = IEC 61188-5-1, Generic requirements - land/joint considerations – [General Description](#)

**IPC-7352** = IEC 61188-5-2, Sectional requirements - land/joint considerations – [Discrete Components](#)

**IPC-7353** = IEC 61188-5-3, Sectional requirements - land/joint considerations – [Gull-wing leads, two sides \(SOP\)](#)

**IPC-7354** = IEC 61188-5-4, Sectional requirements - land/joint considerations – [J leads, two sides \(SOJ\)](#)

**IPC-7355** = IEC 61188-5-5, Sectional requirements - land/joint considerations – [Gull-wing leads, four sides \(QFP\)](#)

**IPC-7356** = IEC 61188-5-6, Sectional requirements - land/joint considerations – [J leads, four sides \(PLCC\)](#)

**IPC-7357** = IEC 61188-5-7, Sectional requirements - land/joint considerations – [Post leads, two sides \(DIP\)](#)

**IPC-7358** = IEC 61188-5-8, Sectional requirements - land/joint considerations – [Area Array Components \(BGA\)](#)

**IPC-7359** = NO IEC Document, Sectional requirements - land/joint considerations – [No Lead Components \(LCC\)](#)

#### Component Zero Orientations Pin 1 Location For CAD Library Construction

- 1) Chip Capacitors, Resistors and Inductors (RES, CAP and IND) – [Pin 1 \(Positive Pin\) on Left](#)
- 2) Molded Inductors (INDM), Resistors (RESM) and Tantalum Capacitors (CAPT) – [Pin 1 \(Positive Pin\) on Left](#)
- 3) Precision Wire-wound Inductors (INDP) – [Pin 1 \(Positive Pin\) on Left](#)
- 4) MELF Diodes – [Pin 1 \(Cathode\) on Left](#)
- 5) Aluminum Electrolytic Capacitors (CAPAE) – [Pin 1 \(Positive\) on Left](#)
- 6) SOT Devices (SOT23, SOT23-5, SOT223, SOT89, SOT143, etc.) – [Pin 1 Upper Left](#)
- 7) TO252 & TO263 (DPAK Type) Devices – [Pin 1 Upper Left](#)
- 8) Small Outline Gullwing ICs (SOIC, SOP, TSOP, SSOP, TSSOP) – [Pin 1 Upper Left](#)
- 9) Ceramic Flat Packs (CFP) – [Pin 1 Upper Left](#)
- 10) Small Outline J Lead ICs (SOJ) – [Pin 1 Upper Left](#)
- 11) Quad Flat Pack ICs (PQFP, SQFP) – [Pin 1 Upper Left](#)
- 12) Ceramic Quad Flat Packs (CQFP) – [Pin 1 Upper Left](#)
- 13) Bumper Quad Flat Pack ICs (BQFP Pin 1 Center) – [Pin 1 Top Center](#)
- 14) Plastic Leaded Chip Carriers (PLCC) – [Pin 1 Top Center](#)
- 15) Leadless Chip Carriers (LCC) – [Pin 1 Top Center](#)
- 16) Leadless Chip Carriers (LCCS Pin 1 on Side) – [Pin 1 Upper Left](#)
- 17) Quad Flat No-Lead ICs (QFN) QFNS, QFN RV, QFN RH – [Pin 1 Upper Left](#)
- 18) Ball Grid Arrays (BGA) – [Pin A1 Upper Left](#)