GATE PROGRESS TRACKER

CHAPTERS	REV 1	REV 2	REV 3	REV 4	DPP 1	DPP 2	PYQ`s 1	PYQ`s 2	MOCK 1	MOCK 2	
COMPUTER NETWORKS											
IPV4 Addressing											
Error Control											
Flow Control											
IPV4 Header & Fragmentation											
TCP & UDP											
Medium Access Control											
Routing Protocols											
Switching											
Application Layer Protocols											
IP Support protocol											
OPERATING SYSTEMS											
Introduction & Background			.,	0 0 1 0					<u> </u>		
Process Management											
CPU Scheduling											
Process Synchronization											
DeadLock											
Memory Management											
File System & Device											
Management System Calls & Threads											
System cans a fineaus		C - F	PROGI	RAMN	/ING						
Data Types & Operators											
Control Flow Statements											
Functions & Storage Classes											
Arrays & Pointers											
Strings											
Structures & Union Miscellaneous											
Miscellaneous		ראם	TA STF	PLICTI	IDEC						
Introduction		DAI	ASII	NOC TO	JNLS		l		Ī		
Arrays											
Linked List											
Stack & Queues											
Trees											
Graphs											
Hashing											
DIGITAL LOGIC											
Logic Gates											
Minimization											
Combinational Circuit											
Sequential Circuit Number System											
Number System					<u> </u>]]	l	<u> </u>	<u> </u>	

CHAPTERS	REV 1	REV 2	REV 3	REV 4	DPP 1	DPP 2	PYQ`S 1	PYQ`S 2	MOCK 1	MOCK 2	
THEORY OF COMPUTATION											
Finite Automata											
Push Down Automata											
Turning Machine Recursively											
Enumerable											
Decidability											
COMPILER DESIGN											
Lexical & Syntax Analysis											
Syntax Directed Translation											
Intermediate Code & Code											
Optimization											
ALGORITHMS											
Analysis Of Algorithms											
Design Strategies											
Greedy Method											
Dynamic Programming											
Graph Algorithms											
Heap Algorithms											
Backtracking & Branch -											
Bound											
	DATAC	BASE	MANA	AGEM	ENT S	YSTEN	1				
FD's and Normalisation											
Transaction and Concurrency											
Control											
ER Model											
Query Language											
File Organisation & Indexing											
COMP	UTER	ORG	ANISA	TION	& AR	CHITE	CTURE				
Introduction Of COA											
Machine Instruction and											
Addressing Modes											
Floating Point Representation											
ALU and Control Unit											
Instruction And Pipelining											
Cache Memory											
Secondary Memory & IO											
Interface					=						
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Graph Theory											
Mathematical Logic											
Set Theory											
Combinatorics				• • • •							
ENGINEERING MATHEMATICS											
Linear Algebra											
Calculus											
Probability & Statistics											