

ELECTRICAL ENGG. DEPARTMENT

CLASS: IV-Sem. (Electrical)

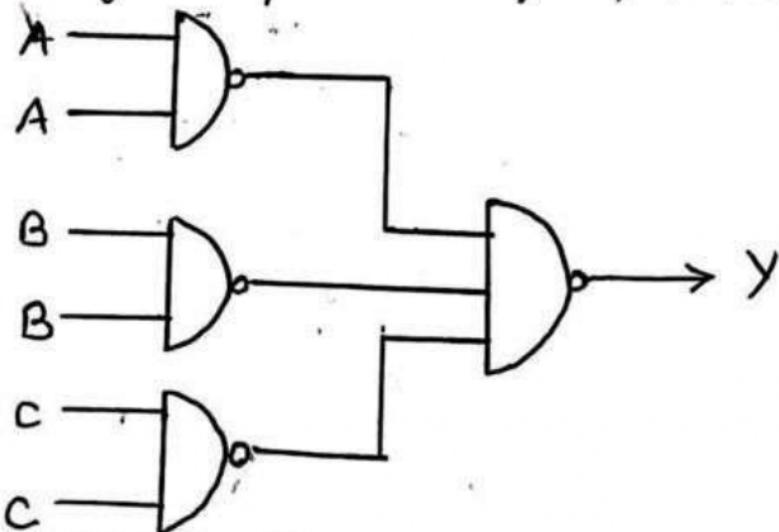
COURSE: Analysis & Design of Digital Logic Circuits

ASSIGNMENT NO-1

Q.N.

PROBLEM

1. Draw the truth table of a 2-input EX-NOR gate and hence derive the logic circuit of it using minimum number of fundamental logic gates.
2. Draw the basic circuit of a 3-input NOR gate using semiconductor diodes & bijunction transistors and explain its working principle using the truth table.
3. Design a Full Adder circuit using minimum number of Half-Adders and additional logic ~~gates~~ gates (if required). Draw the truth table of H.A. and F.A. also.
4. Draw the truth-table of the following logic circuit and analyse the same for the type of the logic operation performed by it.



Q.N.

## PROBLEM

5. Design a  $3 \times 8$  decoder using enable (E) using fundamental logic gates and draw its truth-table. Hence, design a  $4 \times 16$  decoder using  $3 \times 8$  decoder modules.
6. Design an Encoder with 6 inputs ( $X_1$  to  $X_6$ ) and 4 outputs ( $Y_1$  to  $Y_4$ ) as per the following truth-table.
- | $X_6$ | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | $Y_4$ | $Y_3$ | $Y_2$ | $Y_1$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 0     | 1     |
| 0     | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 1     | 1     |
| 0     | 0     | 0     | 1     | 0     | 0     | 1     | 1     | 1     | 1     |
| 0     | 0     | 1     | 0     | 0     | 0     | 0     | 0     | 1     | 0     |
| 0     | 1     | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 1     |
| 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
7. Design a  $8 \times 1$  MUX circuit with enable signal and explain its operation using the complete truth table.  
Design the same  $8 \times 1$  MUX using lower-size MUX (modules).
8. Design a Full-Adder circuit using minimum number of appropriate (optimal) size Multiplexer Modules.
9. Design a Full-Adder circuit using optimal size Decoder/s and additional logic gates (if required).
10. Can a 4-bit Binary Parallel Adder/Subtractor be used as a magnitude comparator to compare two 4-bit numbers? If yes, how? Explain.

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## TUTORIAL SHEET - I

Q. No.	PROBLEM SPECIFICATIONS
1.	<p>Obtain the simplified expressions in SOP form for the following Boolean functions and hence design the corresponding Logic circuit in its most optimal form.</p> <p>(i) <math>F(A, B, C) = \sum(2, 3, 6, 7)</math>  (ii) <math>F(A, B, C, D) = \sum(2, 3, 12, 13, 14, 15)</math></p>
2.	<p>Obtain the Simplified expression in SOP form for the following Boolean functions.</p> <p>(i) <math>Y = \bar{A} \cdot B + B \cdot \bar{C} + \bar{A} \cdot \bar{B} + \bar{B} \cdot \bar{C}</math>  (ii) <math>Y = A \cdot B + \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C}</math></p>
3.	<p>Obtain the most simplified expression using POS method and the Logic circuit for the following functions.</p> <p>(i) <math>F(A, B, C) = \pi(0, 1, 4, 5)</math>  (ii) <math>F(A, B, C, D) = \pi(0, 1, 2, 3, 10, 11)</math></p>
4.	<p>Design a full Adder using minimum number of Half Adders and additional Logic Gates, if required.</p>
5.	<p>Design a Logic circuit which produces on output <math>Y = X^3 + X^2 + X + 1</math> where X is a 2-bit input given by <math>X = X_2 X_1</math>.</p>
6.	<p>Design a logic circuit which receives a decimal digit in its binary form and produces an output which is the 9's complement of the input Decimal digit.</p>



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### TUTORIAL SHEET- I

- | Q. No. | PROBLEM SPECIFICATIONS                                                                                                                                                                                                                                                             |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.     | Obtain the simplified expressions in SOP form for the following Boolean functions and hence design the corresponding Logic circuit in its most optimal form.<br><br>(i) $F(A, B, C) = \sum(2, 3, 6, 7)$<br>(ii) $F(A, B, C, D) = \sum(2, 3, 12, 13, 14, 15)$                       |
| 2.     | Obtain the Simplified expression in SOP form for the following Boolean functions.<br><br>(i) $Y = \bar{A} \cdot B + B \cdot \bar{C} + \bar{A} \cdot \bar{B} + \bar{B} \cdot \bar{C}$<br>(ii) $Y = A \cdot B + \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C}$ |
| 3.     | Obtain the most simplified expression using POS method and the Logic circuit for the following functions.<br><br>(i) $F(A, B, C) = \pi(0, 1, 4, 5)$<br>(ii) $F(A, B, C, D) = \pi(0, 1, 2, 3, 10, 11)$                                                                              |
| 4.     | Design a full Adder using minimum number of Half Adders and additional Logic Gates, if required.                                                                                                                                                                                   |
| 5.     | Design a Logic circuit which produces on output $Y = X^3 + X^2 + X + 1$ where $X$ is a 2-bit input given by $X = X_2 X_1$ .                                                                                                                                                        |
| 6.     | Design a logic circuit which receives a decimal digit in its binary form and produces an output which is the 9's complement of the input Decimal digit.                                                                                                                            |

1. Draw the logic circuit of a 3- input NAND Gate using minimum number of semiconductor components (Diodes / Transistors ) and explain its operation.
8. Design a 2- input EX - NOR Gate using minimum number of NAND Gates only.
9. Implement the following Boolean Expression using a MUX .  
$$Y = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + ABCD + \bar{A} \cdot B \cdot C \cdot D$$
10. Implement the Boolean function given above in Q. 9 by using two  $3 \times 8$  Decoders.
11. Design a  $16 \times 1$  MUX using minimum number of multiplexers of (  $4 \times 1$  ) size.
12. Design a 5 – input EX – OR Gate using 2 – input EX- OR Gates.

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**TUTORIAL SHEET- II**

Q. No.	PROBLEM SPECIFICATIONS
1.	Implement the following function with a multiplexer.  $F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 14, 15)$
2.	A combinational circuit is defined by the following two functions. $F_1(A, B, C) = \sum (0, 3, 6, 7)$ $F_2(A, B, C) = \sum (1, 2, 5, 7)$ Implement the Logic circuit by means of minimum number of Decoders and external logic gates, if required.
3.	Draw the Logic circuit of a 3- bit controlled Shift Right Register and by using timing waveforms briefly explain its operation
4.	Design the Logic circuit of a $8 \times 4$ ROM built around bipolar transistors which can store the following binary words : 1000, 0001, 1010, 0101, 1111, 0111, 1101 and 0110. Use decoder for Addressing and briefly explain the operation of the circuit.
5.	Design the Logic circuit of a Memory cell using J – K flip flop and explain how a binary digit can be read or written into the cell. Use a single bit read / write control in the form of $\bar{R} / W$ .
6.	Design a $32 \times 8$ RAM system using $8 \times 4$ RAM chips and explain its operation. Draw the complete memory Map of the system.
7.	Design a MOD – 6 synchronous ‘ UP ’ counter using J – K flip - flops and explain its working principle. Draw the Timing diagrams for the first 8 clock pulses.
8.	Draw the Logic circuit of a presettable ‘DOWN’ counter which can count from 110 to 000 and explain the operation of the counter. Draw the Timing wave forms.

9.

Draw the Logic circuit of a 2 – input TTL NOR Gate and explain its operation. Draw the complete operation Table of this circuit.

10.

Design a sequential Logic circuit for the counter with the following binary sequence. 0, 1, 5, 6, 7, 4 and repeat. Use J – K flops for the circuit design.

11.

Design a 3 – bit Gray code counter using T – flip flops.

12.

Design a 4 – bit UP counter using D – flip flops.

13.

A sequential circuit has two flip flops ( A and B ), two – inputs ( x and y ) and an output ( z ). The flip – flop functions and the circuit output functions are as follows:

$$J_A = x \cdot B + \bar{y} \cdot \bar{B}$$

$$K_A = x \cdot \bar{y} \cdot \bar{B}$$

$$J_B = x \cdot \bar{A}$$

$$K_B = x \cdot \bar{y} \cdot + A$$

$$Z = x \cdot y \cdot A + \bar{x} \cdot \bar{y} \cdot B$$

Obtain the Logic diagram, state – Table, state Diagram, and the state Equations.

14.

Draw the complete Logic diagram (circuit ) of a  $4 \times 3$  binary array multiplier.

15.

Design a 4 – input CMOS NAND Gate and explain its operation. Draw the complete Truth – Table. Compare the CMOS Logic with TTL and ECL in terms of its various performance parameters.

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