

KAPILAN BALAGOPALAN

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INTRODUCTION

My research focuses on sequential decision-making—including bandit algorithms, partial monitoring games, and reinforcement learning—with applications in fine-tuning and improving large language models and recommender systems. I have a strong foundation in theoretical machine learning and foundational models, complemented by hands-on experience in embedded C, C++, Python, Java, MATLAB, and API-level development for foundation models.

EDUCATION

University of Arizona, USA

PhD in Computer Science
Current GPA: 3.67/4.0

Aug 2022 - present

University of Moratuwa, Sri Lanka

B.S.(Hons) in Engineering
Department Electronic and Telecommunication Engineering
Overall GPA: 3.81/4.2

Feb 2014 - Jan 2018

JOURNALS & CONFERENCES

- AppleTeA: Test-Time Adaptive LLM Cascading via Logistic Apple Tasting. Hyowon Wi, Kapilan Balagopalan, Kwang-Sung Jun, Noseong Park. Second Workshop on Test-Time Adaptation: Putting Updates to the Test! at ICML 2025.
- Minimum Empirical Divergence for Sub-Gaussian Linear Bandits. Kapilan Balagopalan, Kwang-Sung Jun. AISTATS'25: International Conference on Artificial Intelligence and Statistics. 2025.
- Fixing the Loose Brake: Exponential Tail Bounds for Stopping Time in Best Arm Identification. (co 1st author: †) Kapilan Balagopalan†, Tuan Nguyen†, Yao Zhao†, Kwang-Sung Jun. ICML'25: International Conference on Machine Learning. 2025.
- Wang, G., Kapilan, B., Razul, S.G. et al. Blind Equalization in the Presence of Co-channel Interference Based on Higher-Order Statistics. Circuits Syst Signal Process 37, 4150–4161 (2018). doi: 10.1007/s00034-017-0744-x

PROFESSIONAL EXPERIENCE

Amazon AWS

Applied Scientist Intern

May 2025 - August 2025

Amazon, New York

Campaign intent detection using large language models and using the intents to recommend key-words for advertisers to create optimal campaigns.

Thales Digital Identity & Security

Embedded Software Engineer

May 2020 - May 2022

Thales DIS, Singapore

Development of Smart card OS for Telco, Secure Element, Transport and Banking applications to be deployed on micro controller chips.

London Stock Exchange Group

Hardware Acceleration Engineer

Feb 2018 - Feb 2020

LSEG Technology, Sri Lanka

Acceleration of time critical modules in exchange and trading platforms using FPGAs.

Temasek Laboratory, Nanyang Technological University

Research Assistant

Aug 2016 - Dec 2016

NTU, Singapore

Blind channel equalization of OQPSK signals under strong co-channel interference using higher order statistics.

TEACHING & VOLUNTEERING ROLES

- Reviewer
 - Second Workshop on Test-Time Adaptation: Putting Updates to the Test! at ICML 2025
- Teaching Assistant
 - Spring 2025: CSC 445 Algorithms