Hardware Design of Booth Multiplier Circuit with Built – in Self – Test Feature

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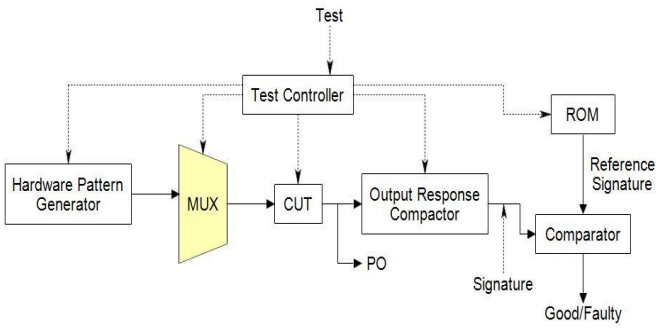
Abstract-**Very Large-Scale Integration (VLSI) has made a dramatic impact on the growth of integrated circuit technology. It has not only reduced the size and the cost but also increased the complexity of the circuits. The positive improvements have resulted in significant performance/cost advantages in VLSI systems. There are, however, potential problems which may retard the effective use and growth of future VLSI technology. Among these is the problem of circuit testing, which becomes increasingly difficult as the scale of integration grows. Because of the high device counts and limited input/output access that characterize VLSI circuits, conventional testing approaches are often ineffective and insufficient for VLSI circuits. Built-in self-test (BIST) is a commonly used design technique that allows a circuit to test itself. BIST has gained popularity as an effective solution over circuit test cost, test quality and test reuse problems. In this paper we are presenting implementation of BIST on Booth's Multiplier.**

***Index Terms*—BIST, CUT;**

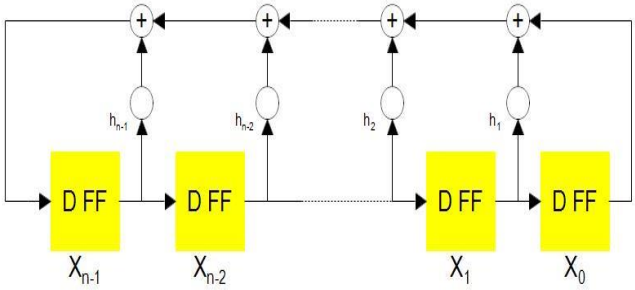
I. INTRODUCTION

Built-in Self-Test (or BIST) is a DFT technique in which testing is accomplished through built in hardware. The basic idea is to have a VLSI chip that tests itself. BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT). The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyser, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyser is a comparator with stored responses or an LFSR used as a signature analyser. It compacts and analyses the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyse the responses. However, in general, several test-related functions can be executed through a test controller circuit.



II-(A) LFSR: LINEAR FEEDBACK SHIFT REGISTER

The LFSR is just a register formed from standard flip-flops, with the outputs of selected flip-flops being fed back to the shift register's inputs. When used as a test generation, an LFSR is about to cycle rapidly through an outsized number of its states. These states, whose choice and order depend upon the planning parameters of the LFSR, define the test patterns. during this mode of operation, an LFSR is seen as a source of (pseudo) random tests that are, in theory, applicable to any fault and circuit types. There are n flip-flops (X_{n-1}……X_0) and this is called n-stage LFSR. It can be a near-exhaustive test pattern generator as it cycles through 2n-1 states excluding the zero state.



Standard LFSR Model

II-(B) OUTPUT RESPONSE COMPACTOR

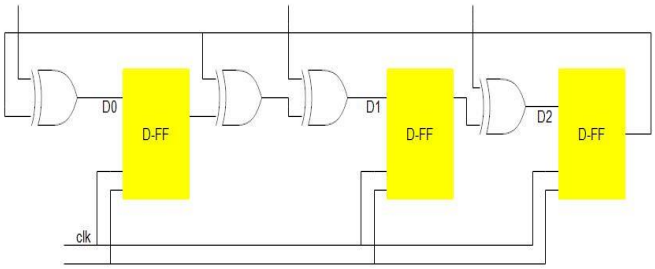
There is huge amount of data involved in CUT response. It is uneconomical to store all these responses on the chip and compare during the BIST operation, therefore it is mandatory to compact responses before compaction. Large volume of response is compacted into a signature before comparison. The signature is stored on the chip. There are two approaches available.

1. In first approach we compact a single serial bit stream into a LFSR based compactor, called signature analyser.
2. In the second approach several bit streams are compacted into a special LFSR based compactor called multi-input signature register (MISR).

II-(C) MISR: MULTIPLE-INPUT SIGNATURE REGISTER

A serial-input signature register can only be used to test logic with a single output. The idea of a serial input signature register can be extended to multiple-input signature register (MISR). There are several ways to connect the inputs of LFSRs to form an MISR. Since the XOR operation is linear and associative, (A XOR B) XOR C = A XOR (B XOR C), if the result of the additions is the same then the different representations are equivalent. If we have an n -bit long MISR we can

accommodate up to n inputs to form the signature. If we use m < n inputs, we do not need the extra XOR gates in the last n – m positions of the MISR. MISR reduce the amount of hardware required to compress a multiple bit stream. MISR circuit is implemented using a memory already existing in a circuit to be tested.



MISR Model

II-(D) CUT: Circuit Under Test

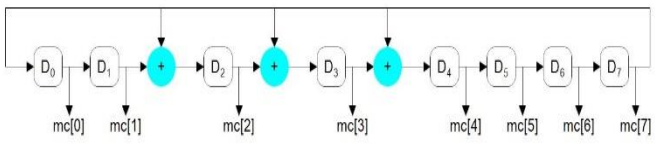
Circuit under test is a 4-bit Booth's Multiplier circuit. It is a very fast multiplication algorithm also capable of signed number multiplication. The Booth's algorithm the state machine used is described in the later sections. Higher bit Booth's Multiplier can also be used, but to keep the testing simple, 4-bit Booth's Multiplier is used.

II-(E) LFSR and MISR used in the design

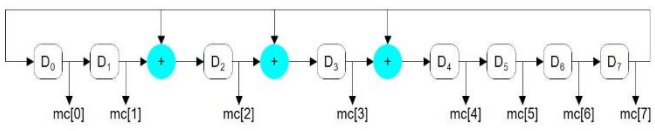
4-bit Booth's Multiplier has two inputs of 4-bit each. Hence a an LFSR capable of generating at least 8-bit pattern is required. The output of 4-bit Booth's Multiplier is 8-bits, so there are 8 output patterns. So, at least 8-bit MISR is required for compaction. An 8-bit internal XOR (type 2/ modular) LFSR and MISR of same characteristic polynomial is used in the design.

Characteristic Polynomial: $x^8 + x^4 + x^3 + x^2 + 1$

This is a primitive polynomial. It can generate all patterns from 1 to 2n-1 exhibited by an 8-bit register except zero. Moreover, the Golden Section will be more unique when using a primitive polynomial MISR as compactor and probability of aliasing will also be minimal.



LFSR output pattern into *mc* (multiplicand) and *mp* (multiplier) of multiplier



prod output of multiplier into MISR compactor

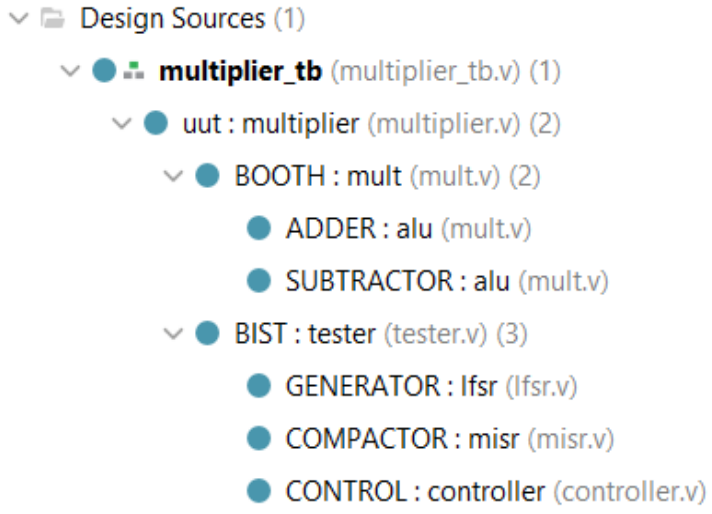
III. Software Environment

The complete project is done in Xilinx Vivado 2018.3 Software Environment using Verilog as HDL. The various tools used include the text editor, Vivado Simulator, Synthesis and RTL Analysis. It is recommended to use the same software for evaluation purposes.

IV. The Design

Source code of the design is provided in the Appendix A. The top module consists of two sub modules, *mult* and *tester*.

1. When operating the multiplier in normal mode, the *tester* circuit is completely removed from the picture using multiplexers. Clock Gating technique is used when tester is not used to decrease the dynamic power.
2. When test mode is set, the I/O ports of multiplier is completely disconnected from user's control, and the tester gets invoked to control the multiplier and begin testing.



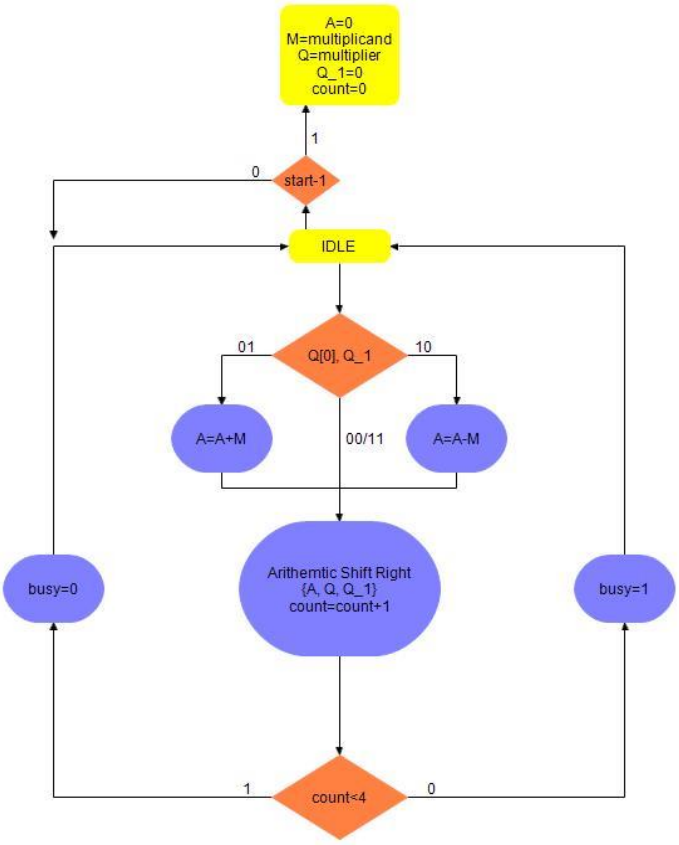
Design Hierarchy

The whole circuit operates on two controllers, Booth's Algorithm Controller and BIST Controller. Hence there are two different state machines. In test mode, both the controller functions together by virtue of a Handshaking Protocol using various control signals between them.

V-(A) Booth's Algorithm for Multiplier Circuit

1. Initially the multiplier is in undefined state. On *start* = *1*, the multiplier resets *A*, *Q_1* and *count* to zero.
2. Next state is Idle, now the *start* signal needs to be zero otherwise it will again move to reset state and ask for parameter's multiplier and multiplicand again.
3. Check for *{Q[0], Q_1}*. If *{0,1}* move to step 4, if {1,0} move to step 5, else skip to step 6.
4. Assign $A = A + M$. Move to step 6 or Assign $A = A - M$. Move to step 6.
5. Arithmetic Shift Right, the triplet *{A, Q, Q_1}*. Decrement *count*.

6. Check for *count* < 4, if true set *busy=0* otherwise set *busy=1*. Move to Idle state and continue to step 3.

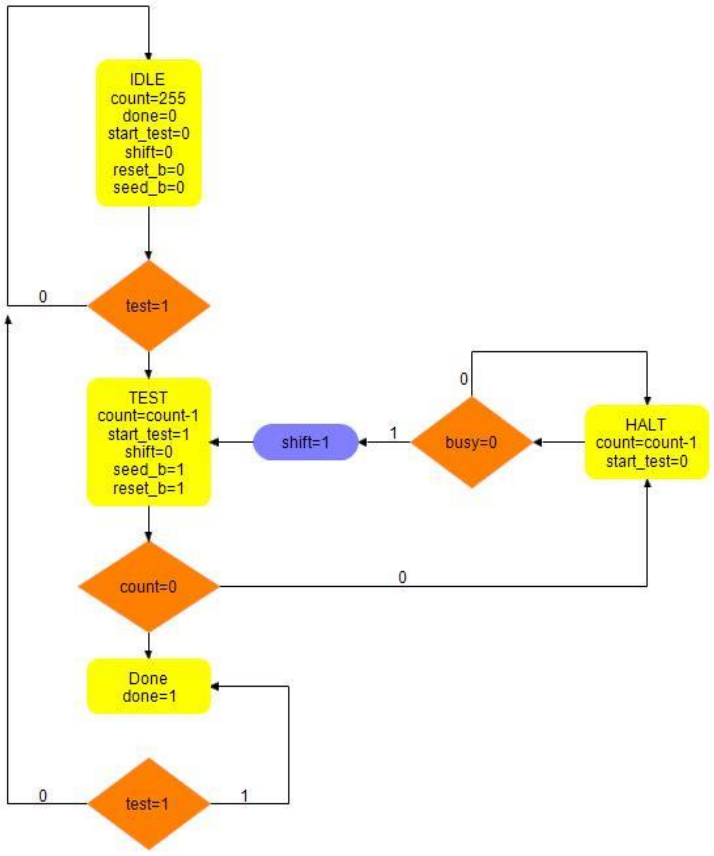


V-(B) BIST ALGORITHM FOR TESTER CIRCUIT

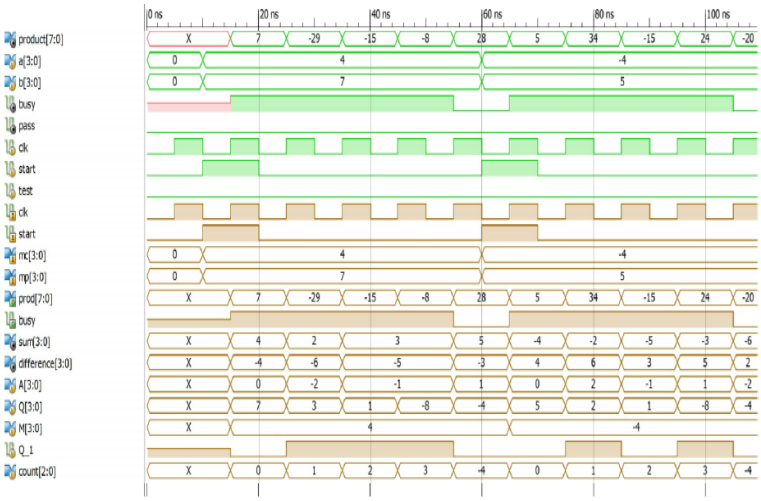
1. Reset all the signals to default zero value in Idle State. Reset to initial seed in LFSR and MISR to **1111_1111 and 0000_0000** by applying *seed_b = 0* and *reset_b = 0* respectively. The LFSR must be seeded to a non-zero value initially to generate pattern.
2. On *test = 1*, move to next state i.e., Test State. Issue *start = 1* on Booth's Multiplier. Set *shift = 0* to pause the pattern generator LFSR and compactor MISR. Set *reset_b* and *seed_b* as 1, as LFSR and MISR are already seeded.
3. If count = 0 jump to step 4, else jump to step 6.
4. This is Halt State, the state machine remains in this state for most amount of time. Set the start *signal = 0* to begin multiplying.
5. If *busy = 0*, move to step 2 with *shift = 1* as mealy output. This signal resumes the LFSR generator and MISR compactor to shift and accept new values. Else stay in the current state.
6. This is Done State, the testing is completed hence set the *done* signal as 1.

After the test has been completed, the *done signal* is set to one and the obtained signature in MISR is compared with the valid signature, i.e., sign[7:0] = 0101_1111B or 95D. This valid signature cannot be calculated manually, because test pattern polynomial is too large with maximum degree = 255. Hence the valid signature is obtained from the waveform in Vivado Simulator when there is not fault in the circuit. Later this signature is compared with the obtained signature in faulty circuit.

When the comparison is true, the *pass* signal is set 1 by the tester to indicate the circuit is not faulty.



VI. SIMULATION WAVEFORMS



Testbench waveform for Booth's Multiplier

The signals in green are the i/o signals of the top UUT i.e., *multiplier*. The signals in golden are some important signals in the *mult* UUT. The inputs *a* and *b* are loaded with respective values and the *start* signal pulse is given to start the multiplication. Since the Booth's multiplier takes O(n) time units, where n in the type of Booth's Multiplier (here n = 4), hence the multiplication takes 40 ns to complete. In the while, the *busy* signal is et 1 to indicate the multiplication is not complete. Just after *busy* signal gets low, we get the desired product as result.

Testbench waveform for BIST Tester Circuit with properly functioning Booth's Multiplier

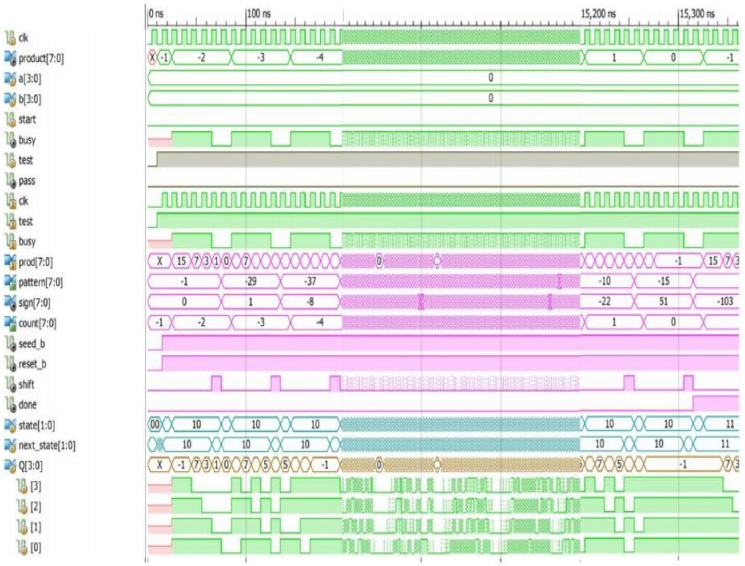
The signals in green are the i/o signals of the top UUT i.e., *multiplier*. The signals in pink are some important signals in the *tester* UUT. The signals in blue indicates state and next state of the BIST *Controller* UUT. The test and pass signals are colored grey to highlight them. When the test signal is high, the multiplier inputs and outputs are completely disconnected from user's control and are connected to the BIST tester. The tester follows the state machine described earlier. The output *product* signal is connected to *count* of the BIST controller. This provides an extra feature to display the time remaining for the test to complete to the user. The product signal down counts from 255 to 0 in (unsigned decimal form). When count value reaches 1111_1111B or -1, it indicates the testing is complete. Since the *pass* signal is 1 in the waveform, this means the signature is matched with the valid signature and test is passed. The tester is reset when *test = 0*. Since same *mult* module is used in this testing purpose, it will obviously *show pass = 1* whenever testing is complete, because no internal modification has been done in the *mult* module.

Since there are 2n-1 total patterns generated by the LFSR generator (excluding pattern 0000_0000B), the time taken to complete the test is approximately O(22n-1) units, where n is the type of multiplier (n=4 for 4 – bit multiplier). Each multiplication takes O(n) time units. And in test mode, 2 more – time units are required for state transition of BIST controller. Hence total time for test can be calculated by using formula:

$$(2^{2n}-1)\ (n+2)\ *10\ ns$$

for 100 MHz clock as used in the simulation or typical FPGA considering zero timing violations.

Time taken for test to complete for 4-bit Booth's Multiplier = $(2^{2*4}-1)\ (4+2)\ *10\ ns = 15300\ ns = 15.3\ \mu s$.



Testbench waveform for BIST Tester Circuit with properly functioning Booth's Multiplier

Using a normal testbench on the circuit will always show *pass = 1* when testing using BIST feature, as the circuit is never faulty in frontend pre-production process. Hence the testbench in Appendix B3 is empty with no stimulus. Faults must be created in *mult* module intentionally. To create stuck-at-0 or stuck-at-1, any individual signals inside *mult* module can be forced to 0 or 1 respectively using Vivado Simulator GUI.

The signals in green are the i/o signals of the top UUT i.e., *multiplier*. The signals in pink are some important signals in the *tester* UUT. The signals in blue indicates *state* and *next state* of the BIST *Controller* UUT. The *test* and *pass* signals are colored grey to highlight them. At last, an extra signal *Q[3:0]* with golden color is added to waveform. This signal shows the value of Q register in *mult* module. Modifying or forcing this signal will interfere with the results of the product and hence change the final signature. In this case the signal *Q[1]* is forced to stuck-at-1 from time interval 6020 ns to 6140 ns (just for 120 ns). The force is removed and then testbench is run normally. The product signal is down counting as always. When BIST testing is complete the product signal reaches 0 and the shows 1111_1111B or -1. At this moment, the *pass* signal is still low, indicating that the circuit is faulty. The test takes same time (i.e., 15300 ns) to complete.

VII. CONCLUSIONS

Probability of aliasing

It is the probability of that fault has occurred but not detected. It can be determined easily using the formula,

Probability of aliasing = 2-n

= 2-8 = 0.0039 (n = 8, size of Compactor)

Utilisation
The BIST multiplier circuit consists of 3 registers (A, Q, M) contributing to 3n FFs. The count register is sized (log2n + 1). One Q_1 reg takes 1 FF more.

Booth's Multiplier hardware utilisation (FF) = 3n + (log2n + 1) + 1 = 3n + log2n + 2

Similarly, for tester circuit compactor and generator contributes to **2*(2n) FFs**. The counter in the controller needs 2n FFs. Two more FFs are required for 4-states.

BIST Tester hardware utilisation (FF) = 2*(2n) + 2n + 2 = 6n + 2

Total hardware utilisation (Booth + tester) = (3n + log2n + 2) + (6n + 2) = 9n + log2n + 4
(for an n-bit Multiplier Circuit)

Hardware (FF) utilisation without tester = 3n + log2n + 2 = 16
Hardware (FF) utilisation without tester = 9n + log2n + 4 = 42
(n = 4)

This can be verified using Utilization Reports from Vivado Synthesis Tool. The following table describes the utilization of various resources.

Resource	Utilization (without BIST)	Utilization (with BIST)	Times Increase
LUT	13	45	3.46x
FF	16	42	2.62x
IO	19	21	1.11x
BUFG	1	1	1.00x

IO and BUFG is irrelevant and LUTs can be assumed to be proportionate to FF consumption. This simplifies the calculation the hardware overhead for the tester.

Type of Multiplier	FF Utilization (without BIST)	FF Utilization (with BIST)	Times Increase
Booth 2-bit	9	23	2.55x
Booth 4-bit	16	45	2.81x
Booth 8-bit	29	79	2.72x
Booth 16-bit	54	152	2.81x
Booth 32-bit	103	297	2.88x

It can be concluded that incorporating BIST tester for a Booth's Multiplier will consume 2.7x more hardware resources. Hence percentage increase in resources almost remains constant with size of multiplier. Other parameters like static and dynamic power will also show similar characteristics.

Test Duration
The test duration can be calculated using the previous formula derived in Simulation Section.

Test Time = (2^{2n} - 1) (n + 2) *10 ns (for 100 MHz clock)

Type of Multiplier	Test Time	
	(ns)	(- units)
Booth 2-bit	600	600 ns
Booth 4-bit	15300	15.3 µs
Booth 8-bit	6553500	6.55 ms
Booth 16-bit	7.731×10^{11}	12 min 53 secs
Booth 32-bit	6.172×10^{21}	195.7 millenniums

Hence it is very impractical to incorporate BIST testing beyond a 16-bit multiplier circuit.

VIII. References

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