Cmpe344 Fall 2021 FF67
Experiment #5: Cache Simulation

You will answer the following questions by using the SMPCache simulator. Set its configuration as follows:

Multiprocessor

Leave all with their defaults: 1 processor, MESI, and random.

Main Memory

- Word size: 4 bytes (called *word wide* in SMPCache and given in bits)
- Block size: 2 Kb (affected by *words by block*)
- Memory size: 8 Mb (affected by *words by block* & *blocks in main memory*)

Caches

- Cache levels: 1
- See the questions for the rest.

Do the following when you need to run the simulator on “EAR.prg”:

1. Load the EAR.prg:
   a. File → Open memory traces.
   b. From the directory selector, navigate into your SMPCache folder, and then SAMPLES\TRACES.
   c. From the file selector, choose EAR.prg.
   d. From the “Load in processors” panel, select only “1”.
   e. Click OK.
2. Start the simulation:
   a. Simulate → Complete execution. (Note: Nothing noticeable happens.)
   b. View → Cache evolution.
   c. Select “Text” format.
   d. Click OK.
   e. Click Execute.

Questions

1) How many bits are there in a word? 32 bits per word

2) How many words are there in a block? 512 words per block

3) How many blocks are there in the memory? 4096 blocks per memory

4) Assuming that the cache size is 16 Kb, how many blocks are there in cache? 8 blocks per cache

5) Assuming that the cache size is 16 Kb, calculate the number of blocks per set and the number of sets for the following cache designs. Furthermore, run the simulator for each of the designs and report their hit ratios.

	Mapping	Number of blocks per set	Number of sets	Hit ratio
a)	Direct	1	8	86.115%
b)	Set associative with 8 sets with LRU	1	8	86.115%
c)	Fully associative with LRU	8	1	97.268%
d)	Fully associative with FIFO	8	1	96.515%

6) Assuming that the cache size is 2 Mb, calculate hit ratios for the following cache designs. Use the LRU (least recently used) replacement policy when applicable.

	Mapping	Hit ratio
a)	Direct	99.303%
b)	Set associative with 16 sets per cache	99.303%
c)	Fully associative	99.303%

7) Compare the cache configurations 5(a), 5(b), 5(c), and 5(d) considering their hit ratios. Rank them from the best to the worst. Explain why. Discuss the factors which may cause this result.

c > d > a = b

Fully associative LRU is the best one because it utilized spatial locality efficiently. LRU is better than FIFO since in LRU, we replace the least recently used block (which is probably the best selection to remove). Fully associative FIFO is better than direct mapping, in direct mapping we are not able to utilize spatial locality, that is we don't fetch the neighbors of the currently called block, which undermines the performance. At last, performance of direct mapping and set associative mapping with 8 sets is the same, because when the correct calculations are performed, it can be seen that set associative with 8 sets corresponds to direct mapping (1-way set associativity). (In direct mapping, there are 8 sets with 1 block each)

8) Compare the cache configurations 6(a), 6(b), and 6(c) considering their hit ratios. Rank them from the best to the worst. Explain why. Discuss the factors which may cause this result.

a = b = c

Cache size is relatively bigger compared to the previous cache (16 Kb) we used. In this case, capacity makes our cache more efficient and it gives a constant hit ratio regardless of the caching mechanism because it always gives the same block address when calculating using modulo. Remaining compulsory misses and conflict misses at this point are a must and cannot be reduced.

9) If we use only direct mapping, find the cache size where making the cache any larger would have no effect on the hit ratio. Briefly explain why the hit ratio is not increasing anymore.

Cache size = 256 Kb

Hit ratio doesn't change because of the cold start (cache misses in the beginning).