

Module-5

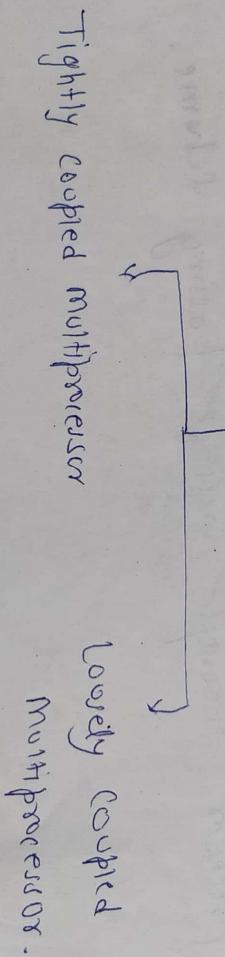
Multiprocessor

"A multiprocessor system is an interconnection of two or more CPUs with memory and input-output equipment."

The term "processor" in

multiprocessor can mean either a central processing unit (CPU) or an input-output processor (IOP).

Multiprocessor



1) Tightly coupled multiprocessor

Multiprocessor are classified

by the way their memory is organized. A multiprocessor system with common shared memory is classified

as Shared memory or tightly coupled multiprocessor.

This does not preclude each processor from having its own local memory. In fact, most commercial

~~PHADESH~~
tightly coupled multiprocessor provide a cache memory with each CPU.

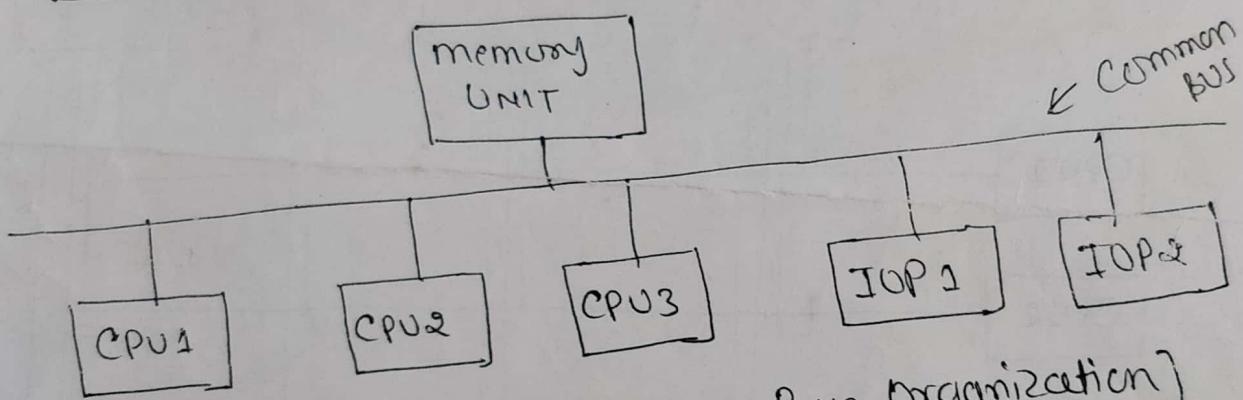
2) Loosely coupled multiprocessor:

Here each processor element in a loosely coupled system has its own private local memory. The processors are tied together by switching scheme designated to route information from one processor to another processor through message-passing scheme.

Multiprocessors 'MODULE-5' ORITIONAL COPY
are several physical forms available for establishing an interconnection network:-

- ① Time-shared common bus
- ② multipoint memory
- ③ crossbar switch
- ④ multistage switching network.
- ⑤ hypercube system.

① Time-Shared common Bus



(Time shared common Bus Organization)

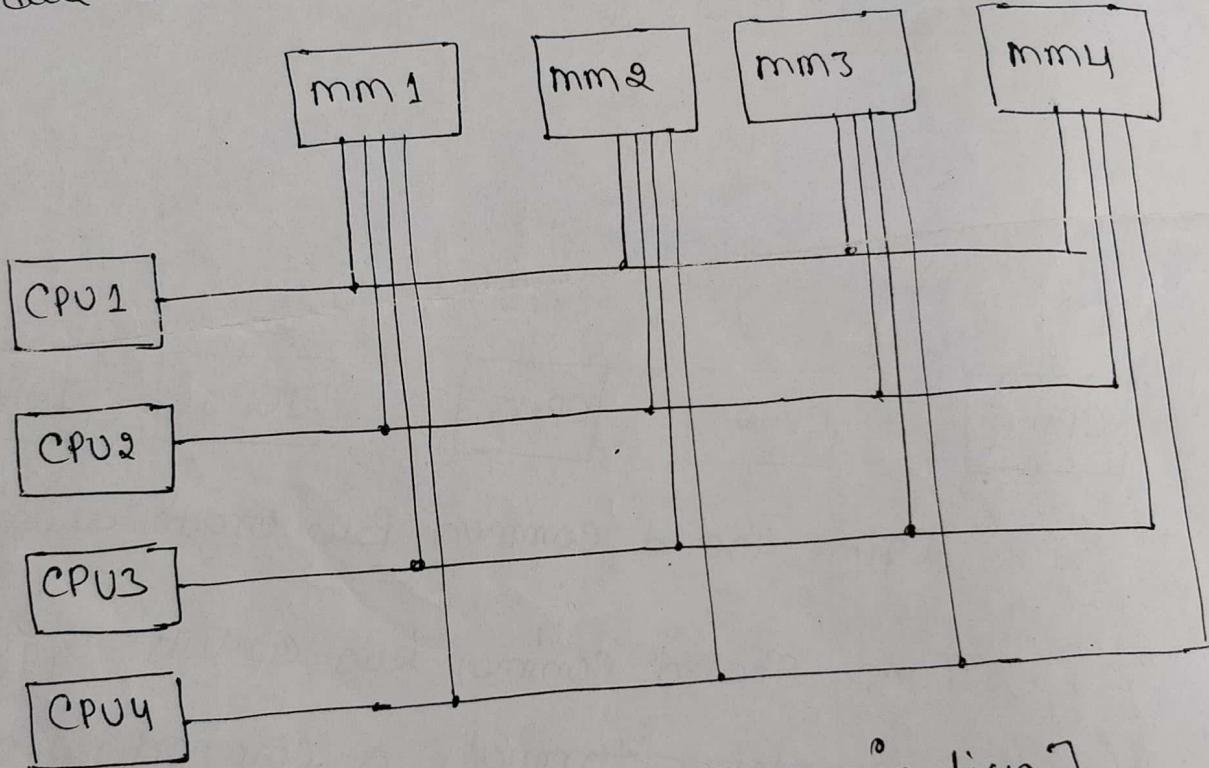
Time shared common bus consists of a number of processors connected through a common path to a memory unit. Only one processor can communicate with the memory.

A command is issued to inform the destination unit what operation is to be performed. The receiving unit recognize its address in the bus and respond to the control signals from the sender, after which transfer is initiated.

The system may exhibit transfer conflict since common bus is shared by all processors. These can be resolved by a bus controller that establishes priority among the requesting line.

② MULTIPORT MEMORY

Multiport memory interconnection network employs separate buses each memory module and each of CPU.



[multiport memory organization]

Each processor bus is connected to each memory & memory access conflicts are resolved by assigning fixed priorities to each memory port.

Advantages:

High transfer rate because of multiple paths between processor and memory.

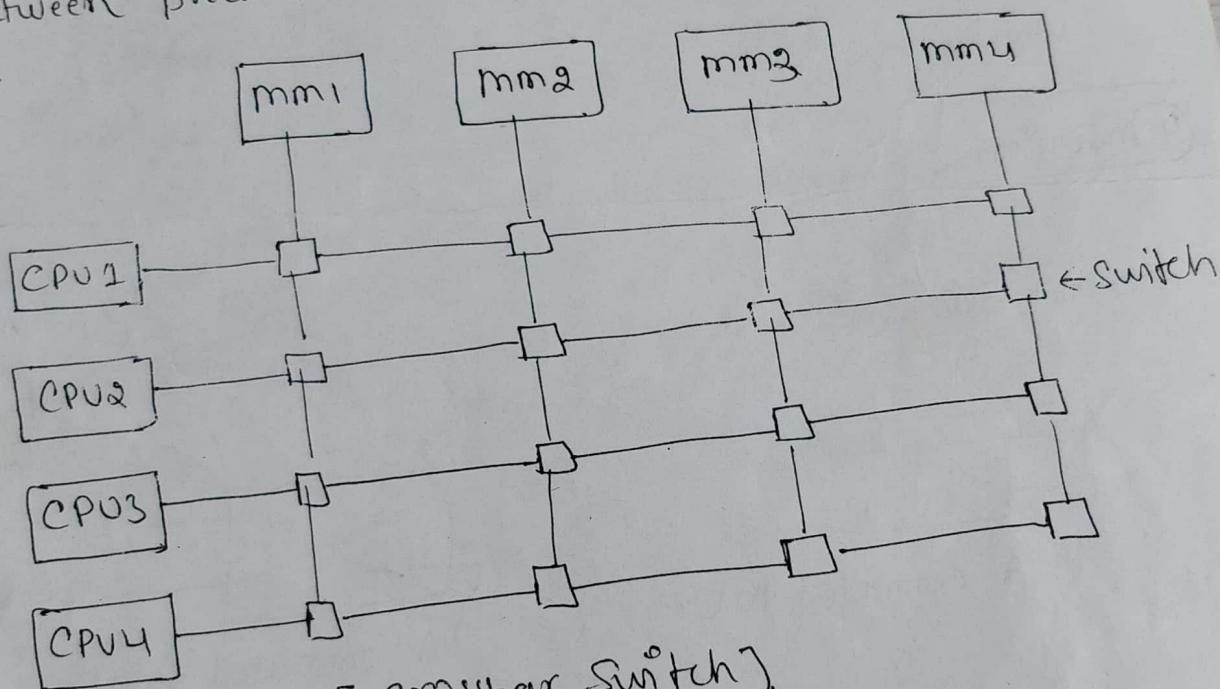
(B)

disadvantages:-

- ① expensive memory control logic
- ② large number of cables and connectors.

③ Crossbar switch Interconnection network,

crossbar switch consists of a number of crosspoints that are placed at intersection between processor buses and memory module paths.



Small square in each cross point is a switch that determines the path from processor to memory module.

Each switch point has control logic to setup the transfer path between a processor and memory.

Advantages,

Crossbar switch support simultaneous transfer from all memory modules because there is a separate path associated with each module.

Disadvantages:

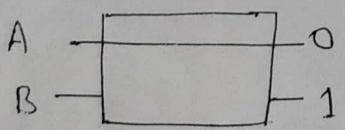
Suppose we have ' m ' number of CPU and we have ' n ' number of memory modules. Then

$$\text{Total required no. of crossswitch} = m \times n$$

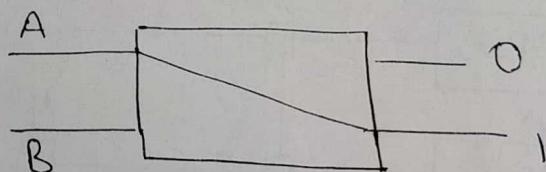
which one of large number of crossbar switch.

4 MULTISTAGE SWITCH NETWORK

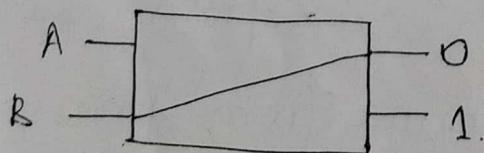
Basic component of a multistage network is 2-input, 2-output Interchange switch.



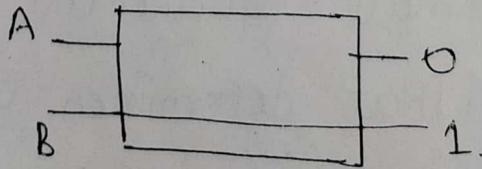
"A connected to 0"



"A connected to 0"
"B connected to 1"



"B connected to 0"

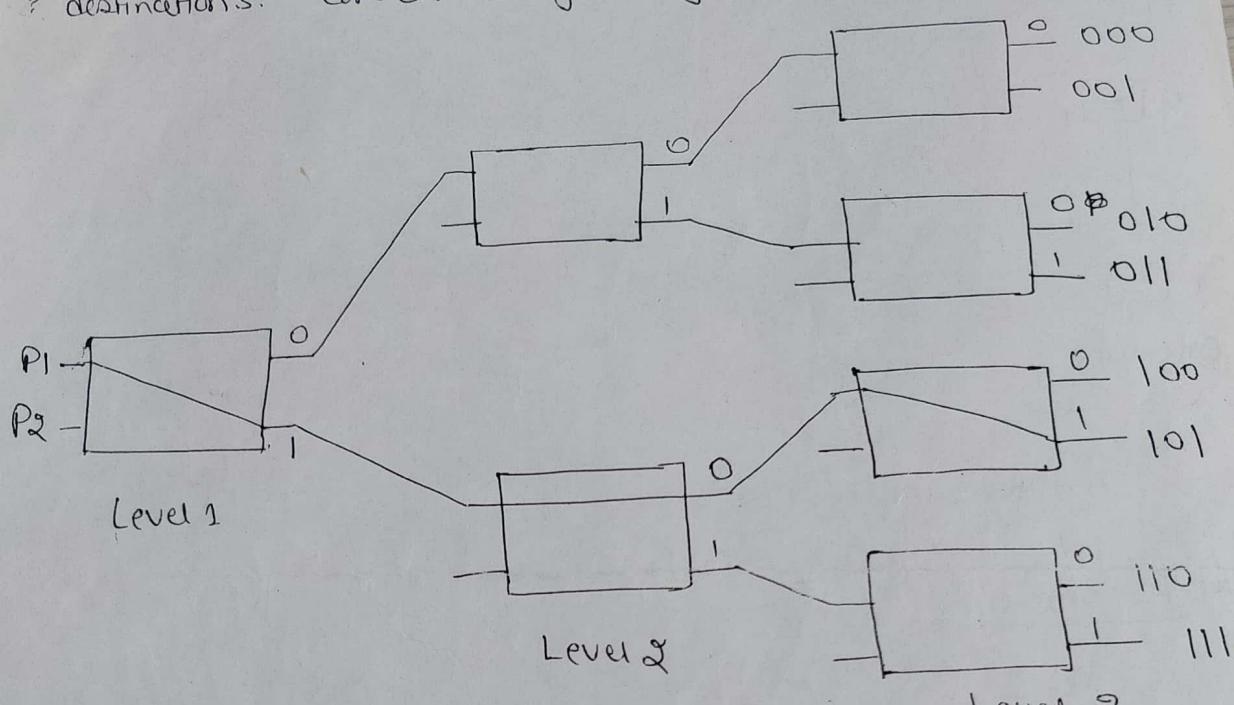


"B connected to 1"

Using the 2×2 switch as a building block, it is possible to build a multistage network to control the

Student Attendance Register

communication between a number of sources and destinations. consider the following binary tree:-



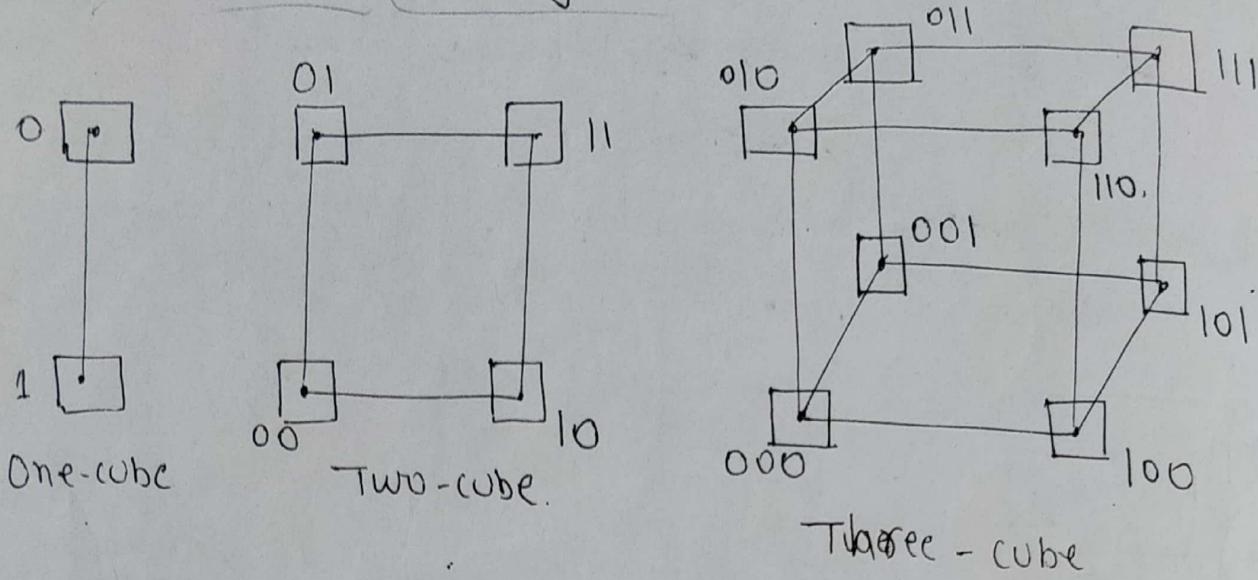
[Binary Tree with 2x2 switches]

many different topologies have been proposed for multistage switching network to control processor-memory communication. One such topology is Omega switching network. In this configuration there is exactly one path from each source to any particular destination.

⑤ Hypercube Interconnection or Binary n-cube

Hypercube interconnection or binary n-cube structure composed of $N = 2^n$ processors interconnected in

on n -dimensional binary cube. Each processor forms a node of the cube. Each processor has direct communication path to n -other neighbours processors.



[Hypercube Structure for $n=1, 2, 3$.]

* A one-cube Structure has

$$n=1, \text{ & } 2^n = 2^1$$

\Rightarrow two processors connected by single path.

* A two-cube Structure,

$$n=2, \text{ & } 2^n = 4$$

\Rightarrow means contains 4-nodes or processors interconnected as a square.

* A Three cube Structure,

$$n=3, \text{ & } 2^n = 8$$

Contains 8-nodes or processors interconnected as cube.



①

Asynchronous Data Transfer:

Two units, such as a CPU and I/O interface are designed independently of each other. If the registers in the interface share a common clock with the CPU registers, the transfer between the two units is said to be synchronous.

In most cases, the internal timing in each unit is independent from the other in that each uses its own private clock for internal registers. In that case two units are said to be asynchronous to each other.

"Asynchronous data transfer between two independent units requires that control signals be transmitted between the communicating units to indicate the time at which data is being transmitted".

We have the two main ways by which you can achieve this:-

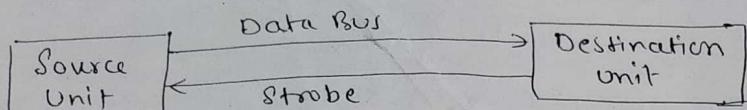
(a) Strobe control and

(b) Handshaking.

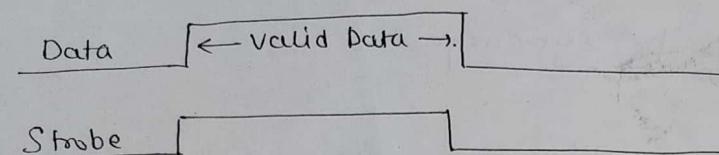
(a) Strobe Control:

Strobe is a single line that informs the destination unit when a valid data word is available in the bus. Strobe may be activated

either by the source or destination unit.



[Block Diagram]



[Timing Diagram].

[Source Initiated Strobe for data Transfer]

As shown in the timing diagram, the source unit first places the data on the data bus. After a brief delay to ensure that the data settle to a steady value, the source activates the strobe pulse. The information on the data bus and the strobe signal remain in active state for a sufficient time period to allow the destination unit to receive the data.

Source removes the data from the bus when destination receives it and disables the Strobe Signal. Now data bus does not contain valid data. New valid data will be available only after the Strobe is enable again.

b) Handshaking

Disadvantage of strobe method →:

Disadvantage of the Strobe method is that source unit that initiates the transfer has no way of knowing whether the destination unit has actually received the data item that was placed on the bus.

Similarly destination unit that

~~initiate~~ initiate the transfer has no way of knowing whether the source unit has actually the data on the bus.

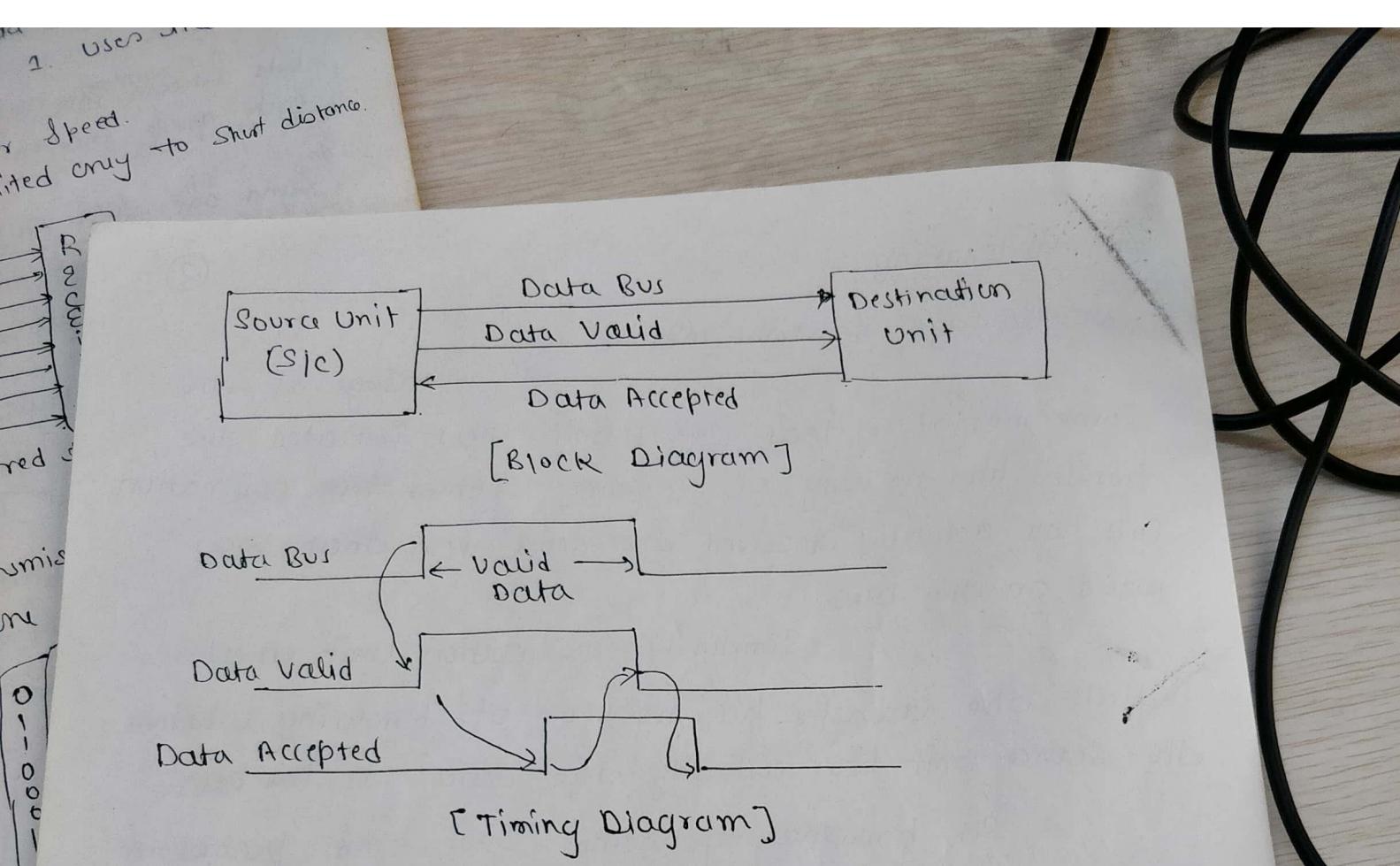
So, Handshaking method solves this problem by introducing the second control signal that provide a reply to the unit that initiates the transfer.

Basic Principle of two-wire handshaking:

One control unit line

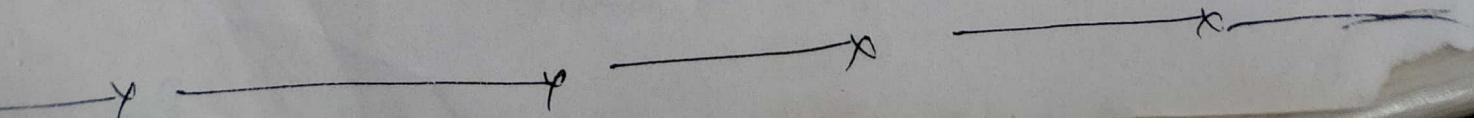
is in the same direction as the data flow in the bus from the source to destination. It is used by the source unit to inform the destination unit whether there are valid data on the bus.

- * The other control unit is in the other direction from the destination to source. It is used by the destination unit to inform source whether whether it can accept the data.

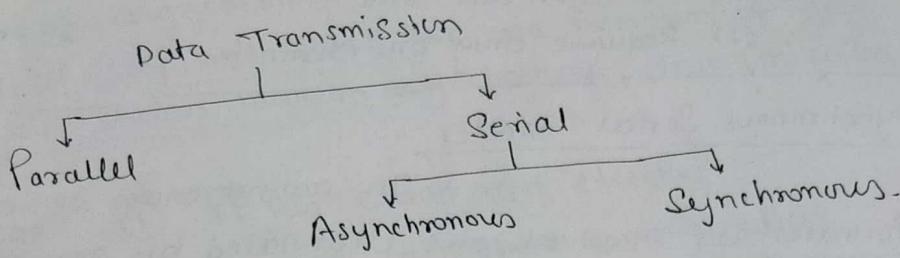


Advantages of Handshaking Scheme

- ① Handshaking scheme provide a high degree of flexibility and reliability because the successful completion of data transfer relies on active participation of both units.
- ② If the one unit is faulty, the data transfer will not be completed.
- ③ Such an error can be detected by means of a time-out mechanism which provide an alarm if data transfer is not completed within a time period.



(3)

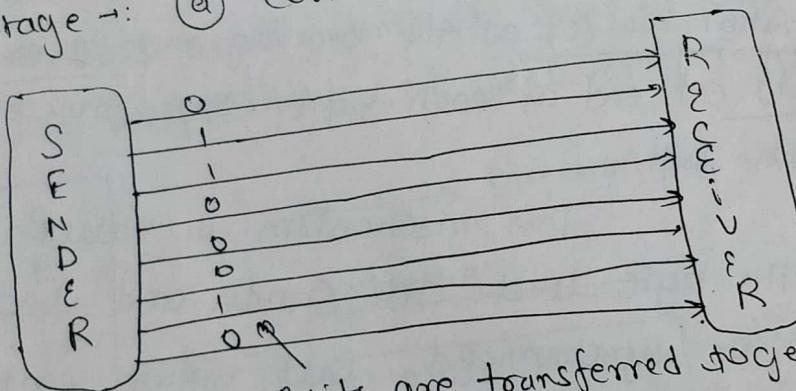


Parallel Data Transmission

Parallel data transmission send data of n -bits at a time instead of 1. Uses the n -wires to spend n -bits.

Advantage → increase the transfer speed.

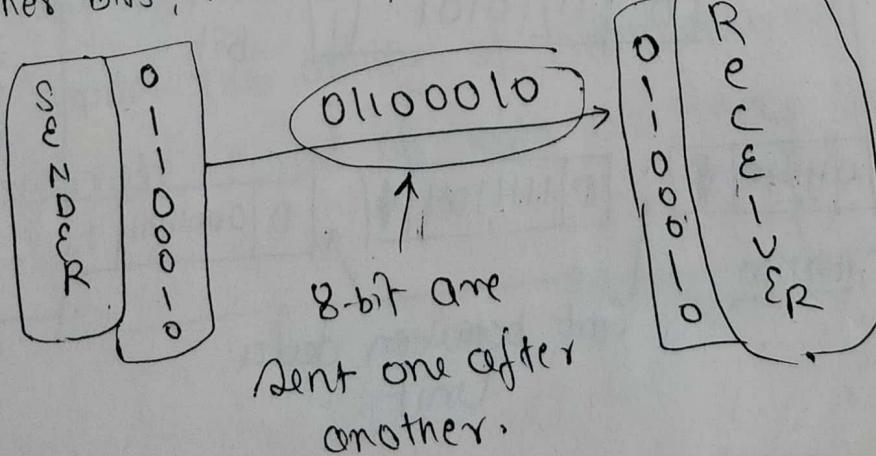
Disadvantage → (a) cost and (b) limited only to short distance.



8-bits are transferred together.

Serial transmission

In serial transmission one-bit follows the another bits, so we need only one unidirectional channel.



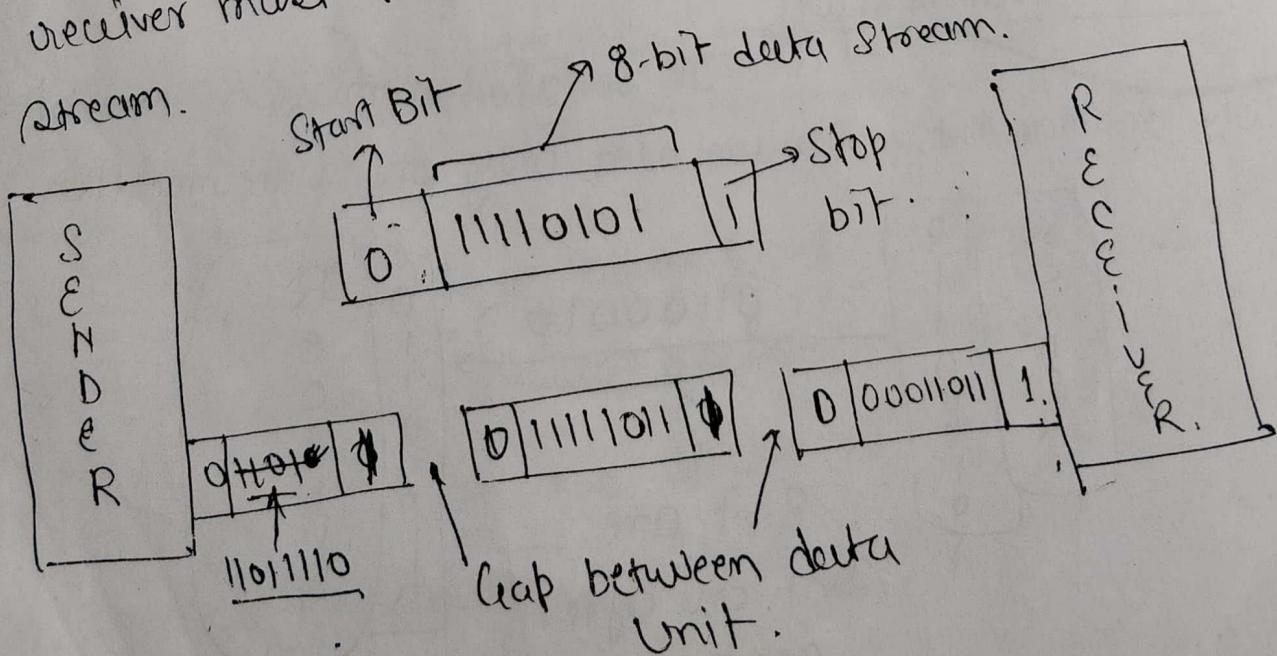
Advantages:-
(a) low cost and
(b) require only one channel.

Asynchronous Serial Transfer

In asynchronous serial transfer information is received and translated by agreed upon pattern. As long as those patterns are followed, the receiving device can retrieve the information. Patterns are based on grouping the bits stream into bytes. The sending device handles each group independently.

In this transmission we send one start bit (0) at the beginning and 1 or more stop bits (1) at end of each byte. There may be a gap between each byte.

This mechanism is called asynchronous because at the byte level, the sender and receiver do not have to be synchronized. But within each byte, the receiver must still be synchronized with incoming bit stream.

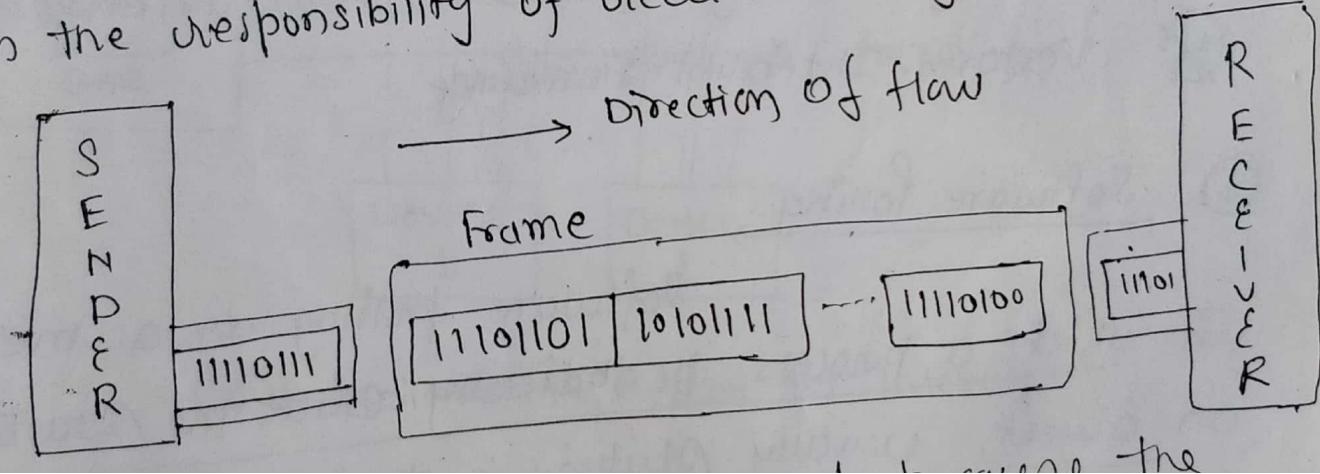


Advantages of asynchronous Serial transfer is that
addition of Stop and Start bit and insertion of gaps
into bit Stream makes asynchronous transmission
slow.

- Advantage:
- ① It is cheap and effective.
 - ② Application in low speed communication.

Synchronous Serial Transmission

In synchronous transmission
the bit stream is combine into longer frames which
may contain multiple bytes.
In this transmission we send
bits one after another without start or stop bits or gaps.
It is the responsibility of receiver to group the bits.



Interrupt Handling in PC

"-interrupt is a signal or event inside a computer system due to which the CPU temporarily suspends the current program execution and start execution of another program related to the interrupt."

methods of servicing Interrupts

Following are the methods of servicing the interrupt :-

- ① Software Polling.
- ② Bus Arbitration
- ③ Daisy chaining (which is HW arrangement)
- ④ vectored Interrupt Handling.

① Software polling

Software polling is a method in which a process periodically checks the status of an object, usually status is that of a flip-flop indicating the status bit. When the status bit changes, a specified action is being taken out. So, software polling is a time consuming process.

② Bus Arbitration

Priority device upto the device with the lowest

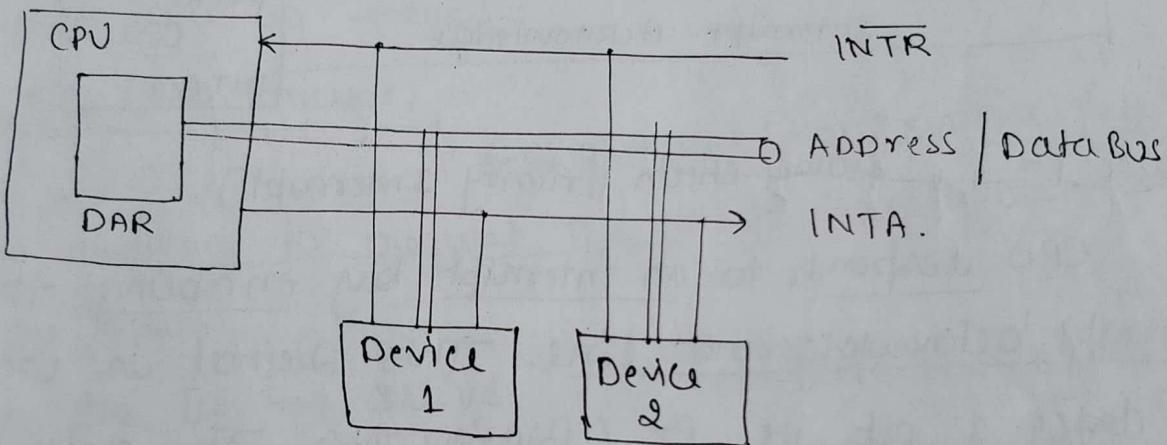
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Bus Arbitration

Polling is a time consuming process.

To reduce the time, a method called bus arbitration is used.

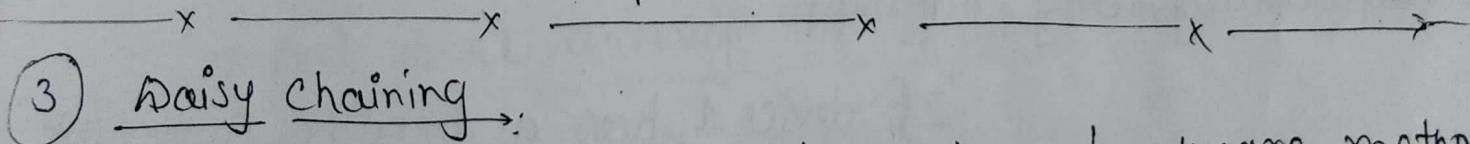
"Process of selecting the next bus master is called arbitration." In this case an interrupting unit gains access to the data bus and place the its device address to device address register. The interrupt service routine reads this address thereby uniquely identify the device.



[Bus Arbitration method for interrupt]

INTR = Interrupt request

INTA = Interrupt Accept.

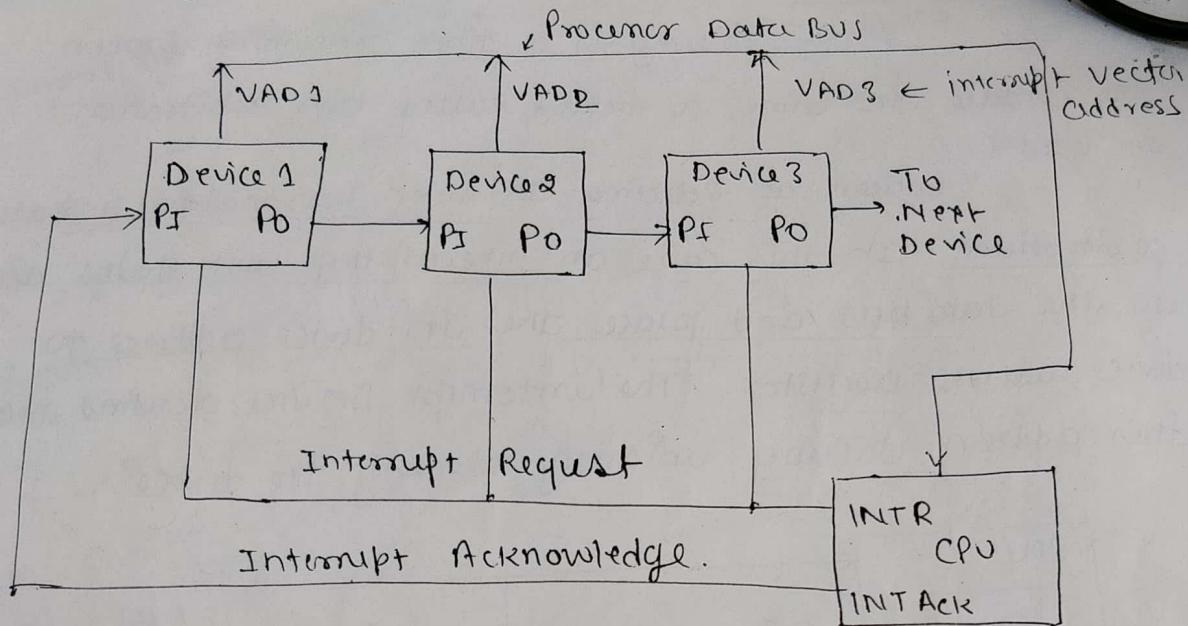


③

Daisy Chaining

Daisy Chaining is a hardware method used to assign order of priority in attending to interrupts. The device with the highest priority is placed in first position, followed by lower-priority device upto the device with the lowest

Priority which is placed last in chain.

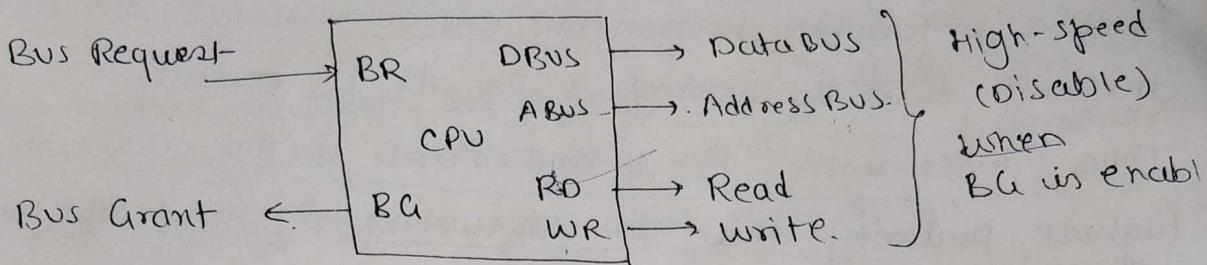


[Daisy chain Priority Interrupt]

CPU responds to an interrupt by enabling the interrupt acknowledgement line. This signal is received by device 1 at its PI (Priority In). The acknowledge signal is passes on to the next device through PO (Priority out) output only if device 1 is not requesting any interrupt.

If device 1 has a pending interrupt it blocks the acknowledgement signal from next device by placing the '0' in PO output. It then proceeds to insert its own interrupt vector address (VAD) into data bus for the CPU to use.

CPU Bus signal for DMA transfer



[CPU Bus signal for DMA transfer]

Two control signals in CPU that facilitate the DMA transfer are as follows:-

① BR (Bus Request)

Bus request input is used by the DMA controller to request the CPU to relinquish control of the buses.

When the BR is active, CPU terminates the execution of current instruction and places the address bus, data buses, read and write lines into high-impedance state. Now DMA communicate with the external peripheral device through the request and acknowledge lines by handshaking procedure.

② BG (Bus Grant Signal)

CPU activates the bus grant (BG) output to inform the external DMA that the buses are in high-impedance state.

(6)

during the interrupt cycle.

If the device does not have

pend pending interru pts it transmit the acknowledge signal to the next device by placing 1 in its P_0 output.

Thus device with $P_F=1$ and $P_0=0$ is the one with the highest priority that is requesting an interrupt and this device place the vector address on data bus.

The daisy chaining arrangement gives the highest priority to the device that receive the interrupt acknowledge signal from CPU.

Direct memory Access

The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of CPU.

Removing CPU from the path and letting the peripheral device to manage the memory buses directly would improve the speed of transfer. This transfer technique is called the Direct memory Access (DMA).

During DMA transfer CPU is idle and has no control of memory buses. A DMA controller takes over the buses to manage the transfer directly.

(2)

b) Handshaking.

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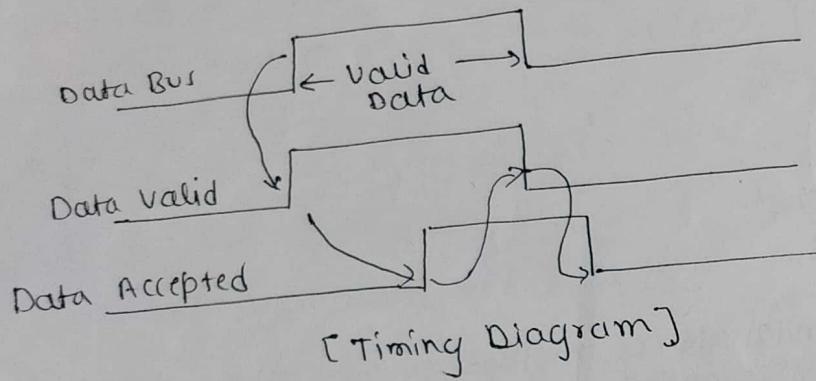
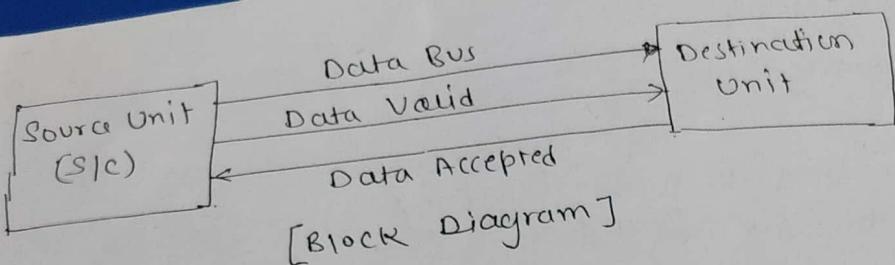
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f.t.o.



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