Semester = 4 , Subject - Microprocessor

Part - A

2) A compiler is used for programs that translate source code from a high-level programming language to a machine-level language to create an executable program.
The Assembler takes as input the assembly code and translates it into relocatable machine code.

3) In assembly language ~~mov~~ mnemonics are used to specify an opcode that represents a complete and operational machine language instruction.

4) **Program Counter**: It is a special purpose register which stores the address of next instruction to be fetched.
Stack pointer (SP): The stack is the reserved area of the memory in the RAM where temporary information may be stored.
It is used to hold the address of the most recent stack entry.

5) In ~~a~~ 1-byte instruction, opcode and the operand of an instruction are represented in one byte.

Example. Mnemonic - MOVB, A
Opcode - MOV
Oprand - B, A
Hex Code - 47H
Binary Code - 01000111

2-byte instruction - Here first 8 ~~bytes~~ bits indicate the opcode and next 8 bits indicate the operand.

Example. Mnemonic - MVI A, 32H
Opcode - MVI
Oprand - A, 32H
Hex Code - 3E
32
Binary Code - 00111110 and 00110010

1) A monitor program is usually in ROM and has a simple user interface. It allows you to examine and after monitoring memory, read or write I/O ports and so on.

Section-C

10) A) Interrupts are ~~an~~ the signals generated by external devices to request the microprocessor to perform a task.

Types of Interrupts in 8085.

a) TRAP: It is a non-maskable interrup

To receive the signal from interrupt TRAP, its signal pin must have high level. If this condition occur, then 8085 completes exution of current instruction, pushes ~~+~~ counter on the stack and branches to 003CH.

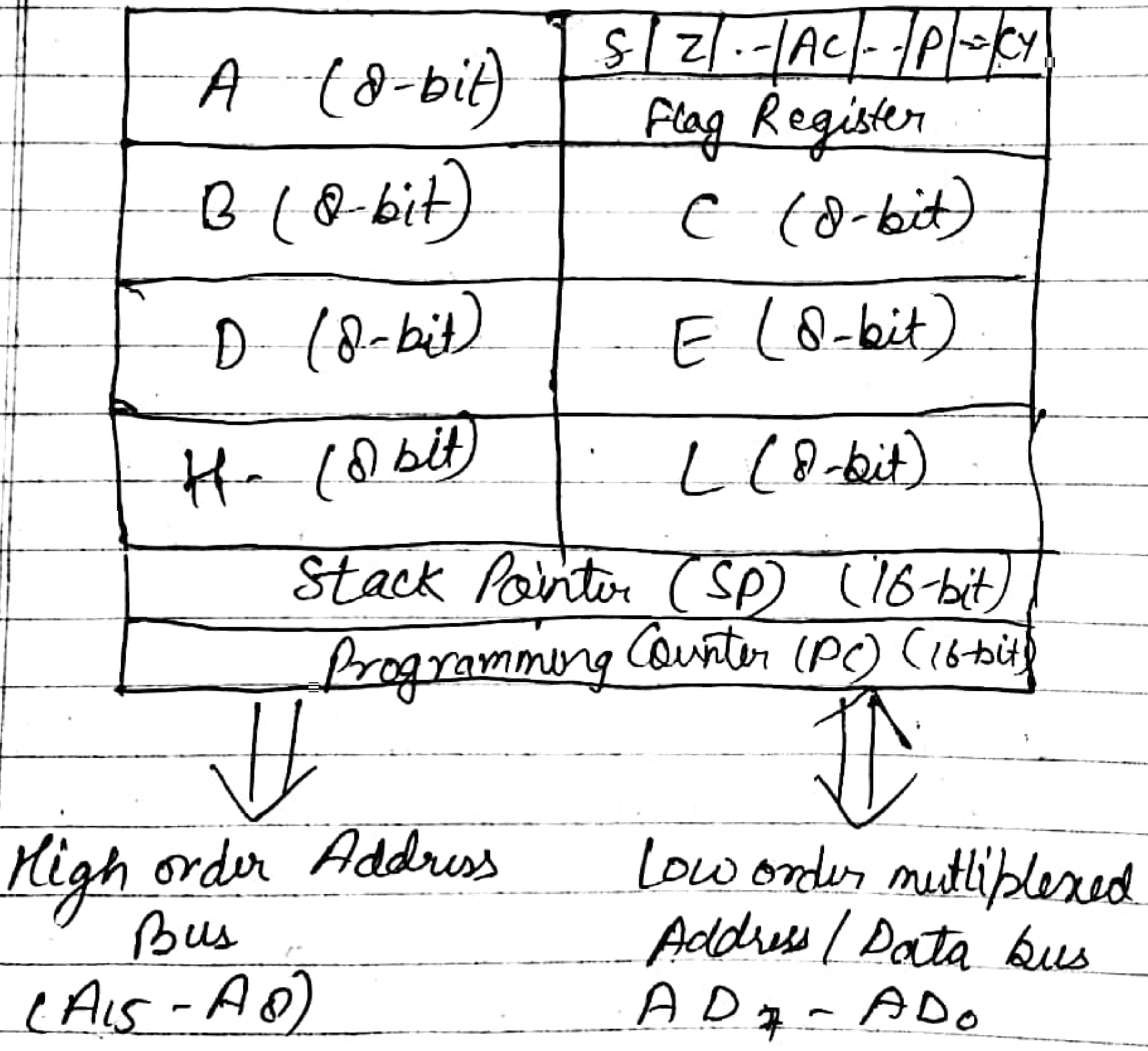
b) RST 7.5: It is maskable interrupt. It can be enabled and disabled using SIM instruction.

c) RST 6.5: This can be enable and displed using SIM instruction. It is high level sensitive, microprocessor 8085 execute current instruction. Save the program counter onto the stack and branches to 003CH.

d) RST 5.5: It is high level sensitive. In order to service this interrupt 8085 completes the exution of current instruction, save the program counter onto the stack and branches to location 002CH.

e) INTR: It is a non-maskable interrupt and ~~can be~~ is enabled in response to INTR signal, external logic places an instruction opcode on data bus on receiving the instruction.

B) Programming model of 8085:
It consits of an 8 bit accumulator, one flag register, 6 general 8-bit purpose registers and two 16-bit speical purpose rigistrs. These registers are critically required when programming a 8085 microprocessor.



A (8-bit)	S | Z | - - | AC | - - | P | - | CY Flag Register
B (8-bit)	C (8-bit)
D (8-bit)	E (8-bit)
H (8 bit)	L (8-bit)

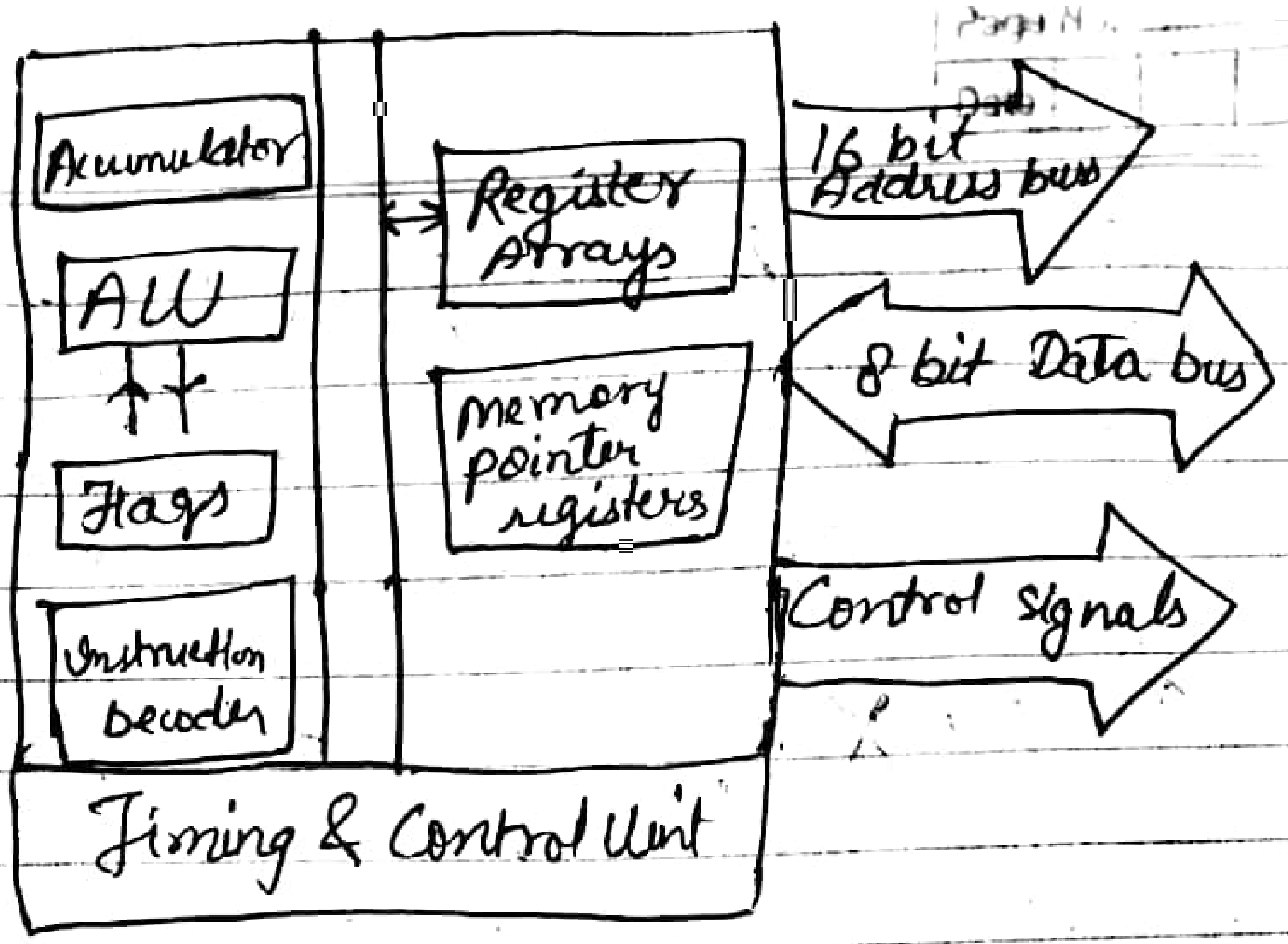
Stack Pointer (SP) (16-bit)

Programming Counter (PC) (16-bit)

High order Address Bus (A15 - A8)

Low order mutliplexed Address / Data bus AD7 - AD0

The hardware model shows two major segments. One segment includes ALU and an 8-bit register called an accumulator, instruction decoder and flags. The second segment shows 8 bit and 16 bit registers.



⇒ Flag Register: It is an 8 bit register in which 5 of the bits carry significant information in the form of flags:
S (Sign flag), Z (zero flag), AC (Auxiliary carry flag), P (Parity flag), C 4 carry flag.

Part - B

9) Any 5 Arithmetic instructions of 8085 are:

a) ADD (Add register data to accumulator):
This instruction adds the contents of register or memory with the content of accumulator and result is stored in accumulator.
Format: ADD R/M.

b) ADI (Add intermediate data to accumulator
The 8-bit data are added to contents of accumulator and result is stored in accumulator.
Format: ADI 8-bit data.

c) SUB(Subtract register or memory from accumulator) : The contents of register or memory location are subtracted from the contents of accumulator.

d) INX (Increment register pair by 1)
This instruction increments the contents of specified register pair by 1.

e) DCX (Decrement register pair by 1):
This instruction decrements the contents of specified register pair by 1.

8) Control and status signals:

a) ALE (Address latch enable): It is a positive ongoing pulse generated every time when 8085 begins an ~~instruct~~ operation. It indicates that bits AD_7-AD_0 are address bits

b) $\overline{RD}$ and $\overline{WR}$: These are used to control the direction of data flow between processor and memory or I/O device/port.

c) IO/$\overline{M}$, S_0 and S_1: These indicates whether I/O operation or memory operation is being carried out. S_1 and S_0 indicate the type of machine cycle in progress.

d) Ready: It is used to sense whether a peripheral is ready or not for data transfer. It is thus used to synchronize slower peripherals to the microprocessor.

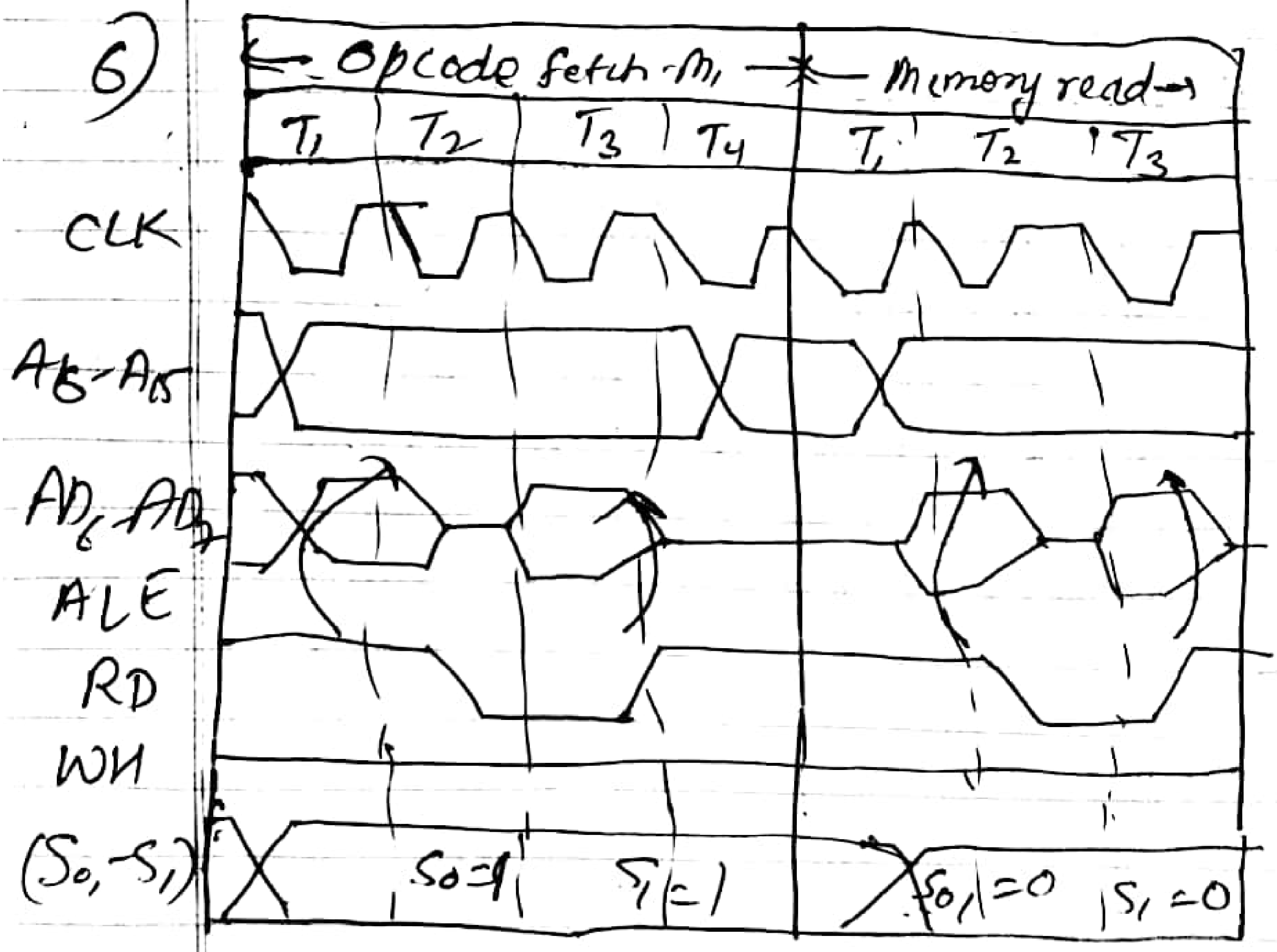
Externally initiated signals:

i) RESET: It is used to clear the program counter and update with 000 DH memory location. When it is activated by any external key, all internal operations are suspended for that time.

b) Interrupt: It has interrupts like TRAP, RST 5.5, RST 6.5, RST 7.5.

c) Ready: If signal is ready, pin is at low state.

6)



Timing Digram of MVI A, 32H.

This is a 2 byte instruction , so it requires 2 machine cycles to fetch instruction.

1) OP code fetch

2) memory read.

1) Opcode fetch: Program counter places address on higher order and lower order address bus the OP code at this memory location is read into the memory of microprocessor. This PC is then incremented by 1 to point to next byte. This machine cycles requires 4 T states

2) Memory Read: This data is read from the addressed memory location into the specific register. The PC is again incremented by one to point ~~on~~ to next instruction. The same timing diagram is applicably for different operations.