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Project Title: Designing and Simulating an **8-Bit Arithmetic Logic Unit** using Verilog HDL

Project Description:

Aim Of The Project:

The aim of this project is to design and simulate an **8-bit Arithmetic Logic Unit (ALU)** using **Verilog HDL**. The objective is to perform basic arithmetic and logical operations such as addition, subtraction, AND, OR, and XOR, and to understand how combinational logic can be used to implement computational units in digital systems.

Working Principle:

The 8-bit ALU is implemented using **combinational digital logic** and operates based on the input operands and control signals.

a.Input Operands

The ALU takes two 8-bit binary inputs, referred to as operand A and operand B.

b.Operation Selection

A control input is used to select the operation to be performed. Depending on the value of the control signal, the ALU performs addition, subtraction, or a logical operation such as AND, OR, or XOR.

c.Arithmetic Operations

For addition and subtraction, the ALU uses binary arithmetic. A carry or borrow flag is generated to indicate overflow or underflow conditions during arithmetic operations.

d.Logical Operations

Logical operations are performed bit-by-bit on the two input operands using standard logic gates.

e.Output Generation:

The result of the selected operation is produced as an 8-bit output. The output changes immediately with any change in inputs, as the ALU is a combinational circuit.

Learning Outcomes:

a.Combinational Logic Design:

Learned how arithmetic and logical operations can be implemented using combinational digital circuits.

b.Verilog HDL Concepts:

Gained experience in using always @(*) blocks, case statements, and concatenation in Verilog.

c.ALU Architecture:

Understood the internal working of an Arithmetic Logic Unit and its role in digital processors.

(1) Overflow and Carry Handling : Learned how carry and borrow flags are generated during arithmetic operations.

(2) Simulation and Debugging : Developed skills in verifying digital designs using testbenches and waveform analysis.

Tools Used:

Verilog HDL

Xilinx Vivado 2022.2

MEMBER: Karan Kumar