Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 6th Semester Examinations, February 2024

Subject: Computing-in-Memory Architecture (CS-3223)

Full marks: 50 Time: 3 hours

Answer any *five*

1. In CPU-centric von Neumann computing model, define memory wall, ILP wall, technology wall, reliability wall and cost wall. Define, in brief, the Computing-in-Memory (CIM) approaches. Denote the working set locations for such CIM approaches. 10

2. Show the construction of a DRAM cell with a capacitor and an access transistor that controls access to the cell. Describe normal read operation of DRAM, following charge sharing, assuming that the cell capacitor is initially charged. Following triple-row activation (TRA) explain how A+B and A.B (each A/B is of 1-bit) can be realized within the DRAM. 10

3. What is memristor? Show the general structure of memristive crossbar memory. Describe write and read operations in the memristive memory. Realize MAGIC (Memristor-Aided Logic) NOT and NOR in the memristive crossbar. 10

4. Define memristor-based Material Implication (IMPLY) logic. Compute Z = A NOR B with IMPLY. Show the construction of IMPLY within a crossbar. Show how a 2:1 MUX can be realized with IMPLY. 10

5. Describe bitonic sorting scheme considering the example unsorted list Y = 19, 2, 72, 3, 18, 57, 603, 101. Realize bitonic sorting scheme in memristive memory. 10

6. What is an Akers array cell? Show how an Akers array realizes the function f=xz'+yz. Describe a procedure, with example, for calculating the binary output of an Akers array. Show how in-memory computation can be done to realize 2-input NAND/NOR gates in QCA Akers array. 10

7. Write short notes on the following 10

a) In-memory searching in SRAM based CAM.

b) *n*-channel enhancement-type MOSFET

Memristor
MOSFET
Biotonic Sequence
DRAM