signal(v) → ↑ ;;

shmget( ) → creates a new shared memory segment if key doesn't have a shared memory Identifier with it. (creates a semaphore set)

Computing in Memory Architecture

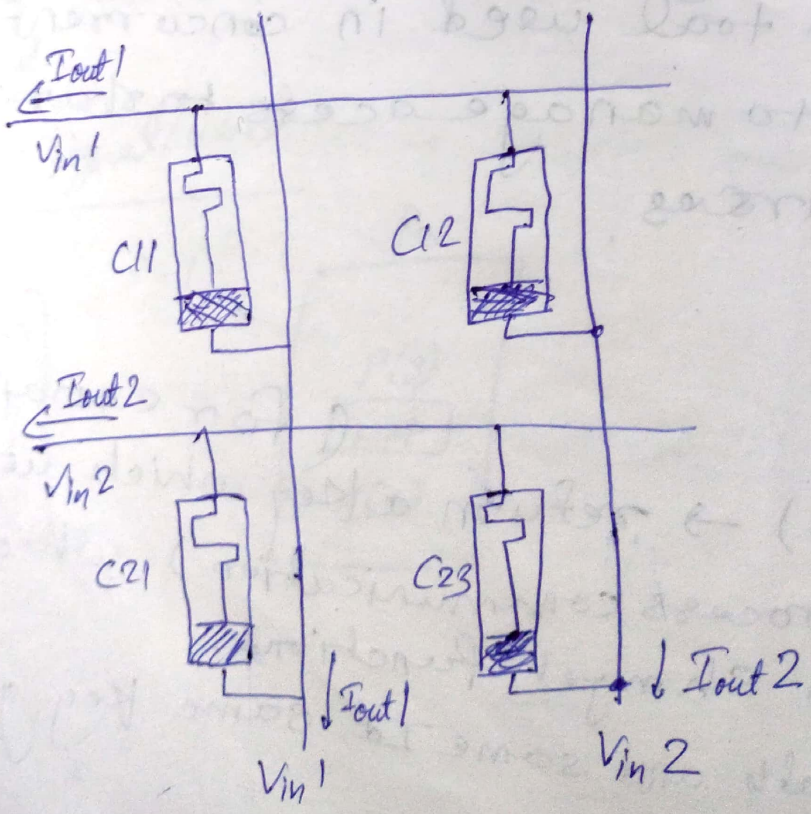
Release
CMOS AND gate pull-up
CMOS OR gate

In-memory Matrix-multiplication

VMM:- Vector Matrix-multiplication

$Ax = B$

↑ matrix ↑ vector



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$$i_j = \sum_{i=0}^{n} \frac{v_i}{R(i,j)} = \sum_{i=0}^{n} v_i C(i,j)$$

$I = V_i \times C$ (C: conductance)

$A_{m \times p} B_{p \times n}$ → we have to n times cycle. by using in memory matrix-multiplication

In-memory Sorting

Bitonic-~~sorting~~ Sequence generation algorithm

Eg. 1, 3, 7, 8, 3, 2, 0
ascending then decending

Eg. 8, 9, 2, 1, 0, 4 not bitonic sequence

* Bitonic Sort: (Compare and Swap)

$S = \langle a_0, a_1, \ldots a_{n-1} \rangle$

$S1 = \min\{a, a_{n/2}\}, \min\{a_1, a_{n/2+1}\}, \ldots \min\{a_{n/2-1}, a_{n-1}\}>$

$S2 = \max\{a, a_{n/2}\}, \max\{a_1, a_{n/2+1}\}, \ldots \max\{a_{n/2-1}, a_{n-1}\}.$

S1 & S2 Both are Bitonic

1	2	3	4	5	6	7	8	9	10

Eg. 1, 5, 7, 9, 11, 13, 10, 8, 4, 2, 0

S1 = 1 5 7 4 2

S2 = 13 10 8 9 11

* For bitonic, we need a comparator and two n-bit MUX.
* We release it using NOR.
* Figure NOR ~~based~~ MAGIC design of 2-bit comparator

Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 6th Semester Mid Semester Examination, February 2025

Subject: Computing-in-Memory Architecture (CS-3223)

Full marks: 30 Time: 2 hours

Answer all

1a) In CPU-centric von Neumann computing model, define ILP wall, Technology walls and Reliability wall. 4

b) Introduce Chip multi processors (CMPs), Processing-in-Memory (PIM) and In-memory Computing (IMC). Identify the working set locations in such computing systems. 2

2a) What is TiO_2 based memristor? What is RVM and RRM in memristive design? MAGIC (Memristor-Aided Logic) belongs to which class? Justify your answer. 3

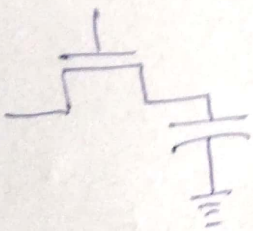
b) Explain how 2-input NAND and NOR truth table can be realized with MAGIC memristor devices. 3

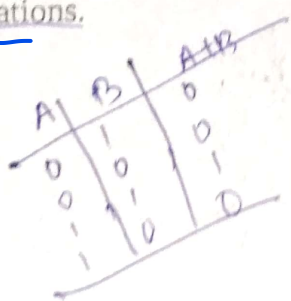
3a) Define memristor-based Material Implication (IMPLY) logic. In IMPLY logic, Vset is applied at Q and Vcond at P to realize P implies Q. Vth is for switching of memristor device. Explain why the relation Vset > Vth > Vcond is to be satisfied? 3

b) Compute Z = X NAND Y with IMPLY. Show how 2:1 MUX can be realized with IMPLY. 3

4. Show the construction of a DRAM cell with a capacitor and an access transistor. Describe normal read operation of DRAM, following charge sharing. Following triple-row activation (TRA) explain how A+B (each A/B is of 1-bit) can be realized within the DRAM. 6

5. Explain how a 6T SRAM cell can be written (assume logic 1). Design a logic circuit that can perform In-SRAM AND and NOR operations. 6





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