Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 6th Semester Mid-Semester Examination, February 2025

Operating Systems (CS 3201)

Full Marks: 30 Time: 2 Hours

- **Attempt all four (4) questions.**
- **Answers should be precise, to the point, and in your own words as far as practicable.**
- **Make your own assumptions, if necessary, and state them at proper places.**

1. (a) Enumerate the cases in which a process in a time-sharing multitasking system can "go" into wait state. [3]

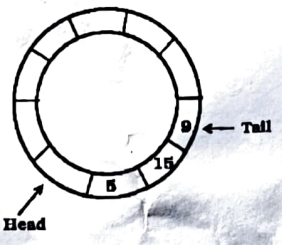
   (b) Let there be no **Operating System** on an IBM PC compatible computer. After it is powered on, the computer is needed to execute a fixed user program stored in one of its secondary storage devices. State a step by step account of how this can be achieved. [4]

2. (a) With the help of suitable **example**(s) explain when and how the "**Operating System**" gets executed in a running time-sharing multitasking system. [3]

   (b) With the help of suitable **diagram**(s) explain how the idea of **Virtual Memory** helps the implementation of shared memory in a multitasking "**Operating System**". [4]

3. (a) Explain with suitable example(s) how access rights and/or permissions (in terms of read-write-execute aka rwx) can be granted on **System V shared memory segments** and **semaphores**. [2]

   (b) Let there be a circular queue (holding at most 10 integer items) shared among **independent processes**, as shown in the following figure. These processes can add items (one at a time) to the queue, and/or delete items (one at a time) from the queue.



   - Since the circular queue is shared (updated) among more than one concurrent processes, there are possibilities for race conditions to occur. Ensure that there is no race condition.

[Contd.]

- A process cannot add an item if the queue is full and should wait for some other process to delete an item. This must not be a "**busy waiting**", that is, the process, in that case, should "go" into wait-state.
- A process, on the other hand, cannot delete an item if the queue is empty, and should wait for another process to add one item. This too must not be a "**busy waiting**", that is, the process, in that case, should "go" into wait-state.

Propose a scheme to implement the above-mentioned circular queue using System V IPC tools. [6]

4. Propose a working scheme for implementation of a **shared linked list** data structure, which can be used (shared) by multiple threads within a processes. Propose solution for **(i) create a new linked list (ii) add a node to a linked list, (iii) delete a node from a linked list**, and **(iv) search for a node in a linked list** operations.

   Please note the following.

   - At a time multiple linked lists can be there (created and being used by the threads).
   - Nodes (struct in C) of the linked lists have only one integer data field (other than the fields needed for implementing a shared linked list).
   - Since multiple threads may attempt to modify (add a node, delete a node, etc.) a linked list, race condition may occur. Judicious **identification and handling of critical section(s)** are utmost important. For example, deletion of a node starts with finding out the previous node of the node to be deleted and this step does not involve any modification but takes most of the time, etc. That is, both **race condition** and **unnecessary blocking of threads** should be avoided. [8]

Indian Institute of Engineering Science and Technology, Shibpur
BTech 6th Semester Mid-Semester Examination, February 2025

Data Communication and Computer Network (CS3202)

Full Marks: 30 **Time: 2 Hours**

Attempt all questions

1. Answer all questions

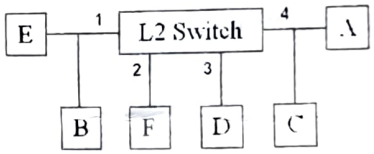
a) What is the use of Carrier Signal in communication system?

b) Draw the Manchester and Differential Manchester encodings waveform for the bit sequence '0 1 1 1 0 0 1 1'.

c) The following 8 bits '1 1 0 0 1 0 0 1' are to be transmitted using the CRC polynomial $(x^3 + 1)$. What is the bit pattern that should be transmitted? Answer with justification.

d) In a Selective-Reject ARQ protocol, 3 bits are used for Sequence Number. What will be the maximum window size for sender and receiver? Answer with justification.

d) Six hosts A, B, C, D, E, and F are connected using a Layer-2 switch. Assume that the switch initially does not know anything about any of the hosts (empty lookup table). The first few frames are transmitted in the given order:



(i) A → D, (ii) C → E, (iii) C → A, (iv) E → B, (v) E → F, (vi) E → C, (vii) F → E

Which of these frames are broadcast by the L2-switch and which frames are unicast? Answer with brief justification.

(1+3+3+3+4 = 14)

2. Answer any 4 from the following questions

a) Consider two stations S (sender) and R (receiver) using the "Selective reject/repeat ARQ" for error control. Illustrate with examples how the following cases are handled:
   (i) A data frame sent by S does not reach R
   (ii) A data frame sent by S reaches R but is corrupted

b) Explain 'p-persistent CSMA'. Discuss the effects of the choice of the value of 'p' on the performance of p-persistent CSMA.

d) Discuss various types of Radio Wave Propagation methods.

e) State the primary functions of Network and Transport layer as per OSI reference model.

e) What does a node using CSMA/CD protocol do on detecting a collision? How does it decide when to try re-transmitting the frame?

f) Illustrate how different signal states can be obtained by mixing different Shift Keying methods. What are the challenges involved in higher-order digital modulation?

(4x4 = 16)

Indian Institute of Engineering Science and Technology, Shibpur

B. Tech (CST), 6th Semester, Mid-Semester Examination, 2025

Software Engineering (CS3203)

Full Marks: 30 *Time: 2 Hours*

- *Answer only three questions*
- *No answer to extra question will be evaluated.*
- *Use diagram/code wherever possible*

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1. (a) Choose the correct alternative. No explanation is needed for your answer.

(i) Which of the following is NOT a level in the DIKW pyramid?
(A) Data (B) Information (C) Intelligence (D) Wisdom

(ii) What is one key benefit of software engineering is
(A) Faster initial development (B) Reduced costs through structured processes
(C) More creativity in coding (D) Less need for documentation

(iii) Which of the following is NOT typically included in an SRS document?
(A) User requirements (B) System design diagrams (C) Performance specifications (D) Functional requirements

(iv) What does technical feasibility in software engineering primarily assess?
(A) Project cost and budget (B) Availability of technology and resources to complete the project
(C) User feedback and satisfaction (D) Marketing potential of the software

(v) In which model must each phase be completed before the next begins?
(A) Evolutionary Model (B) Agile Model (C) Waterfall Model (D) Prototype Model

(b) Clearly write **True** or **False** for the following statements. No justification is needed for your answer.

(i) Wisdom is the application of knowledge to make informed decisions, considering ethical implications and potential consequences.

(ii) An exploratory approach is more suitable for large, complex software systems than software engineering.

(iii) SRS acts as a formal agreement between stakeholders and the development team

(iv) Legal feasibility focuses on improving the software's performance speed.

(v) The Evolutionary Model delivers the complete software product only at the end of the final phase

(5+5=10)

2. (a) Answer in **one full sentence** only

Which phase of SDLC involves translating requirements into technical solutions?

In which phase, updates are applied to the software?

Which phase ensures that system architecture and data structures are well-defined?

Which testing technique is used to identify defects in individual units or components of the software?

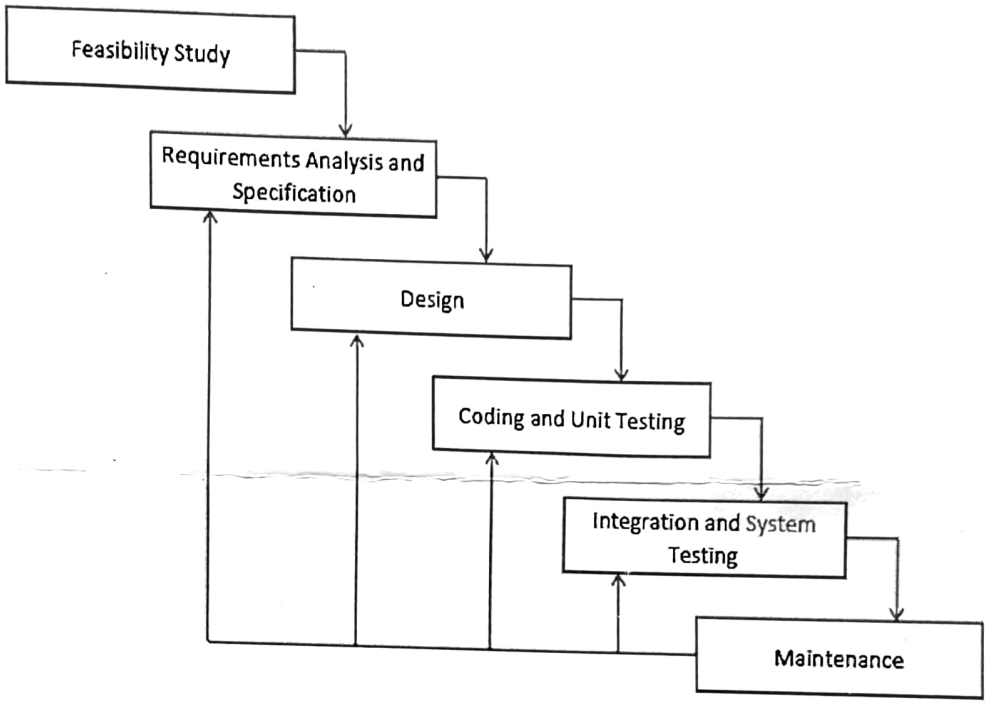
How does software testing contribute to software reliability?

(b) Match the following. No marks will be awarded for partially correct matching

A. Non-functional Requirements	1. Emphasizes risk assessment and iterative refinement
B. Spiral Model	2. Breaks system into smaller, manageable components
C. Waterfall Model	3. Produces an early working version for user feedback
D. Prototyping Model	4. Describe system performance and security needs
E. Modular Design	5. A linear, phase-based software development approach

(5+5=10)

3. Consider a software lifecycle development model as shown in figure



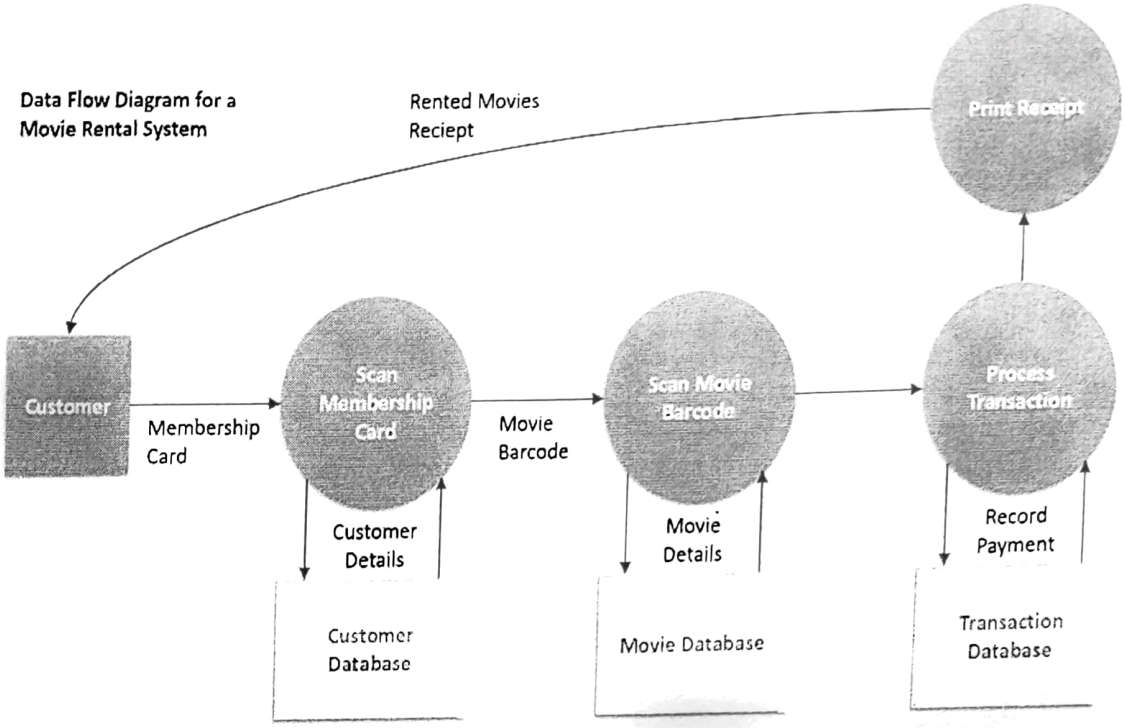
(a) Identify the SDLC model. Mention also the name of SDLC model which can be considered as its purely sequential version.

(b) Discuss 'feedback path' with the help of this figure.

(c) Describe how this SDLC model differs from its purely sequential model. Discuss one advantage and one drawback when the model is used instead of the purely sequential model.

(2+2+6)

4. Consider a data flow diagram of movie rental system



(a) Carefully examine the provided Data Flow Diagram. Identify the key processes involved in the movie rental system and briefly describe the function of each process.

(b) Describe (in 1-2 lines) how each data store contributes to the overall functionality of the movie rental system?

(c) Based on the DFD, analyse the flow of data from the customer to the final receipt generation.

(2+2+6)

5. Write short note on the following

(a) Draw a labelled diagram of V-Model in SDLC. No description of V-Model is needed.
(b) Describe (word limit: 50) the core principles of Agile software development.
(c) Write a short note on: Service oriented software architecture

(2+2+6)

Indian Institute of Engineering Science and Technology, Shibpur

B. Tech. (CST) 6th Semester Mid-Semester Examination, February 2025

Information Security and Cryptography (CS 3204)

Time: 2 Hours **Full Marks: 30**

[Answer all the following questions.]

1. (a) Explain different phases of security life-cycle.
   (b) Explain different principles of security mentioning the names of different attacks that try to break these principles.

[4 + 6]

2. (a) Explain the working principle of Vigenere cipher with an example.
   Is there any drawback of Vigenere cipher?
   (b) Draw and explain the working principle of Feistel cipher structure.
   (c) What is the problem of Electronic Code Book (ECB) mode?
   How Cipher Block Chaining (CBC) mode solves this problem?

[(2 + 1) + 3 + (2 + 2)]

3. (a) Consider that the 10-bit initial key in Simplified Data Encryption Standard (S-DES) is (1010000010). Find out the corresponding two 8-bit keys where the P10 and P8 boxes are as follows:

P10									
3	5	2	7	4	10	1	9	8	6

P8							
6	3	7	4	8	5	10	9

   (b) Explain the mechanism of S-box substitution in a round of Data Encryption Standard (DES).
   (c) Briefly explain the method of key expansion in AES.
   (d) Alice & Bob want to establish a secret key using Diffie-Hellman Key-exchange algorithm assuming the following values:

   n = 11 (divisor), g = 5 (power), x = 2 (chosen by Alice), y = 3 (chosen by BoB);

   Find the value of the secret keys (k1 & K2) calculated by them.

[3 + 2 + 3 + 2]

Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 6th Semester Mid Semester Examination, February 2025

Subject: Computing-in-Memory Architecture (CS-3223)

Full marks: 30 Time: 2 hours

Answer all

1a) In CPU-centric von Neumann computing model, define ILP wall, Technology walls and Reliability wall. 4

b) Introduce Chip multi processors (CMPs), Processing-in-Memory (PIM) and In-memory Computing (IMC). Identify the working set locations in such computing systems. 2

2a) What is TiO_2 based memristor? What is RVM and RRM in memristive design? MAGIC (Memristor-Aided Logic) belongs to which class? Justify your answer. 3

b) Explain how 2-input NAND and NOR truth table can be realized with MAGIC memristor devices. 3

3a) Define memristor-based Material Implication (IMPLY) logic. In IMPLY logic, Vset is applied at Q and Vcond at P to realize P implies Q. Vth is for switching of memristor device. Explain why the relation Vset > Vth > Vcond is to be satisfied? 3

b) Compute Z = X NAND Y with IMPLY. Show how 2:1 MUX can be realized with IMPLY. 3

4. Show the construction of a DRAM cell with a capacitor and an access transistor. Describe normal read operation of DRAM, following charge sharing. Following triple-row activation (TRA) explain how A+B (each A/B is of 1-bit) can be realized within the DRAM. 6

5. Explain how a 6T SRAM cell can be written (assume logic 1). Design a logic circuit that can perform In-SRAM AND and NOR operations. 6