

# ***Operating Systems***

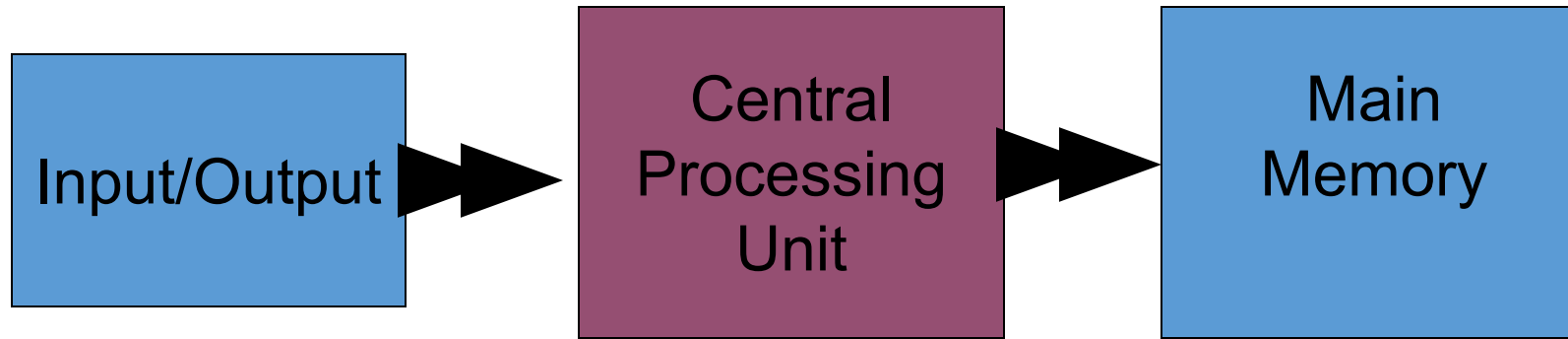
**CSE 231 (Section B)**

**Instructor: Sambuddho Chakravarty**

(Semester: Monsoon 2020)

Week 2: Aug 31 – Sept. 6

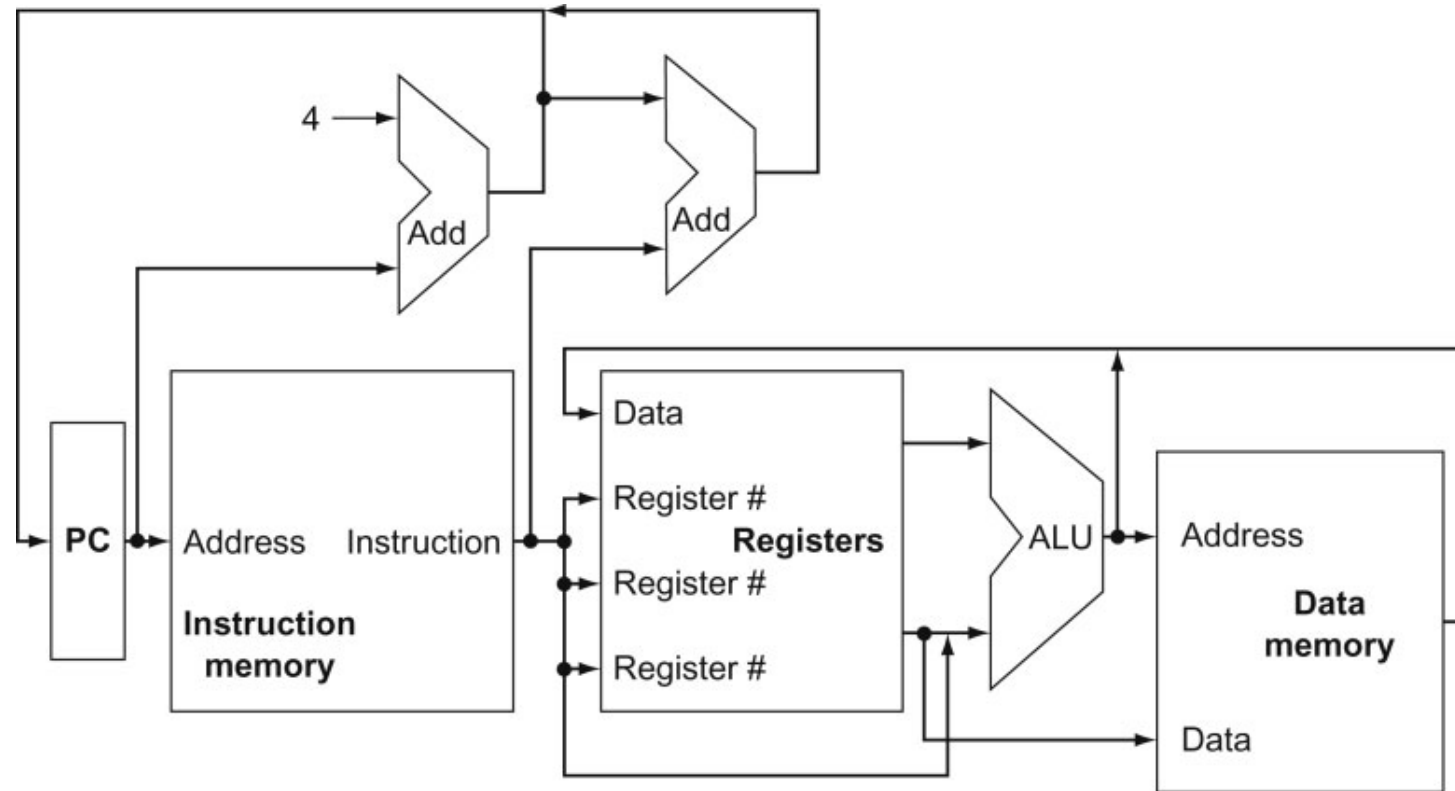
# Abstract model



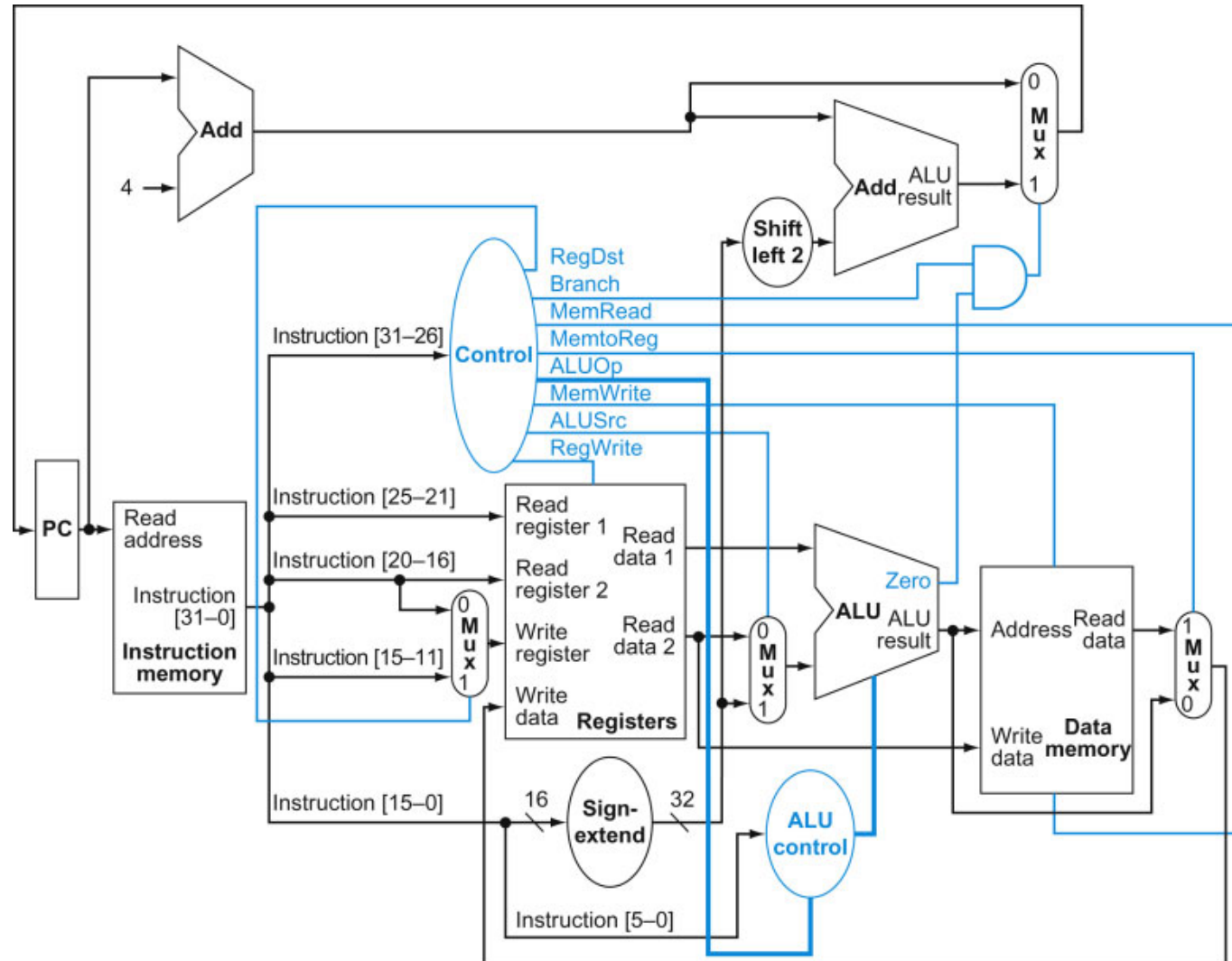
- I/O: communicating data to and from devices
- CPU: digital logic for performing computation
- Memory:  $N$  words of  $B$  bits

# View from 30,000 Feet

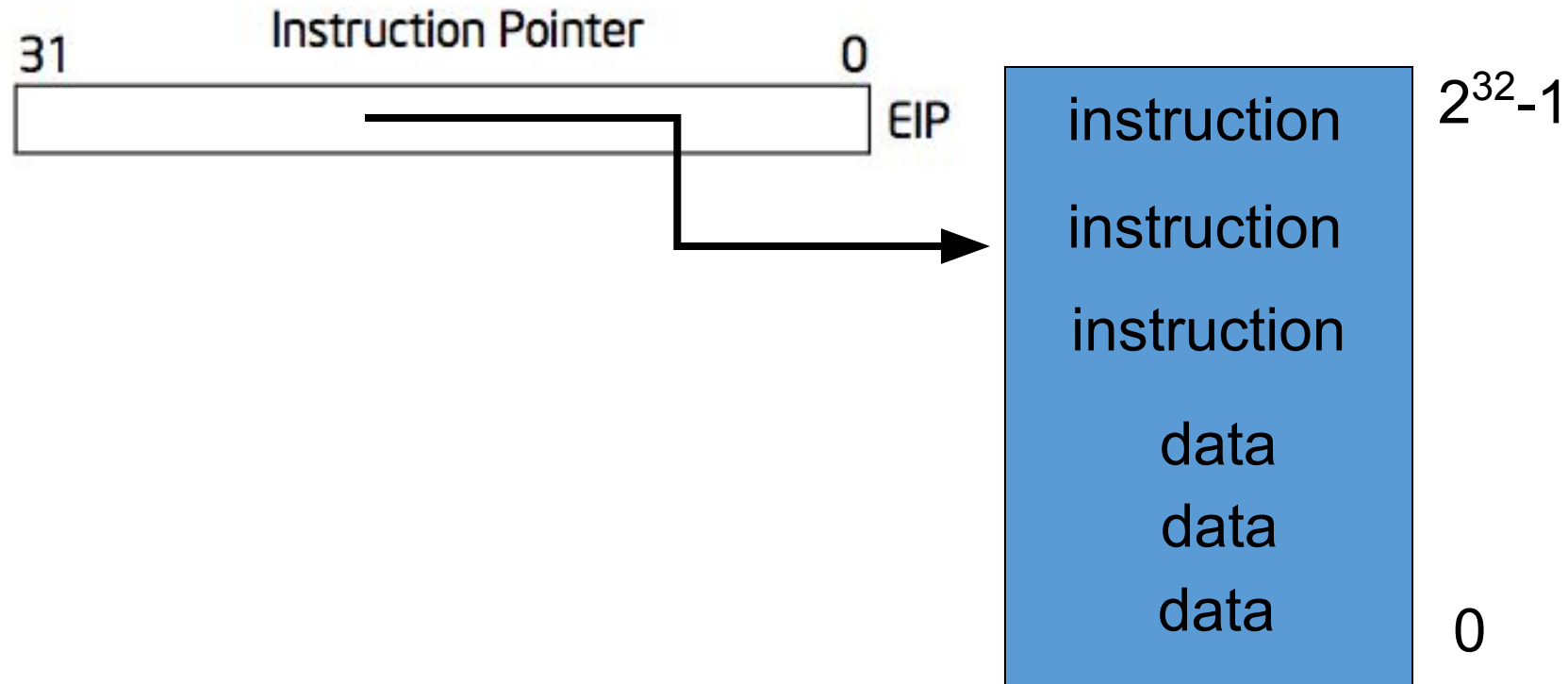
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# View from 5,000 Feet



# x86 implementation



- EIP is incremented after each instruction
- Instructions are different length
- EIP modified by CALL, RET, JMP, and conditional JMP

# Integer Registers (IA32)

				Origin (mostly obsolete)
general purpose	%eax	%ax	%ah   %al	<i>accumulate</i>
	%ecx	%cx	%ch   %cl	<i>counter</i>
	%edx	%dx	%dh   %dl	<i>data</i>
	%ebx	%bx	%bh   %bl	<i>base</i>
	%esi	%si		<i>source index</i>
	%edi	%di		<i>destination index</i>
	%esp	%sp		<i>stack pointer</i>
	%ebp	%bp		<i>base pointer</i>
16-bit virtual registers (backwards compatibility)				

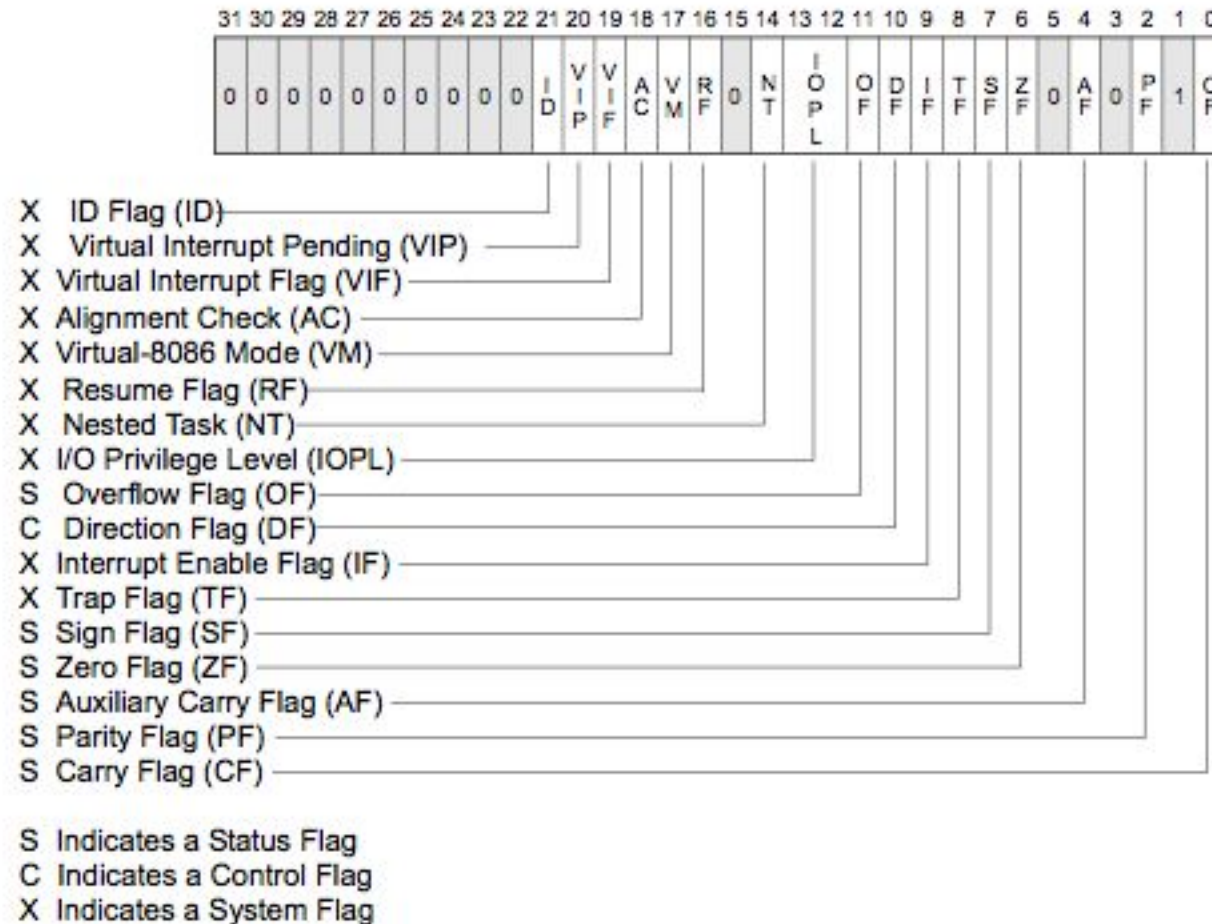
# x86-64 Integer Registers

<b>%rax</b>	<b>%eax</b>
<b>%rbx</b>	<b>%ebx</b>
<b>%rcx</b>	<b>%ecx</b>
<b>%rdx</b>	<b>%edx</b>
<b>%rsi</b>	<b>%esi</b>
<b>%rdi</b>	<b>%edi</b>
<b>%rsp</b>	<b>%esp</b>
<b>%rbp</b>	<b>%ebp</b>

<b>%r8</b>	<b>%r8d</b>
<b>%r9</b>	<b>%r9d</b>
<b>%r10</b>	<b>%r10d</b>
<b>%r11</b>	<b>%r11d</b>
<b>%r12</b>	<b>%r12d</b>
<b>%r13</b>	<b>%r13d</b>
<b>%r14</b>	<b>%r14d</b>
<b>%r15</b>	<b>%r15d</b>

- Extend existing registers. Add 8 new ones.
- Make **%ebp/%rbp** general purpose

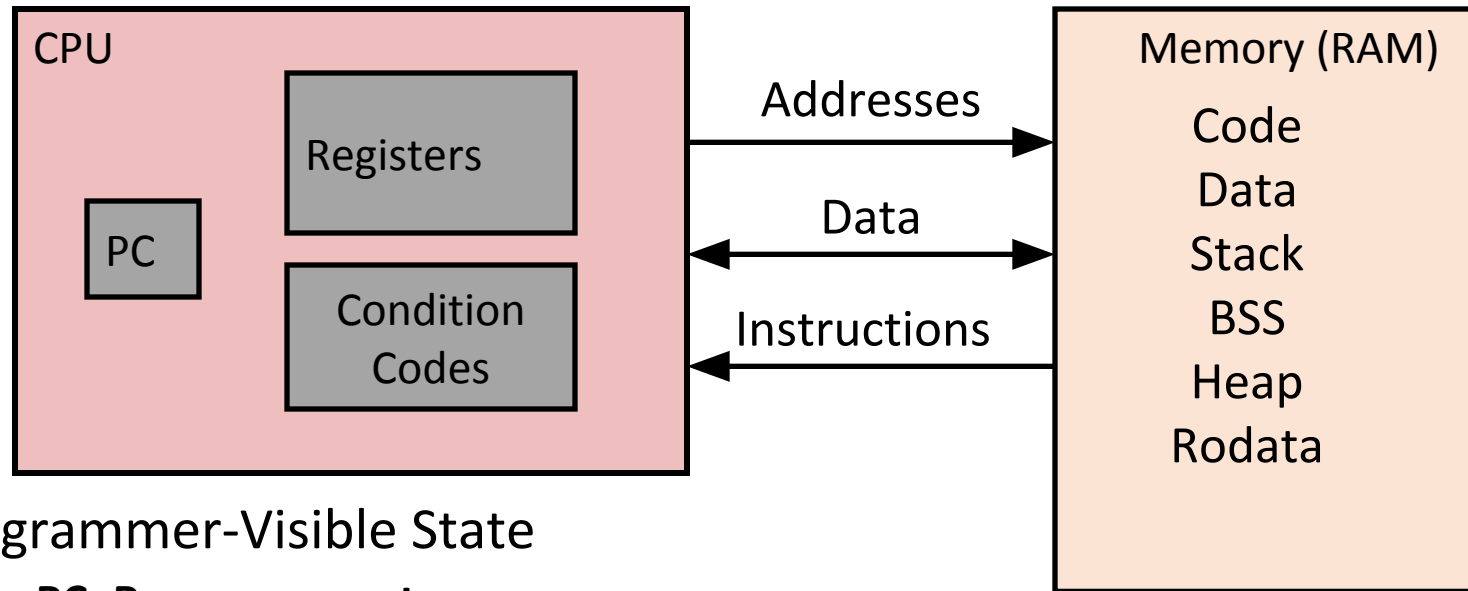
# EFLAGS register



- Test instructions: TEST EAX, 0
- Conditional JMP instructions: JNZ address



# Assembly Programmer's View



## Programmer-Visible State

- **PC: Program counter**

- Address of next instruction
- Called “EIP” (IA32) or “RIP” (x86-64)

- **Register file**

- Heavily used program data

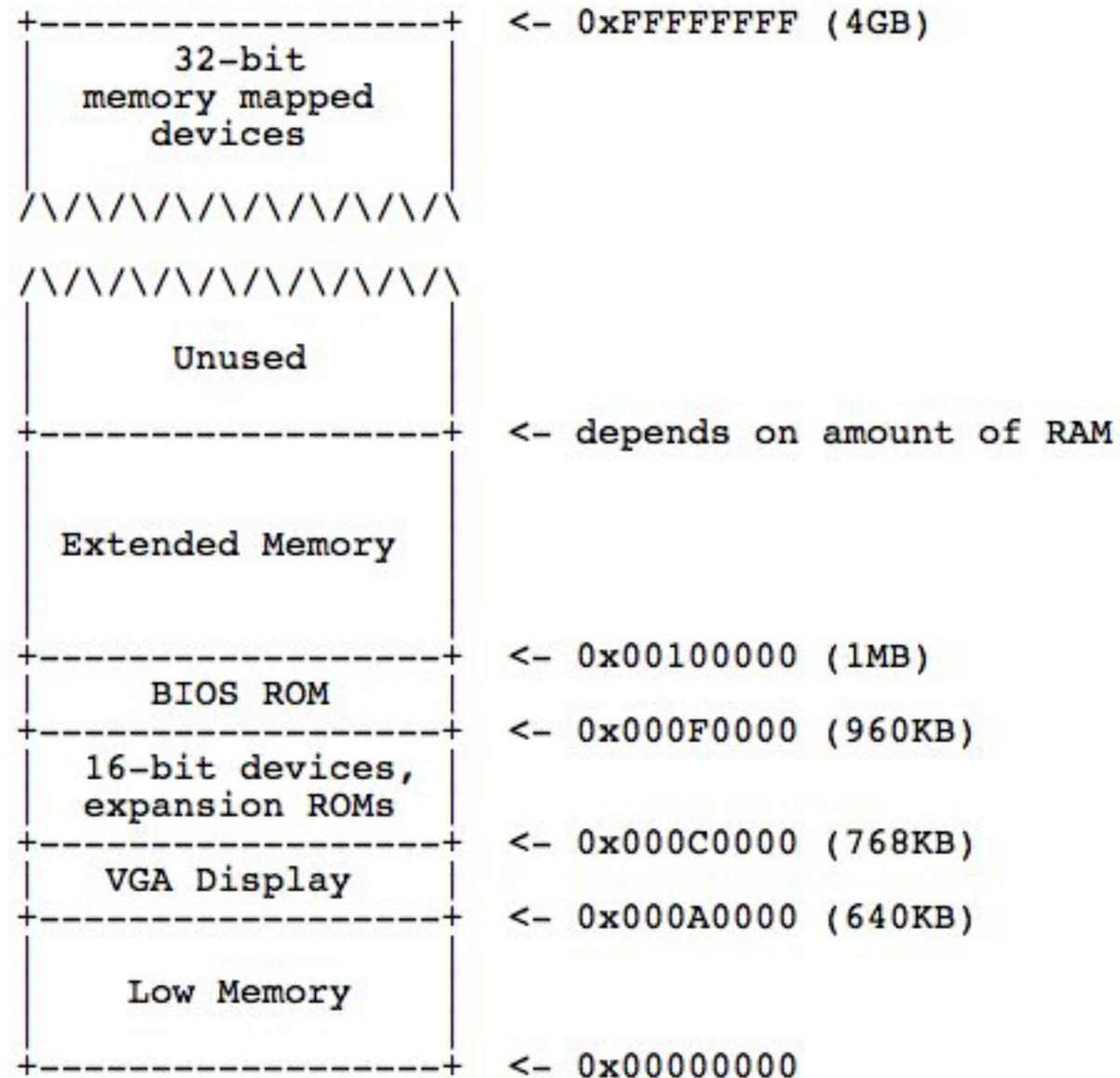
- **Condition codes**

- Store status information about most recent arithmetic operation
- Used for conditional branching

- **Memory**

- Byte addressable array
- Code and user data
- Stack to support procedures
- **Heap: Dynamic memory allocation (malloc(), calloc() etc.)**

# Physical memory layout



# x86 instruction set

- Instructions classes:
  - Data movement: MOV, PUSH, POP, LEA...
  - Arithmetic: TEST, SHL, ADD, MUL...
  - I/O: IN, OUT, ...
  - Control: JMP, JZ, JNZ, CALL, RET
  - String: MOVSB, ...
  - System: IRET, INT, SYSCALL

# x86 instruction set (Data movement)

- MOV , LEA

- MOV: Move (byte/word/long/long long) from Reg. to mem. / mem. to Reg. / Imm. to reg. / Imm. to mem.

Corresponding C syntax:

```
fun(){  
    int a=10;    //Imm. to mem.  
    ....  
}
```

- LEA: Load effective address to register (byte/word/long/long long) of mem. location to Reg.

Corresponding C syntax:

```
fun(){  
    int a=10;  
    int b;  
    b=&a;    // effective address of 'a' on the stack.  
    ....  
}
```

# x86 instruction set (Arithmetic)

- ADD, SUB, DIV, MUL, IMUL, etc.
  - Arithmetic operations (evident from the names).
  - Can use any of the general purposes registers or mem. loc. as the target (accumulator), where the result is saved.
  - Flags register (EFLAGS/RFLAGS) bits set to indicate, carry, overflow, sign etc.

add <reg>,<reg>

add <reg>,<mem>

add <mem>,<reg>

add <reg>,<imm>

add <imm>,<con>

addl %rax, %rbx

addw (%rcx), %ax

addq %rax, (%rsi)

add rbx, rax

add ax, [rcx]

add [rsi],rax

# x86 instruction set (I/O)

- IN, OUT

- Read/write bytes to hard ware device identified with address.

IN    Read from a port

OUT   Write to a port

INS/INSB   Input string from port/Input byte string from port

INS/INSW   Input string from port/Input word string from port

INS/INSD   Input string from port/Input doubleword string from port

OUTS/OUTSB   Output string to port/Output byte string to port

OUTS/OUTSW   Output string to port/Output word string to port

OUTS/OUTSD   Output string to port/Output doubleword string to port

# x86 instruction set (Control)

- JMP, JZ, JNZ, CALL, RET
  - Unconditional / conditional jump to an address, call a function (procedure) using its address (in code memory).

Instruction	Description
JMP <i>rel8</i>	Jump short, $RIP = RIP + 8\text{-bit displacement sign extended to 64-bits}$
JMP <i>rel16</i>	Jump near, relative, displacement relative to next instruction. Not supported in 64-bit mode.
JMP <i>rel32</i>	Jump near, relative, $RIP = RIP + 32\text{-bit displacement sign extended to 64-bits}$
JMP <i>r/m16</i>	Jump near, absolute indirect, address = zero-extended <i>r/m16</i> . Not supported in 64-bit mode.
JMP <i>r/m32</i>	Jump near, absolute indirect, address given in <i>r/m32</i> . Not supported in 64-bit mode.
JMP <i>r/m64</i>	Jump near, absolute indirect, $RIP = 64\text{-Bit offset from register or memory}$

# x86 instruction set (Control)

- CALL, RET

CALL <mem>/<reg>

RET

Equivalent to:

Equivalent to:

push eip

pop <reg\_1>

jmp <mem>/<reg>

jmp <reg\_1>



# x86 instruction set (System)

- IRET

- Return from an interrupt handler
- During interrupt handling, the flags are saved on the stack.  
IRET restores the flags from the stack.

- INT

- Software interrupt instruction (aka *trap*).
- Emulates interrupt and jumps to interrupt handler.

INT <int\_num>

- SYSCALL

- System call interrupt handler (added in X86\_64).
- Software interrupt specifically for system call interrupt (aka *trap*).
- System call interrupt handler number identified via registers.