MEHRAN UNIVERSITY OF ENGINEERING AND TECHNOLOGY, JAMSHORO
DEPARTMENT OF ELECTRONIC ENGINEERING

FPGA Based Digital Design (ES-373)
Batch: 20ES (6th Semester)

Lab Experiment #04
Simulation of Basic Digital Logic Circuits using ISIM

Name KARAN	**Roll #** 20ES062
Signature of Lab Tutor	**Date**

RUBRICS:

Performance Metric	TEAMWORK	PARTICIPATION	CONDUCTING EXPERIMENT	USE OF MODERN ENGINEERING TOOLS	DATA ANALYSIS	CALCULATION AND CODING	OBSERVATION/ PROGRAM RESULTS	**Total Score**
	0.5	**0.5**	**1**	**1**		**1**	**1**	**05**
Obtained								

OBJECTIVE(S)

#	Topic	# Of Lectures	CLO	Taxonomy level
1	The purpose of this lab is to simulate Logic circuits using Xilinx ISE ISIM simulator.	3	4,5	P3, A4

OUTCOME(S)

a. An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	**PL-5**: Modern Tool Usage
b. An ability to communicate effectively	**PLO10**: Communication

LAB REQUIREMENTS:

- Standard PC with Xilinx ISE Design Suite 12.3 or latest, Software installed.
- Digilent Adept Software.
- Xilinx ISE compatible board such as NEXYS4, NEXYS3, NEXYS2, OR BASYS2

DISCUSSION:

✓ Simulation:

Simulation is the process of testing the logical or processing functionality of designed logic. Several kinds of Software and hardware Tools to provide this functionality. With Xilinx ISim Simulator you can simulate your design by writing "Test benches" and/or by assigning Manual wave flows to inputs and check functionality of outputs after simulation.

The Xilinx ISE Design Suite provides an integrated flow with the Mentor ModelSim simulator and the Xilinx ISim simulator that allows simulations to be run from the Xilinx Project Navigator.

➢ Behavioral Simulation (For NAND Gate):

After Creating New project and New source File now it is ready to simulate our design.to simulate the Design follow the following steps.

i. In the Design Panel, select the **Simulation** radio button. The Simulation type drop-down list appears.

ii. Select gate_logic_Behavioral file (**figure 1**) and double click on Simulator Behavioral Model in the Process window, following ISim window (**Figure 2**) will appear.

Some features of this window include:

1. A Source Files panel where source files to be viewed can be selected
2. An Objects panel where different signals can be added to the simulation
3. A simulation panel where the state of signals can be observed
4. A Console panel

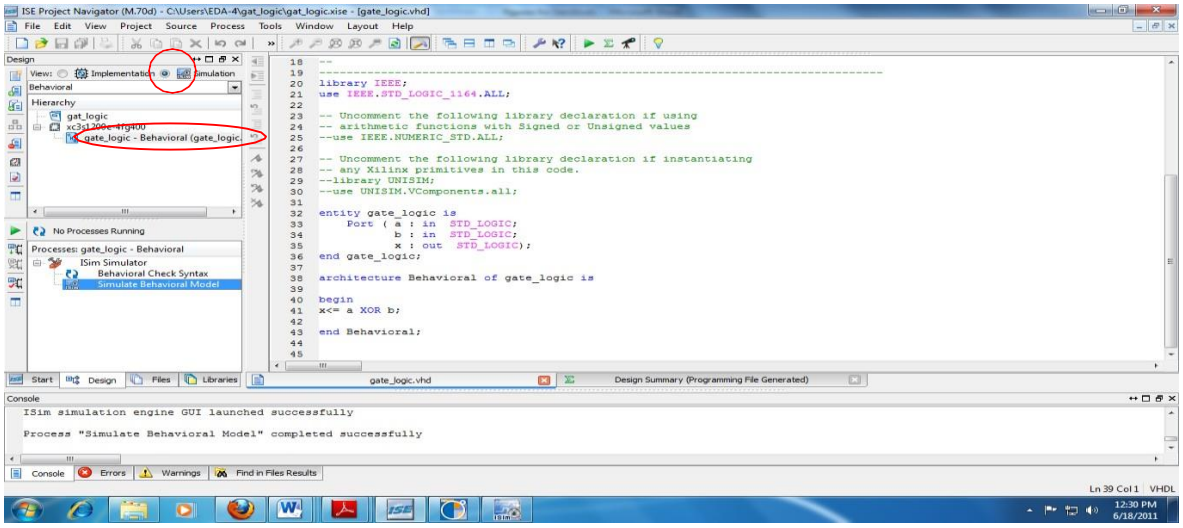


Figure 1: Behavioral Simulation Process

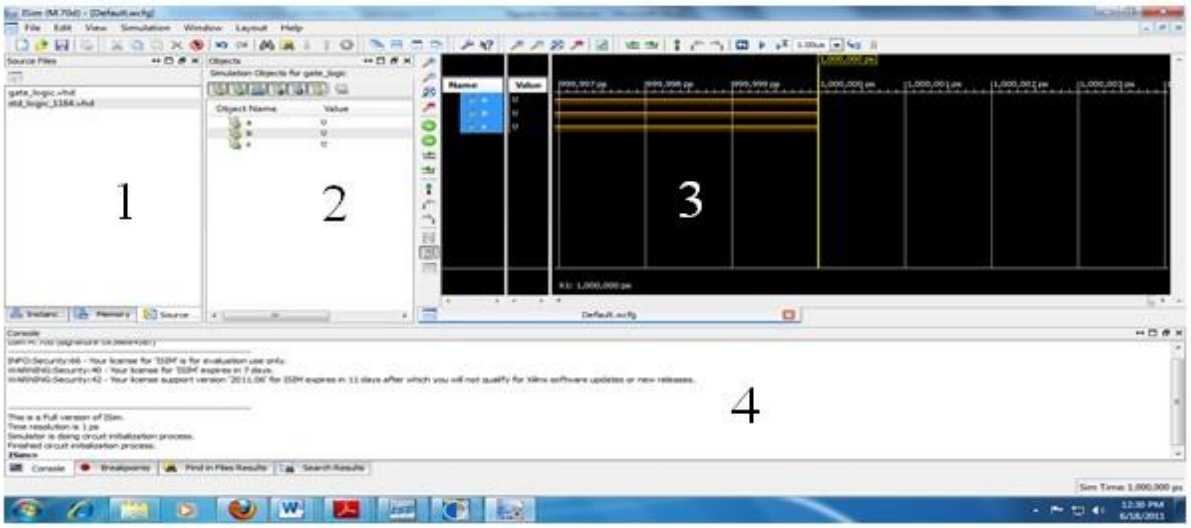


Figure 2: ISim window

- Select the Simulation from the menu bar and click on Restart as shown in following **figure 3**. After clicking on Restart window (**figure 4**) will appear.

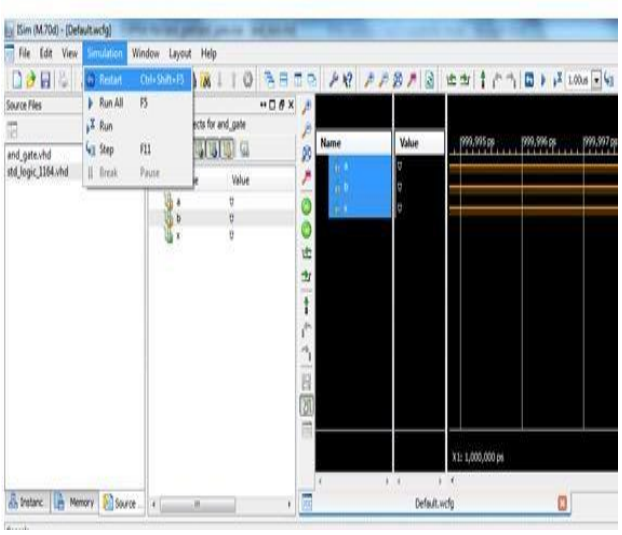


Figure 3: ISim window- Simulation Process

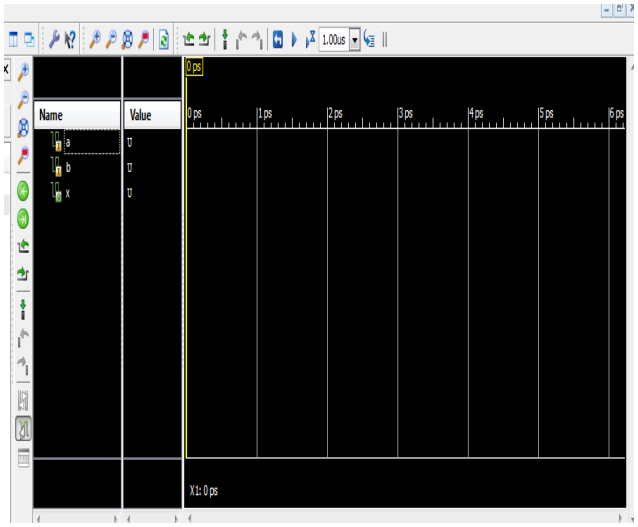


Figure 4: Simulation Process-**After Restart**

- To force the input signal (a & b) by an alternating pattern (clock), Right click on the input port "**a**" (**figure 5**) and select the Force clock.

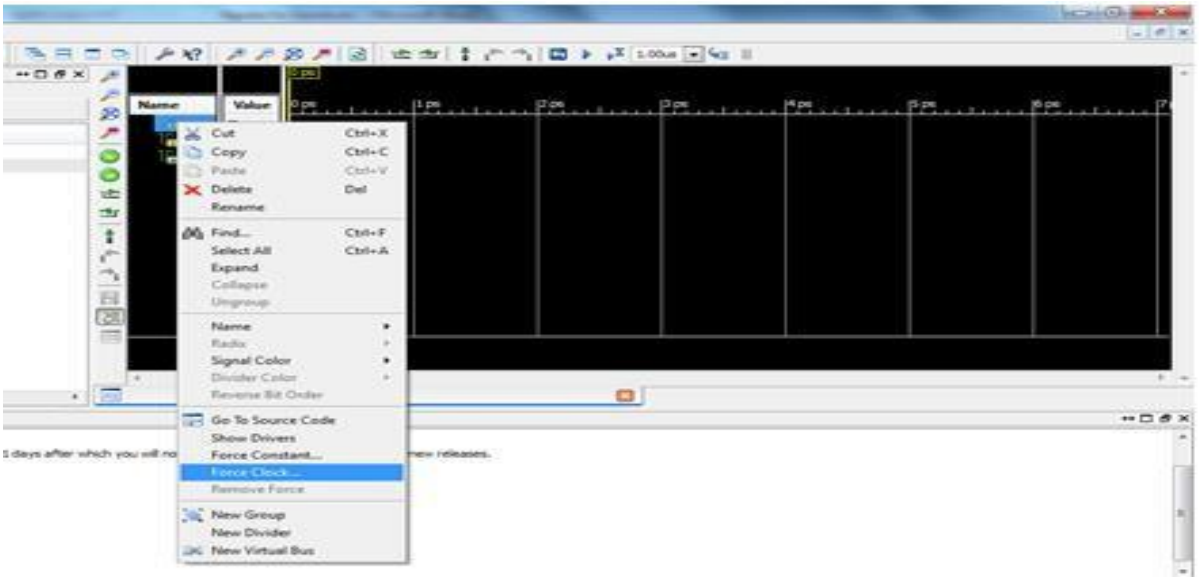


Figure 5: Simulation Process-**Assigning clock input**

- Enter the following parameter (**figure 6**). Click on apply and OK.
  - Leading Edge Value: **1/0**
  - Trailing Edge Value: **1/0**
  - Starting at the time offset: 0
  - Cancel after the time offset: **100, 200, … or can be left blank**
  - Duty cycle (%): **10, 20, 30 ,……upto 100**
  - Period: **100**

Similarly, Right click on the input port "**b**" (**figure 6**), select the Force clock and set the parameter.

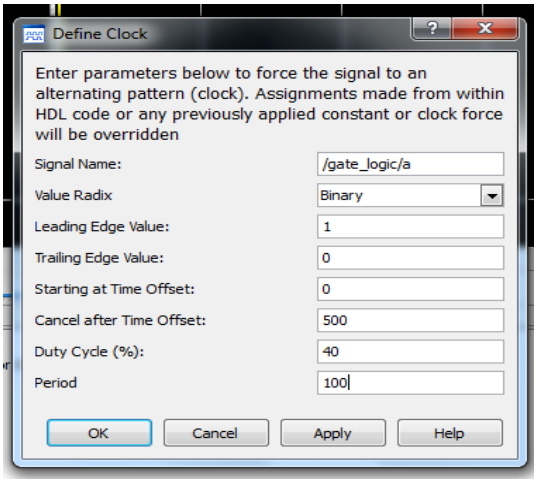


Figure 6: Force the Signal- **Enter Parameter**

- Select the Simulation from the menu bar and click on Run as shown in following **figure 7**. After click on Run following waveform window (**figure 8**) will appear.

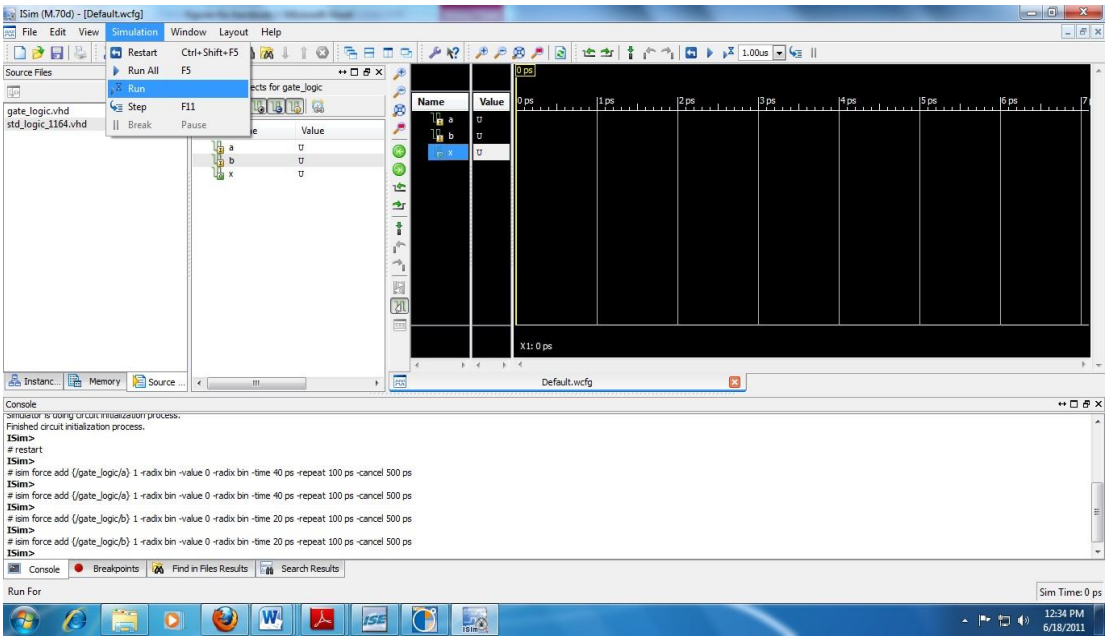


Figure 7: Force the Signal- **Run the process**

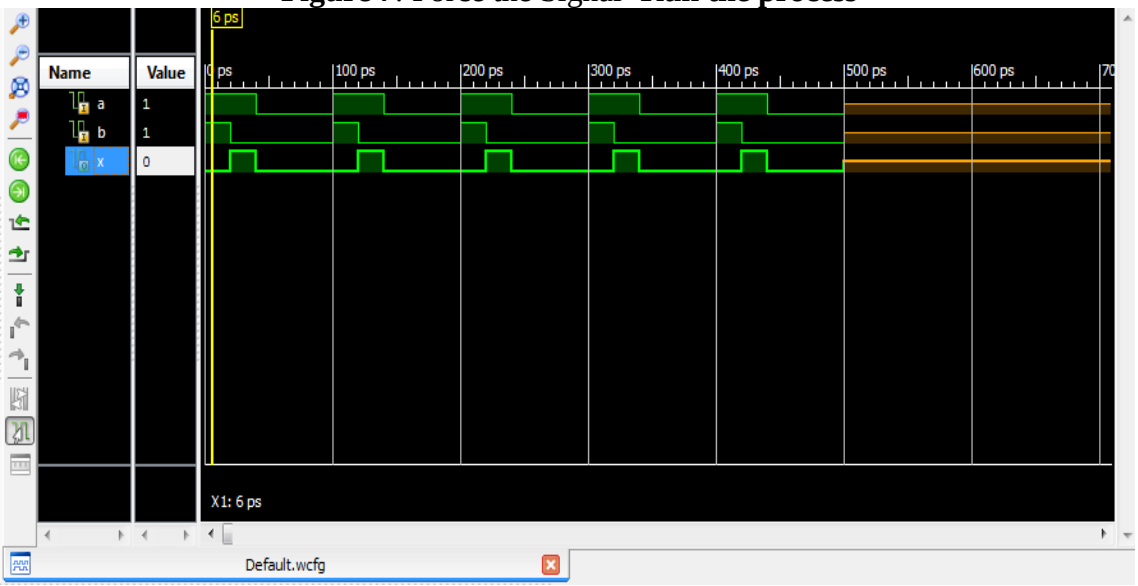
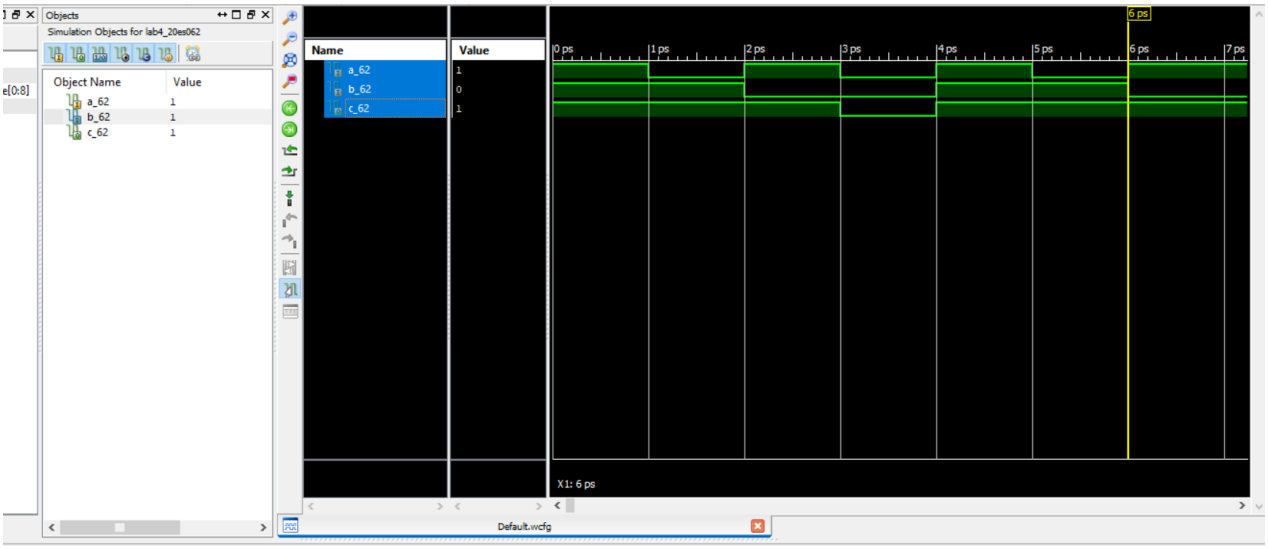


Figure 8: Behavioral Simulation- Output Waveform **Result**

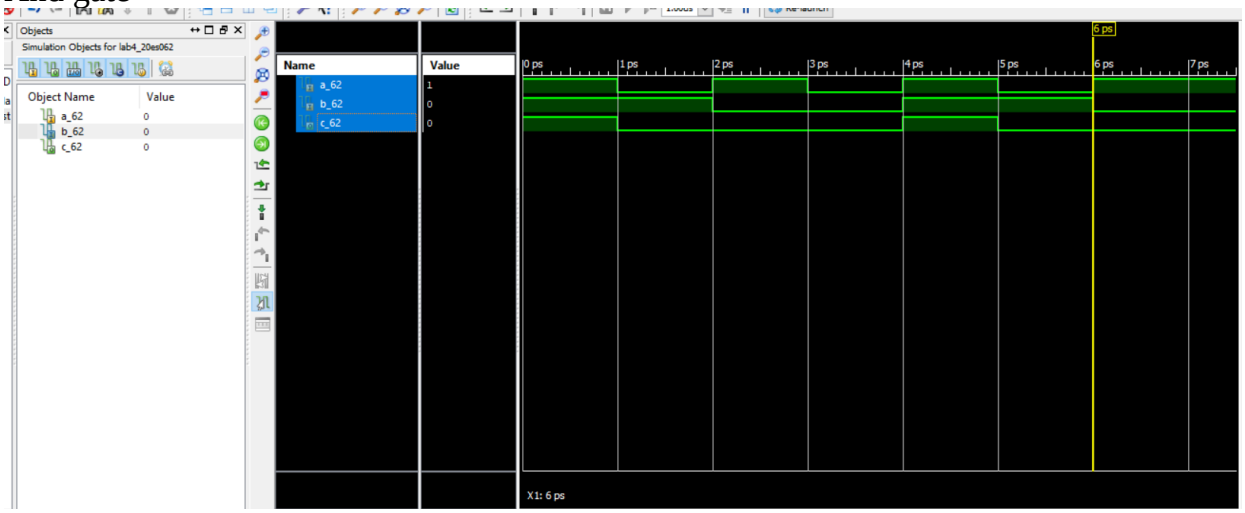
Review Questions:

- ✓ Repeat the same Exercise for all Logical Gates.

OR gate simulation

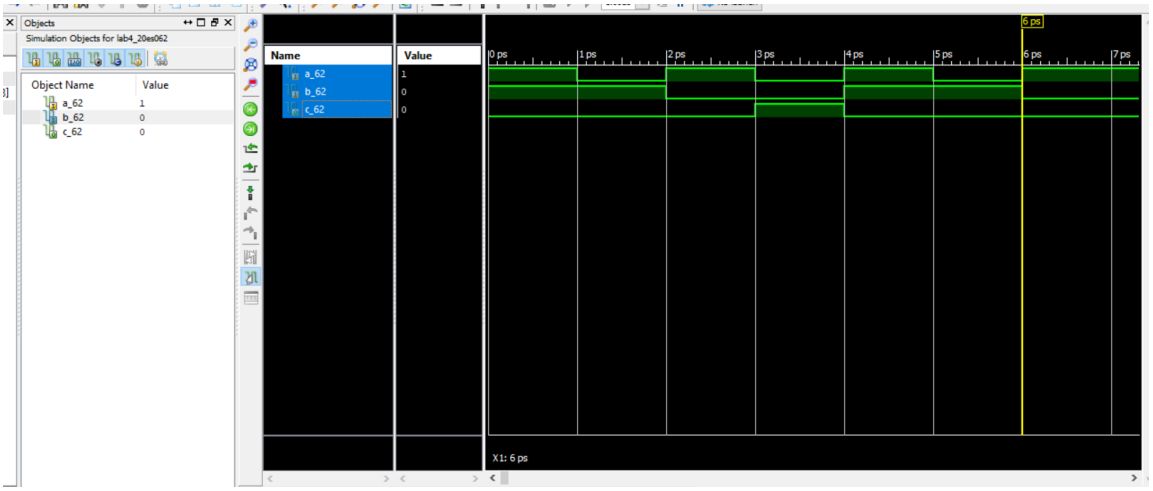


And gate

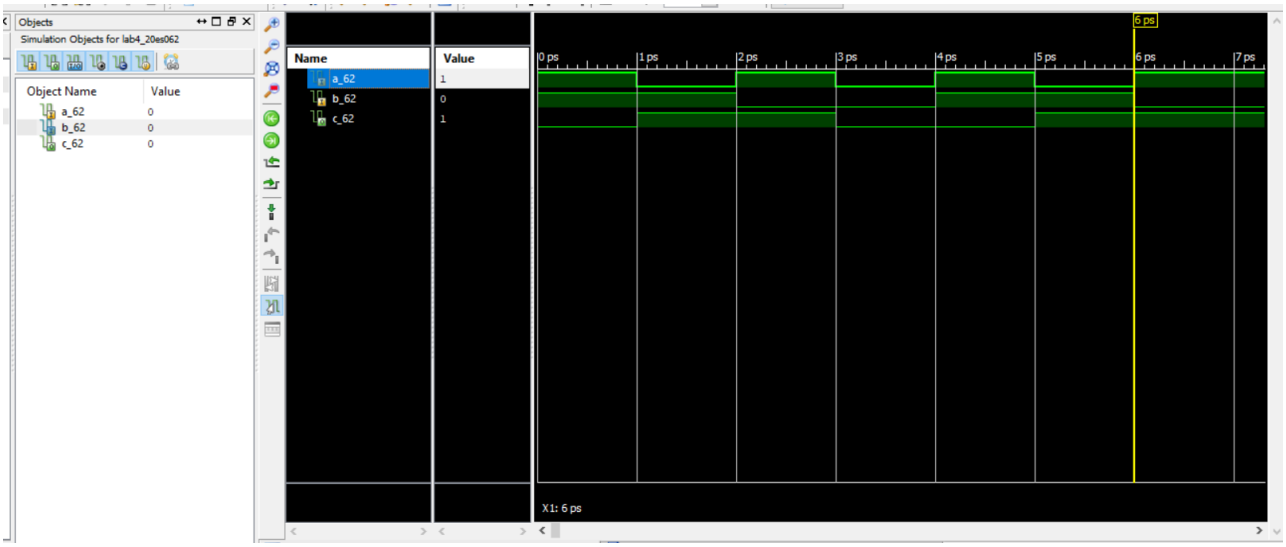


Nand gate

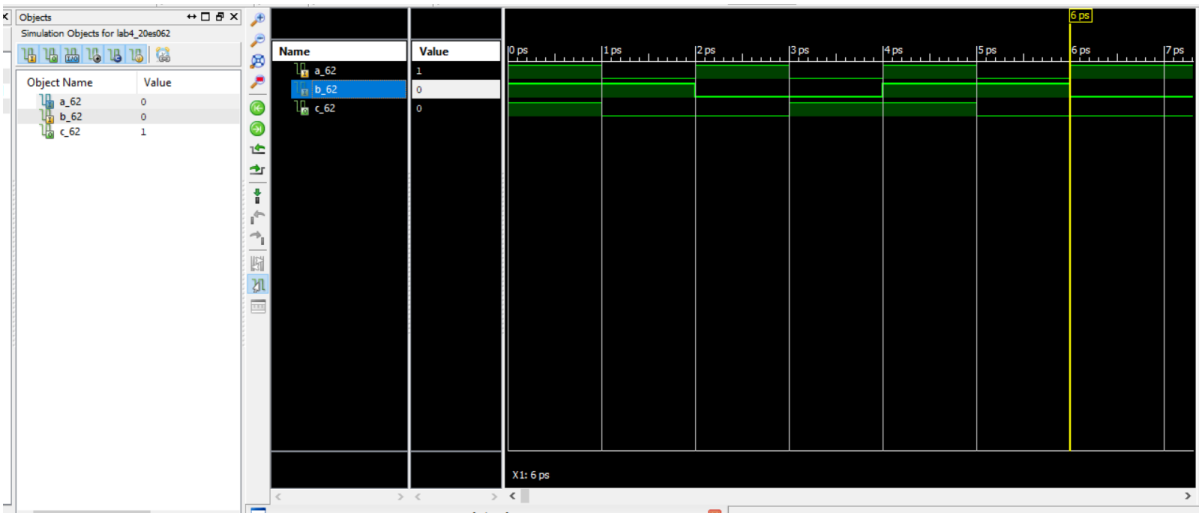
Nor gate



Xor :-

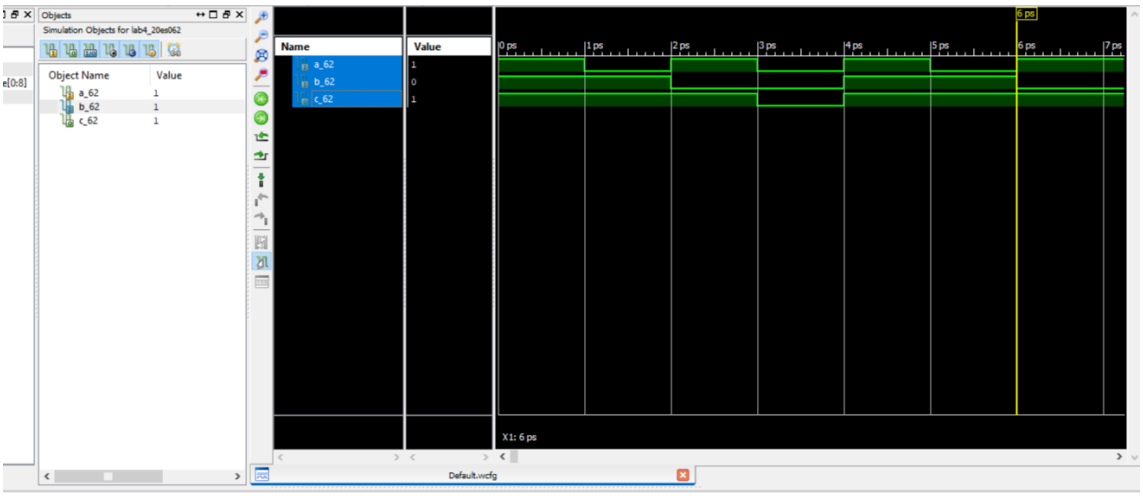


XNOR :-

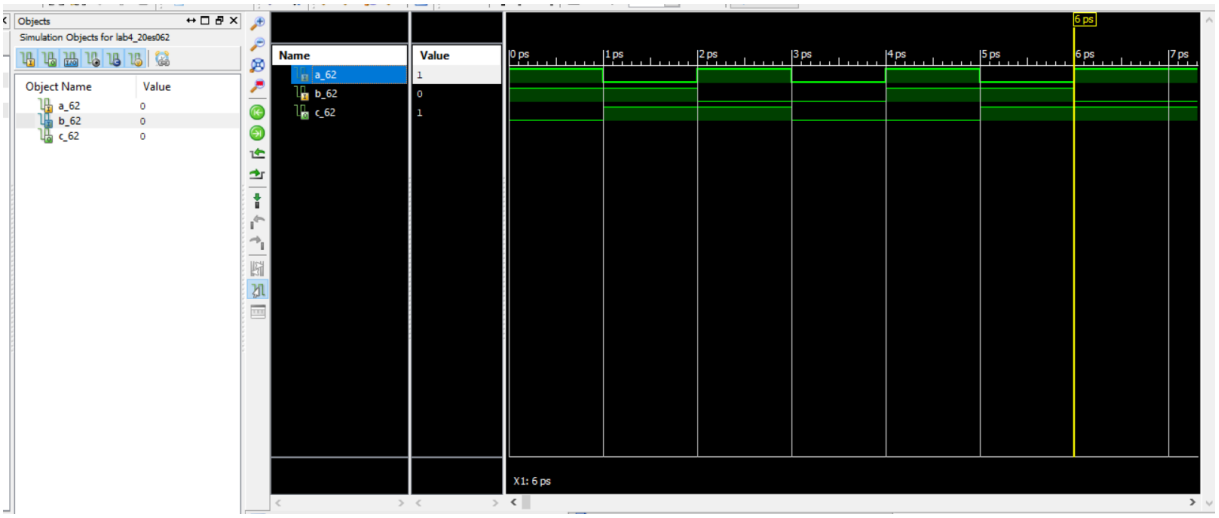


simulation results for OR, XOR, and NAND gates.

OR gate



XOR gate :-



Nand gate :-

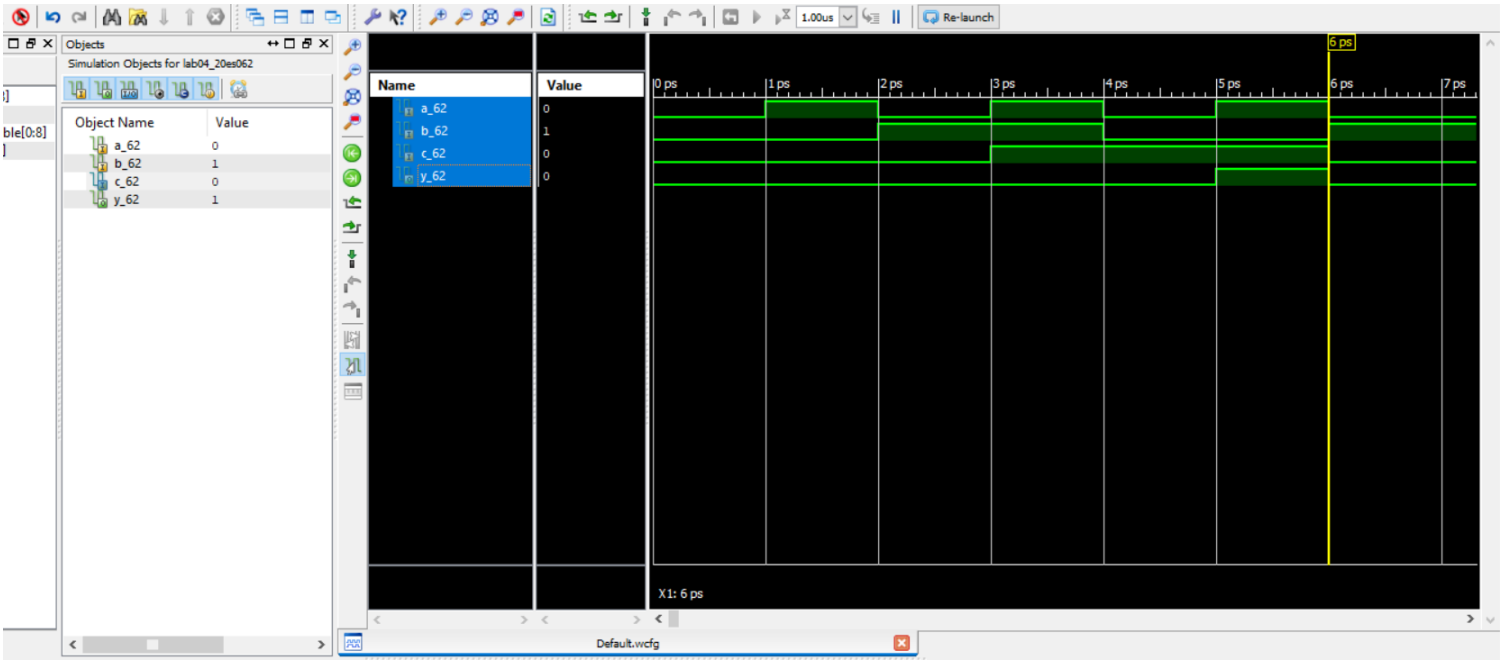
$Y = \bar{A}BC + A\bar{B}C + AB\bar{C}$

Code :-

```
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity lab04_20es062 is
    Port ( A_62 : in  STD_LOGIC;
           B_62 : in  STD_LOGIC;
           C_62 : in  STD_LOGIC;
           Y_62 : out  STD_LOGIC);
end lab04_20es062;

architecture Behavioral of lab04_20es062 is

begin
Y_62<=(((NOT A_62)AND B_62 AND C_62) OR (A_62 AND(NOT B_62) AND C_62) OR (A_62 AND B_62 AND (NOT C_62)));

end Behavioral;
```

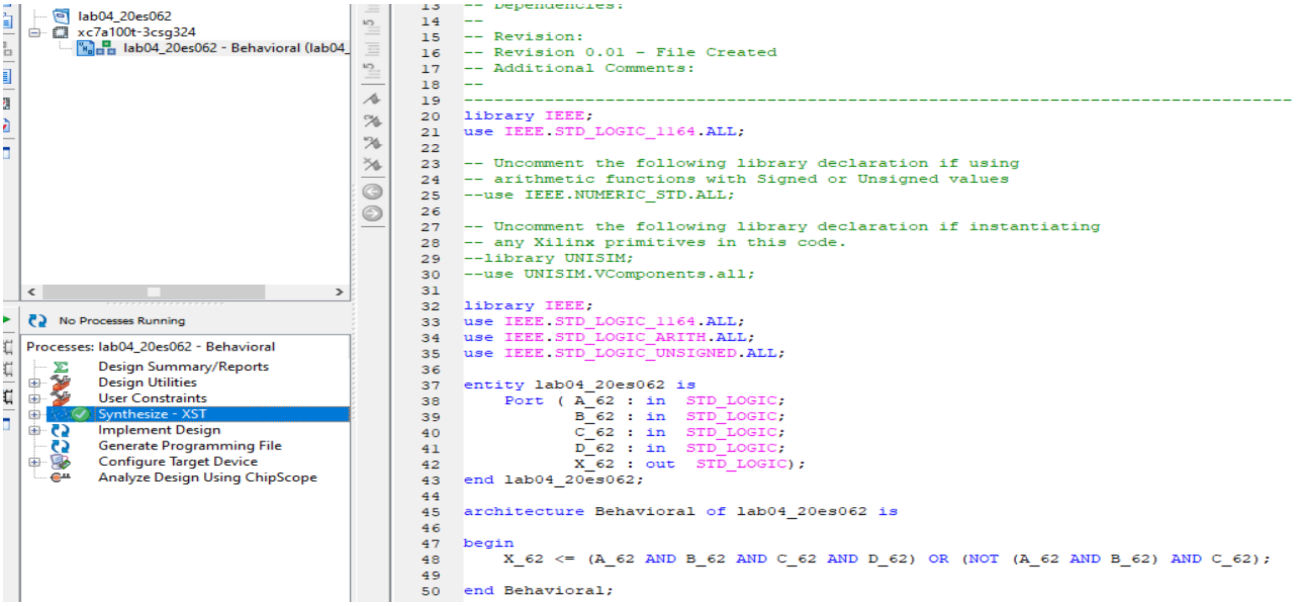
$Y = \bar{A}BC + A\bar{B}C + AB\bar{C}$

Simulation :-



$X = ABCD + \bar{A}\bar{B}C$

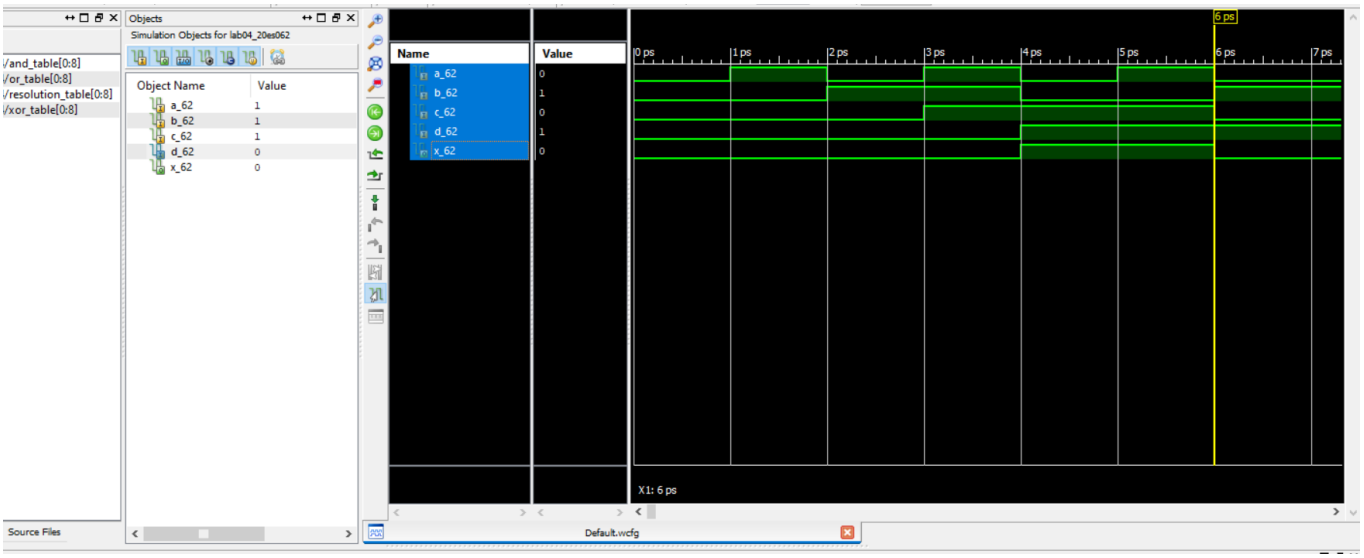
Code :-



```
lab04_20es062
xc7a100t-3csg324
lab04_20es062 - Behavioral (lab04_
No Processes Running
Processes: lab04_20es062 - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity lab04_20es062 is
    Port ( A_62 : in  STD_LOGIC;
           B_62 : in  STD_LOGIC;
           C_62 : in  STD_LOGIC;
           D_62 : in  STD_LOGIC;
           X_62 : out  STD_LOGIC);
end lab04_20es062;

architecture Behavioral of lab04_20es062 is

begin
    X_62 <= (A_62 AND B_62 AND C_62 AND D_62) OR (NOT (A_62 AND B_62) AND C_62);

end Behavioral;
```

$X = ABCD + \bar{A}\bar{B}C$
Simulation :-



Final Assignment:

1. Generate the simulation results for OR, XOR, and NAND gates.

2. Write VHDL codes and generate simulation results for following Boolean expressions.

   - ✓ $Y = \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$
   - ✓ $X = ABCD + \bar{A}B$