INPUT_SIGNAL

R2
Res1
100000K

V1
VSIN

U1
AD711JRZ

7

−

+

6

R3
Res1
1K

+1.25V

V2
VSRC

R4
Res1
1K

R5
Res1
4K

R1
Res1
4K

U2
AD711JRZ

7

−

+

6

OUTPUT_SIGNAL

R7
Res1
200

+15V

V4
VSRC

−15V

V3
VSRC

Title		
Size	Number	Revision
A4		
Date:	02.04.2019	Sheet of
File:	D:\pavel\..\DAC_TEST.SchDoc	Drawn By: