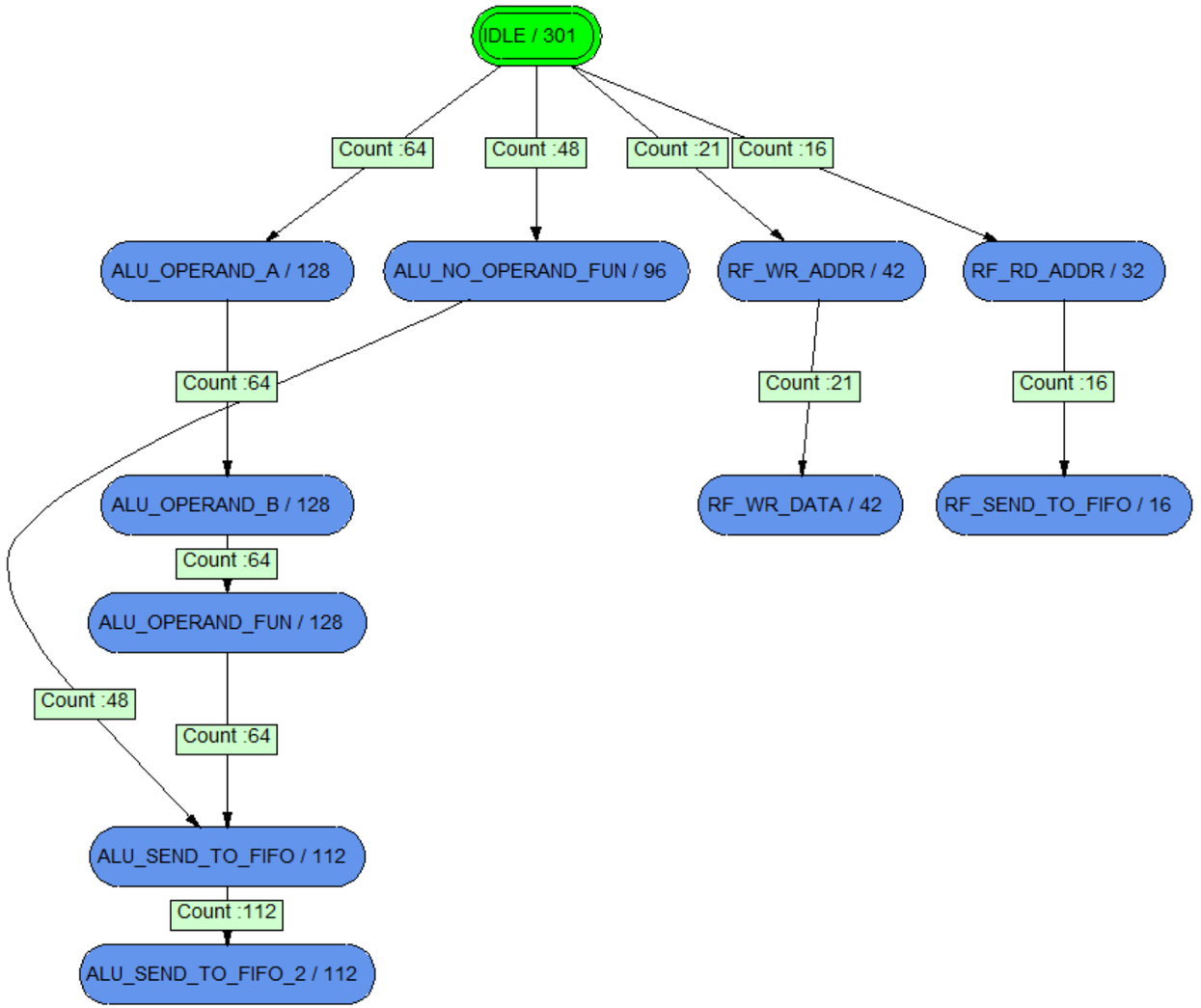
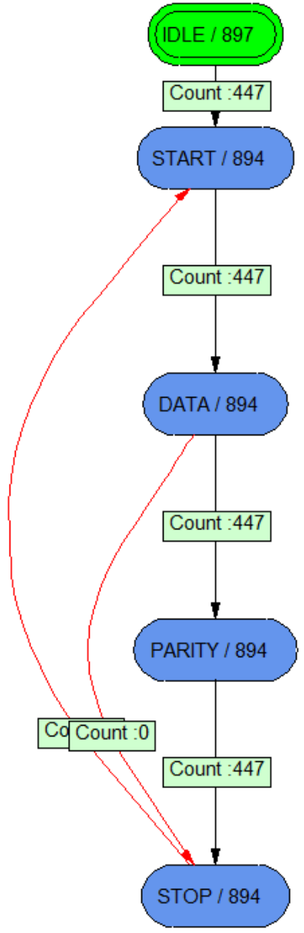
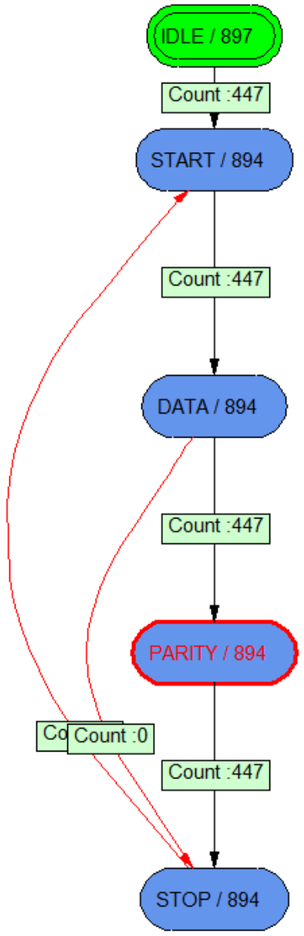
sim:/SYS_TOP_tb/SYS_TOP/SYS_CTRL/cs - Default

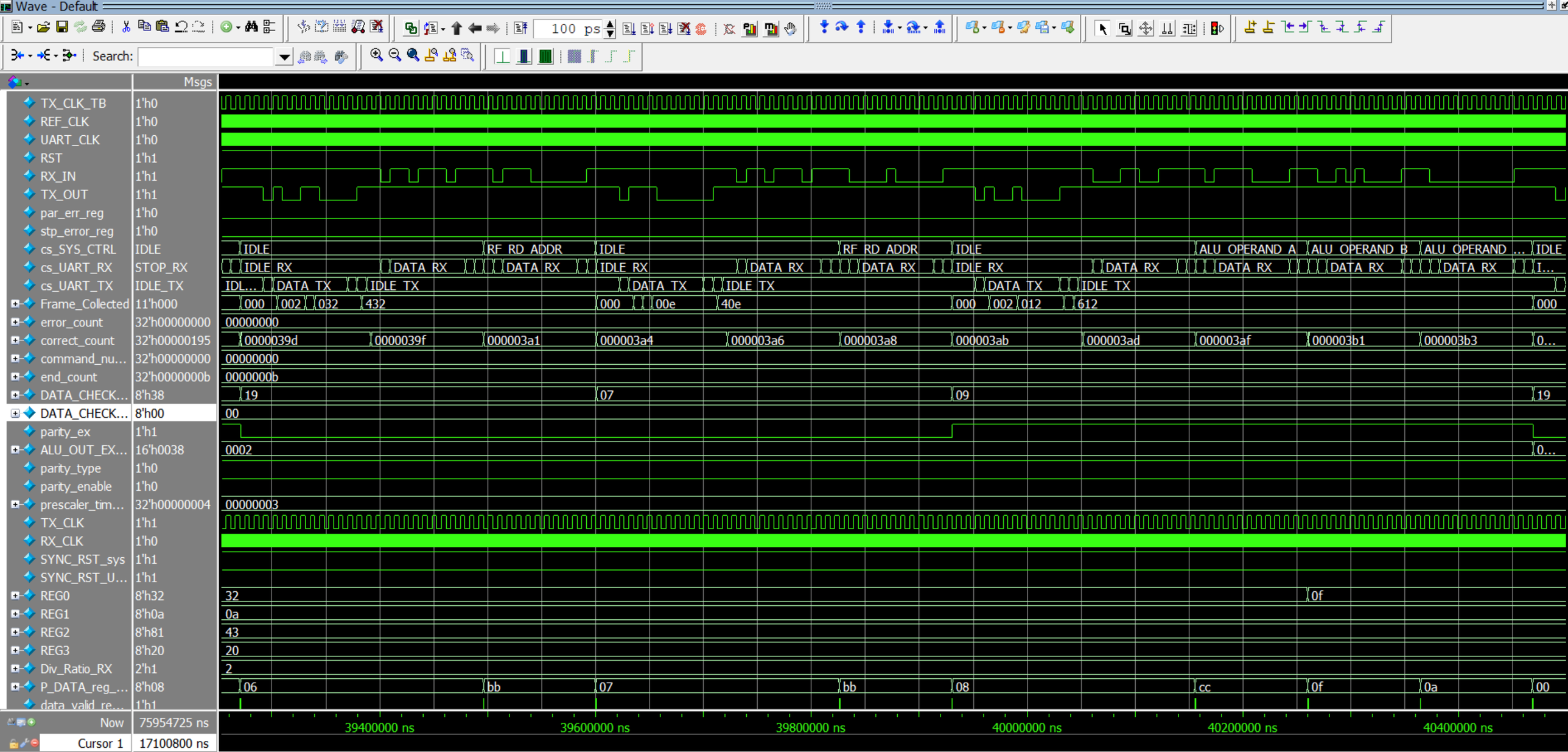


sim:/SYS_TOP_tb/SYS_TOP/RX/fsm/cs - Default

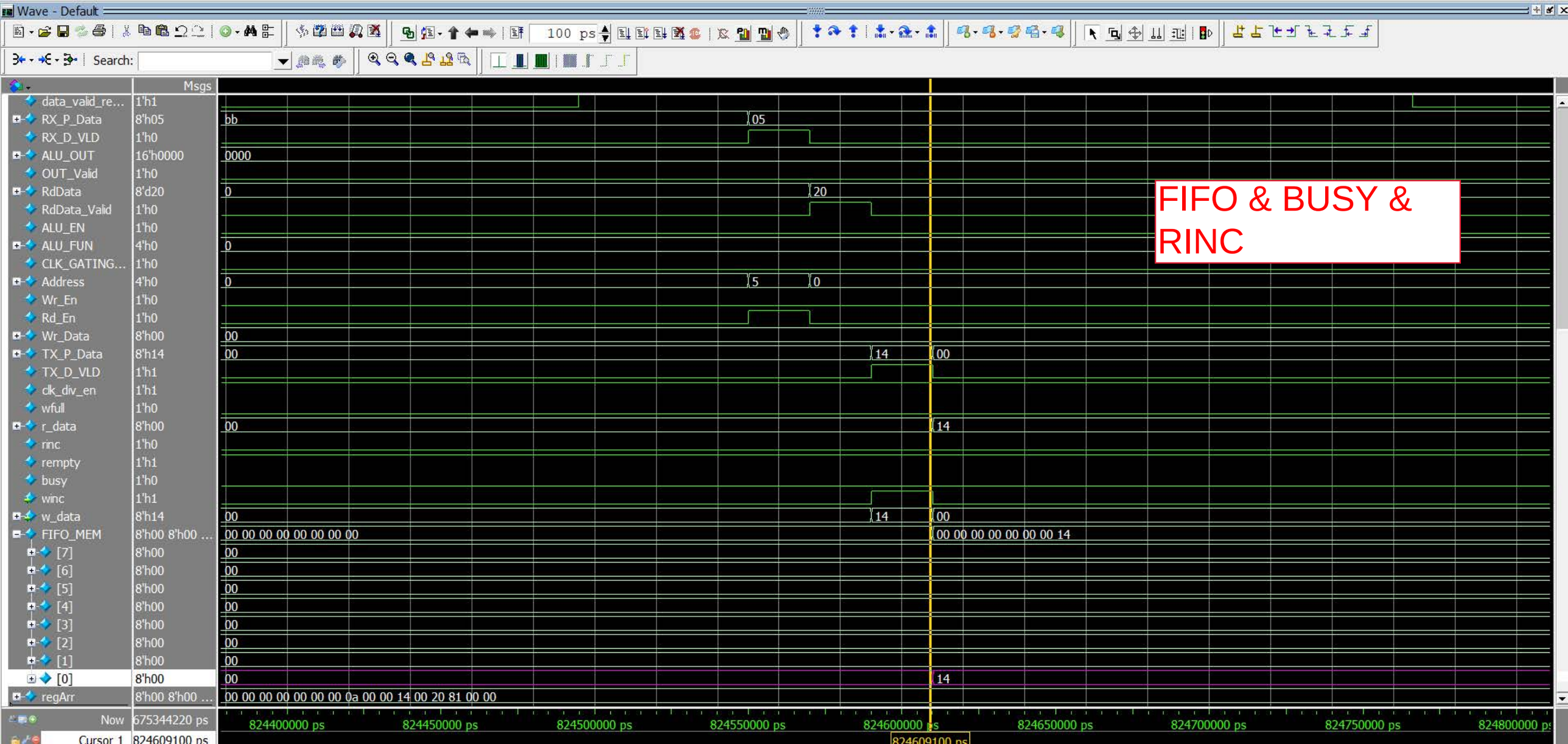


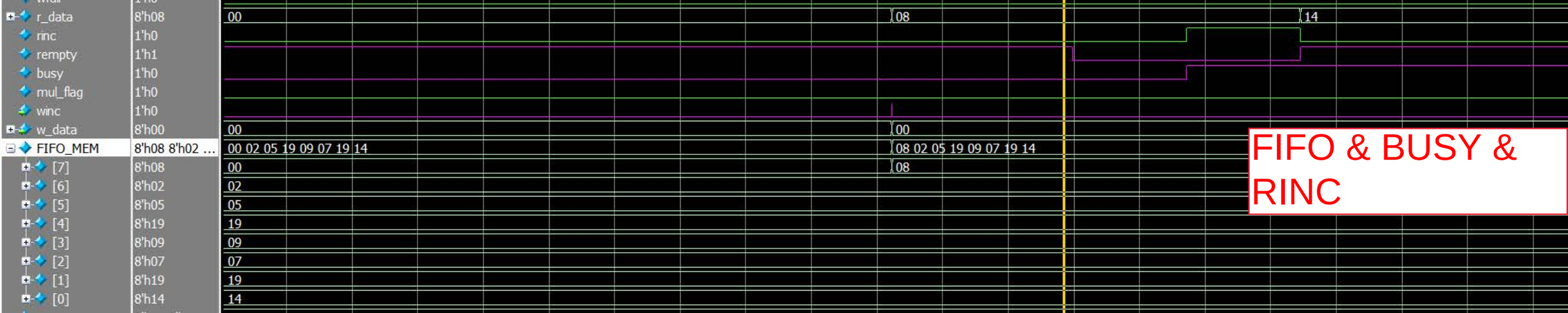
sim:/SYS_TOP_tb/SYS_TOP/RX/fsm/cs - Default

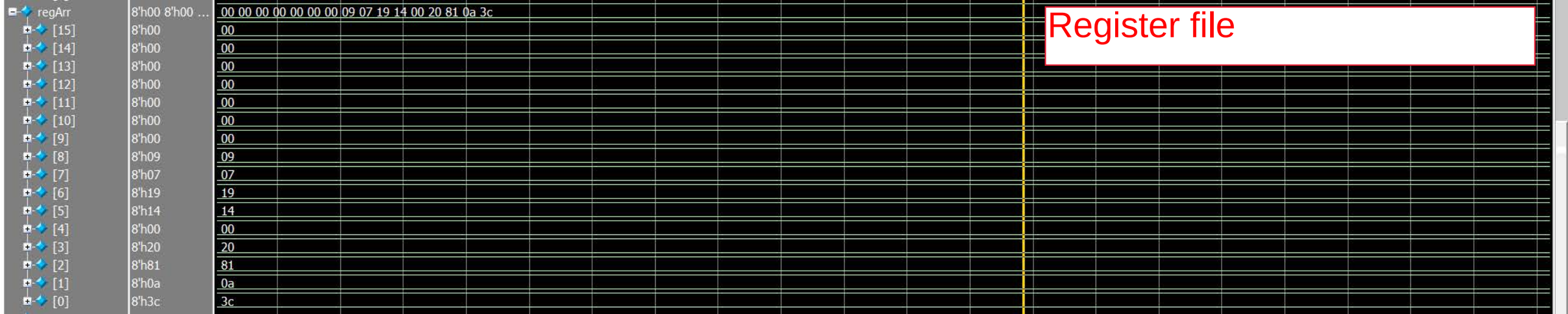



Wave - Default
Search:
Msgs
TX_CLK_TB 1'h0
REF_CLK 1'h0
UART_CLK 1'h0
RST 1'h1
RX_IN 1'h1
TX_OUT 1'h1
par_err_reg 1'h0
stp_error_reg 1'h0
cs_SYS_CTRL IDLE
cs_UART_RX STOP_RX
cs_UART_TX IDLE_TX
Frame_Collected 11'h000
error_count 32'h00000000
correct_count 32'h00000195
command_nu... 32'h00000000
end_count 32'h0000000b
DATA_CHECK... 8'h38
DATA_CHECK... 8'h00
parity_ex 1'h1
ALU_OUT_EX... 16'h0038
parity_type 1'h0
parity_enable 1'h0
prescaler_tim... 32'h00000004
TX_CLK 1'h1
RX_CLK 1'h0
SYNC_RST_sys 1'h1
SYNC_RST_U... 1'h1
REG0 8'h32
REG1 8'h0a
REG2 8'h81
REG3 8'h20
Div_Ratio_RX 2'h1
P_DATA_reg_... 8'h08
data_valid_re... 1'h1
IDLE
RF_RD_ADDR
ALU_OPERAND_A
ALU_OPERAND_B
ALU_OPERAND_...
IDLE_RX
DATA_RX
IDL...
DATA_TX
IDLE_TX
000
002
032
432
00e
40e
012
612
00000000
0000039d
0000039f
000003a1
000003a4
000003a6
000003a8
000003ab
000003ad
000003af
000003b1
000003b3
0000000b
19
07
09
00
0002
00000003
32
0f
0a
43
20
2
06
bb
08
cc
Now
75954725 ns
Cursor 1
17100800 ns
39400000 ns
39600000 ns
39800000 ns
40000000 ns
40200000 ns
40400000 ns

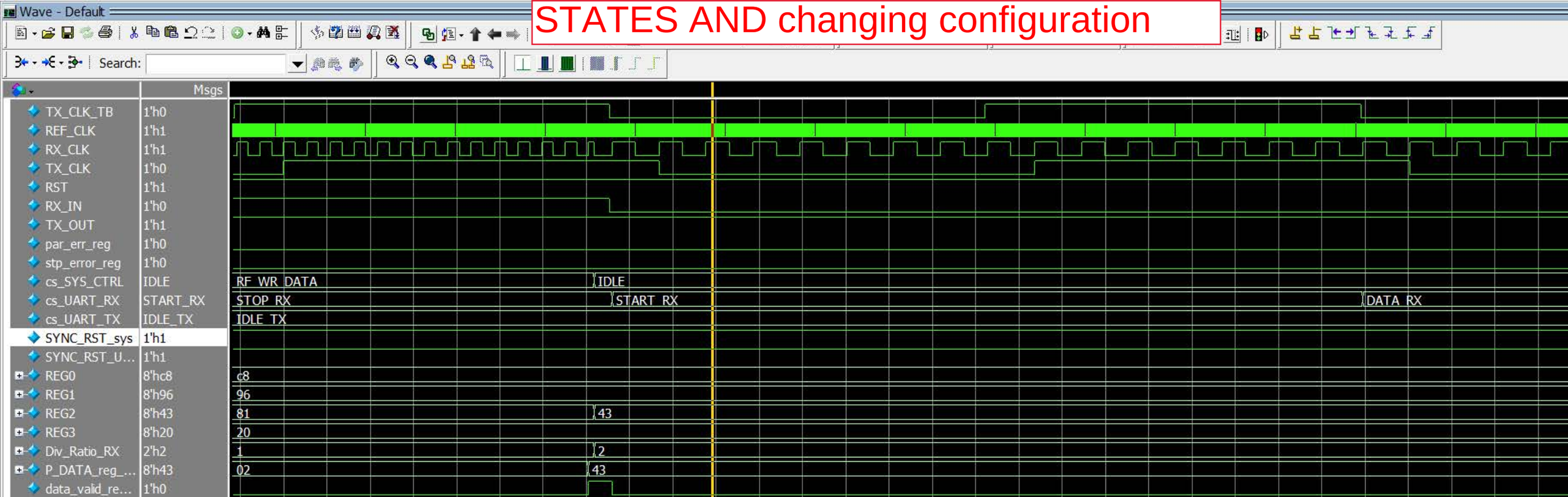

Div_Ratio_RX
2'h1
P_DATA_reg_...
8'haa
data_valid_re...
1'h1
RX_P_Data
8'haa
RX_D_VLD
1'h1
ALU_OUT
16'h0000
OUT_Valid
1'h0
RdData
8'h00
1
00
aa
00
aa
0000
00
RX_RECEIVE THEN THROUGH DATA SYNC TO SYS_CTRL

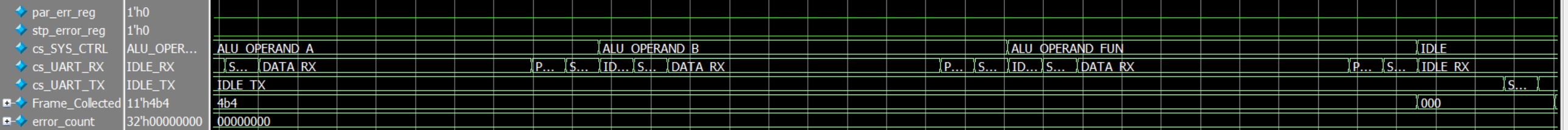

Wave - Default
Search:
Msgs
data_valid_re... 1'h1
RX_P_Data 8'h05
RX_D_VLD 1'h0
ALU_OUT 16'h0000
OUT_Valid 1'h0
RdData 8'd20
RdData_Valid 1'h0
ALU_EN 1'h0
ALU_FUN 4'h0
CLK_GATING... 1'h0
Address 4'h0
Wr_En 1'h0
Rd_En 1'h0
Wr_Data 8'h00
TX_P_Data 8'h14
TX_D_VLD 1'h1
clk_div_en 1'h1
wfull 1'h0
r_data 8'h00
rinc 1'h0
rempty 1'h1
busy 1'h0
winc 1'h1
w_data 8'h14
FIFO_MEM 8'h00 8'h00 ...
[7] 8'h00
[6] 8'h00
[5] 8'h00
[4] 8'h00
[3] 8'h00
[2] 8'h00
[1] 8'h00
[0] 8'h00
regArr 8'h00 8'h00 ...
00 00 00 00 00 00 00 00 0a 00 00 14 00 20 81 00 00
FIFO & BUSY & RINC
Now 675344220 ps
Cursor 1 824609100 ps
824400000 ps
824450000 ps
824500000 ps
824550000 ps
824600000 ps
824650000 ps
824700000 ps
824750000 ps
824800000 ps


r_data 8'h08
rinc 1'h0
rempty 1'h1
busy 1'h0
mul_flag 1'h0
winc 1'h0
w_data 8'h00
FIFO_MEM 8'h08 8'h02 ...
[7] 8'h08
[6] 8'h02
[5] 8'h05
[4] 8'h19
[3] 8'h09
[2] 8'h07
[1] 8'h19
[0] 8'h14
00
08
14
00
00
00 02 05 19 09 07 19 14
08 02 05 19 09 07 19 14
00
08
02
05
19
09
07
19
14
FIFO & BUSY & RINC


regArr 8'h00 8'h00 ... 00 00 00 00 00 00 00 09 07 19 14 00 20 81 0a 3c
[15] 8'h00 00
[14] 8'h00 00
[13] 8'h00 00
[12] 8'h00 00
[11] 8'h00 00
[10] 8'h00 00
[9] 8'h00 00
[8] 8'h09 09
[7] 8'h07 07
[6] 8'h19 19
[5] 8'h14 14
[4] 8'h00 00
[3] 8'h20 20
[2] 8'h81 81
[1] 8'h0a 0a
[0] 8'h3c 3c
Register file

STATES AND changing configuration




par_err_reg
1'h0
stp_error_reg
1'h0
cs_SYS_CTRL
ALU_OPER...
ALU_OPERAND_A
ALU_OPERAND_B
ALU_OPERAND_FUN
IDLE
cs_UART_RX
IDLE_RX
S...
DATA_RX
P...
S...
ID...
S...
DATA_RX
P...
S...
ID...
S...
DATA_RX
P...
S...
IDLE_RX
cs_UART_TX
IDLE_TX
IDLE_TX
S...
Frame_Collected
11'h4b4
4b4
000
error_count
32'h00000000
00000000

Transcript

```
# -------------- 1) WE RECEIVE COMMAND -------------------------
# RX_Done:Time=6270822100 P_DATA_reg=000000dd and---> Expected=000000dd
#
# synchronizer_Done:Time=6270830000 out=11011101 and---> Expected=11011101
#
# ------------- 2) WE RECEIVE FUN ------------------
# RX_Done:Time=6281238700 P_DATA_reg=  2 and---> Expected=  2
#
# synchronizer_Done:Time=6281246000 out=00000010 and---> Expected=00000010
#
# ------------- 3) here we check alu_operation through golden model ------------------
# ALU_Done:Time=6281248000 DATA=  500   and---> Expected=  500
#
# ------------- 4) here we check that data moved from ALU to FIFO ------------------
# FIFO_Done:Time=6281252000 DATA=  500   and---> Expected=  500
#
# ------------- 5) here we check that Data is sent through TX ------------------
# TX_DONE:Time=6293299800 DATA=11110100  and---> Expected=11110100
#
# TX_DONE:Time=6293299800 parity=0  and---> Expected=0
#
# TX_DONE:Time=6303716200 DATA=1  and---> Expected=1
#
# TX_DONE:Time=6303716200 parity=0  and---> Expected=0
#
# ********************************************************************************************
# ********************************************************************************************
#       --------ALU_Operation_command_with_No_operand ---/config/--- parity_enable=1 ,parity_type=1
#
# -------------- 1) WE RECEIVE COMMAND -------------------------
# RX_Done:Time=6314224800 P_DATA_reg=000000dd and---> Expected=000000dd
#
# synchronizer_Done:Time=6314232000 out=11011101 and---> Expected=11011101
#
# ------------- 2) WE RECEIVE FUN ------------------
# RX_Done:Time=6324641400 P_DATA_reg=  3 and---> Expected=  3
#
# synchronizer_Done:Time=6324648000 out=00000011 and---> Expected=00000011
#
# ------------- 3) here we check alu_operation through golden model ------------------
# ALU_Done:Time=6324650000 DATA=    5   and---> Expected=    5
#
# ------------- 4) here we check that data moved from ALU to FIFO ------------------
# FIFO_Done:Time=6324654000 DATA=  5   and---> Expected=    5
```

TB IS SELF CHECKING INCLUDING ALL CASES ALSO 4 CONFIG WITH ALL POSSIBLE INPUTS

Transcript

```
# FIFO_Done:Time=7572916000 DATA=    2   and---> Expected=    2
#
# ------------- 5) here we check that Data is sent through TX ------------------
# TX_DONE:Time=7584931400 DATA=10  and---> Expected=10
#
# TX_DONE:Time=7584931400 parity=0  and---> Expected=0
#
# TX_DONE:Time=7595347800 DATA=0  and---> Expected=0
#
# TX_DONE:Time=7595347800 parity=1  and---> Expected=1
#
# ********************************************************************************************
# Finish:Time=7595472500 error_count=          0 correct_count=       1763
# ** Note: $stop    : SYS_TOP_tb.sv(705)
#    Time: 75954725 ns  Iteration: 1  Instance: /SYS_TOP_tb
# Break in Module SYS_TOP_tb at SYS_TOP_tb.sv line 705

VSIM 2>
```

Formality (R) Console - Synopsys Inc.

File Edit View Designs Run ECO Window Help

Verification Succeeded

Reference: Ref:/WORK/SYS_TOP

Implementation: Imp:/WORK/SYS_TOP

✔ 0. Guid. | ✔ 1. Ref. | ✔ 2. Impl. | 3. Setup | 4. Match | 5. Verify | 6. Debug

Failing Points | Passing Points | Aborted Points | Unverified Points | Probe Points | Analyses | Loops

	Type	Reference	Size	Implementation	Size	+/-
1	DFF	ALU/ALU_OUT_reg[0]		ALU/ALU_OUT_reg[0]		
2	DFF	ALU/ALU_OUT_reg[10]		ALU/ALU_OUT_reg[10]		
3	DFF	ALU/ALU_OUT_reg[11]		ALU/ALU_OUT_reg[11]		
4	DFF	ALU/ALU_OUT_reg[12]		ALU/ALU_OUT_reg[12]		
5	DFF	ALU/ALU_OUT_reg[13]		ALU/ALU_OUT_reg[13]		
6	DFF	ALU/ALU_OUT_reg[14]		ALU/ALU_OUT_reg[14]		
7	DFF	ALU/ALU_OUT_reg[15]		ALU/ALU_OUT_reg[15]		
8	DFF	ALU/ALU_OUT_reg[1]		ALU/ALU_OUT_reg[1]		
9	DFF	ALU/ALU_OUT_reg[2]		ALU/ALU_OUT_reg[2]		
10	DFF	ALU/ALU_OUT_reg[3]		ALU/ALU_OUT_reg[3]		
11	DFF	ALU/ALU_OUT_reg[4]		ALU/ALU_OUT_reg[4]		

# of Passing Points: 360

Display names: ○ Original ◉ Mapped

Analyze | Analyze Selected Points

Filter:

Get Loop Data

Log | Errors | Warnings | History | Last Command

Formality (verify)>

Ready

Shell State: verify

fm - File Browser | [System_Lab.pdf] | [Final_System.pdf] | [fm_script.tcl (~/Assig... | [G@IC:~/Assignments/ | Formality (R) Console