TASK

Steps: -

1) Create a tcl script named Task.tcl
2) Display on the screen the following message
   - "****Writing Verilog Block Interface****"

3) Create a variable of name **modname** with value of "Up_Dn_Counter".
4) Create a list of name **in_ports** contains the following elements
   - IN
   - Load
   - Up
   - Down
   - CLK
5) Create a list of name **in_ports_width** contains the following elements
   - 4
   - 1
   - 1
   - 1
   - 1

6) Create a list named **out_ports** contains the following elements
   - High
   - Counter
   - Low
7) Create a list named **out_ports_width** contains the following elements
   - 1
   - 4
   - 1

The target of this Task to write the Verilog block interface based on the information in the above variables then generate .v File, noted that the port at a certain position in **in_ports** list has its width in the same position in **in_ports_width** as well as the port at a certain position in **out_ports** list has its width in the same position in **out _ports_width**

It is the expected output

```
module Up_Dn_Counter (
    input    [3:0]    IN,
    input             Load,
    input              Up,
    input             Down,
    input             CLK,
    output            High,
    output  [3:0]     Counter,
    output             Low
    );
```