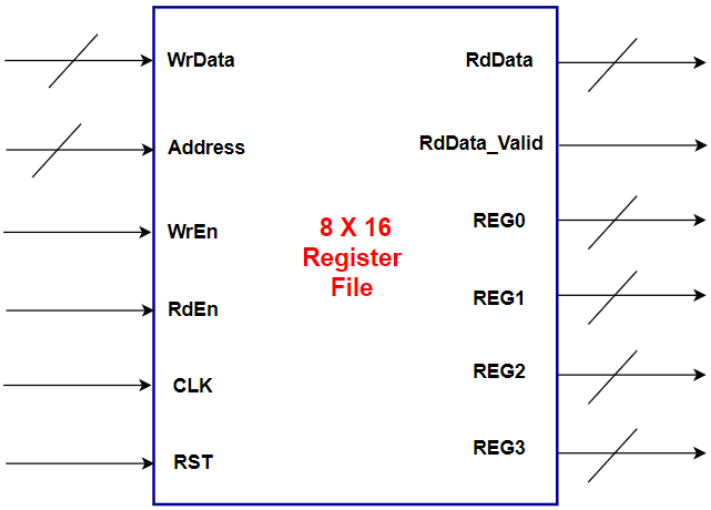
REG_FILE

- **Block Interface: -**



- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (REF_CLK)
RST	IN	1	Active Low Reset	RST_SYNC
Address	IN	Parameterized (default : 4 bits)	Address bus	SYS_CTRL
WrEn	IN	1	Write Enable	SYS_CTRL
RdEn	IN	1	Read Enable	SYS_CTRL
WrData	IN	Parameterized (default : 8 bits)	Write Data Bus	SYS_CTRL
RdData	OUT	Parameterized (default : 8 bits)	Read Data Bus	SYS_CTRL
RdData_Valid	OUT	1	Read Data Valid	SYS_CTRL
REG0	OUT	Parameterized (default : 8 bits)	Register at Address 0x0	ALU
REG1	OUT	Parameterized (default : 8 bits)	Register at Address 0x1	ALU
REG2	OUT	Parameterized (default : 8 bits)	Register at Address 0x2	UART
REG3	OUT	Parameterized (default : 8 bits)	Register at Address 0x3	Clock Divider

- **Reserved Registers Description: -**

1) **REG0 (Address: 0x0)**

ALU Operand A

2) **REG1 (Address: 0x1)**

ALU Operand B

3) **REG2 (Address: 0x2)**

UART Config

REG2[0]: Parity Enable
(Default = 1)
REG2[1]: Parity Type
(Default = 0)
REG2[7:2]: Prescale
(Default = 32)

4) **REG3 (Address: 0x3)**

Div Ratio

REG3[7:0]: Division ratio
(Default = 32)