Digital System Project (ASIC Flow)

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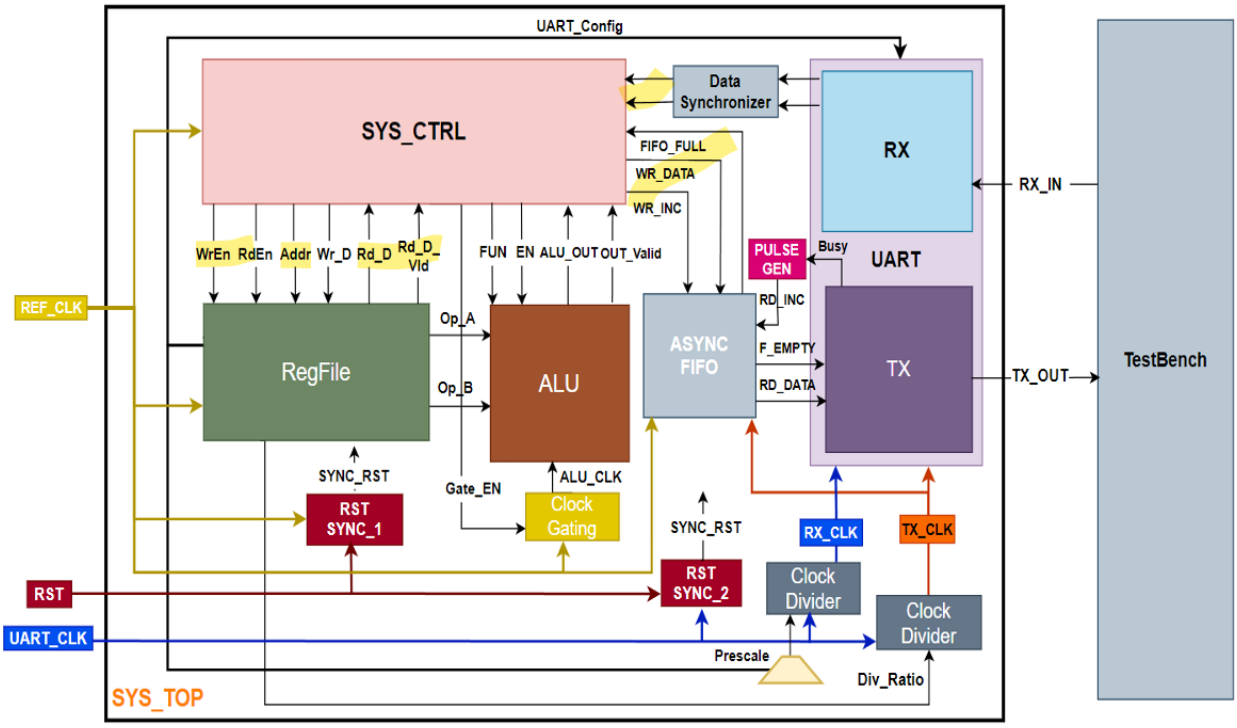
Final System

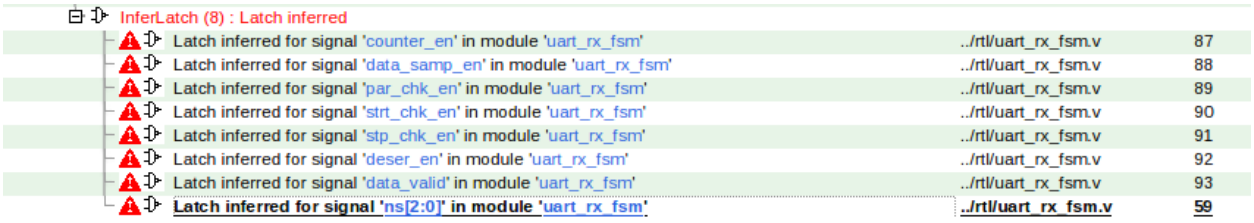


1. Spyglass

a. Linting Step

W362 (7) : Unequal length in arithmetic comparison operator		
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_plus1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:fsm_inst@uart_rx_fsm']	../rtl/uart_rx_fsm.v	78
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_plus1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:fsm_inst@uart_rx_fsm']	../rtl/uart_rx_fsm.v	80
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_plus1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:fsm_inst@uart_rx_fsm']	../rtl/uart_rx_fsm.v	81
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_plus1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:fsm_inst@uart_rx_fsm']	../rtl/uart_rx_fsm.v	83
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_neg1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:samp_inst@data_sampling']	../rtl/data_sampling.v	27
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:samp_inst@data_sampling']	../rtl/data_sampling.v	28
For operator (==), left expression: "edge_cnt" width 6 should match right expression: "half_edges_plus1" width 5 [Hierarchy: ':SYSTEM_TOP:U0_UART@UART:U0_RX@UART_RX:samp_inst@data_sampling']	../rtl/data_sampling.v	29

- Some width mismatch problems in sub modules [**uart_rx_fsm.v** , **data_sampling.v**] in top module **UART_RX.**



InferLatch (8) : Latch inferred		
Latch inferred for signal 'counter_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	87
Latch inferred for signal 'data_samp_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	88
Latch inferred for signal 'par_chk_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	89
Latch inferred for signal 'strt_chk_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	90
Latch inferred for signal 'stp_chk_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	91
Latch inferred for signal 'deser_en' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	92
Latch inferred for signal 'data_valid' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	93
Latch inferred for signal 'ns[2:0]' in module 'uart_rx_fsm'	../rtl/uart_rx_fsm.v	59

- Some Latches inferred:
  In the **uart_rx_fsm** there was no initial states for some enable signals, so the problem solved by adding them before the case statement as shown:

```
// output logic
always @(*) begin

        counter_en = 1'b0;
        data_samp_en = 1'b0;
        par_chk_en = 1'b0;
        strt_chk_en = 1'b0;
        stp_chk_en = 1'b0;
        deser_en = 1'b0;
        data_valid = 1'b0;

    case(cs)
    IDLE: begin
```

Violations Window After Solving Linting problems

b. CDC_CHECKS

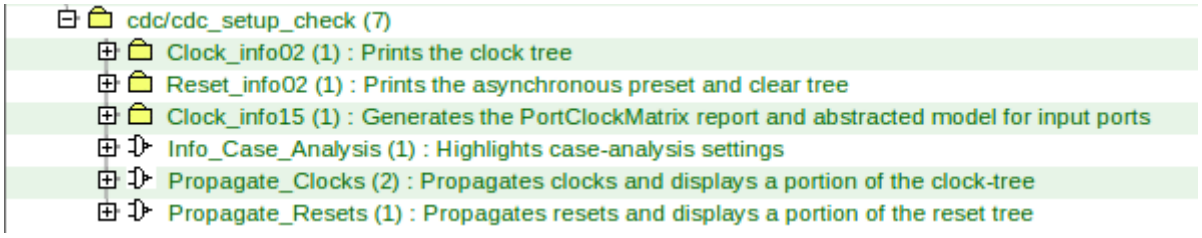
- At first the constraints.sgdc file is created:

```
1
2  # define top_module
3  current_design SYSTEM_TOP
4
5  # define all the clock sources in top_module with their port_names in the rtl
6  clock -name "REF_CLK" -edge {"0" "5"} -period 10
7  clock -name "UART_CLK" -edge {"0" "135.633"} -period 271.267
8
9  # define any generated_clk as the TX_CLK
10 generated_clock -name "TX_CLK" -source "UART_CLK" -divide_by 32
11 reset -name "RST" -value 0
12
13 # define the in_s/out_s in the top_module and their clk_domains
14 input -name RX_IN -clock TX_CLK
15 output -name TX_OUT -clock TX_CLK
16
```

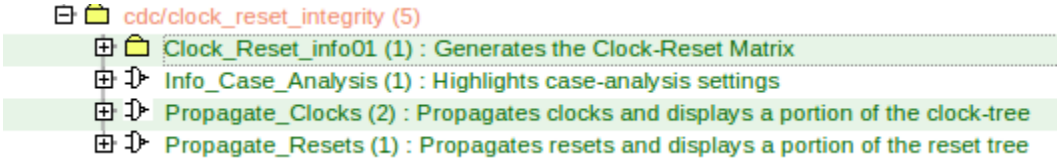
- Secondly, the .prj file must be updated with the following parameters to support the generated_clks under the **##Common Options Section**

```
read_file -type verilog ../rtl/strt_check.v
read_file -type verilog ../rtl/SYS_CTRL.v
read_file -type verilog ../rtl/SYSTEM_TOP.v
read_file -type verilog ../rtl/UART.v
read_file -type verilog ../rtl/UART_RX.v
read_file -type verilog ../rtl/uart_rx_fsm.v
read_file -type verilog ../rtl/UART_TX.v
read_file -type sgdc ../cons/constraints.sgdc

##Common Options Section

set_option projectwdir .
set_option language_mode mixed
set_option designread_enable_synthesis no
set_option designread_disable_flatten no
set_option active_methodology $SPYGLASS_HOME/GuideWare/latest/block/rtl_handoff

# Set parameters to enable generated clocks
set_parameter sdc_generated_clocks yes
set_parameter enable_generated_clocks yes

##Goal Setup Section

current_methodology $SPYGLASS_HOME/GuideWare/latest/block/rtl_handoff


current_goal lint/lint_rtl -alltop
read_file -type awl ./spyglass-1/lint/lint_rtl/spyglass-1_waiver_file.awl
set_goal_option default_waiver_file ./spyglass-1/lint/lint_rtl/spyglass-1_waiver_file.awl
```

- **cdc_setup_check** showed no errors or problems, which ensures setup correctness and completeness.



- **cdc_reset_integrity**

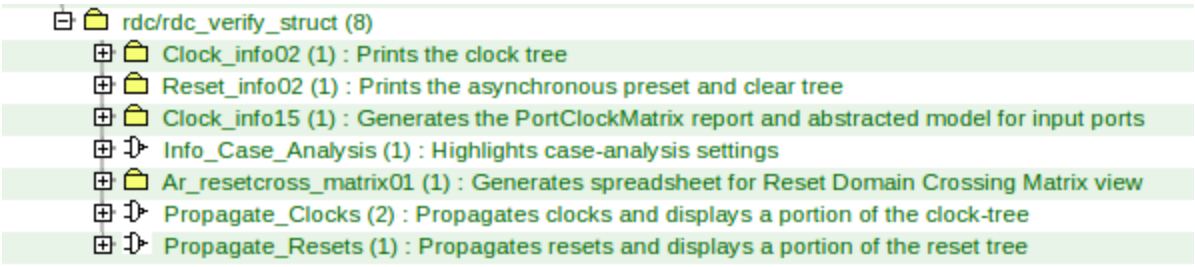


- **cdc_verify_struct**

It shows that there are unshychronized crossing, but these paths are all due to the UART_CONFIG bus which is sent from the REG_FILE to the UART but since this register is a configuration register which changes rarely, and it does remains stable during data_paths operations, so we can waivers these violations easily.

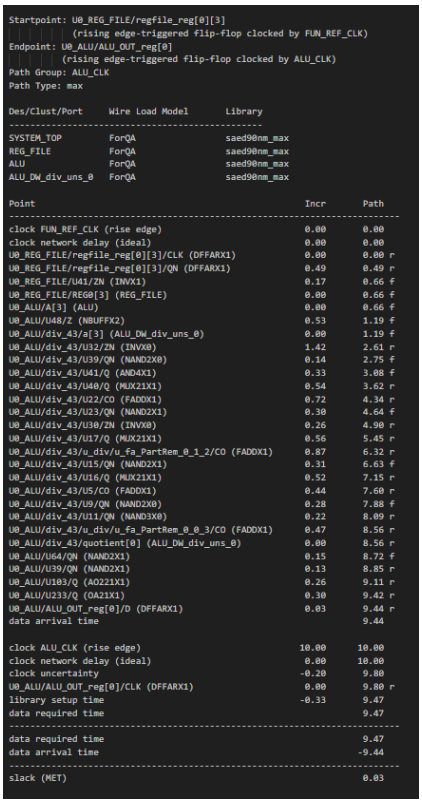
C. RDC_CHECKS

- **rdc_verify_struct**
  since we added 2 RST_SYNC for the 2 clock domains in the system the rdc_verify check showed no violations.



2. Synthesis

- Note: ASIC Implementation of the system is performed on SAED90nm technology.
- The main problem I faced is that I had setup violation in the divider block which was the critical path while when working on TSMC 130nm showed no violations, so since SAED90 was more realistic and aggressive than larger technologies, I simplified the division operation in the design to perform only on 4-bit operands and therefore this relaxed the timing.



```
Startpoint: U0_REG_FILE/regfile_reg[0][3]
            (rising edge-triggered flip-flop clocked by FUN_REF_CLK)
Endpoint: U0_ALU/ALU_OUT_reg[0]
          (rising edge-triggered flip-flop clocked by ALU_CLK)
Path Group: ALU_CLK
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
SYSTEM_TOP         ForQA                 saed90nm_max
REG_FILE           ForQA                 saed90nm_max
ALU                ForQA                 saed90nm_max
ALU_DW_div_uns_0   ForQA                 saed90nm_max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock FUN_REF_CLK (rise edge)                           0.00       0.00
clock network delay (ideal)                             0.00       0.00
U0_REG_FILE/regfile_reg[0][3]/CLK (DFFARX1)             0.00       0.00 r
U0_REG_FILE/regfile_reg[0][3]/QN (DFFARX1)              0.49       0.49 r
U0_REG_FILE/U41/ZN (INVX1)                              0.17       0.66 f
U0_REG_FILE/REG0[3] (REG_FILE)                          0.00       0.66 f
U0_ALU/A[3] (ALU)                                       0.00       0.66 f
U0_ALU/U48/Z (NBUFFX2)                                  0.53       1.19 f
U0_ALU/div_43/a[3] (ALU_DW_div_uns_0)                   0.00       1.19 f
U0_ALU/div_43/U32/ZN (INVX0)                            1.42       2.61 r
U0_ALU/div_43/U39/QN (NAND2X0)                          0.14       2.75 f
U0_ALU/div_43/U41/Q (AND4X1)                            0.33       3.08 f
U0_ALU/div_43/U40/Q (MUX21X1)                           0.54       3.62 r
U0_ALU/div_43/U22/CO (FADDX1)                           0.72       4.34 r
U0_ALU/div_43/U23/QN (NAND2X1)                          0.30       4.64 f
U0_ALU/div_43/U30/ZN (INVX0)                            0.26       4.90 r
U0_ALU/div_43/U17/Q (MUX21X1)                           0.56       5.45 r
U0_ALU/div_43/u_div/u_fa_PartRem_0_1_2/CO (FADDX1)      0.87       6.32 r
U0_ALU/div_43/U15/QN (NAND2X1)                          0.31       6.63 f
U0_ALU/div_43/U16/Q (MUX21X1)                           0.52       7.15 r
U0_ALU/div_43/U5/CO (FADDX1)                            0.44       7.60 r
U0_ALU/div_43/U9/QN (NAND2X0)                           0.28       7.88 f
U0_ALU/div_43/U11/QN (NAND3X0)                          0.22       8.09 r
U0_ALU/div_43/u_div/u_fa_PartRem_0_0_3/CO (FADDX1)      0.47       8.56 r
U0_ALU/div_43/quotient[0] (ALU_DW_div_uns_0)            0.00       8.56 r
U0_ALU/U64/QN (NAND2X1)                                 0.15       8.72 f
U0_ALU/U39/QN (NAND2X1)                                 0.13       8.85 r
U0_ALU/U103/Q (AO221X1)                                 0.26       9.11 r
U0_ALU/U233/Q (OA21X1)                                  0.30       9.42 r
U0_ALU/ALU_OUT_reg[0]/D (DFFARX1)                       0.03       9.44 r
data arrival time                                                  9.44

clock ALU_CLK (rise edge)                              10.00      10.00
clock network delay (ideal)                             0.00      10.00
clock uncertainty                                      -0.20       9.80
U0_ALU/ALU_OUT_reg[0]/CLK (DFFARX1)                     0.00       9.80 r
library setup time                                     -0.33       9.47
data required time                                                 9.47
-----------------------------------------------------------------------
data required time                                                 9.47
data arrival time                                                 -9.44
-----------------------------------------------------------------------
slack (MET)                                                        0.03
```

Violations Faced:

```
max_transition

                          Required        Actual
Net                      Transition     Transition        Slack
-------------------------------------------------------------------
U0_REG_FILE/n23              0.50           0.52          -0.02  (VIOLATED)
    PIN :   U0_REG_FILE/U5/S     0.50       0.52          -0.02  (VIOLATED)
    PIN :   U0_REG_FILE/U225/INP     0.50     0.52        -0.02  (VIOLATED)
    PIN :   U0_REG_FILE/U6/S     0.50       0.52          -0.02  (VIOLATED)
    PIN :   U0_REG_FILE/U48/INP     0.50     0.52         -0.02  (VIOLATED)
    PIN :   U0_REG_FILE/U402/QN     0.50     0.52         -0.02  (VIOLATED)
U0_REG_FILE/n27              0.50           0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U385/INP     0.50     0.51        -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U11/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U14/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U49/INP     0.50     0.51         -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U390/QN     0.50     0.51         -0.01  (VIOLATED)
U0_REG_FILE/n28              0.50           0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U50/INP     0.50     0.51         -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U12/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U19/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U224/INP     0.50     0.51        -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U398/QN     0.50     0.51         -0.01  (VIOLATED)
U0_REG_FILE/n31              0.50           0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U52/INP     0.50     0.51         -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U16/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U21/S     0.50      0.51          -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U223/INP     0.50     0.51        -0.01  (VIOLATED)
    PIN :   U0_REG_FILE/U397/QN     0.50     0.51         -0.01  (VIOLATED)

-------------------------------------------------------------------
Total                        4                  -0.06
```

- Some violations resulted from the command set_max_transition.

Area report:

```
Library(s) Used:

    saed90nm_max (File: /home/ICer/Downloads/Lib/synopsys/models/saed90nm_max.db)
    saed90nm_max_cg (File: /home/ICer/Downloads/Lib/synopsys/models/clock_gating/saed90nm_max_cg.db)

Number of ports:                          776
Number of nets:                          3016
Number of cells:                         2177
Number of combinational cells:           1770
Number of sequential cells:               360
Number of macros/black boxes:               0
Number of buf/inv:                        585
Number of references:                      22

Combinational area:              17432.063975
Buf/Inv area:                     3587.788849
Noncombinational area:           10924.646774
Macro/Black Box area:                0.000000
Net Interconnect area:             571.924429

Total cell area:                 28356.710749
Total area:                      28928.635178
1
```

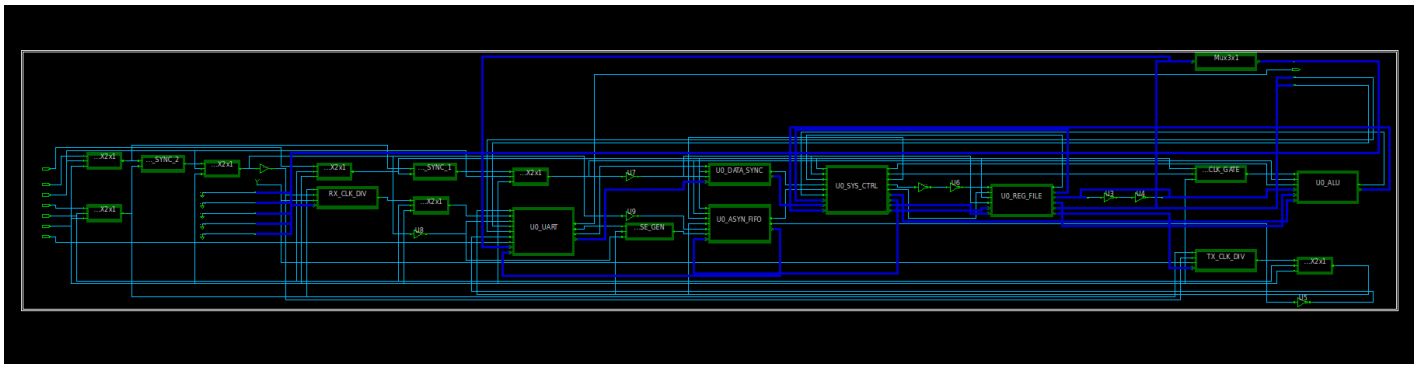
Power Report:

```
Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   5.6260 uW   (17%)
  Net Switching Power  =  26.8772 uW   (83%)
                         ---------
Total Dynamic Power    =  32.5032 uW  (100%)

Cell Leakage Power     =  97.5032 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      2.5245          24.2527        5.0071e+05           27.2780  (  20.98%)
register       2.5523e-02        1.1592e-02        2.6707e+07           26.7441  (  20.57%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational      3.0759           2.6128        7.0296e+07           75.9843  (  58.45%)
--------------------------------------------------------------------------------------------------
Total              5.6260 uW        26.8772 uW     9.7503e+07 pW       130.0064 uW
1
```

Clocks Report

```
Attributes:
    d - dont_touch_network
    f - fix_hold
    p - propagated_clock
    G - generated_clock
    g - lib_generated_clock

Clock          Period   Waveform            Attrs     Sources
------------------------------------------------------------------------------
ALU_CLK         10.00   {0 5}               G         {U0_CLK_GATE/GATED_CLK}
FUN_REF_CLK     10.00   {0 5}               d         {FUN_REF_CLK}
FUN_RX_CLK     271.27   {0 135.633}         G         {RX_CLK_DIV/o_div_clk}
FUN_TX_CLK    8680.54   {0 4340.27}         G         {TX_CLK_DIV/o_div_clk}
FUN_UART_CLK   271.27   {0 135.633}         d         {FUN_UART_CLK}
------------------------------------------------------------------------------

Generated     Master         Generated      Master         Waveform
Clock         Source         Source         Clock          Modification
------------------------------------------------------------------------------
ALU_CLK       FUN_REF_CLK    {U0_CLK_GATE/GATED_CLK}
                                            FUN_REF_CLK    divide_by(1)
FUN_RX_CLK    FUN_UART_CLK   {RX_CLK_DIV/o_div_clk}
                                            FUN_UART_CLK   divide_by(1)
FUN_TX_CLK    FUN_UART_CLK   {TX_CLK_DIV/o_div_clk}
                                            FUN_UART_CLK   divide_by(32)
------------------------------------------------------------------------------
1
```

System Schematic



3. DFT Insertion

3.1. RTL Modification

- For the RTL Modification, added the following signals scan_clk, scan _rst, test_mode and added a mux for each clock in the system to vary between it and the scan_clk in the testing mode and also for the reset signals, so added Muxes for:
  1) REF_CLK
  2) UART_CLk
  3) TX_CLK
  4) RX_CLK
  5) FUN_RST
  6) SYNC_REF_RST
  7) SYNC_UART_RST

- Note: For the ALU_CLK since it was an output of the clock gating cell so I just added and OR Gate between the gate_en signal and the test_mode signal.

3.2. Input Files

- The DFT needed the netlist from the synthesis step so I read the ddc file to operate faster on the netlist instead of reading the .v file
- Needed also the .sdc file from the synthesis step to have all the info about the clocks in my system and its constraints.

3.3. DFT Operation

- My System had 338 flip-flops, so I created 4 scan_chains each chain with a maximum 100 flop.
- Added the other remaining signals as specs in the script itself as these signals and its logical routing will be handled by the tool itself during the DFT insertion, theses signals are:
  1) scan_en
  2) scan_in signals
  3) scan_out signals

Scan_path	Len	ScanDataIn	ScanDataOut	ScanEnable	MasterClock	SlaveClock
I 1	85	SCAN_IN_1	SCAN_OUT_1	SCAN_EN	SCAN_CLK	-
I 2	85	SCAN_IN_2	SCAN_OUT_2	SCAN_EN	SCAN_CLK	-
I 3	84	SCAN_IN_3	SCAN_OUT_3	SCAN_EN	SCAN_CLK	-
I 4	84	SCAN_IN_4	SCAN_OUT_4	SCAN_EN	SCAN_CLK	-

Figure 1: Scan Chains

- Ran test_protocol to ensure the connectivity and the correct routing of the existing dft signals as scan_clk, scan_rst and test_mode
- Made the Scan insertion using compile -scan -map_effort high -incremental_mapping
- Checked for any DRCs Violations of any uncontrollable or unscannable cells using dft_drc command

```
---------------------------------------------------------------
  DRC Report

  Total violations: 0

---------------------------------------------------------------


Test Design rule checking did not find violations

---------------------------------------------------------------
  Sequential Cell Report

  1 out of 339 sequential cells have violations

---------------------------------------------------------------

SEQUENTIAL CELLS WITH VIOLATIONS
      *   1 cell is a clock gating cell
SEQUENTIAL CELLS WITHOUT VIOLATIONS
      * 338 cells are valid scan cells

Information: Test design rule checking completed. (TEST-123)
1
```

- DFT Coverage can be seen that is more than 99 %

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
--------------------------------  ----  ---------
Detected                         DT       16429
Possibly detected                PT           3
Undetectable                     UD         108
ATPG untestable                  AU         123
Not detected                     ND           9
-----------------------------------------------
total faults                                16672
test coverage                               99.19%
-----------------------------------------------
```

- Resulted From the DFT with some violations as:

  1) Hold Negative Slack

  2) Max_transition

  3) Max_fanout

  But these violations will be handled in the further steps.

- Functional Critical Path:

```
Point                                                   Incr       Path
---------------------------------------------------------------------------
clock FUN_REF_CLK (rise edge)                           0.00       0.00
clock network delay (ideal)                             0.00       0.00
U0_REG_FILE/regfile_reg[0][3]/CLK (SDFFARX1)            0.00       0.00 r
U0_REG_FILE/regfile_reg[0][3]/QN (SDFFARX1)             0.49       0.49 r
U0_REG_FILE/U27/ZN (INVX1)                              0.17       0.66 f
U0_REG_FILE/REG0[3] (REG_FILE)                          0.00       0.66 f
U0_ALU/A[3] (ALU)                                       0.00       0.66 f
U0_ALU/U150/Z (NBUFFX2)                                 0.52       1.18 f
U0_ALU/U48/ZN (INVX0)                                   0.49       1.67 r
U0_ALU/U141/ZN (INVX0)                                  0.94       2.61 f
U0_ALU/U152/Z (NBUFFX4)                                 1.78       4.39 f
U0_ALU/add_40/A[3] (ALU_DW01_add_0)                     0.00       4.39 f
U0_ALU/add_40/U1_3/CO (FADDX1)                          1.74       6.14 f
U0_ALU/add_40/U1_4/CO (FADDX1)                          0.50       6.64 f
U0_ALU/add_40/U1_5/CO (FADDX1)                          0.50       7.14 f
U0_ALU/add_40/U1_6/CO (FADDX1)                          0.50       7.64 f
U0_ALU/add_40/U1_7/S (FADDX1)                           0.52       8.17 f
U0_ALU/add_40/SUM[7] (ALU_DW01_add_0)                   0.00       8.17 f
U0_ALU/U233/Q (AO22X2)                                  0.40       8.57 f
U0_ALU/U34/Q (AO221X1)                                  0.28       8.85 f
U0_ALU/U32/Q (OA21X1)                                   0.30       9.15 f
U0_ALU/ALU_OUT_reg[7]/D (SDFFARX1)                      0.03       9.18 f
data arrival time                                                  9.18

clock ALU_CLK (rise edge)                              10.00      10.00
clock network delay (ideal)                             0.00      10.00
clock uncertainty                                      -0.20       9.80
U0_ALU/ALU_OUT_reg[7]/CLK (SDFFARX1)                    0.00       9.80 r
library setup time                                     -0.62       9.18
data required time                                                 9.18
---------------------------------------------------------------------------
data required time                                                 9.18
data arrival time                                                 -9.18
---------------------------------------------------------------------------
slack (MET)                                                        0.00
```

- Testing Critical Path:

```
Startpoint: U0_UART/U0_TX/U0_MUX/TX_OUT_reg
            (rising edge-triggered flip-flop clocked by SCAN_CLK)
Endpoint: SCAN_OUT_4 (output port clocked by SCAN_CLK)
Path Group: SCAN_CLK
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
SYSTEM_TOP         ForQA                 saed90nm_max

Point                                                    Incr       Path
--------------------------------------------------------------------------
clock SCAN_CLK (rise edge)                               0.00       0.00
clock network delay (ideal)                              0.00       0.00
U0_UART/U0_TX/U0_MUX/TX_OUT_reg/CLK (SDFFASX1)           0.00       0.00 r
U0_UART/U0_TX/U0_MUX/TX_OUT_reg/Q (SDFFASX1)             0.79       0.79 r
U0_UART/U0_TX/U0_MUX/TX_OUT (mux4x1)                     0.00       0.79 r
U0_UART/U0_TX/TX_OUT (UART_TX)                           0.00       0.79 r
U0_UART/TX_OUT_S (UART)                                  0.00       0.79 r
U17/Z (NBUFFX32)                                         0.99       1.78 r
SCAN_OUT_4 (out)                                         0.01       1.79 r
data arrival time                                                   1.79

clock SCAN_CLK (rise edge)                             100.00     100.00
clock network delay (ideal)                              0.00     100.00
clock uncertainty                                       -1.20      98.80
output external delay                                  -20.00      78.80
data required time                                                 78.80
--------------------------------------------------------------------------
data required time                                                 78.80
data arrival time                                                  -1.79
--------------------------------------------------------------------------
slack (MET)                                                        77.01
```

4. NDM Creation

4.1. Introduction

- NDM is an easy and simple way to collect all views in a specific format called ndm or clib format.
- It's a technology-specific in which for any asic flow compliance all the tools requires to consider all the views of the std_cells in order to achieve an optimized design without (timing, physical DRC, or functional) violations.
- Therefore we create an NDM Container that have the timing,frame and the design and layout views that will be a standered to use in all the pnr flow which will make the flow easier instead of reading these views everytime we go to a new step in pnr flow.

4.2. Inputs & Outputs

- Inputs:
  a) .tf : the technology file : contains all the info about the metal layers such as color for the gui, etc.. all the physical DRCs for this lib or technology such as : min spacing, min width and so many more..
  b) .db : which is the timing/power/area views of all the standard cells in the included libraries, for my system I used 3 libraries:
     1) saed90nm_max
     2) saed90nm_min
     3) saed90nm_max_cg
  c) .lef file: the abstract view of the standered cell, which contains some info about each cell such as:
     1) Cell boundaries.
     2) Pin shapes
     3) Pins location
     4) Pins directions and names
     5) Layer used with the cell
- Output: the tool groups all these infos from the file into a unique workspace specific for the used libraries and to be able to use it directly in the upcoming steps.

4.3. Design Library Creation

- This is a project-specific library that contains design data.
- It stores all relevant data such as logical views, physical views, timing information, parasitic data, and constraints. By linking it with the reference library, technology file, and TLU+ files.
- TLU+files is important because they provide RC parasitic modeling, which is critical for accurate timing and signal integrity analysis and used for the calculation of the actual wire delays, instead of the inaccurate delays from the wire load model
- Inputs: NDM Library, Design Files as: the .v file and the sdc file, finally the RC parasitics information from the TLU+ files.
- Outputs: **SYSTEM_TOP_setup.dlib**, which will be used as the initial step for the floor_plan stage.

5. Floor Planning

- In this step's script, I defined the following:
  a) Opened the setup.dlib and copied it to a new .dlib with a name **SYSTEM_TOP_fp.dlib** to work on it as to be able to come to the previous step at any time for future modifications if needed.
  b) Defined the Metal Layers Direction, in a cross-metal wire orientation style, which is better in less crosstalk between the adjacent metal layers and overlapping only occurs at the cross section to be able to have access to most of the metal layers by using stacked vias if I want as it will be used in the power plan step
  c) Ignored using the layers M8 and M9 as they are only dedicated for the power supply.
  d) Intilialized the floor plan with a core utilization of 0.5 in R shape with core offset from the die of 10 and side ratio of 1:1.
  e) Defiend the Pins Placement in a way in which:
     1) Functional Clocks on the top side: FUN_REF_CLK, FUN_UART_CLK.
     2) Input pins on the Right Side: RX_IN and SCAN_IN signals
     3) Output pins on the Left Side: TX_OUT and SCAN_OUT signals
     4) Control and Reset Pins on the bottom side

  f) Generating reports and output files.

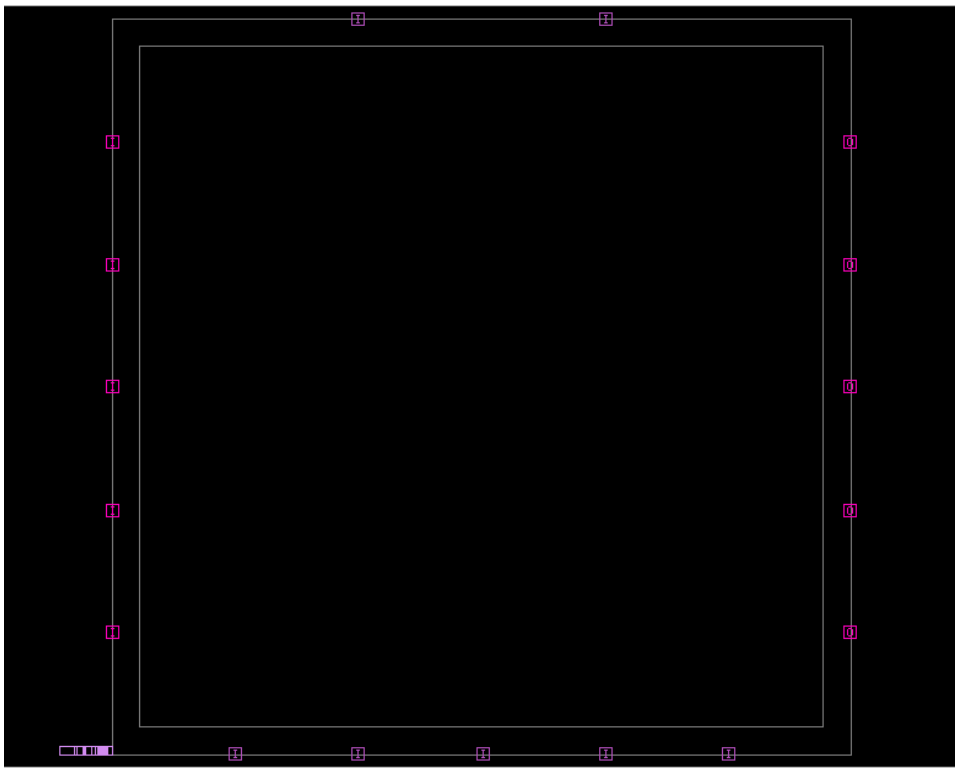


Figure 2: Output of the Floor Planning Stage

Utilization Report:

```
****************************************
Utilization Ratio:                      0.5029
Utilization options:
 - Area calculation based on:           site_row of block SYSTEM_TOP_fp
 - Categories of objects excluded:      hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                             61662.4128
Total Capacity Area:                    61662.4128
Total Area of cells:                    31009.0752
Area of excluded objects:
 - hard_macros         :                0.0000
 - macro_keepouts      :                0.0000
 - soft_macros         :                0.0000
 - io_cells            :                0.0000
 - hard_blockages      :                0.0000

Utilization of site-rows with:
 - Site 'unit':                         0.5029

0.5029
```

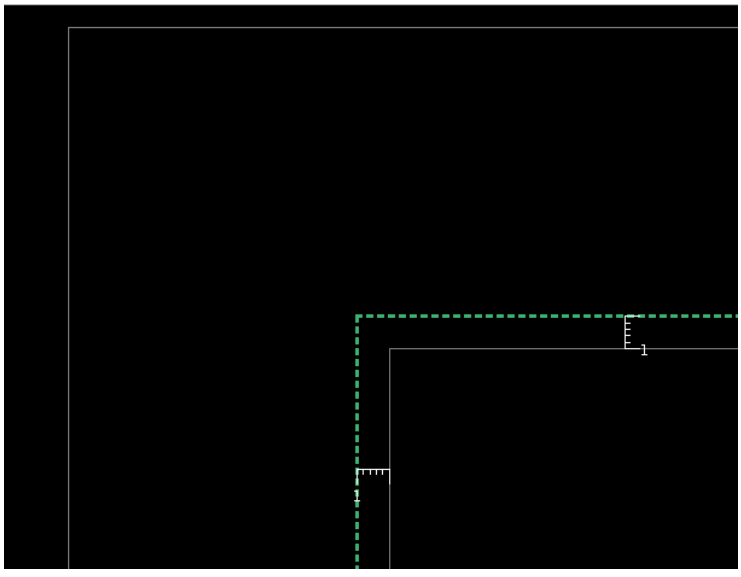
6. Power Planning

- In this step's script, I defined the following:

  a) Opened the fp.dlib and copied it to a new .dlib with the name of **SYSTEM_TOP_pp.dlib** to work on it as to be able to come to the previous step at any time for future modifications if needed.

  b) Created the Vdd and Vss pins and connected them to the hierarchical system

  c) Defined the power ring region of offset 1 from the core and its purpose is that when creating the power ring on the chip do not create it on the core boundary itself but leaving a small offset between the core and the power ring itself



d) Defined the power ring itself by setting the following:
   1) Horizontal Layer: M8
   2) Vertical Layer: M9
   3) Ring Width = 2
   4) Ring Spacing = 1.5

- Note: Ring Width is relatively small as it is considered a low-power design as the total power of the design is approximately 130 uW so we will be able to deliver the power from the pins to the ring just fine.

e) Defined the power mesh, which is responsible for delivering the power supply from the ring to every standard cell in the design and its specs as the following:
   1) Width = 5
   2) Pitch = 20
   3) Horizontal offset = 1
   4) Vertical offset = 6

- Note: Ring Width is slightly bigger than the ring as it should be able to deliver the supply to the cells with the lowest IR drop possible, since the metal thickness is inversely proportional to the resistance.

f) Finally created the power rails on M1, as their purpose is the power delivered from M8,M9 through stacked vias and through the cells actually happens through the M1 rails which are connected directly to the cells' VDD and VSS of the cell transistors, in which these rails are connected to the cells in the FEOEL.

- Note: The Rail Width must be the same width as the Vdd and Vss rails in the std_cell itself to avoid any violations in the placement step.

g) Resulting the outputs and reports.

Track Utilization Report:

```
Percentage of routing tracks used by P/G nets
=============================================
       layer |    Shape |  Spacing |    Total
=============================================
          PO |   0.000% |   0.000% |   0.000%
          M1 |   6.479% |  17.000% |  23.479%
          M2 |   1.710% |   1.710% |   3.420%
          M3 |   1.275% |   2.550% |   3.825%
          M4 |   1.737% |   3.358% |   5.094%
          M5 |   1.290% |   2.579% |   3.869%
          M6 |   1.852% |   3.358% |   5.210%
          M7 |   1.283% |   2.566% |   3.849%
          M8 |  66.790% |   1.103% |  67.893%
          M9 |  46.939% |  12.245% |  59.184%
```

PG Connectivity Report:

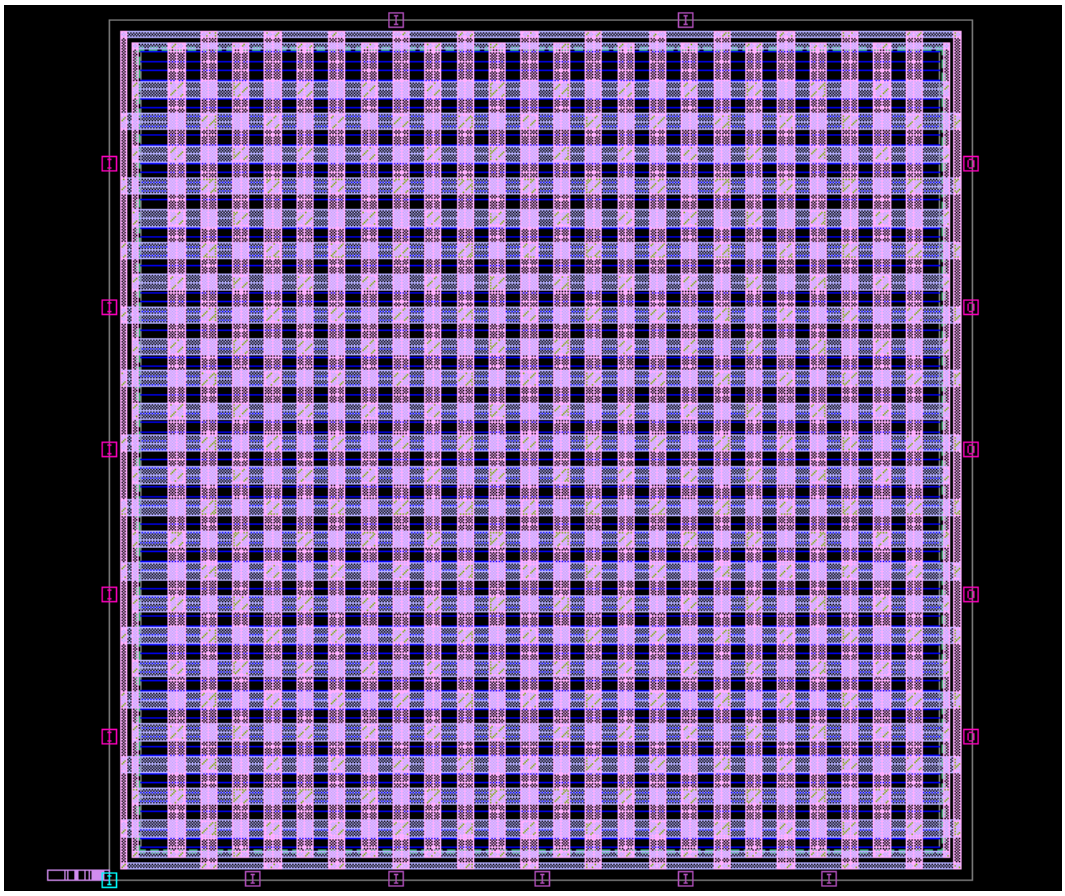
```
Number of Standard Cells: 2195
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 71
Number of VDD Vias: 2860
Number of VDD Terminals: 0
Number of VSS Wires: 72
Number of VSS Vias: 2944
Number of VSS Terminals: 0
**************Verify net VDD connectivity*****************
  Number of floating wires: 14
  Number of floating vias: 0
  Number of floating std cells: 2195
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
**************Verify net VSS connectivity*****************
  Number of floating wires: 14
  Number of floating vias: 0
  Number of floating std cells: 2195
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
```

- As can be seen, all the std cells are floating, since we did not perform placement yet.

```
CPU usage for check_pg_drc: 0.09 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.09 seconds ( 0.00 hours)
No errors found.
```

- No PG DRC Violations were found

Output of the Power Plan Step:



7. Placement

- In this step's script, the flow moved as the following:
  a) Opened the pp.dlib and copied it to a new .dlib with the name of **SYSTEM_TOP_pl.dlib** to work on it as to be able to come to the previous step at any time for future modifications if needed
  b) I read the .def file from the dft step that maybe used to operate scan chain reordering to solve any congestion problem if there was
  c) Excute a check design command pre_placement stage that runs pre-defined or user-defined checks on current design.
  d) Define some options as max_util, max_density and max_fanout, since in this step the utilization may increase due to the addition of spare cells, HFS cells and Tie cells
  e) Added the spare cells in a legalized way
  f) Added the tie cells
  g) Connected all the new added cells to the VDD and VSS
  h) Ran the place_opt command that performs the following:
     1) Coarse Placement
     2) Legalized Placement
     3) HFS for the signals as rst, and scan_en and any signal that has high fanout except the clock of course.
     4) Optimization in terms of Congestion and Timing
  i) Generate Outputs and Reports.

Report_QoR:

```
Scenario           'default'
Timing Path Group  'FUN_REF_CLK'
----------------------------------------
Levels of Logic:                      14
Critical Path Length:               4.45
Critical Path Slack:                4.72
Critical Path Clk Period:          10.00
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:              -0.24
Total Hold Violation:              -21.72
No. of Hold Violations:               230
----------------------------------------

Scenario           'default'
Timing Path Group  'FUN_UART_CLK'
----------------------------------------
Levels of Logic:                       7
Critical Path Length:               2.94
Critical Path Slack:              267.51
Critical Path Clk Period:         271.27
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:              -0.20
Total Hold Violation:              -2.27
No. of Hold Violations:               18
----------------------------------------
```

```
Timing Path Group  'FUN_TX_CLK'
----------------------------------------
Levels of Logic:                       2
Critical Path Length:               1.49
Critical Path Slack:              269.58
Critical Path Clk Period:        8680.54
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:              -0.21
Total Hold Violation:              -7.83
No. of Hold Violations:               37
----------------------------------------

Scenario           'default'
Timing Path Group  'FUN_RX_CLK'
----------------------------------------
Levels of Logic:                       3
Critical Path Length:              54.88
Critical Path Slack:              215.56
Critical Path Clk Period:         271.27
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:              -0.11
Total Hold Violation:              -3.11
No. of Hold Violations:               28
----------------------------------------

Scenario           'default'
Timing Path Group  'ALU_CLK'
----------------------------------------
Levels of Logic:                      21
Critical Path Length:               6.31
Critical Path Slack:                2.85
Critical Path Clk Period:          10.00
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:              -0.14
Total Hold Violation:              -1.06
No. of Hold Violations:               17
```

- As can be seen from the quality of results report, I have some serious hold violations but we will consider them in the CTS Step.

Report_Placement:

```
Wire length report (all)
==================
wire length in design SYSTEM_TOP_pl: 64901.352 microns.
wire length in design SYSTEM_TOP_pl (see through blk pins): 64901.352 microns.

Physical hierarchy violations report
====================================
Violations in design SYSTEM_TOP_pl:
   0 cells have placement violation.

Voltage area violations report
==================================
Voltage area placement violations in design SYSTEM_TOP_pl:
   0 cells placed outside the voltage area which they belong to.
```

Report_Congestion:

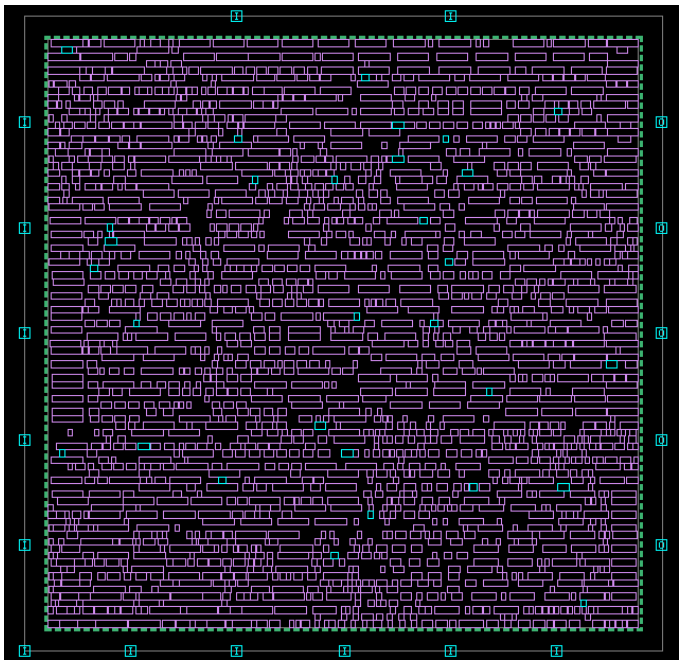
```
Layer     |    overflow     |              # GRCs has
Name      |  total  |  max  | overflow (%)      | max overflow
-------------------------------------------------------------
Both Dirs |       0 |     0 |       0  ( 0.00%) |       0
H routing |       0 |     0 |       0  ( 0.00%) |       0
V routing |       0 |     0 |       0  ( 0.00%) |       0

1
```

Report_Cell:

PLACE_HFSBUF_1046_161	NBUFFX2	saed90nm_m	PLACE_optlc_1693	TIEL	saed90nm_m
PLACE_HFSBUF_1190_93	NBUFFX2	saed90nm_m	PLACE_optlc_1695	TIEL	saed90nm_m
PLACE_HFSBUF_1411_163	NBUFFX2	saed90nm_m	PLACE_optlc_1697	TIEL	saed90nm_m
PLACE_HFSBUF_1461_97	NBUFFX2	saed90nm_m	PLACE_optlc_1699	TIEL	saed90nm_m
PLACE_HFSBUF_1672_164	NBUFFX2	saed90nm_m	PLACE_optlc_1701	TIEL	saed90nm_m
PLACE_HFSBUF_1719_181	NBUFFX2	saed90nm_m	PLACE_optlc_1703	TIEL	saed90nm_m
PLACE_HFSBUF_196_188	NBUFFX2	saed90nm_m	PLACE_optlc_1705	TIEL	saed90nm_m
PLACE_HFSBUF_2158_173	NBUFFX2	saed90nm_m	PLACE_optlc_1706	TIEL	saed90nm_m
PLACE_HFSBUF_224_269	NBUFFX2	saed90nm_m	PLACE_optlc_1710	TIEL	saed90nm_m
PLACE_HFSBUF_2251_171	NBUFFX2	saed90nm_m	PLACE_optlc_1712	TIEL	saed90nm_m
PLACE_HFSBUF_2798_174	NBUFFX2	saed90nm_m	PLACE_optlc_1714	TIEL	saed90nm_m
PLACE_HFSBUF_2817_69	NBUFFX2	saed90nm_m	PLACE_optlc_1716	TIEL	saed90nm_m
PLACE_HFSBUF_3079_176	NBUFFX2	saed90nm_m	PLACE_optlc_1718	TIEL	saed90nm_m
PLACE_HFSBUF_313_187	NBUFFX2	saed90nm_m	PLACE_optlc_1721	TIEL	saed90nm_m
PLACE_HFSBUF_3159_72	NBUFFX2	saed90nm_m	PLACE_optlc_1723	TIEL	saed90nm_m
PLACE_HFSBUF_3205_179	NBUFFX2	saed90nm_m	PLACE_optlc_1725	TIEL	saed90nm_m
PLACE_HFSBUF_3659_83	NBUFFX2	saed90nm_m	PLACE_optlc_1726	TIEL	saed90nm_m
PLACE_HFSBUF_383_271	NBUFFX2	saed90nm_m	PLACE_optlc_1729	TIEH	saed90nm_m
PLACE_HFSBUF_4063_183	NBUFFX8	saed90nm_m	PLACE_optlc_1730	TIEH	saed90nm_m
PLACE_HFSBUF_5080_146	NBUFFX2	saed90nm_m	PLACE_optlc_1731	TIEH	saed90nm_m
PLACE_HFSBUF_5147_98	NBUFFX8	saed90nm_m	RST_SYNC_1	RST_SYNC_0	
PLACE_HFSBUF_5316_147	NBUFFX2	saed90nm_m	RST_SYNC_2	RST_SYNC_1	
PLACE_HFSBUF_5393_148	NBUFFX2	saed90nm_m	RX_CLK_DIV	ClkDiv_1	
PLACE_HFSBUF_5460_149	NBUFFX2	saed90nm_m	SpareCell_0	NAND2X2	saed90nm_m
PLACE_HFSBUF_5504_152	NBUFFX2	saed90nm_m	SpareCell_0_0	INVX2	saed90nm_m
PLACE_HFSBUF_5576_150	NBUFFX2	saed90nm_m	SpareCell_0_1	INVX2	saed90nm_m
PLACE_HFSBUF_5641_151	NBUFFX2	saed90nm_m	SpareCell_0_2	INVX2	saed90nm_m
PLACE_HFSBUF_5823_153	NBUFFX2	saed90nm_m	SpareCell_0_3	INVX2	saed90nm_m
PLACE_HFSBUF_637_190	NBUFFX2	saed90nm_m	SpareCell_0_4	INVX2	saed90nm_m
PLACE_HFSBUF_6556_154	NBUFFX2	saed90nm_m	SpareCell_0_5	INVX2	saed90nm_m
PLACE_HFSBUF_69_110	NBUFFX2	saed90nm_m	SpareCell_0_6	INVX2	saed90nm_m
PLACE_HFSBUF_752_111	NBUFFX8	saed90nm_m	SpareCell_0_7	INVX2	saed90nm_m
PLACE_HFSBUF_908_100	NBUFFX2	saed90nm_m	SpareCell_0_8	INVX2	saed90nm_m
PLACE_HFSBUF_962_95	NBUFFX2	saed90nm_m	SpareCell_0_9	INVX2	saed90nm_m
PLACE_HFSINV_170_257	INVX2	saed90nm_m	SpareCell_1	NAND2X2	saed90nm_m
PLACE_HFSINV_350_248	INVX0	saed90nm_m	SpareCell_1_0	XOR2X1	saed90nm_m
PLACE_HFSINV_907_243	INVX2	saed90nm_m	SpareCell_1_1	XOR2X1	saed90nm_m
			SpareCell_1_2	XOR2X1	saed90nm_m
			SpareCell_1_3	XOR2X1	saed90nm_m
			SpareCell_1_4	XOR2X1	saed90nm_m

- As can be seen there are some added cells used in HFS, Tie cells and spare cells

Output of the Placemet Step:



8. CTS

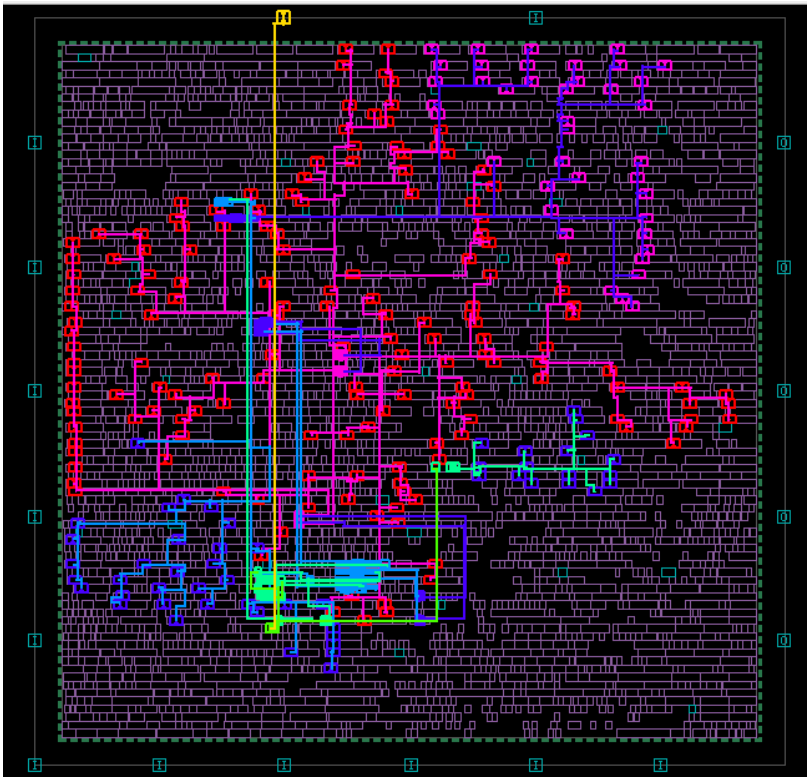
- The flow moved as follows:
  a) Opened the pl.dlib and copied it to a new .dlib with the name of **SYSTEM_TOP_cts.dlib** to work on it as to be able to come to the previous step at any time for future modifications if needed.
  b) Ran some pre_cts_checks using " check_design -checks pre_clock_tree_stage"
  c) Checked for any common problems that may impact the clock tree synthesis by using check_clock_trees command, and it noted that the clock gating cell has a don't touch attrubuite set to false in the .lib file so I sat it to true.
  d) For the clock routing, I ignored routing on M8,M9 and M1.
  e) Removed any previous definitions of the CTS Targets which represent in the latency and skew.
  f) Added a driving cells and input transition constraints on all the clock pins
  g) Excluding all the std cells used in my design for to be used in CTS as I will define the cells that will the tool only use it for CTS

h) Define some bufs/invs for cts and also for hold fixing
i) Define the CTS targets in which for:
   1) REF_CLK: target skew = 0.01, target latency = 0.5
   2) UART_CLK: target skew = 0.2, target latency = 0
j) Defined some NDRs for the width and spacing be multiplied by 2, and these NDRs are defined on the following:

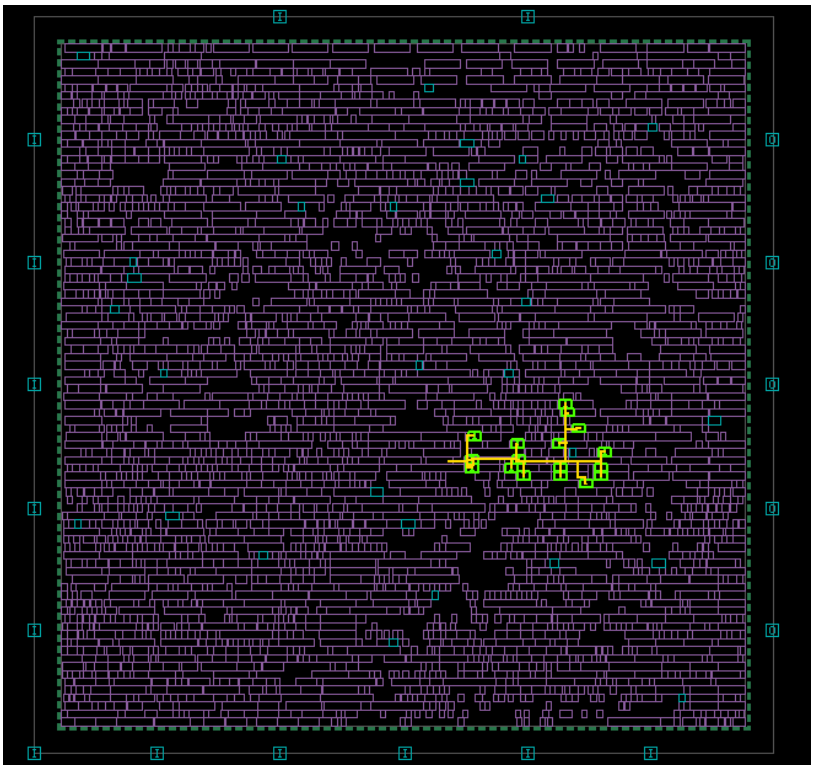
- The Root which is from the clock port to first buffer has layers availability from M7 to M2.
- From the First Buffer to the Last one before the sink
- Then from the last buffer to the sink pin use the default rules

k) Defined some cts DRCs as: the max_transition, max_fanout and max_capacitance
l) Performed clock_opt.
m) Checked for any violations such as timing, congestion and so on
n) Connected all the new added cells to VDD and VSS.
o) Reports and outputs

FUN_REF_CLK Tree:

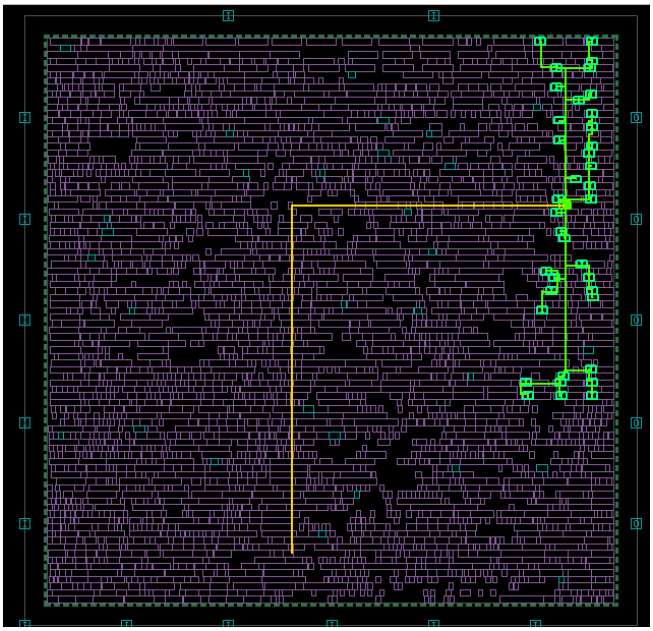


ALU_CLK Tree:

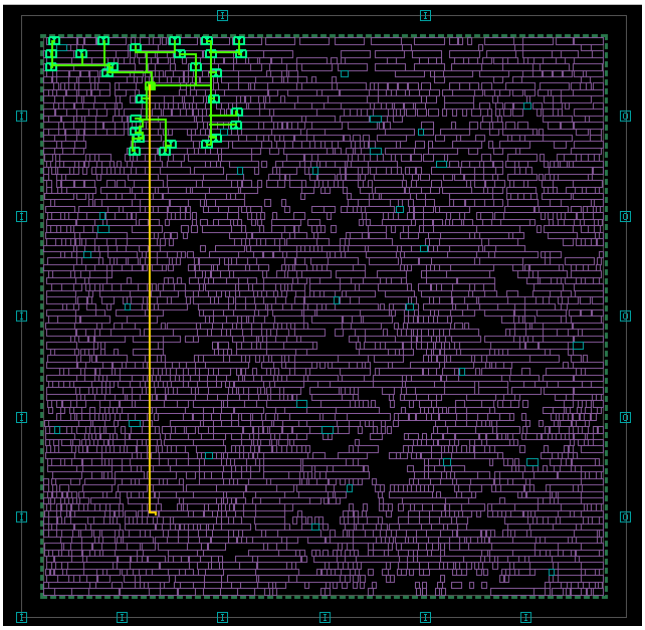


FUN_UART_CLK Tree:

TX_CLK Tree:



RX_CLK Tree:



9. Routing & Finishing

- The Flow in this step goes as follows:
  a) Opened the cts.dlib and copied it to a new .dlib with the name of **SYSTEM_TOP_route.dlib** to work on it as to be able to come to the previous step at any time for future modifications if needed.
  b) Performed some checks to ensure the design is ready for the routing step.
  c) Provided for the tool all the metal layers to route with them from M1 to M9.
  d) Ran the Global Routing step in which the tool tries to find the shortest path for every net in a gcell and the metal layers it will be using for this path as it does not make any physical routing only planning
  e) Ran the Track Assignment step in which the tool assign a specific track from the metal layer that was assigned to this path in the global routing step so it defines the physical path itself with its horizontal and vertical directions, but the metal still not placed.
  f) Ran the Detailed Routing step in which it takes the routing plan resulted from the global routing and the tracks that was assigned to eacgh route from the track assignment then start to put metals and start the actual routing between the nets and pins, it also tries to solve any DRC violation that arises
  g) Then I performed route optimization in which it tries to optimize the routing process itself to solve any violations as setup or hold
  h) Added the filler cells and connect them to Vdd and Vss.
  i) Generate the reports and the output files and most importantly the .GDS file.

Final DRC Report

```
Verify Summary:

Total number of nets = 2700, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

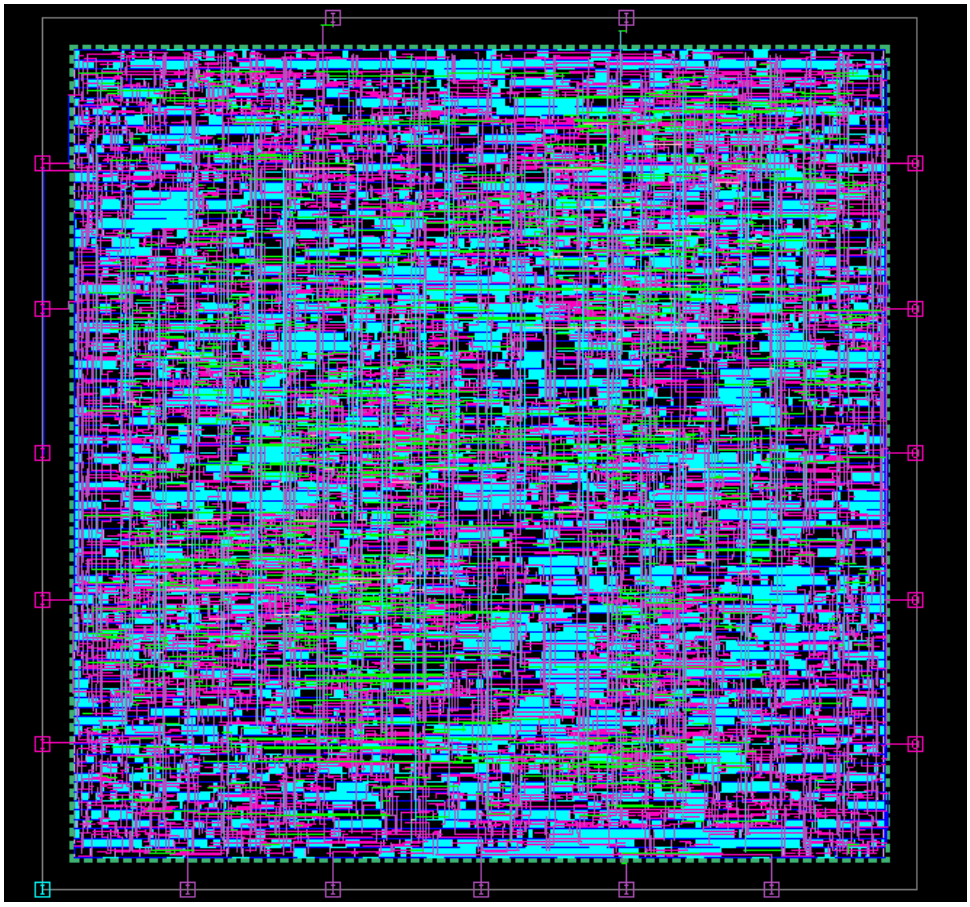
Final Setup Slack of the Critical path:

```
--------------------------------------------------------------------------------
data required time                                                       10.02
data arrival time                                                       -10.01
--------------------------------------------------------------------------------
slack (MET)                                                               0.01
```

Final Hold Slack of the Critical path:

```
--------------------------------------------------------------------------------
data required time                                                       1.09
data arrival time                                                       -1.09
--------------------------------------------------------------------------------
slack (MET)                                                              0.00
```

Output of the Routing and Finishing Step:



Final Chip Before Tape-out: