Group 3 5 test circuits + timing diagrams

Key

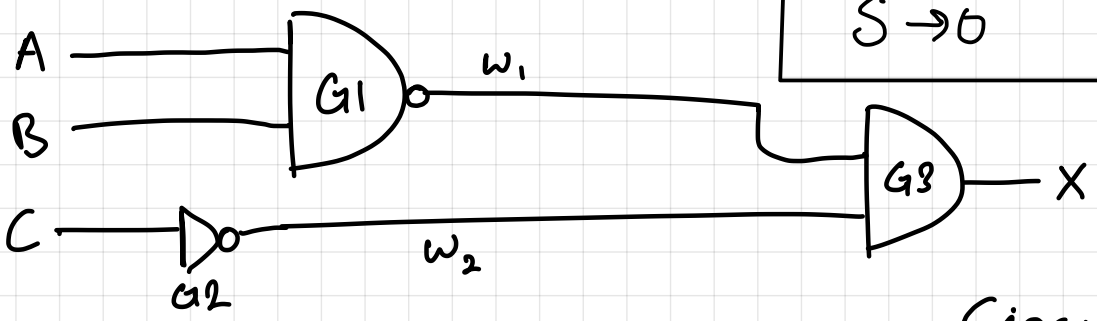
↔ 100 ps

Delays (ps)

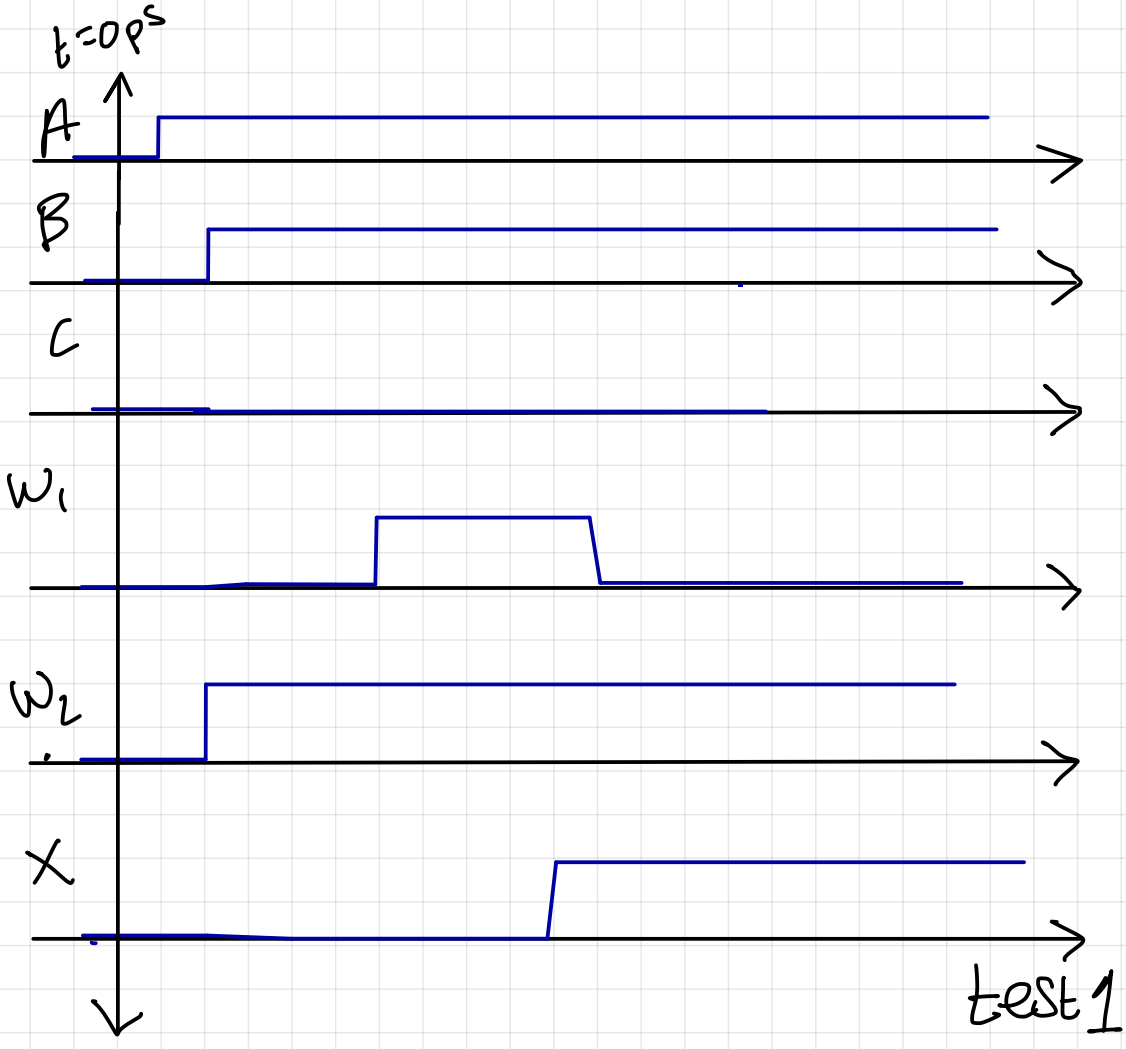
XOR3	350
NOT	100
NAND2	250
NOR3	300
AND2	200
OR2	200
NAND3	300

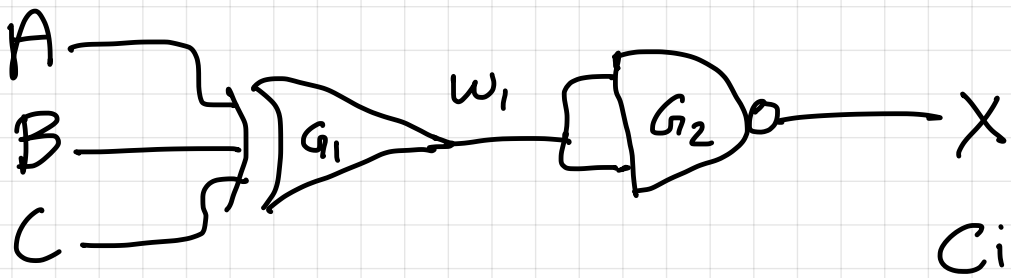
Time Stamps (ps)

A → 1	50
B → 1	100
C → 0	0
D → 0	0
E → 1	100
S → 0	0

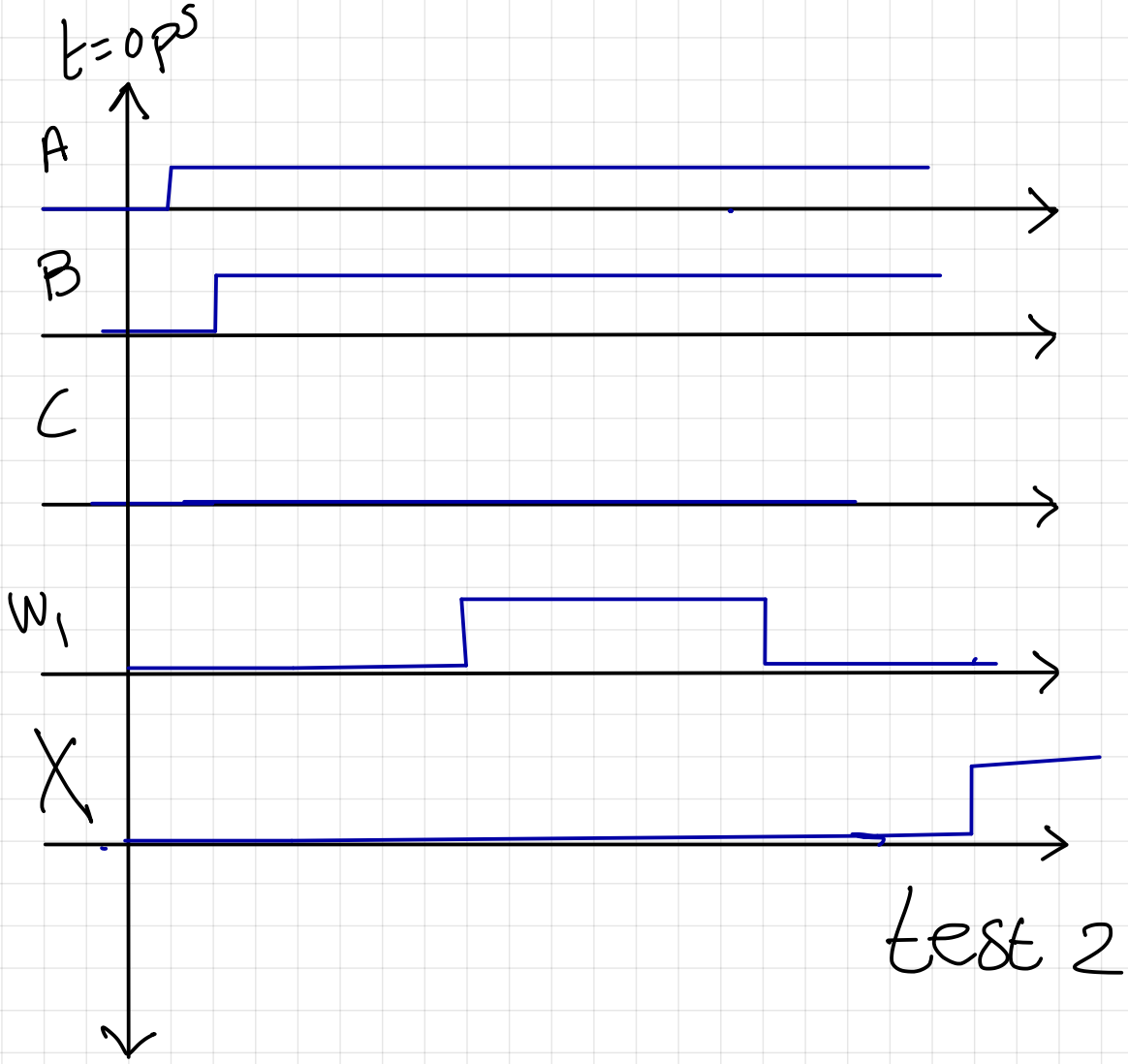


Circuit 1

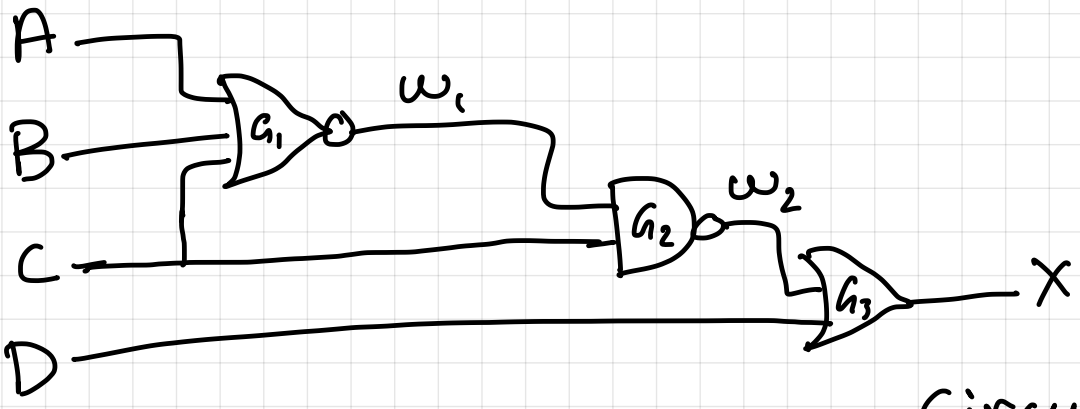




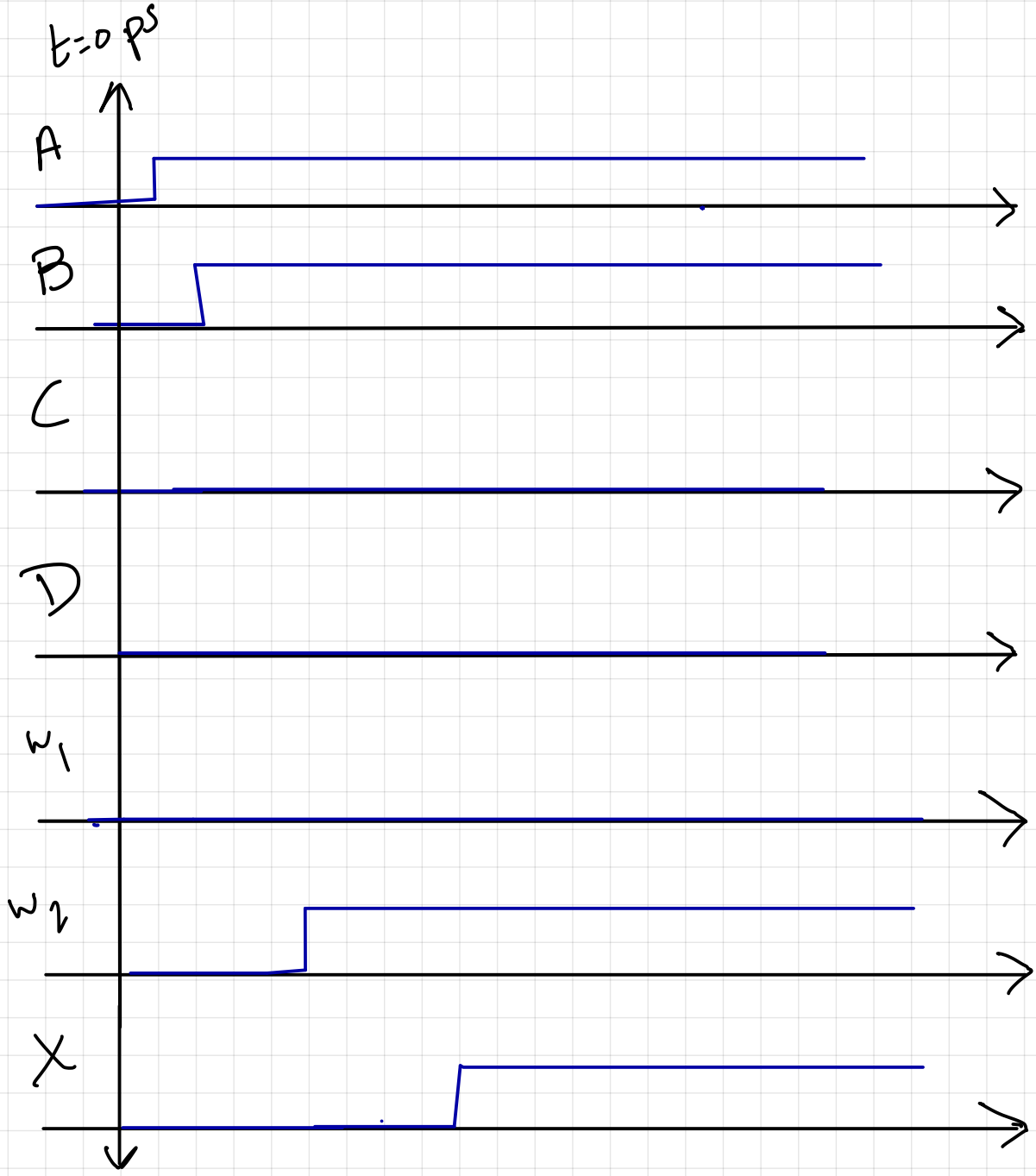
Circuit 2



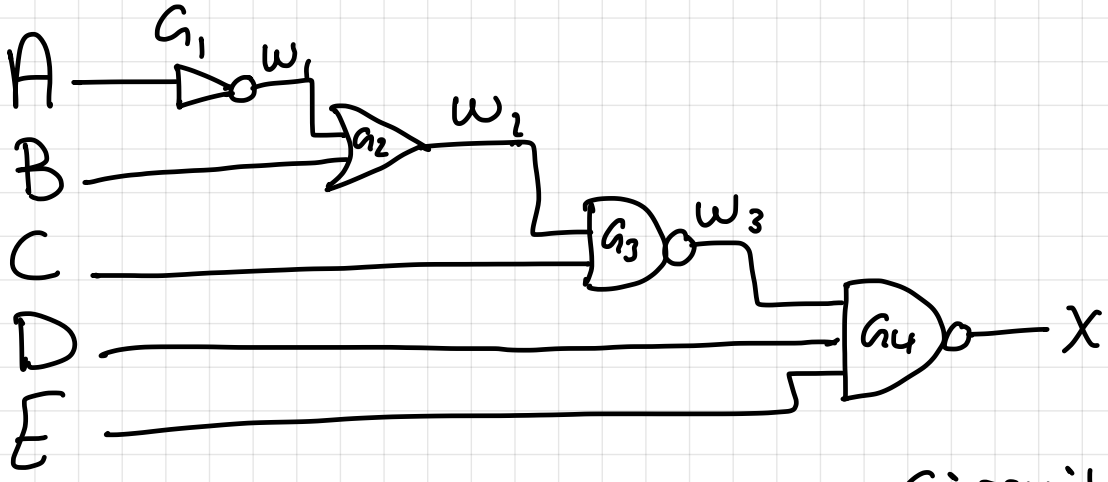
test 2



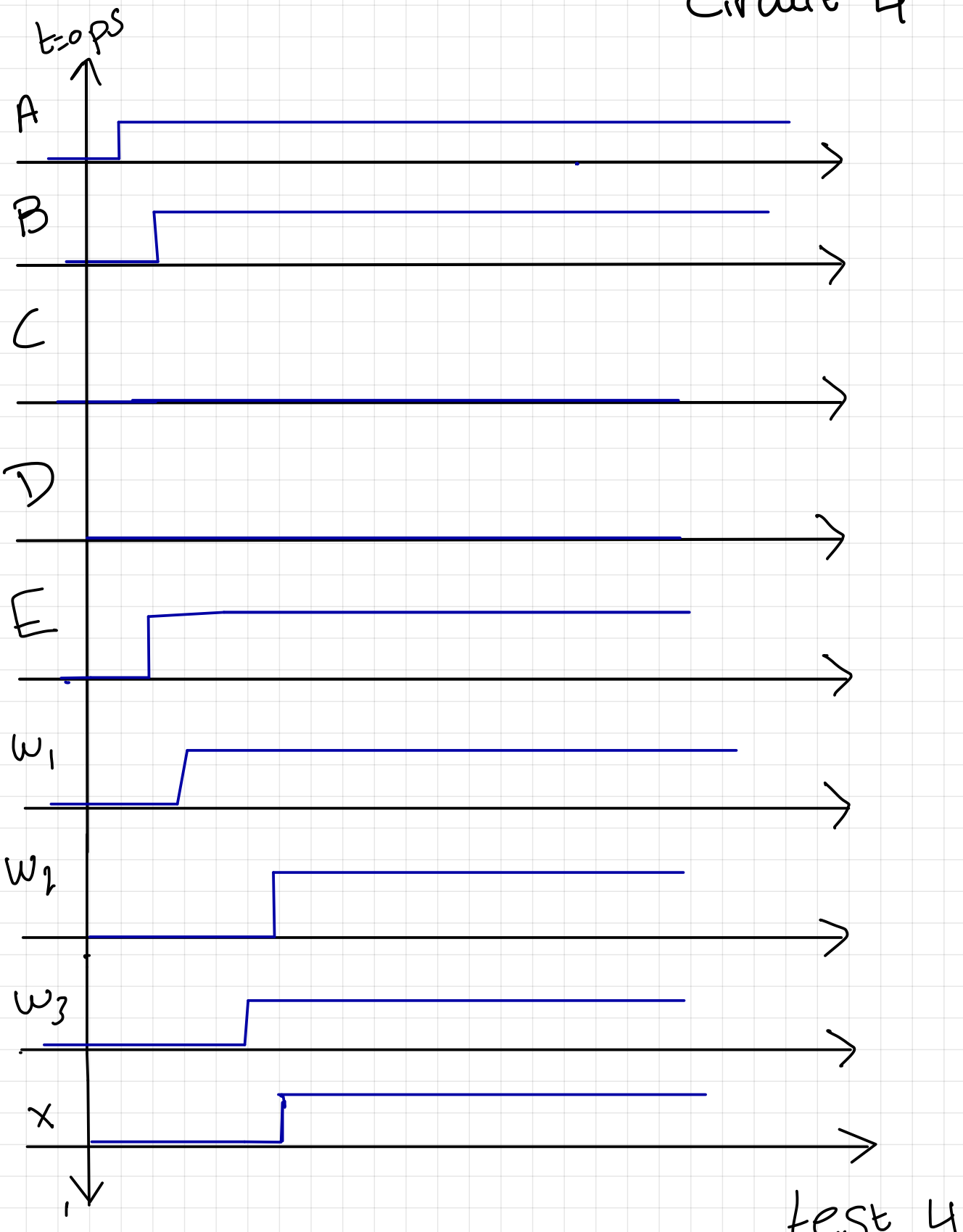
Circuit 3



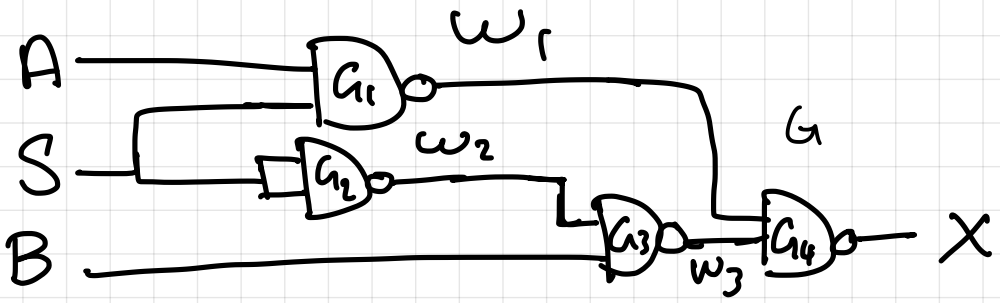
test 3



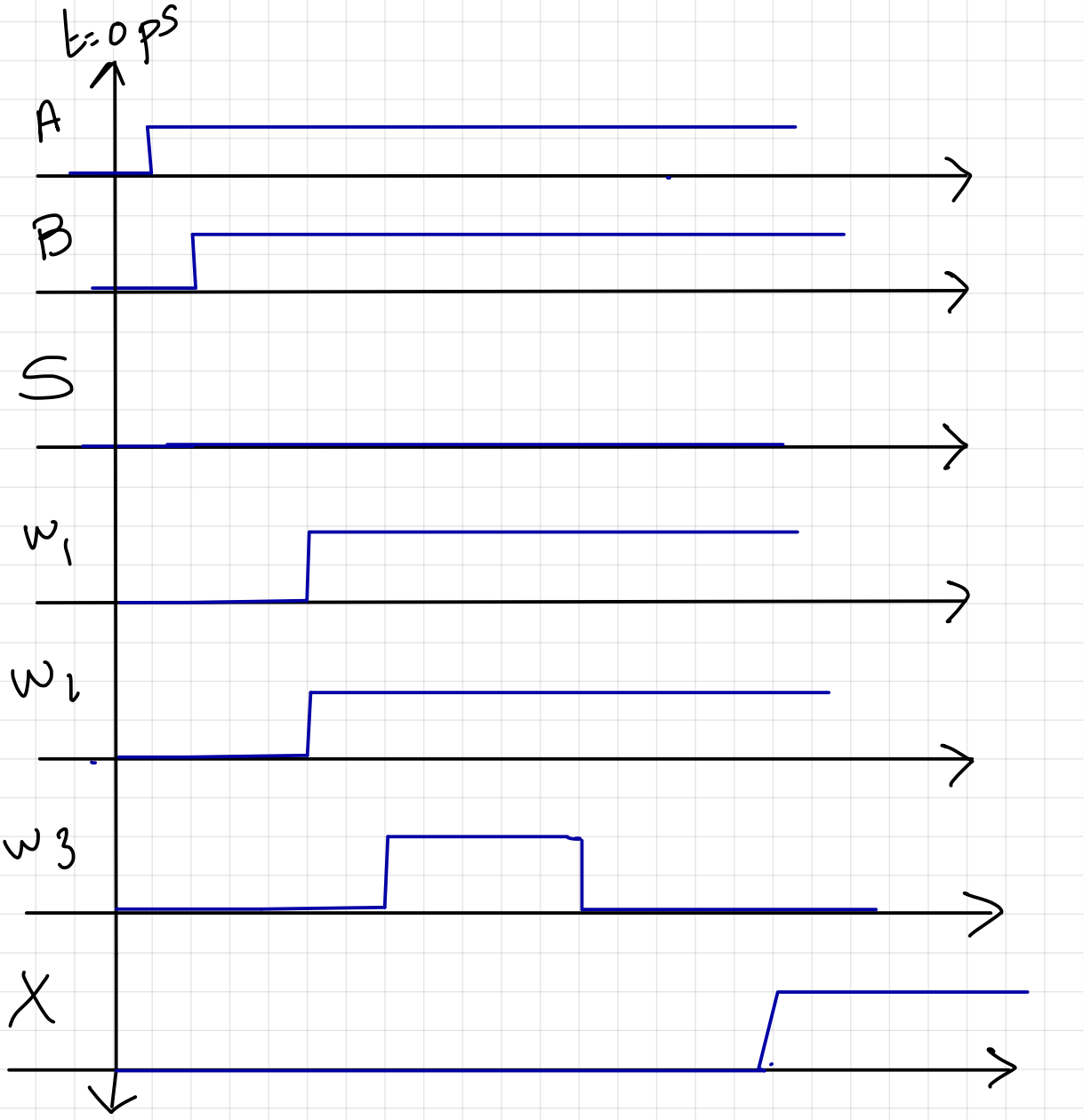
Circuit 4



test 4



Circuit 5



test 5