Ain Shams University
Faculty of Engineering
CSE Department

Juniors / Fall 2023
CSE 312: EDA
Group Project

Project Title:

ATM - based bank system

Project Description:

The project aims at practicing the complete ASIC flow by implementing the core of the bank ATM design as well as verification environment.
The student should assume all auxiliary devices like card handling, money counting, and timers exist. As well as assume account information like passwords, account numbers and balances exist locally with no need for database connection.
ATM System Can contain the following auxiliaries:

- Card handling
- Language used
- Card password
- Timers
- Operation (Deposit – Withdraw – Balance service)
- Balance exists
- Deposit value
- Withdraw value
- Another service wanted

Teamwork:

Every group should be divided into “Design Team” and “Verification Team”

- Design Team: to Put System Architect/Design, Write High Level Model of the System, Create Reference Model, Write the Verilog Code

- Verification Team: Create Testbench that covers (Test Stimulus using variation of directed, constraint random), Self-Checking TB Using Reference Model from Step#1, define design properties or assertion using PSL, and enable code coverage and create coverage report for Statement, Branch, FSM Coverage.

Delivery Time:

Upload Projects Deliverables at IMS portal @ 16 Dec 2022

Project Deliverables Discussion:

will be schedule on weekly basics using MS-Teams

- Each group will have 15 minutes time slot to show deliverables and go through project work.

Tools to Use

- QuestaSim

Deliverables List

- Design Document
- Verification Plan
- Slides (Group Member List, 1 Slide for System Architect, 1 Slide for High LEVEL Model, 1 Slides for FSM Design, 1 Slide for RTL, 1 Slides for Verification Techniques/Plans, 1 Slide for Verification Results, Conclusion/Summary)
- Zip File contains the Verilog Design, TB, Simulation Results

Grades:

- 15 Grade for Each Contributor