Digital Design Diploma

Assignment 2 [Extra]

Combinational Circuit Design

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1) Gray One-Hot Encoder:

```
Gray_One_Hot_Encoder.v > ...
 module Gray_One_Hot_Encoder (input [2:0] A, output reg [6:0] B);
 parameter USE_GRAY= 1; // Set to 1 for Gray encoding, 0 for One-hot encoding
 generate
     if (USE_GRAY) begin // Binary-Gray encoding logic
         always @(*) begin
              case (A)
                  3'b000: B = 7'b00000000; // 0 in Gray
                  3'b001: B = 7'b00000001; // 1 in Gray
                  3'b010: B = 7'b00000011; // 2 in Gray
                 3'b011: B = 7'b00000010; // 3 in Gray
                 3'b100: B = 7'b00000110; // 4 in Gray
                  3'b101: B = 7'b00000111; // 5 in Gray
                 3'b110: B = 7'b0000101; // 6 in Gray
                 3'b111: B = 7'b00000100; // 7 in Gray
                  default: B = 7'b0000000; // Default case
              endcase
         end
      else begin
         always @(*) begin
              case (A)
                  3'b000: B = 7'b00000000; // 0 in One-hot
                  3'b001: B = 7'b00000001; // 1 in One-hot
                  3'b010: B = 7'b00000010; // 2 in One-hot
                  3'b011: B = 7'b0000100; // 3 in One-hot
                 3'b100: B = 7'b0001000; // 4 in One-hot
                  3'b101: B = 7'b0010000; // 5 in One-hot
                  3'b110: B = 7'b0100000; // 6 in One-hot
                  3'b111: B = 7'b1000000; // 7 in One-hot
                  default: B = 7'b0000000; // Default case
              endcase
          end
  endgenerate
 endmodule
```

Figure 1: Q1 Code

4	Msgs															
USE_GRAY	32'd1	1														
⊞ - ♦ A	3'b110	(000	001		010		011		100		101		110		111	
≖- → B	7b0000101	(0000000	000000	1	000001	1	000001	0	000011	0	000011	1	000010	1	000010	0

Figure 2: Q1 Wave (Gray)

€ 1 +	Msgs								
♦ USE_GRAY	32'd0	0							
⊕ -♦ A	3'b110	000	001	010	011	100	101	110	111
■ -◆ B	7b0100000	0000000	0000001	0000010	0000100	0001000	0010000	0100000	1000000
<u> </u>									

Figure 3: Q1 Wave (One-Hot)

Figure 4: Q1 Testbench (Gray)

Figure 5: Q1 Testbench (One-Hot)

2) DEMUX:

```
DEMUX.v > ...

 module DEMUX(input D, input [1:0] S, output reg [3:0] Y);
 always @(*) begin
     case (S)
         2'b00:
                   Y = {3'b000, D};
         2'b01:
                  Y = \{2'b00, D, 1'b0\};
         2'b10:
                   Y = \{1'b0, D, 2'b00\};
         2'b11:
                   Y = \{D, 3'b000\};
         default: Y = 4'b0000;
     endcase
 end
endmodule
```

Figure 6: Q2 Code

```
DEMUX_tb.v > ...
  module DEMUX_tb ();
  reg D;
  reg [1:0] S;
  wire [3:0] Y;
  DEMUX DUT(D,S,Y);
  integer i,j;
  initial begin
      for (i = 0; i < 2; i = i + 1) begin
          for (j = 0; j < 4; j = j + 1) begin
              #10;
          end
      end
      $stop;
  end
  endmodule
```

Figure 7: Q2 Testbench

^	Msgs												
∲ S		00	01	10	11		00	01	10	11			
♦ D	1'b0												
+ - ♦ Y	4'b0000	0000					0001	0010	0100	1000			

Figure 8: Q2 Wave