Digital Design Diploma

# **Assignment 4**

# **Sequential Logic Design**

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| **Group** | G2 |

**Submitted to: Eng. Kareem Waseem**

1. **ALSU:**

Figure1: Q1 Code

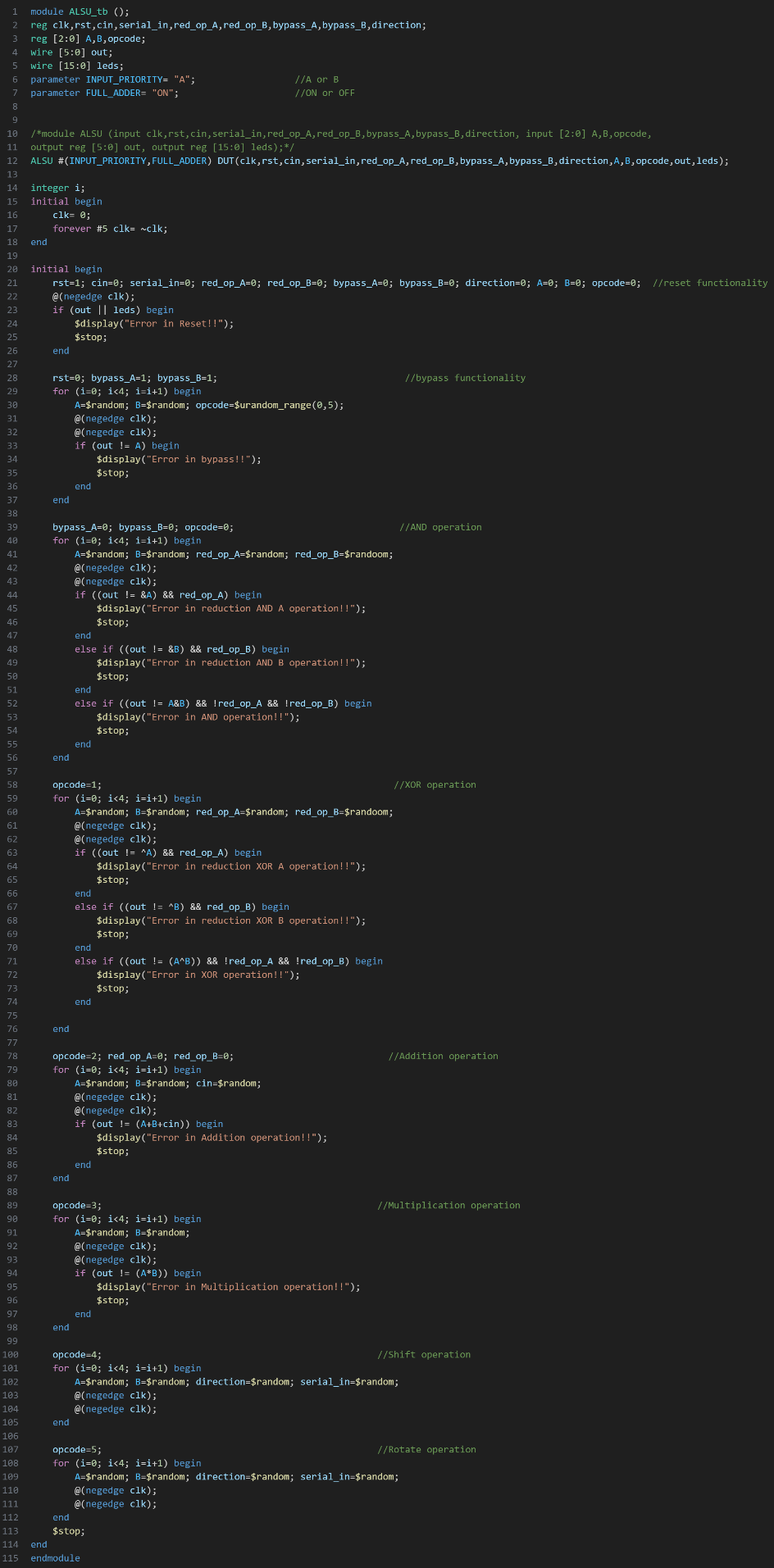
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Figure2: Q1 Testbench

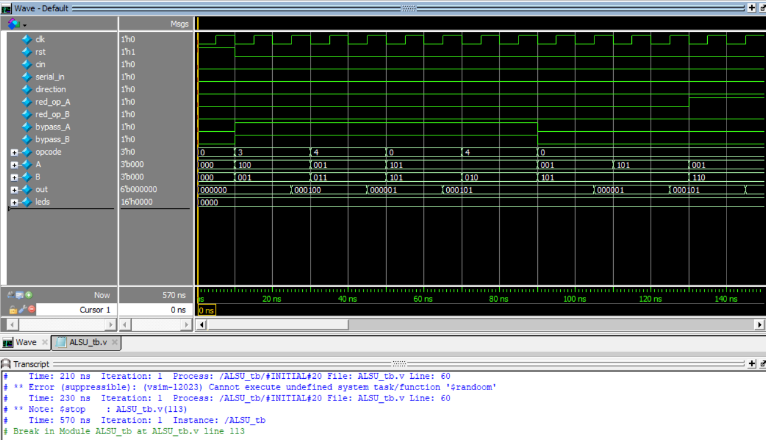
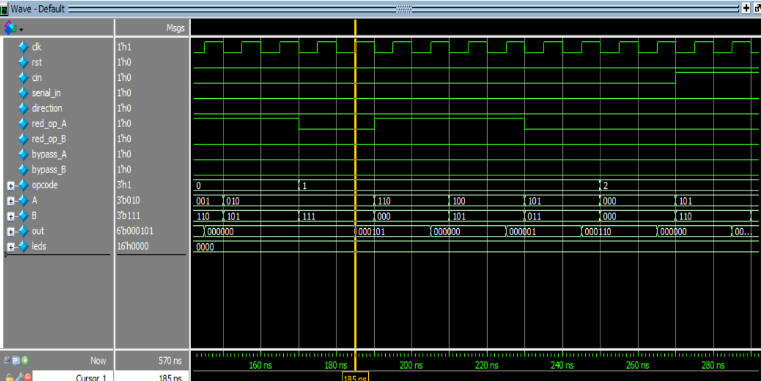
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Figure4: Q1 Wave2

Figure3: Q1 Wave1

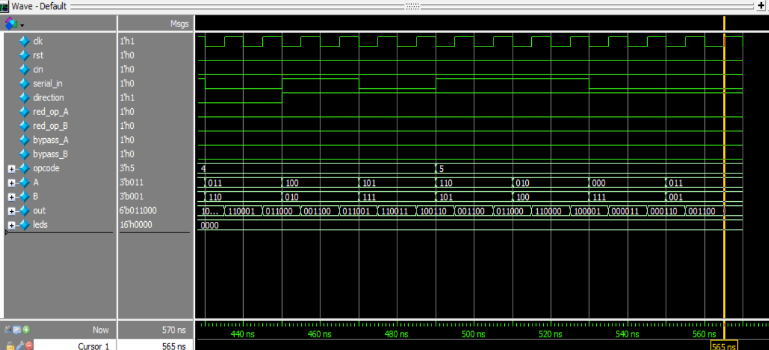
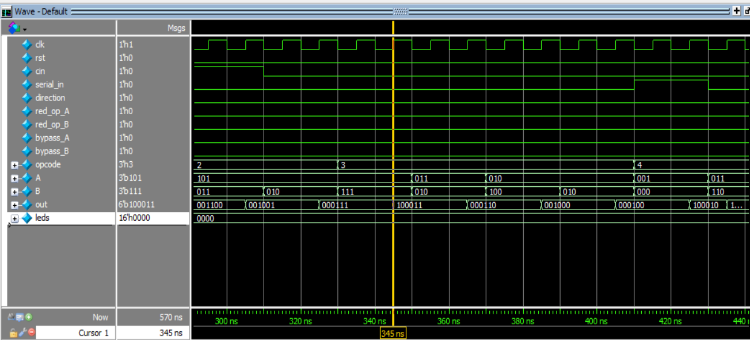
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Figure6: Q1 Wave4

Figure5: Q1 Wave3

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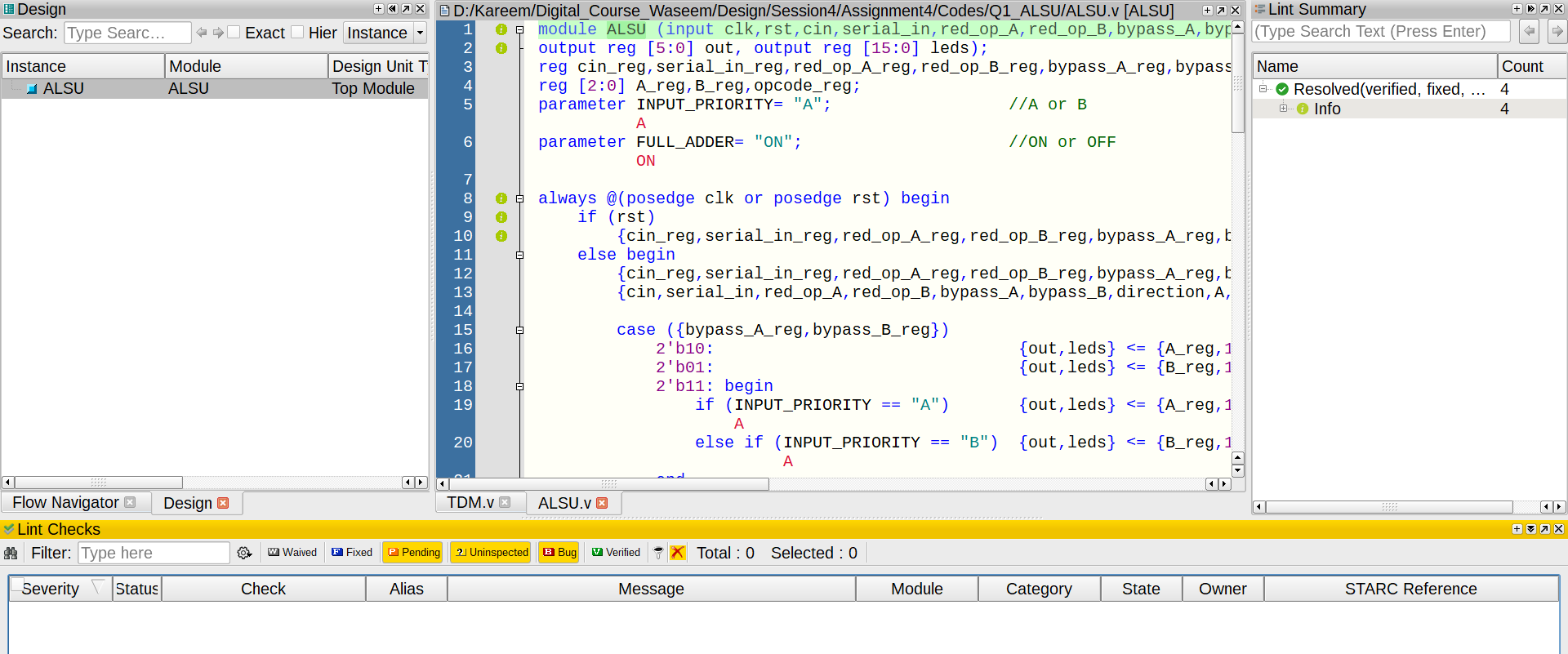
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Figure7: Q1 Lint

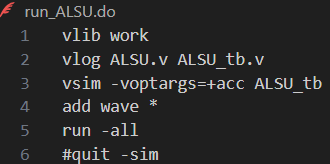
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Figure8: Q1 DO File

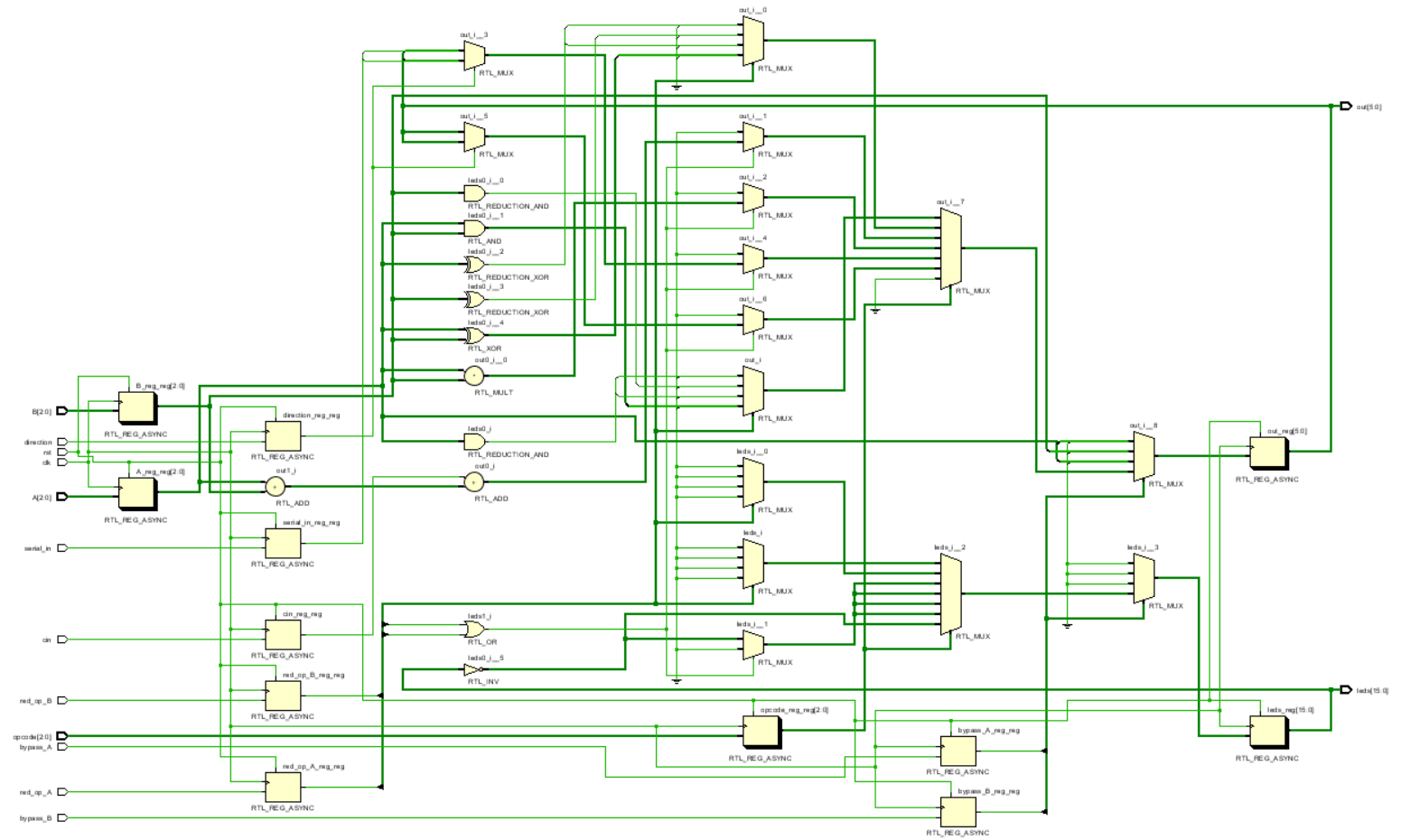
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Figure9: Q1 RTL

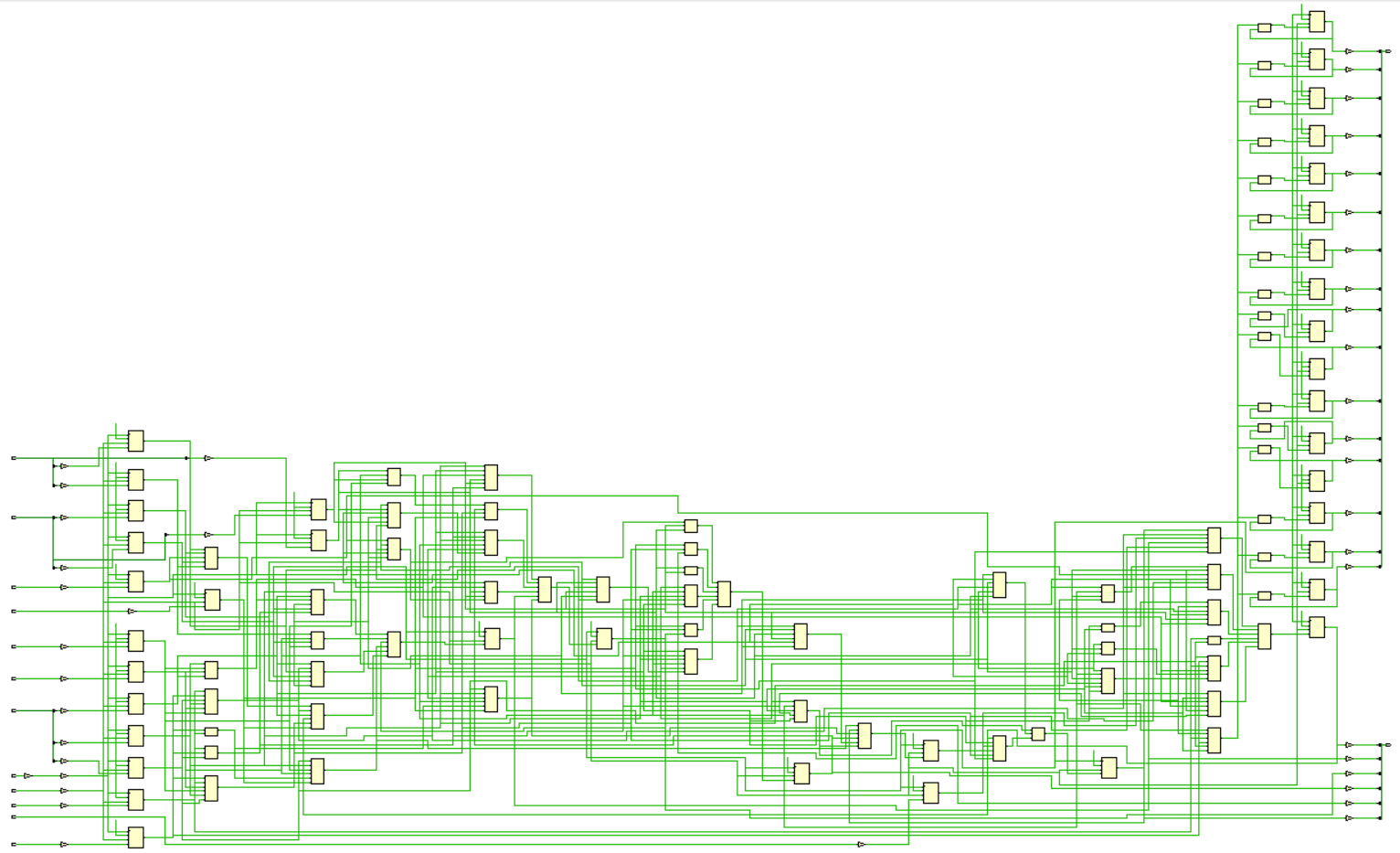
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Figure10: Q1 Synthesis

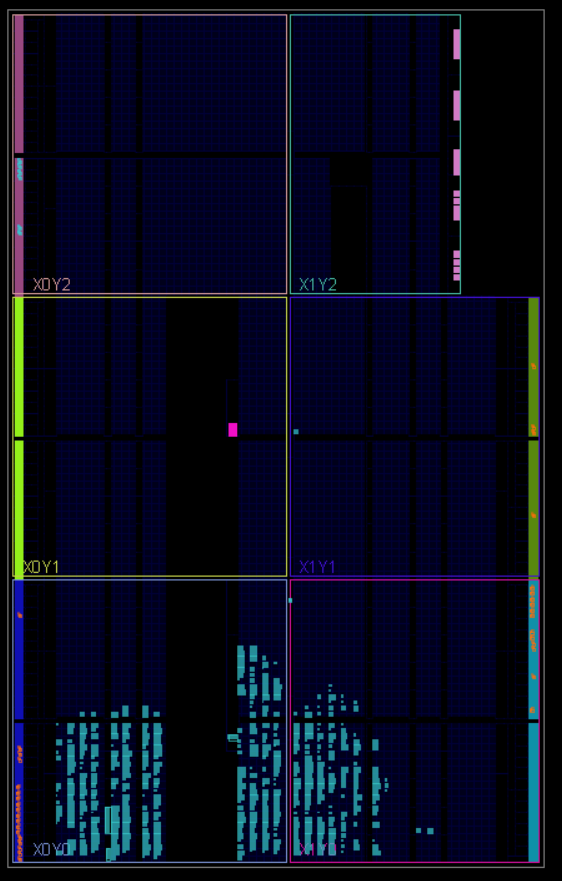
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Figure11: Q1 Device

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Figure12: Q1 Messages

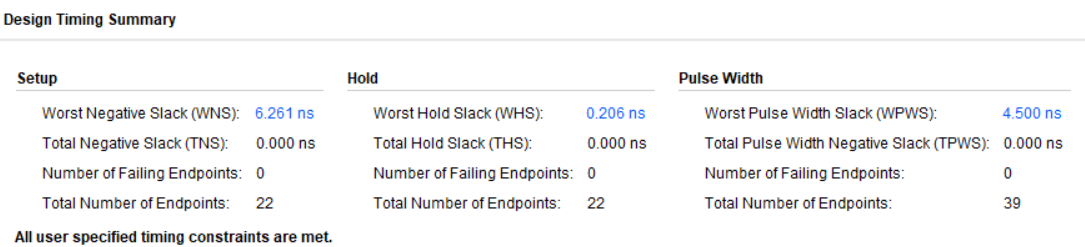
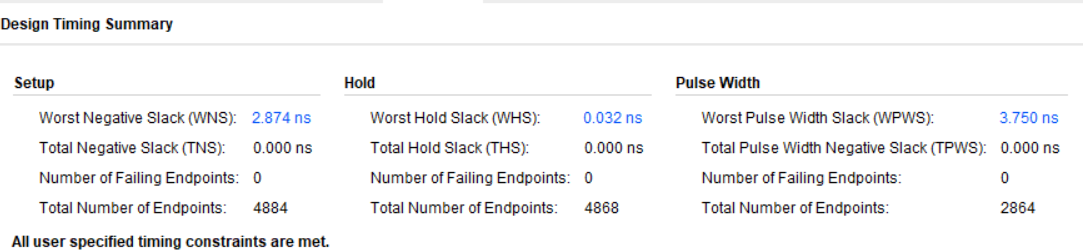
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Figure13: Q1 Synthesis Timing Report

Figure14: Q1 Implementation Timing Report

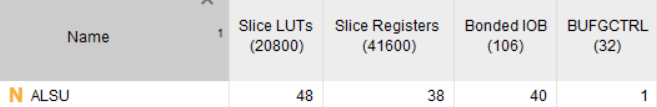
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Figure15: Q1 Synthesis Utilization Report

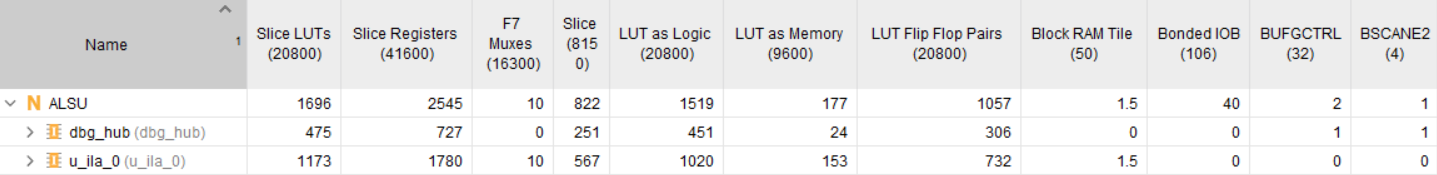
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Figure16: Q1 Implementation Utilization Report

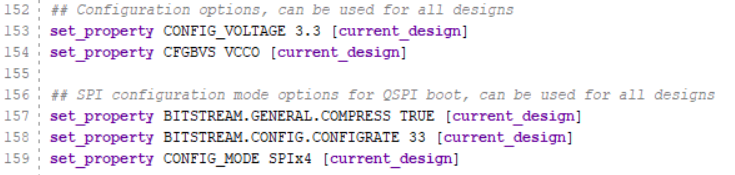
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Figure17: Q1 Constraints File

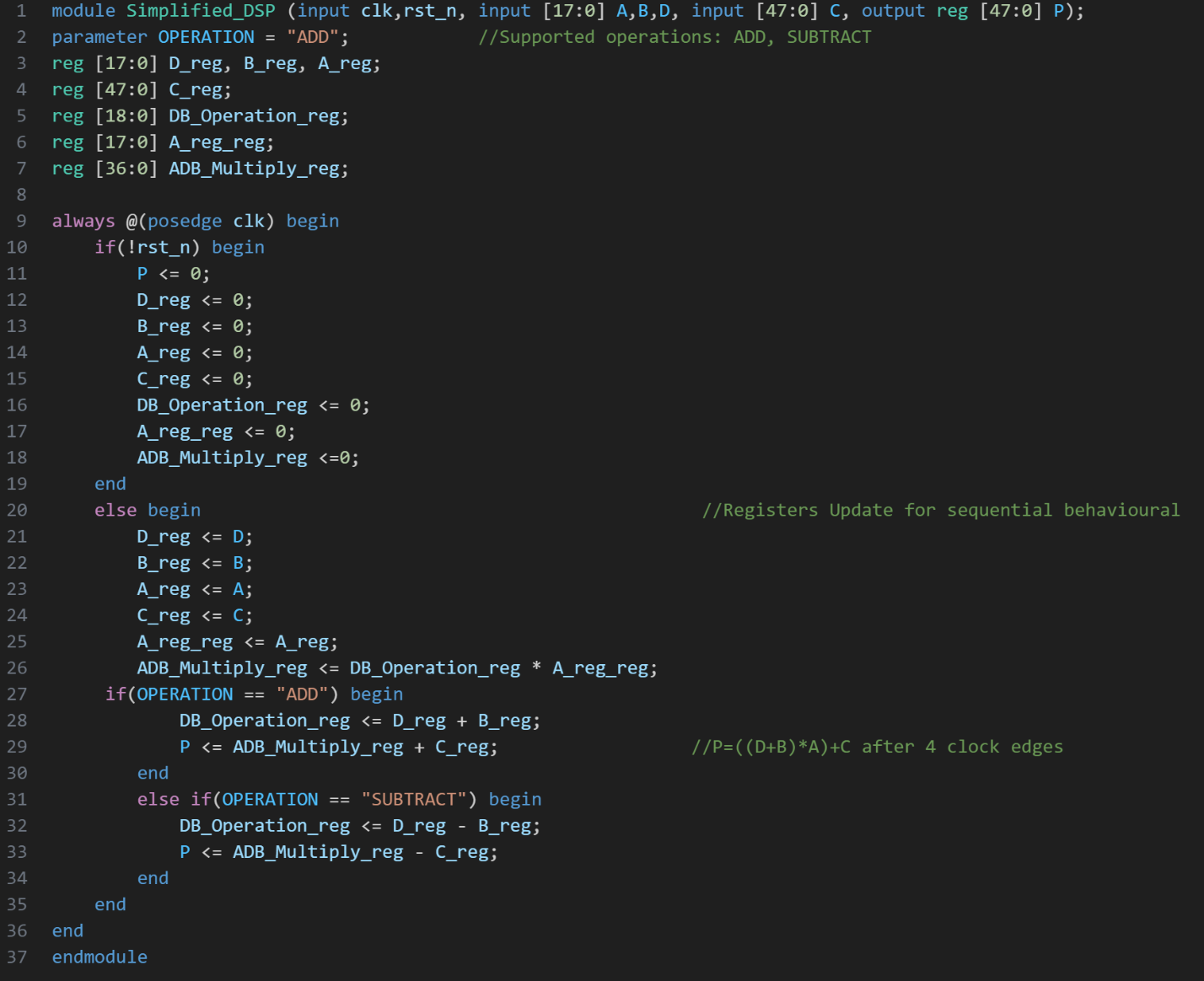
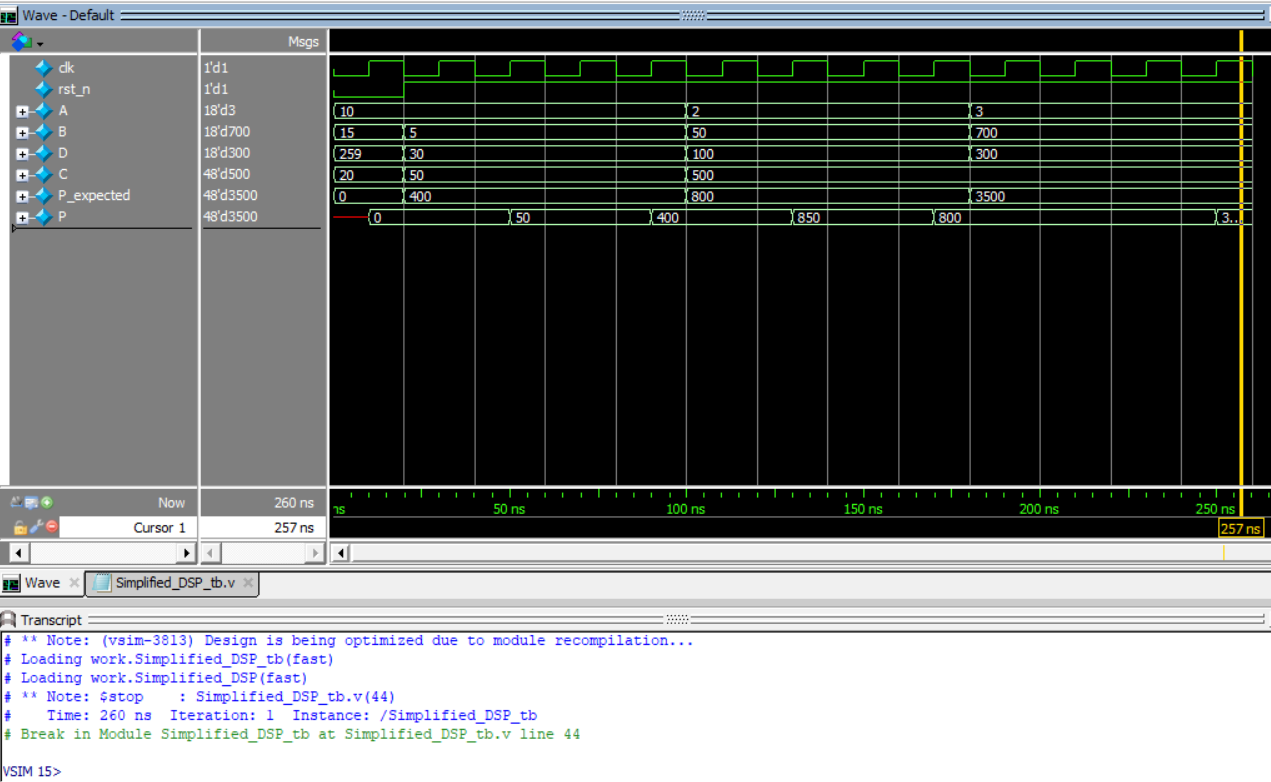
1. **Simplified DSP:**

Figure18: Q2 Code

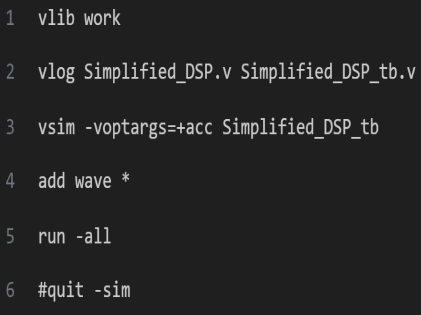
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Figure20: Q2 Do File

Figure19: Q2 Wave

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Figure21: Q2 Testbench

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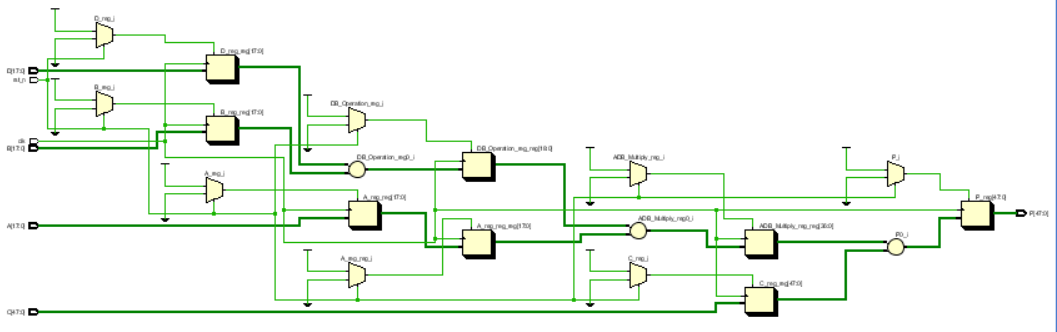
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Figure22: Q2 Lint

Figure23: Q2 RTL

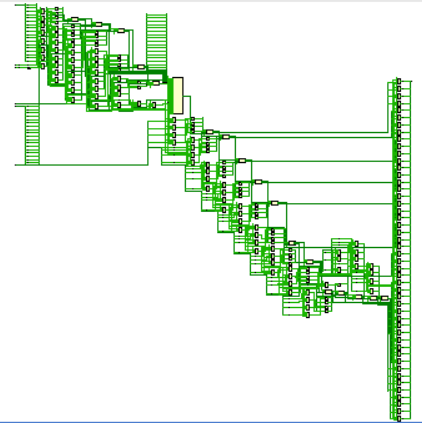
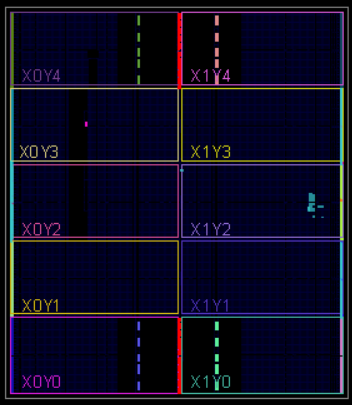
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Figure24: Q2 Synthesis

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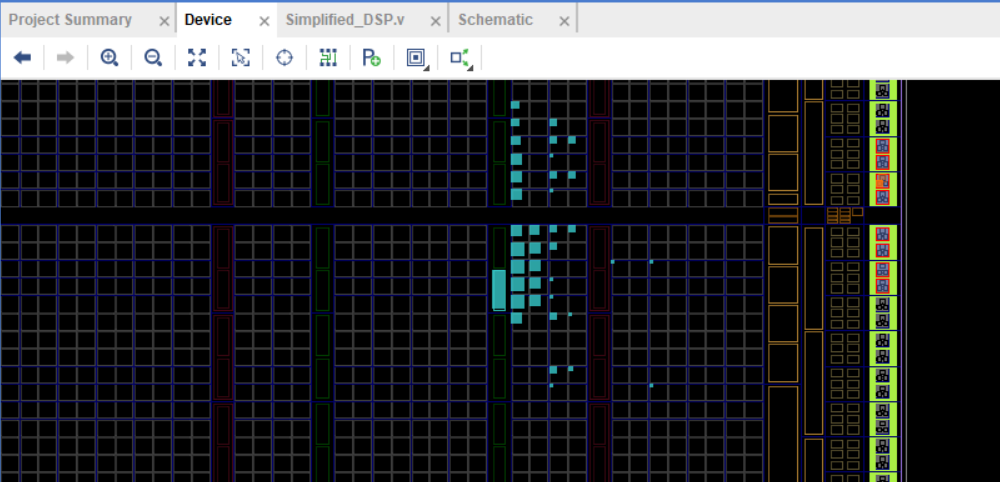
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Figure25: Q2 Device1

Figure26: Q2 Device2

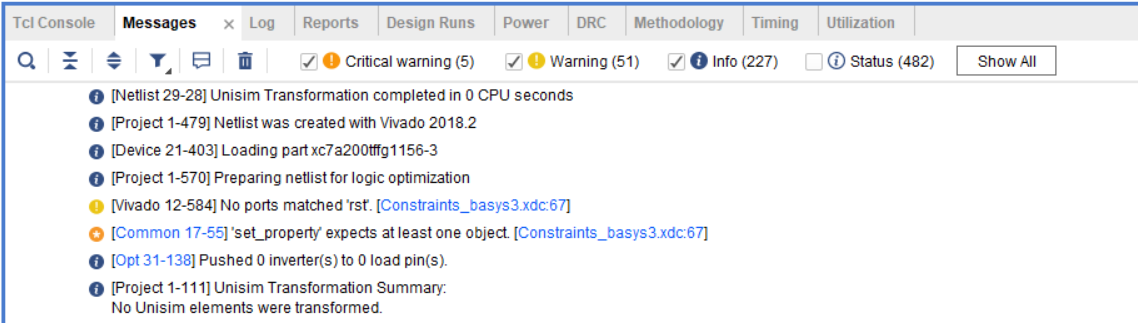
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Figure27: Q2 Messages

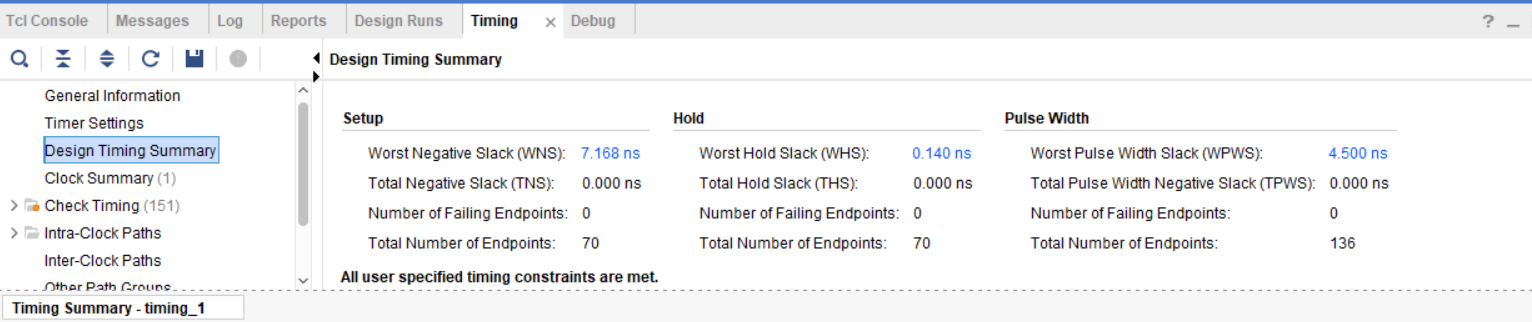
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Figure28: Q2 Synthesis Timing Report

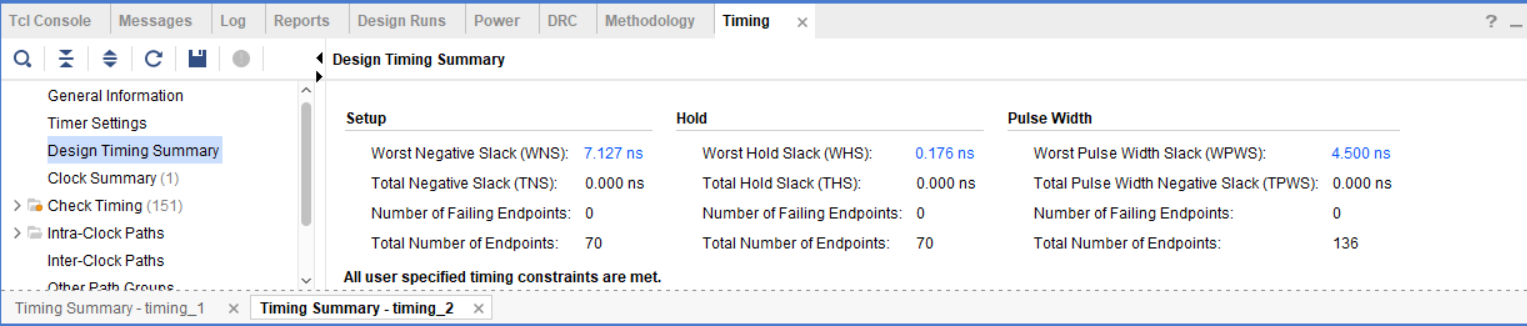
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Figure29: Q2 Implementation Timing Report

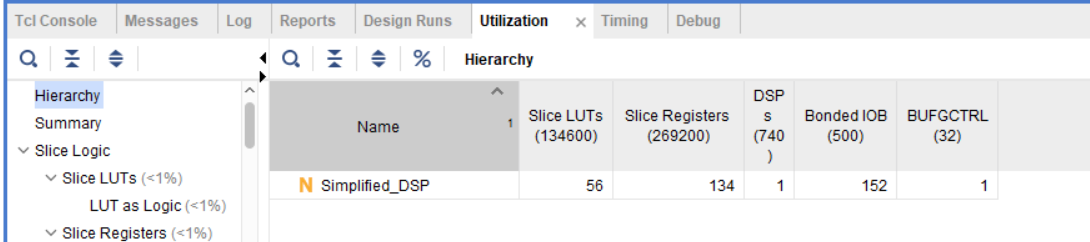
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Figure30: Q2 Synthesis Utilization Report

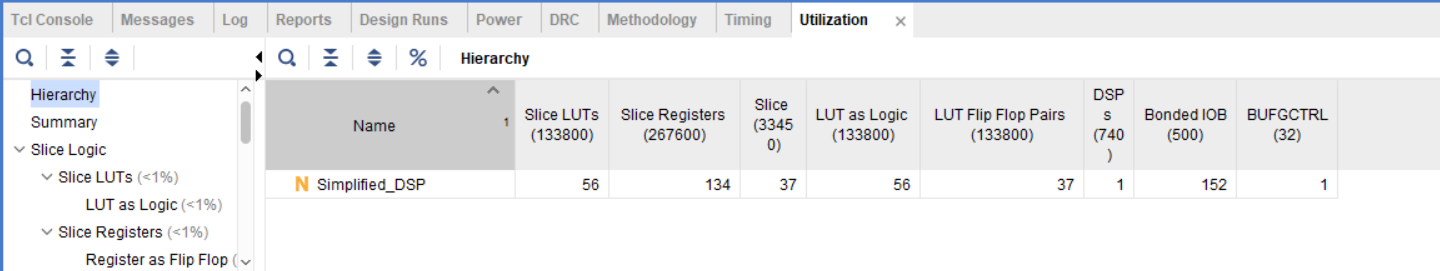
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Figure31: Q2 Implementation Utilization Report

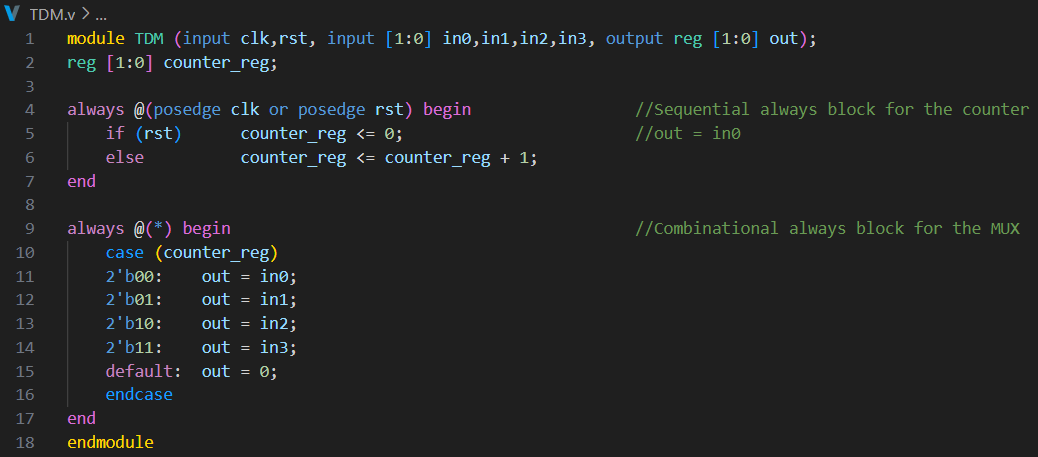
1. **TDM:**

Figure32: Q3 Code

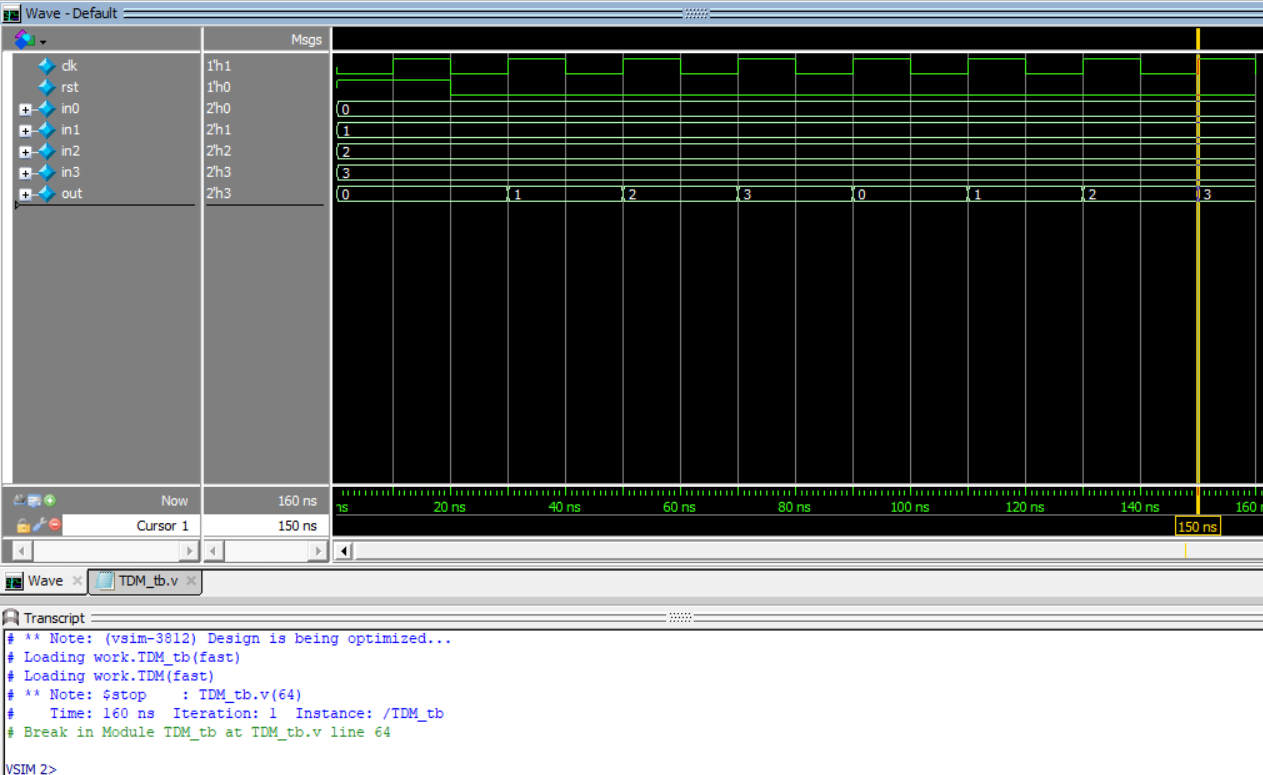
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Figure33: Q3 Wave

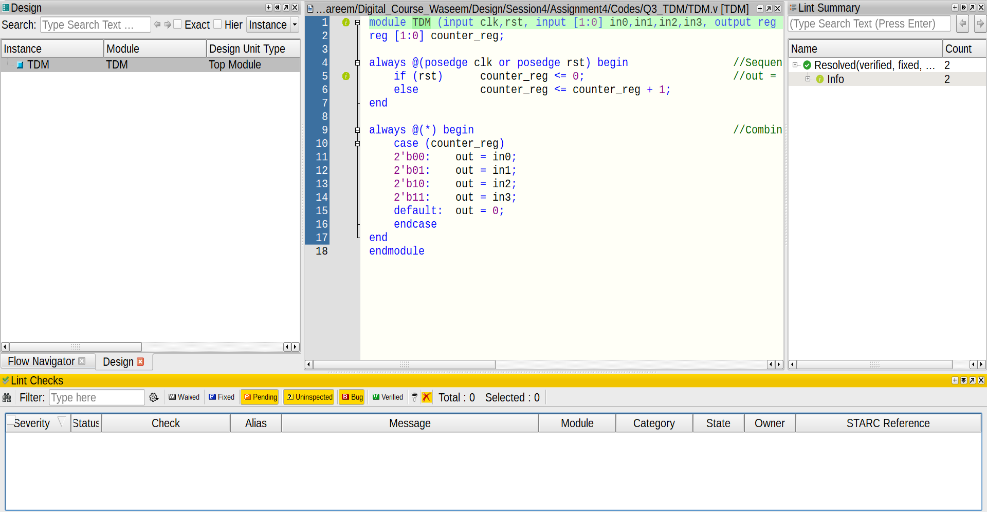
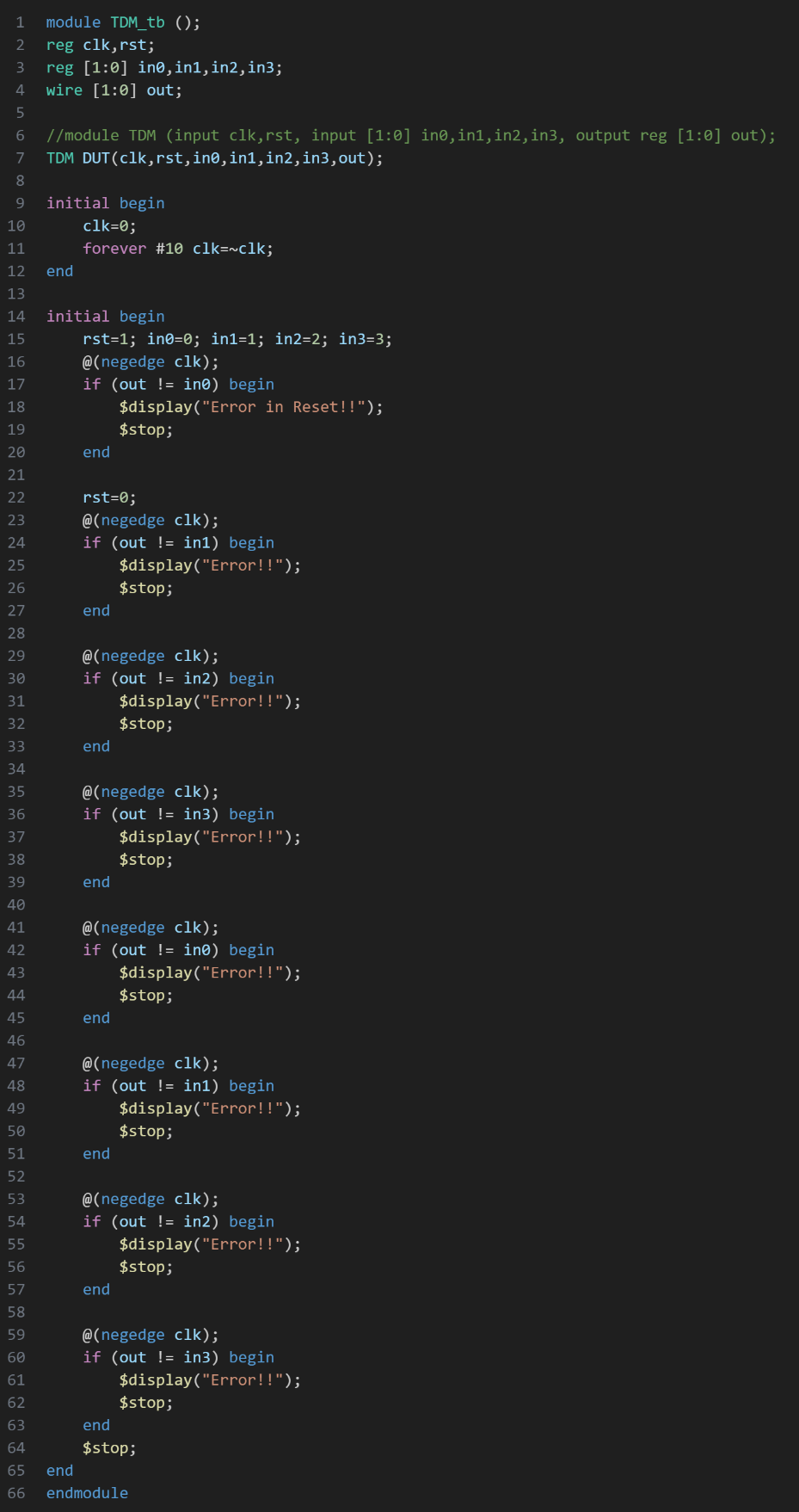
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Figure34: Q3 Lint

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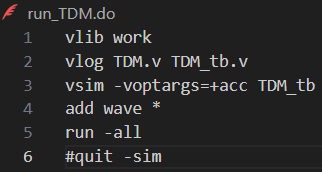
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Figure36: Q3 DO File

Figure35: Q3 Testbench

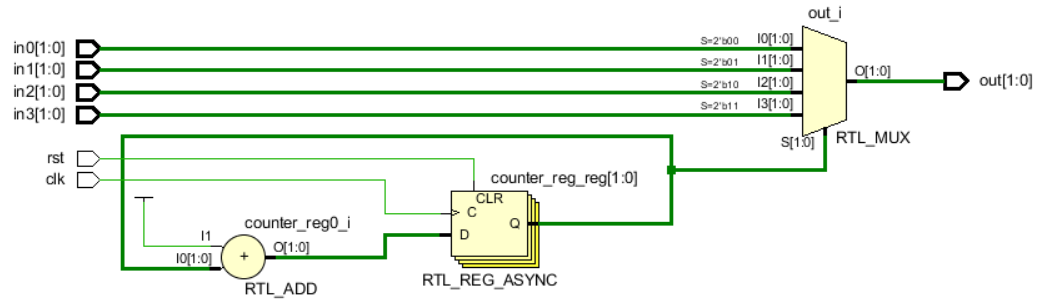
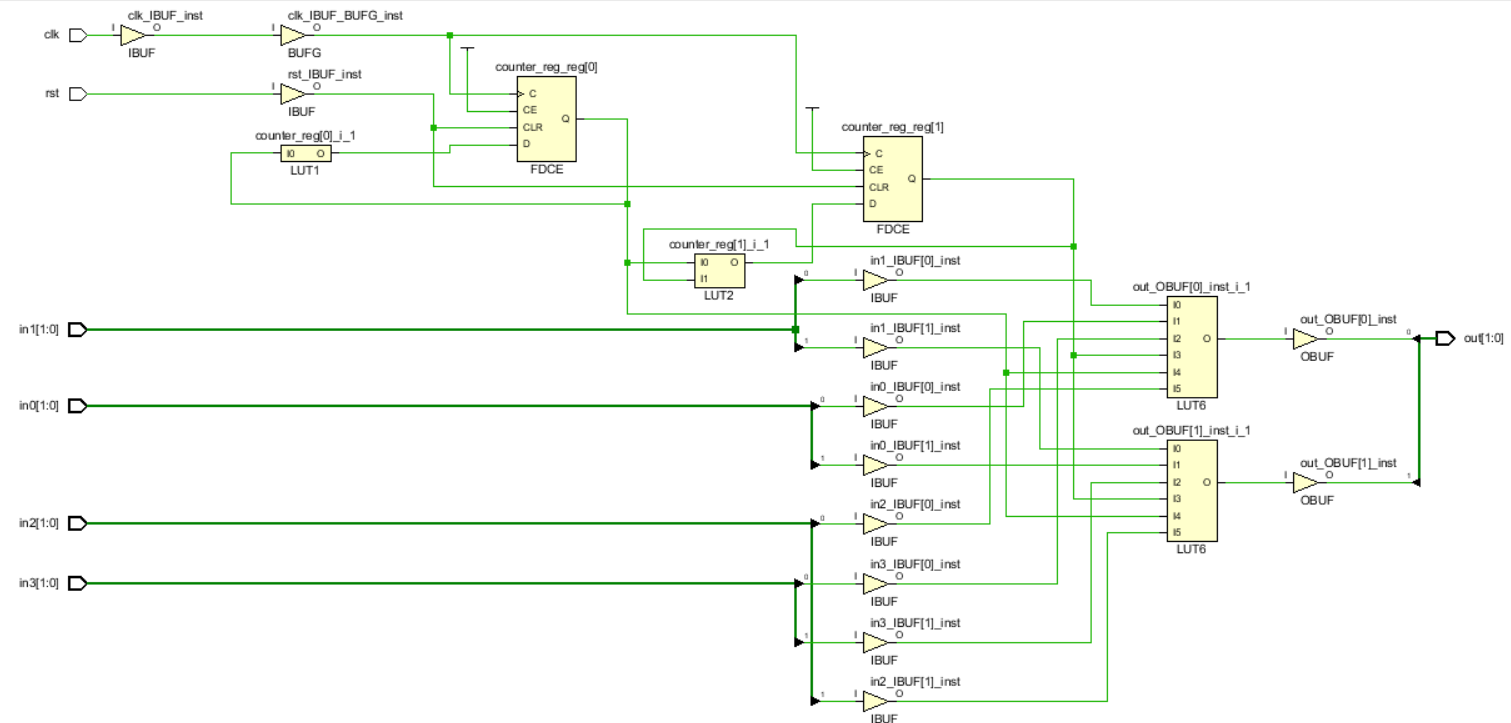
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Figure38: Q3 Synthesis

Figure37: Q3 RTL

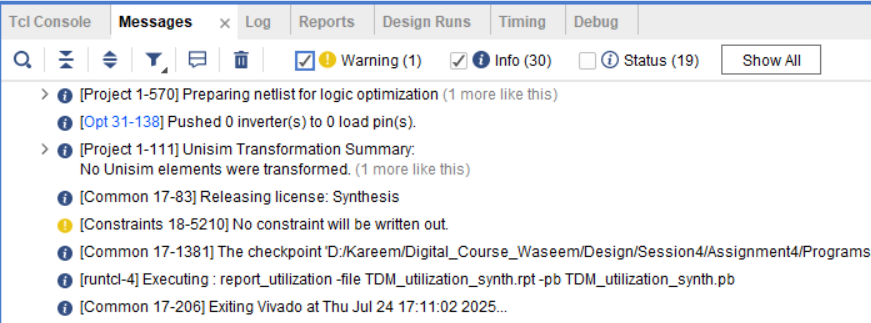
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Figure39: Q3 Messages

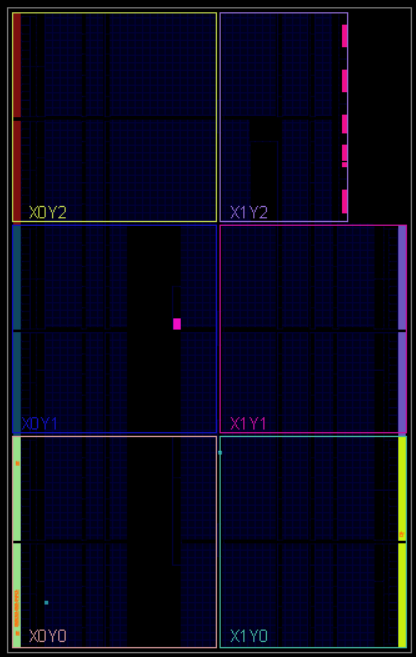
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Figure40: Q3 Device1

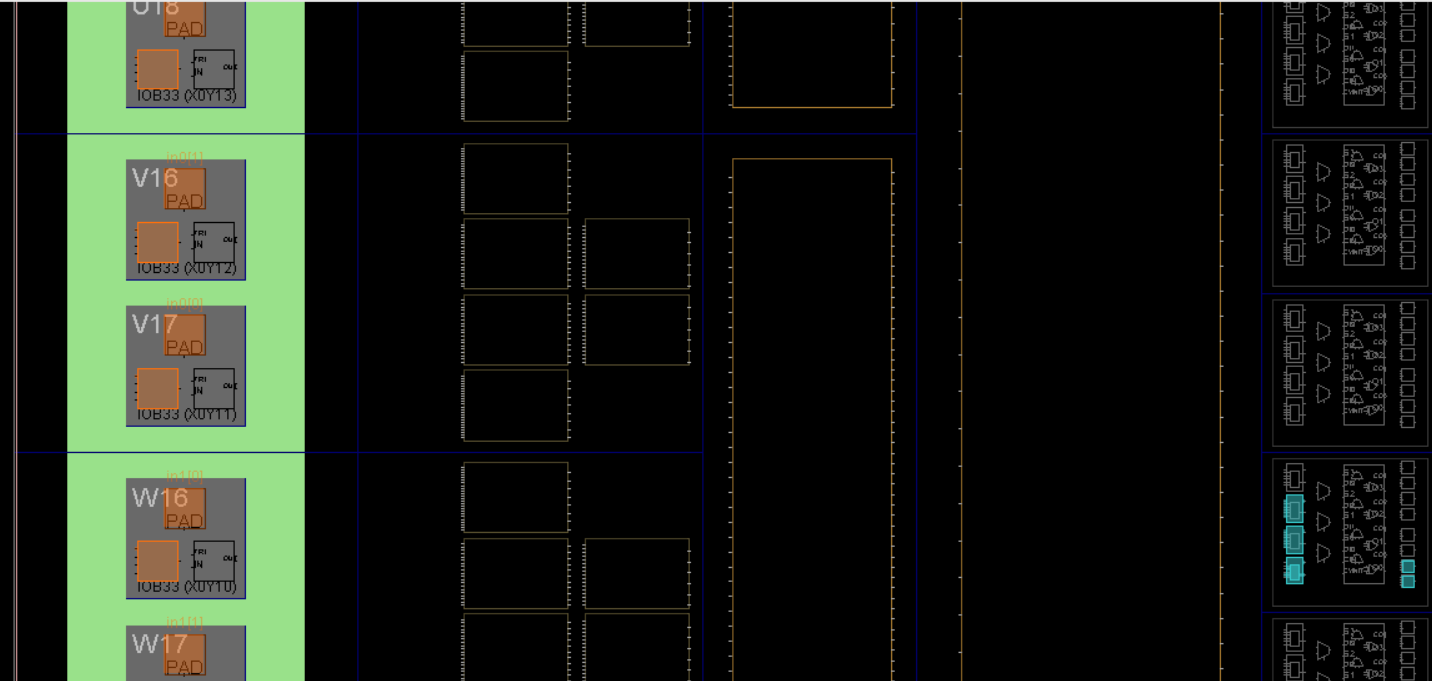
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Figure41: Q3 Device2

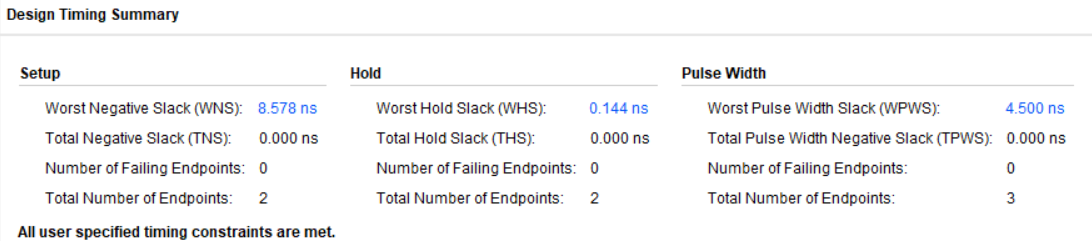
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Figure42: Q3 Synthesis Timing Report

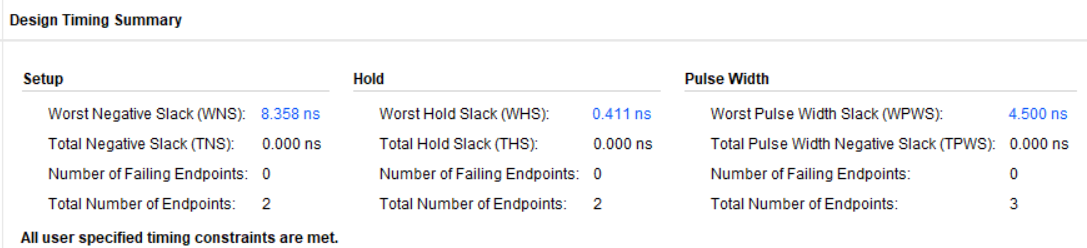
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Figure43: Q3 Implementation Timing Report

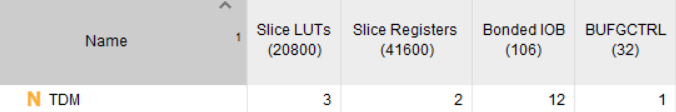
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Figure44: Q3 Synthesis Utilization Report

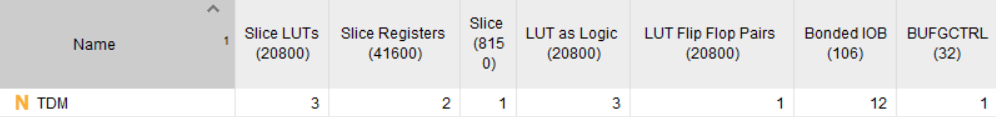
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Figure45: Q3 Implementation Utilization Report