Digital Design Diploma

Assignment 1

Combinational Circuit Design

Name	كريم حسن عاطف علي
Group	G2

Submitted to: Eng. Kareem Waseem

1)

```
Q1.v > Q1
1   module Q1 (input A,B,C,D,E,F,sel, output out,out_bar);
2   wire w0,w1;
3   assign w0= A&B&C;
4   assign w1= ~(D^E^F);
5   assign out = (sel) ? w1 : w0;
6   assign out_bar = ~out;
7   endmodule
```

Figure 1: Q1 Code

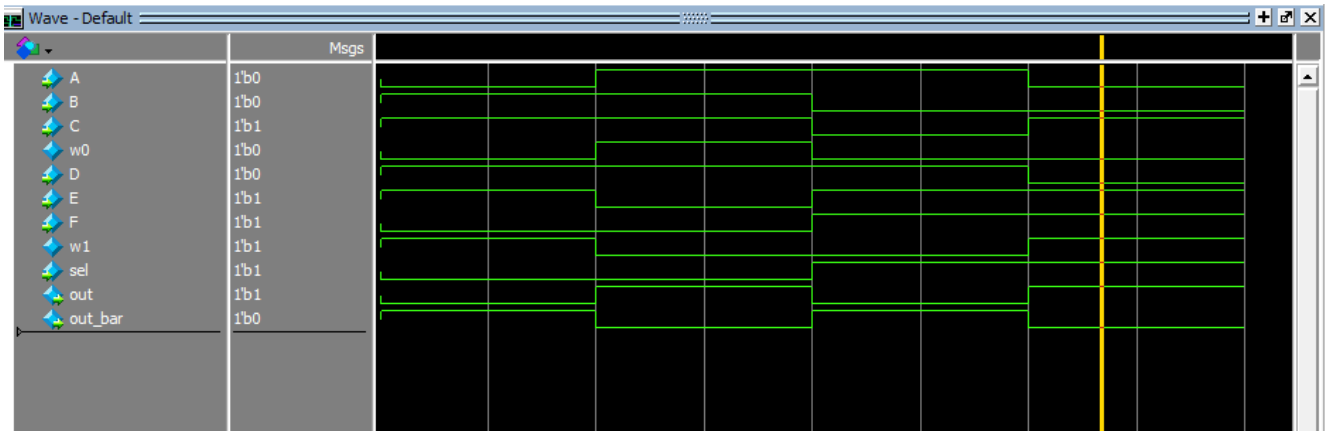

Figure2: Q1 Wave

2)

```
Q2.v > Q2
1   module Q2 (input A,B,C,sel, input [2:0] D, output reg out,out_bar);
2   reg w0,w1;
3   always @(*) begin
4   w0= (D[0] & D[1]) | D[2];
5   w1= ~(A^B^C);
6   out = (sel) ? w1 : w0;
7   out_bar = ~out;
8   end
9   endmodule
```

Figure 3: Q2 Code

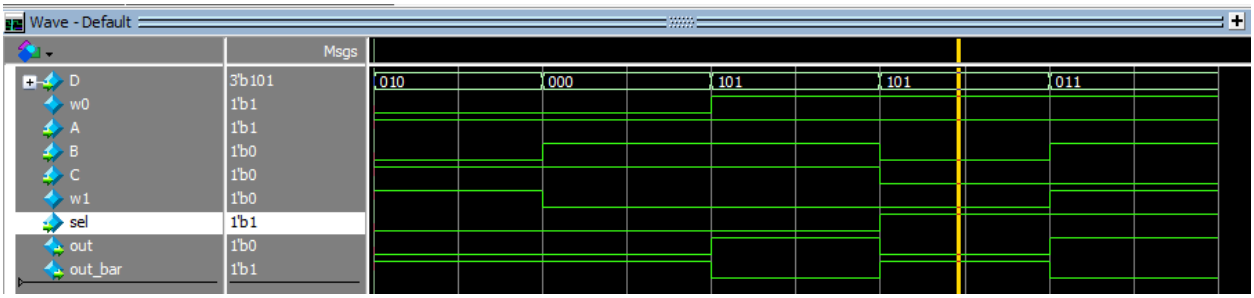

Figure 4: Q2 Wave

3)

```
Adder 4-bits.v > Adder_4bits
1   module Adder_4bits (input [3:0] A,B, output [3:0] C);
2   assign C = A + B;
3   endmodule
```

Figure 5: Q3 Code

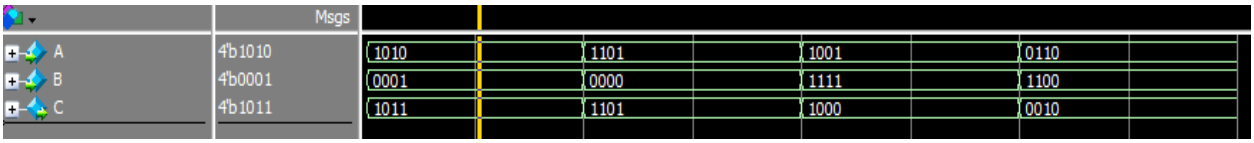

Figure 6: Q3 Wave

4)

```
Decoder 2x4.v
1   module Decoder2x4 (input [1:0] A, output [3:0] D);
2   assign D = (A==2'b00)? 4'b0001 :
3              (A==2'b01)? 4'b0010 :
4              (A==2'b10)? 4'b0100 :
5              (A==2'b11)? 4'b1000 : 4'b0000;
6   endmodule
```

Figure 7: Q4 Code

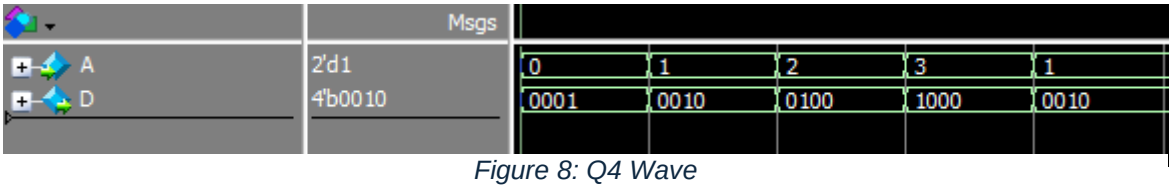

Figure 8: Q4 Wave

5)

```
Even Parity.v > Even_Parity
1   module Even_Parity (input [7:0] A, output [8:0] out_with_parity);
2   assign out_with_parity = {A,^A};
3   endmodule
```

Figure 9: Q5 Code

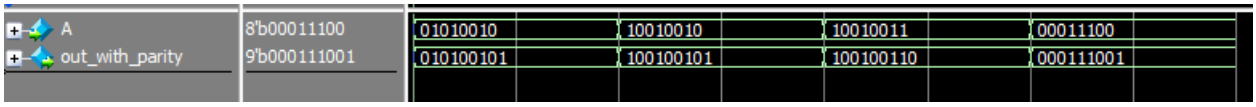

Figure 10: Q5 Wave

6)

ALU with 7-Segment display.v > ...

```
1   module ALU_with_7Segment_display #(parameter WIDTH = 4)
2   (input [WIDTH-1:0] A, B, input [1:0] opcode, input Enable, output reg a,b,c,d,e,f,g);
3
4   wire [WIDTH-1:0] result;
5
6   //N_bit_ALU #(parameter N=4) (input [N-1:0] in0,in1, input [1:0] opcode, output reg[N-1:0] out);
7   N_bit_ALU #(.N(WIDTH)) ALU(.in0(A), .in1(B), .opcode(opcode), .out(result));
8
9   always @(*) begin
10      if (Enable) begin
11          case (result)
12              4'b0000: {a,b,c,d,e,f,g} = 7'b1111110; // 0
13              4'b0001: {a,b,c,d,e,f,g} = 7'b0110000; // 1
14              4'b0010: {a,b,c,d,e,f,g} = 7'b1101101; // 2
15              4'b0011: {a,b,c,d,e,f,g} = 7'b1111001; // 3
16              4'b0100: {a,b,c,d,e,f,g} = 7'b0110011; // 4
17              4'b0101: {a,b,c,d,e,f,g} = 7'b1011011; // 5
18              4'b0110: {a,b,c,d,e,f,g} = 7'b1011111; // 6
19              4'b0111: {a,b,c,d,e,f,g} = 7'b1110000; // 7
20              4'b1000: {a,b,c,d,e,f,g} = 7'b1111111; // 8
21              4'b1001: {a,b,c,d,e,f,g} = 7'b1111011; // 9
22              4'b1010: {a,b,c,d,e,f,g} = 7'b1110111; // A
23              4'b1011: {a,b,c,d,e,f,g} = 7'b0011111; // B
24              4'b1100: {a,b,c,d,e,f,g} = 7'b1001110; // C
25              4'b1101: {a,b,c,d,e,f,g} = 7'b0111101; // D
26              4'b1110: {a,b,c,d,e,f,g} = 7'b1001111; // E
27              4'b1111: {a,b,c,d,e,f,g} = 7'b1000111; // F
28              default: {a,b,c,d,e,f,g} = 7'b0000000; // Off for other values
29          endcase
30      end
31      else begin
32          {a,b,c,d,e,f,g} = 7'b0000000; // Off when Enable is low
33      end
34  end
35  endmodule
```

Figure 11: Q6 Code

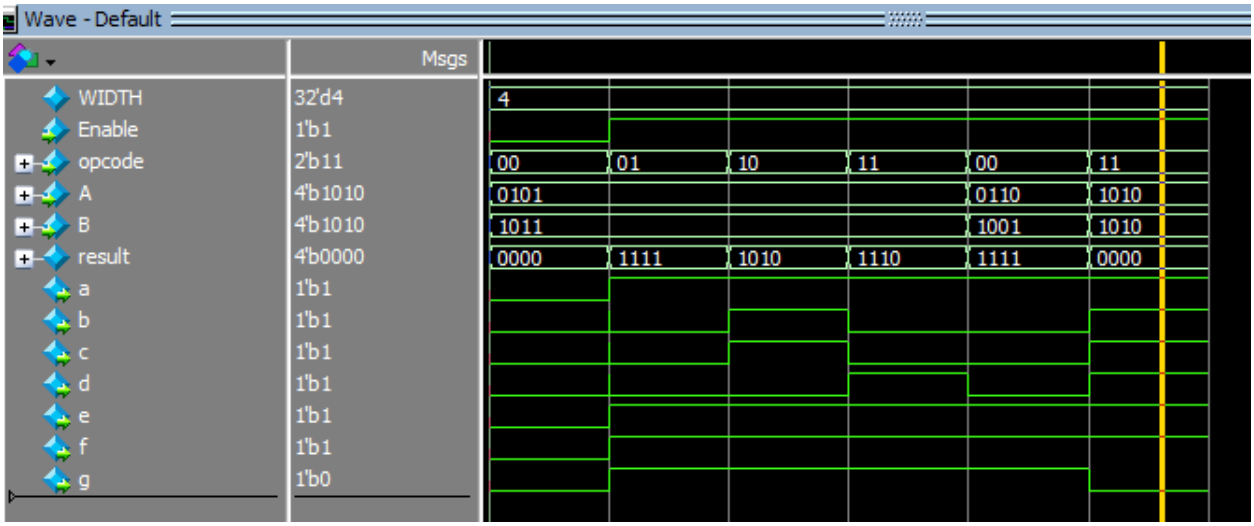

Figure 12: Q6 Wave