Digital Design Diploma

Assignment 1 [Extra]

Combinational Circuit Design

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1)

```
Q1) Ass1 Extra.v > ...
1   module Q1_Ass1_Extra (input [3:0] A, output out);
2   assign out= (A > 4'b0010 && A < 4'b1000)? 1 : 0;
3   endmodule
```

Figure 1: Q1 Code

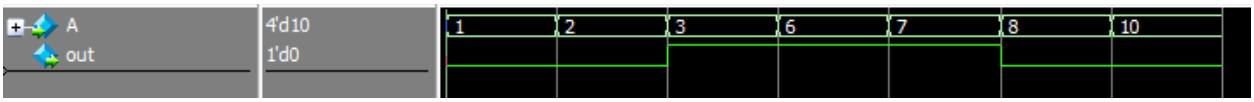

Figure2: Q1 Wave

2)

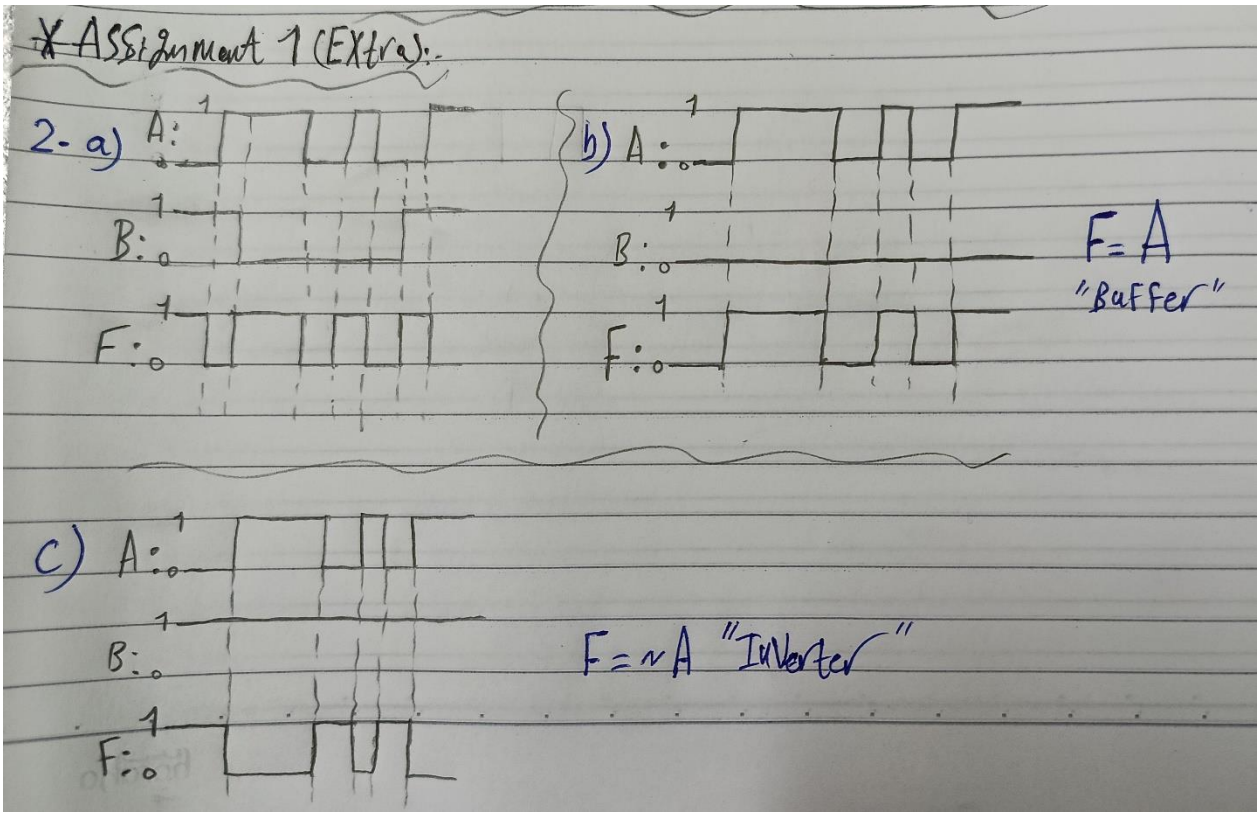

Figure 3: Q2 Wave

3)

```
Q3 Ass1 Extra.v > ...
1   module Q3_Ass1_Extra (input A,B,C, output F);
2   assign F = (A ^ B) & (B ~^ C) & C ;
3   //for F=1: A=0, B=1, C=1
4   endmodule
```

Figure 4: Q3 Code

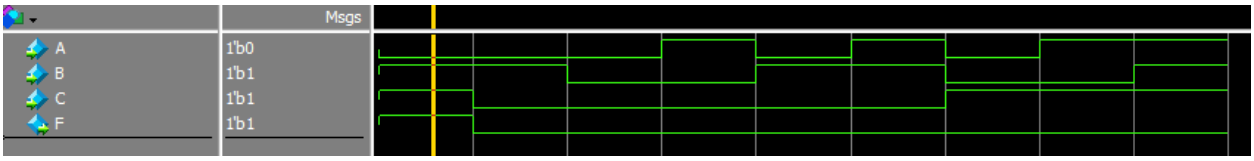

Figure 5: Q3 Wave

4)

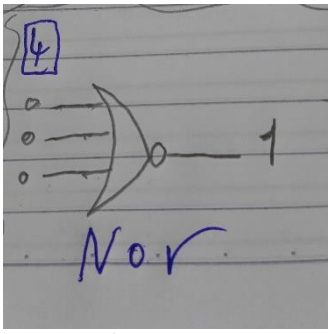

Figure 6: Q4

5)

```
Q5) ALU Ass1 Extra.v > ...
1   module ALU_Ass1_Extra(input A, B, Ainvert, Binvert, CarryIn, input [1:0] Operation,
2   output CarryOut, Result);
3
4   wire a,b;
5
6   assign a= (Ainvert)? ~A : A;
7   assign b= (Binvert)? ~B : B;
8   assign {CarryOut, Result} = (Operation==2'b00)? {1'b0,(a & b)}:
9                               (Operation==2'b01)? {1'b0,(a | b)}:
10                              (Operation==2'b10)? a + b + CarryIn: {2'b0};
11  endmodule
```

Figure 7: Q5 Code

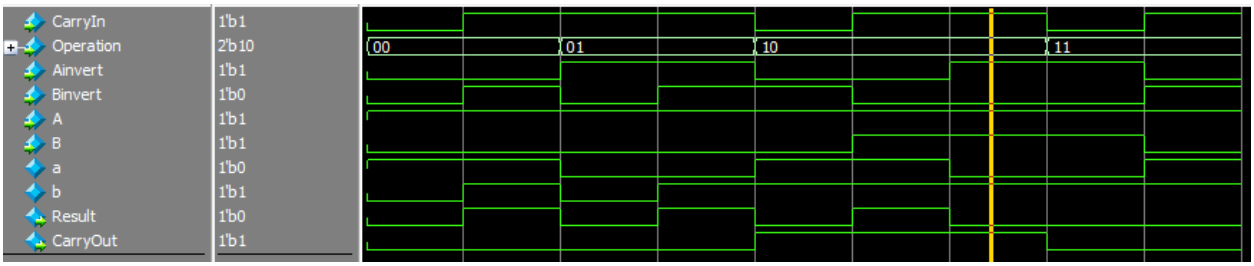

Figure 8: Q5 Wave