COMP4300
Computer Architecture, Fall 2017
Final Examination
December 13, 2017

NAME SOLUTION JET

(If you are unsure of the answer to any question, tell all your reasoning for giving the answer you did, for partial credit)

1. (15 points) Suppose that a given machine spends 40% of its execution time doing conditional jumps. The design team for the manufacturer is considering adding dedicated hardware to calculate jump conditions and jump target addresses to speed up conditional jumps. Suppose that simulation indicates the machine overall will have a 1.5x speedup with that additional hardware. What is the speedup of conditional jump instructions ONLY due to that optimization?

0.4 = time spent on jumps before

s = speedup of conditional jumps

$$\frac{1}{1.5} = (1-.4) + \frac{0.4}{s}$$

$$0.66 - 0.6 = \frac{0.4}{s}$$

$$0.06s = 0.4$$

$$s = 6.01$$

2. (6 points) What is the theoretical maximum speedup you could get in the previous problem by speeding up conditional jumps?

If jumps take zero time, new execution time is 0.6 of old

$$S = \frac{1}{0.6} = 1.67$$

3. (5 points) Suppose on a non-pipelined single-processor machine, you have the following breakdown: alu instructions make up 35% of the dynamic instruction count, and take 1 cycle to execute. Load/store instructions take 5 cycles to execute and make up 20% of the mix. Jumps take 2 cycles and make up 15%. All other instructions average 1.5 cycles. What is the average CPI?

$1 \times 0.35 + 5 \times 0.2 + 2 \times 0.15 + 1.5 \cdot 0.3$

$.35 + 1 + 0.3 + 0.45 = 2.1$

4. (5 points) Suppose the architecture above is pipelined. If there are no stalls for any reason, what is the new CPI?

Ideal pipelined CPI = 1

5. (8 points) If Load/store instructions generate 2 stalls on average, alu 0.2 stalls, and jumps cause 1 stall, what is the actual pipelined cpi?

$$cpi = 1 + \underset{L/S}{0.2 \cdot 2} + \underset{ALU}{0.35 \cdot 0.2} + 0.15 \cdot 1$$

$$= 1 + 0.4 + 0.07 + 0.15$$

$$= 1.62$$

6. (10 points) Describe two CPU design techniques that exploit instruction level parallelism to give an average CPI of less than one?

superscalar

VLIW

7. (5 points) Which would be more suited to a vector architecture: computing the eigenvalues of a matrix of floating point numbers, or compiling a large program?

eigenvalues

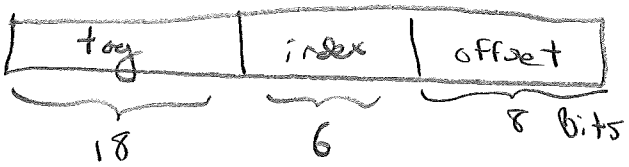
8. (5 points) "The nVidia GPU architecture is both MIMD and SIMD". Explain how this can be.

Each streaming multiprocessor executes SIMD instructions
The Giga Thread Engine schedules MIMD threads

9. (7 points) Why was cache memory common on mainframe computers in the 1960's with magnetic core memory, and in today's microprocessor-based computers, but not in computers of the late 1970's and early 1980's which used early integrtated-circuit-based DRAM and SRAM memory?

In both 1960's and today there was a large speed mismatch between cpu & memory.
That went away for a time in early days of DRAM/SRAM main memory.

10. (7 points) In a machine with 32-bit physical addresses, a cache line is 256 bytes in size. The cache can hold 32K bytes. It is 2-way set associative. How many bits is the index value used with this cache?



32K / 256 = 128 Cache lines

⇒ 64 sets since 2-way S.A.

⇒ 2^6 sets ⇒ 6 bit index

11. (10 points) In the cache system described in question 10, the following sequence of memory reads occurs. At the end of the sequence what blocks will be in each set of the cache? Give the set number and the tag number for the non-empty blocks in each set.

X 0x5fff03e2 — 0101 1111 1111 1111 00|00 0011| e2

0x5ff103f7 - 0101 1111 1111 0001 00|00 0011| f7

0x5fff03ab - 0101 1111 1111 1111 00|00 0011| ab

0x5f1f5100 - 0101 1111 0001 1111 01|01 0001| 00

0x00000000 } tag 0, index 0

0x00000001 }

set 000011: tag 0101 1111 1111 0001 00

tag 0101 1111 1111 1111 00

set 010001: tag 0101 1111 0001 1111 01

set 000000: tag 0000 0000 0000 0000 00

12. (10 points) Does Moore's Law still apply? Be sure to address transistor count and clock speed.

Yes transistor count

No clock speed

13. (7 points) Assuming there are 1.8 memory references per instruction in a machine with a single-level integrated instruction- and data- cache, and that the hit time for the cache is 1 cycle, the miss time is 10 cycles, and the miss rate is 1%. What is the average delay per instruction due to memory access?

$1.8\left(1 + 0.01 \cdot 10\right) = 1.8(1+.1) = 1.1 \cdot 1.8 = 1.98$