Winbond

64 K × 8 HIGH SPEED CMOS STATIC RAM

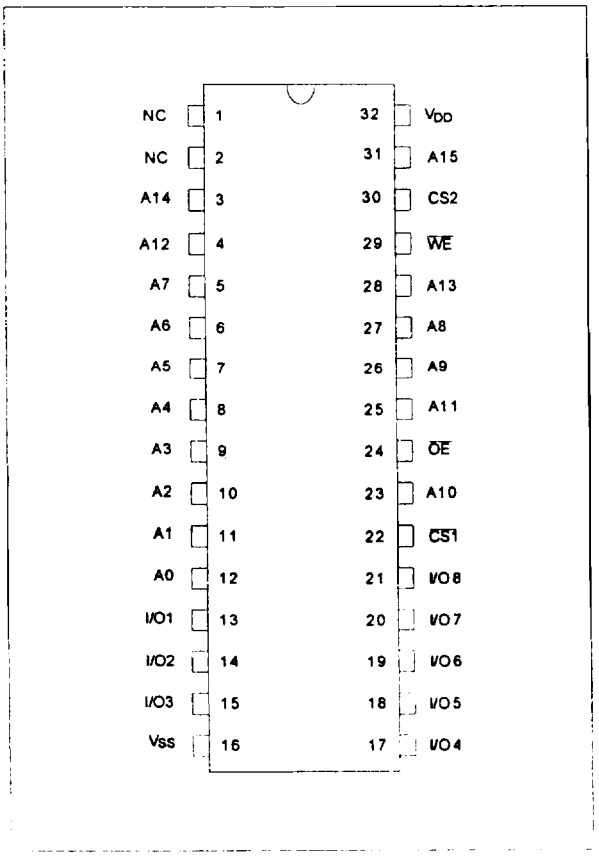
GENERAL DESCRIPTION

The W24M512A is a high speed, low power CMOS static RAM organized as 65536 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

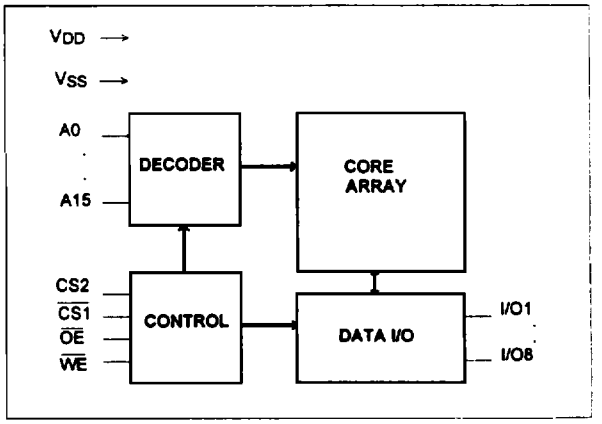
FEATURES

- High speed access time: 15/20 nS (max.)
- Low power consumption:
  - Active: 250 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Output level: 3.3 V
- Available packages: 32-pin 300 mil SOJ and skinny DIP

PIN CONFIGURATIION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
Vss	Ground
NC	No Connection

Publication Release Date: September 1994
Revision A1

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to +7.0	V
Input/Output to Vss Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1-I/O8	V_{DD} CURRENT
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

(V_{DD}= 5V ± 5%, Vss= 0V, Ta= 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN}= Vss to V_{DD}		-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$= Vss to V_{DD} $\overline{CS1}$= V_{IH} or CS2= V_{IL} or $\overline{OE}$= V_{IH} or $\overline{WE}$= V_{IL}		-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL}= +8.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}= -4.0 mA		2.4	-	3.4	V
Operating Power Supply Current	I_{DD}	$\overline{CS1}$= V_{IL}, CS2= V_{IH} I/O= 0 mA, Cycle= Min	15	-	-	200	mA
		Duty= 100%	20	-	-	160	
Standby Power Supply Current	I_{SB}	$\overline{CS1}$= V_{IH}, or CS2= V_{IL} Cycle= MIN, Duty= 100%		-	-	30	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2 V or CS2 ≤ 0.2 V		-	-	10	mA

Note: Typical characteristics are at V_{DD}= 5V, Ta= 25° C

CAPACITANCE

(V_{DD}= 5V, Ta= 25° C, f= 1MHz)

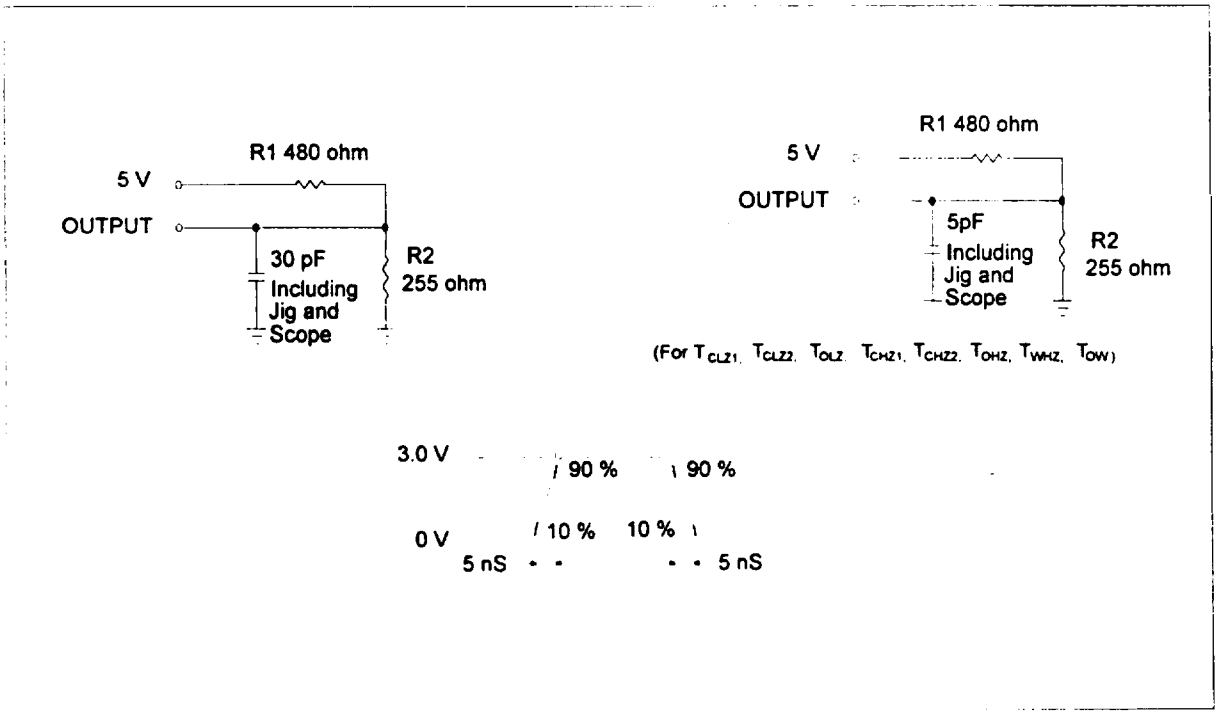
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN}= 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT}= 0V	10	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0 V to 3 V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5 V
Output Load	C_L= 30 pF, I_{OH}/I_{OL}= -4 mA/8 mA

AC TEST LOADS AND WAVEFORM



AC CHARACTERISTICS

(VDD= 5V ± 5%, Vss= 0V, Ta= 0 to 70° C)

(1) Read Cycle

PARAMETER		SYM.	W24M512A-15		W24M512A-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		TRC	15	-	20	-	nS
Address Access Time		TAA	-	15	-	20	nS
Chip Select Access Time	$\overline{CS1}$	TACS1	-	15	-	20	nS
	CS2	TACS2	-	15	-	20	nS
Output Enable to Output Valid		TAOE	-	7	-	10	nS
Chip Selection to Output in Low Z	$\overline{CS1}$	TCLZ1*	3	-	3	-	nS
	CS2	TCLZ2*	3	-	3	-	nS
Output Enable to Output in Low Z		TOLZ*	0	-	0	-	nS
Chip Deselection to Output in High Z	$\overline{CS1}$	TCHZ1*	-	7	-	10	nS
	CS2	TCHZ2*	-	7	-	10	nS
Output Disable to Output in High Z		TOHZ*	-	7	-	10	nS
Output Hold from Address Change		TOH	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

(2) Write Cycle

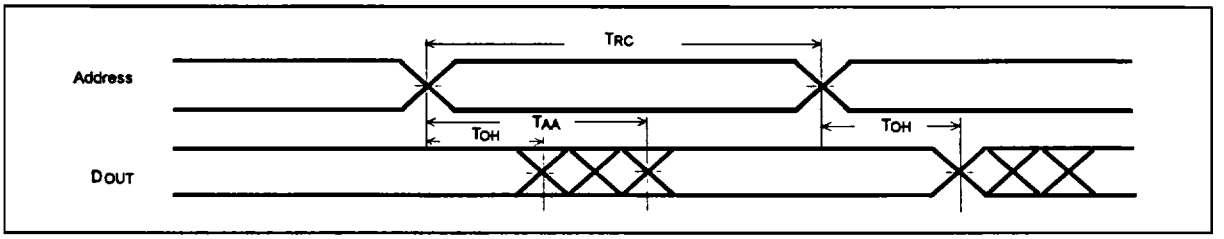
PARAMETER		SYM.	W24M512A-15		W24M512A-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	15	-	20	-	nS
Chip Selection to End of Write	$\overline{CS1}$	TCW1	13	-	17	-	nS
	CS2	TCW2	13	-	17	-	nS
Address Valid to End of Write		TAW	13	-	17	-	nS
Address Setup Time		TAS	0	-	0	-	nS
Write Pulse Width		TWP	10	-	12	-	nS
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	TWR1	0	-	0	-	nS
	CS2	TWR2	0	-	0	-	nS
Data Valid to End of Write		TDW	9	-	10	-	nS
Data Hold from End of Write		TDH	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	8	-	10	nS
Output Disable to Output in High Z		TOHZ*	-	8	-	10	nS
Output Active from End of Write		TOW	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

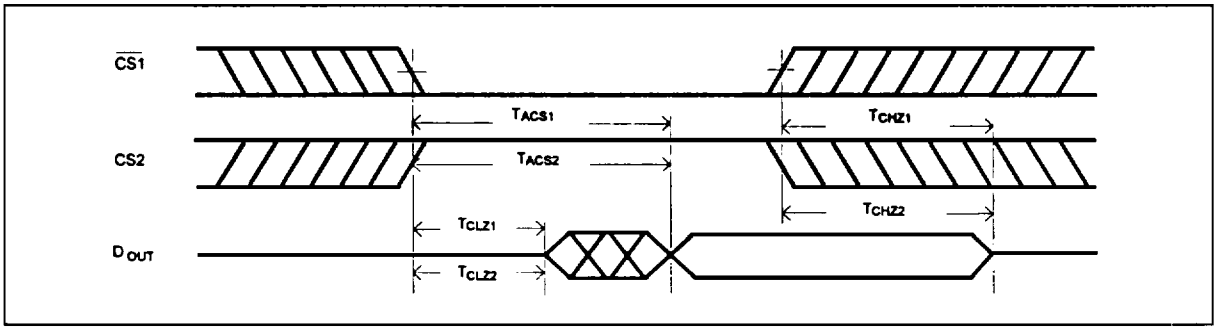
Read Cycle 1

(Address Controlled)



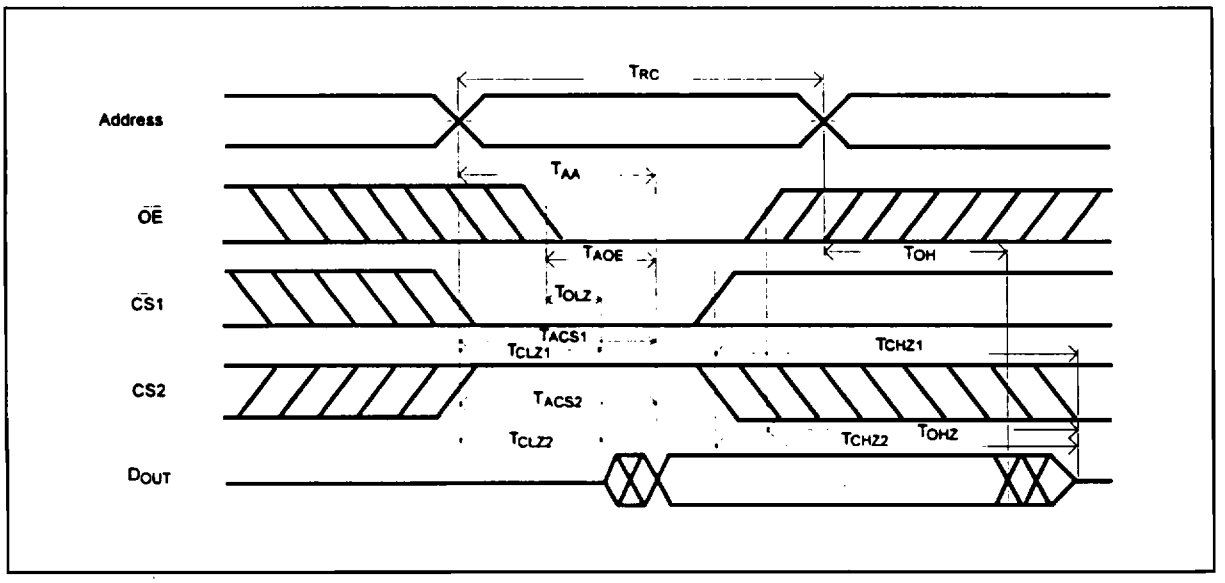
Read Cycle 2

(Chip Select Controlled)

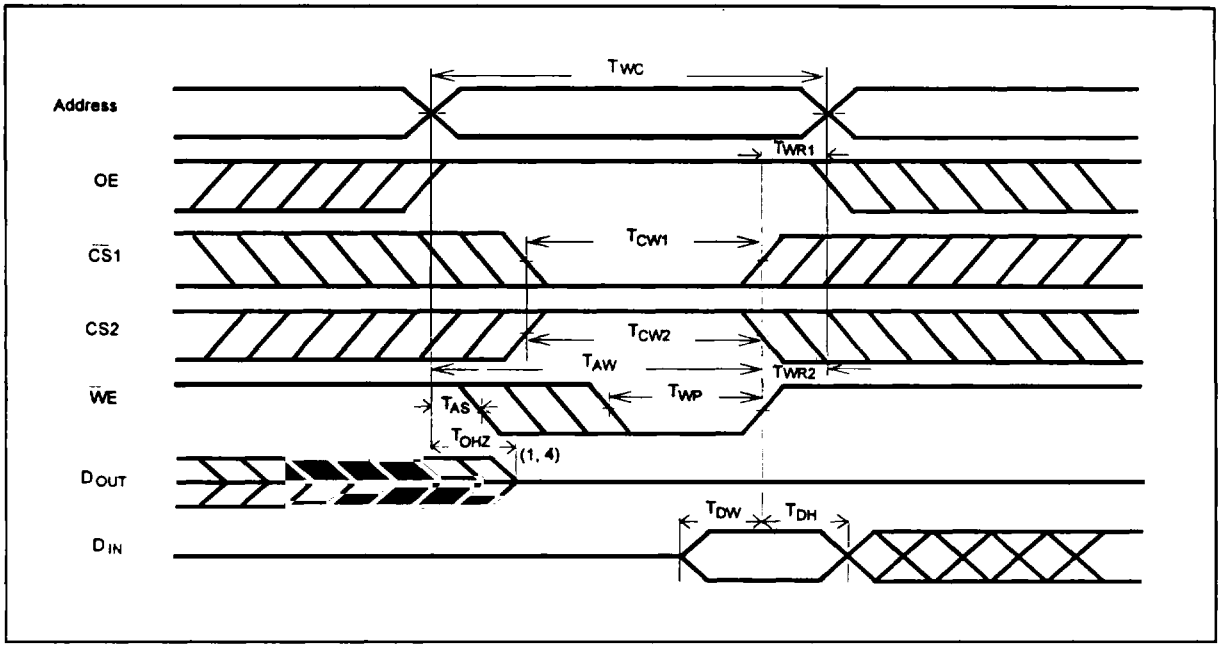


Read Cycle 3

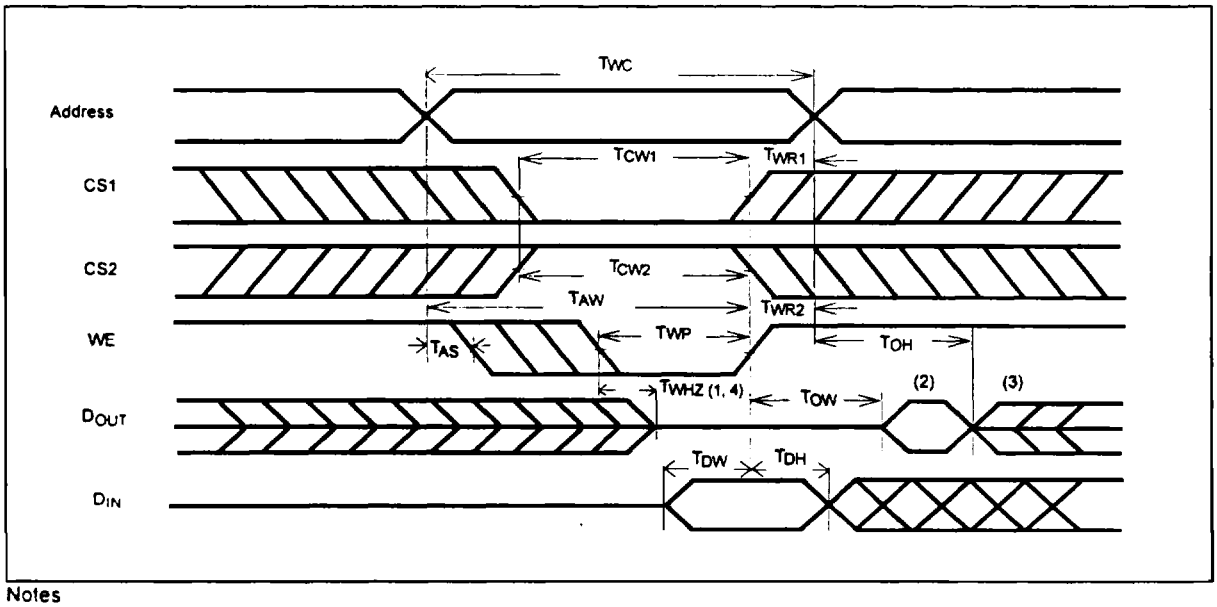
(Output Enable Controlled)



Write Cycle 1
($\overline{OE}$ Clock)



Write Cycle 2
($\overline{OE}$= Vil Fixed)



Notes

1 During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2 The data output from DOUT are the same as the data written to DIN during the write cycle.
3 DOUT provides the read data for the next address.
4 Transition is measured ±500 mV from steady state with CL= 5pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

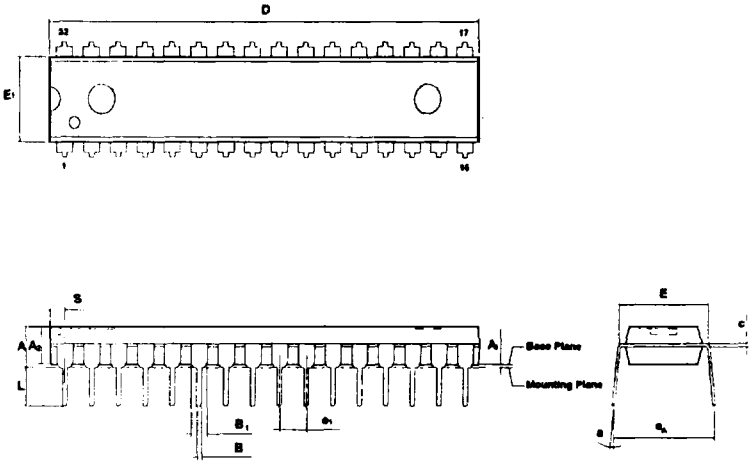
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24M512AK-15	15	200	10	300mil Skinny
W24M512AK-20	20	160	10	300mil Skinny
W24M512AJ-15	15	200	10	400mil SOJ
W24M512AJ-20	20	160	10	400mil SOJ

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-Lead P-DIP Skinny (300mil)



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.200	—	—	5.08
A_1	0.015	—	—	0.38	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D						
E						
E_1						
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
θ	0	—	15	0	—	15
e_A	0.430	0.450	0.470	10.92	11.43	11.94
S	—	—	0.065	—	—	1.65

Notes:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

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