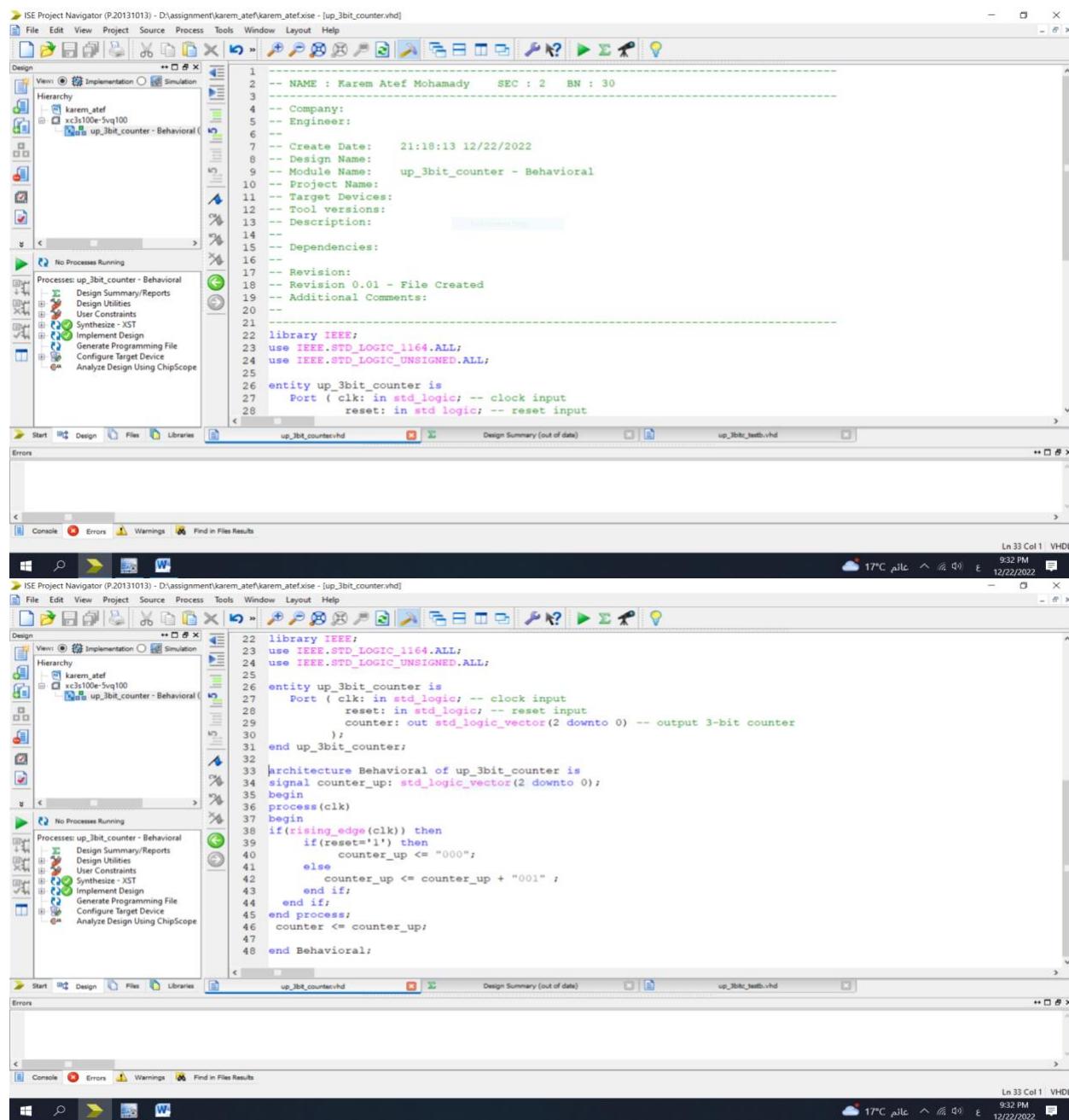


NAME : Karem Atef Mohamady SEC : 2 BN : 30

ASSIGNMENT (3bit Up Counter)

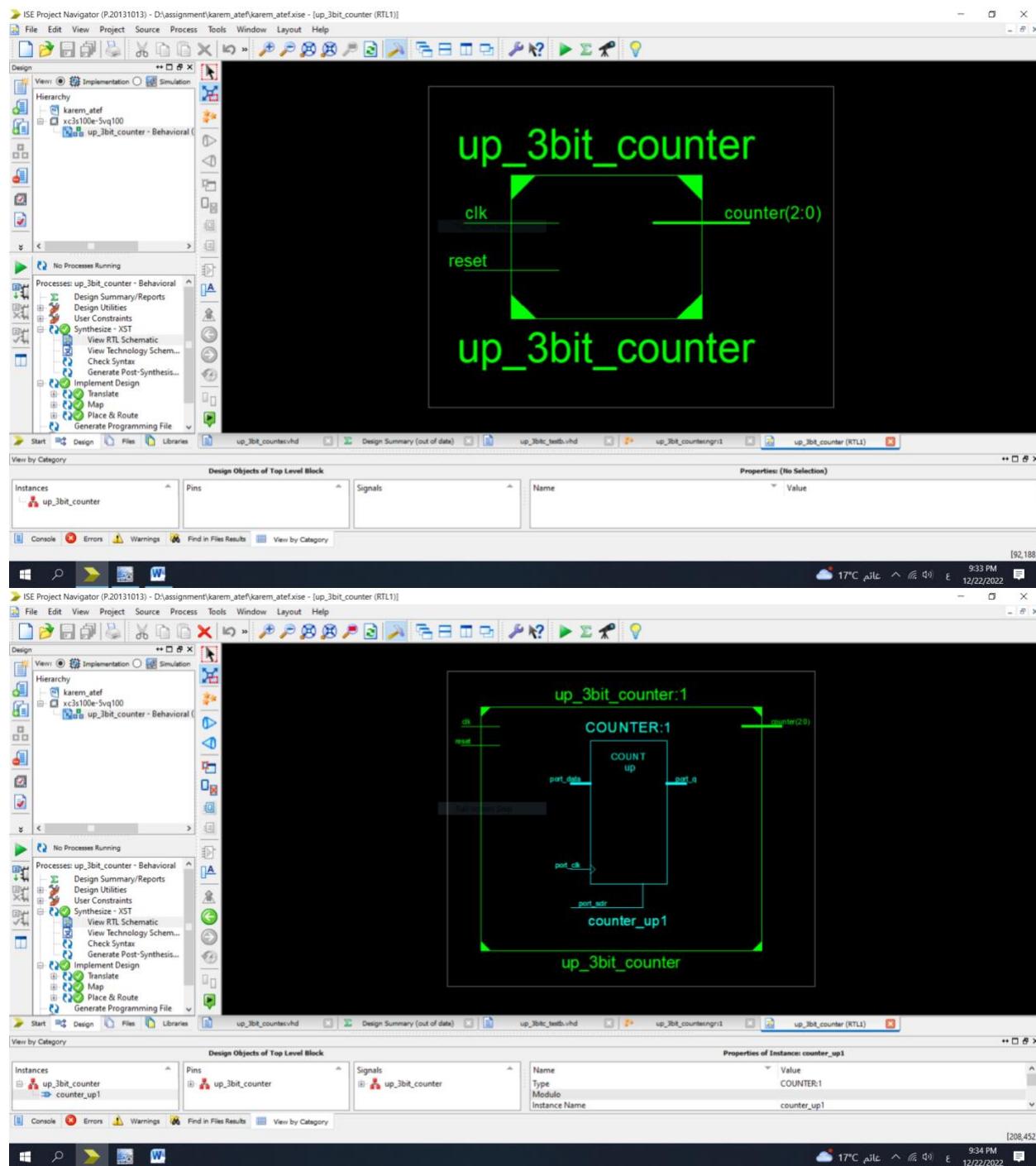
Vhdl code



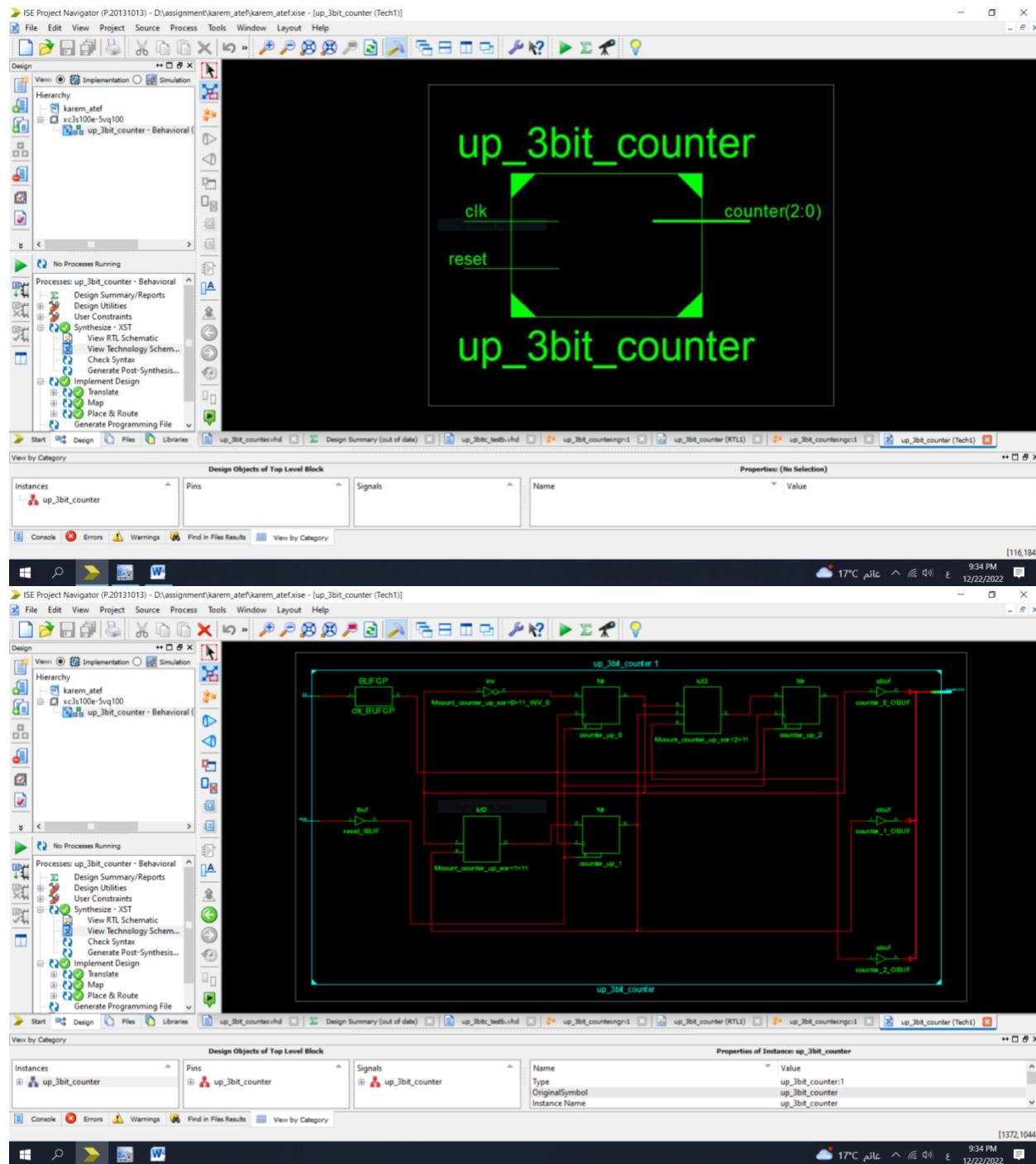
The image shows two side-by-side screenshots of the ISE Project Navigator interface. Both screens display the same VHDL code for a 3-bit up counter, with minor differences in the scroll position of the code editor.

```
-- NAME : Karem Atef Mohamady SEC : 2 BN : 30
-- Company:
-- Engineer:
--
-- Create Date: 21:18:13 12/22/2022
-- Design Name:
-- Module Name: up_3bit_counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD.LOGIC_UNSIGNED.ALL;
entity up_3bit_counter is
    Port ( clk: in std_logic; -- clock input
           reset: in std_logic; -- reset input
           counter: out std_logic_vector(2 downto 0) -- output 3-bit counter
    );
end up_3bit_counter;
architecture Behavioral of up_3bit_counter is
begin
    process(clk)
    begin
        if(rising_edge(clk)) then
            if(reset='1') then
                counter_up <= "000";
            else
                counter_up <= counter_up + "001";
            end if;
        end if;
    end process;
    counter <= counter_up;
end Behavioral;
```

RTL Schematic



Technology Schematic



Design Summary

ISE Project Navigator (P-20131013) - D:\assignment\karem_atef\karem_atef.xise - [Design Summary (out of date)]

Design Overview

- Project File: karem_atef.xise
- Module Name: up_3bit_counter
- Target Device: xc3s100e-5vq100
- Product Version: ISE 14.7
- Design Goal: Balanced
- Design Strategy: Xilinx Default (Unlocked)
- Environments: System Settings

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	3	1,920	1%	
Number of 4 input LUTs	2	1,920	1%	
Number of occupied Slices	2	960	1%	
Number of Slices containing only related logic	2	2	100%	
Number of Slices containing unrelated logic	0	2	0%	
Total Number of 4 input LUTs	2	1,920	1%	
Number of bonded IOBs	5	66	7%	
Number of BUFRMULs	1	24	4%	
Average Fanout of Non-Clock Nets	3.00			

Performance Summary

Final Timing Score:	0 [Setup: 0, Hold: 0]	Pinned Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Dec 22 21:29:15 2022	0	0	0
Translation Report	Current	Thu Dec 22 21:29:19 2022	0	0	0
Map Report	Current	Thu Dec 22 21:29:22 2022	0	0	2 Infos (2 new)
Place and Route Report	Current	Thu Dec 22 21:29:27 2022	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu Dec 22 21:29:29 2022	0	0	6 Infos (6 new)
Bilgen Report					

Secondary Reports

Report Name	Status	Generated
XHM Simulator Log	Out of Date	Thu Dec 22 21:29:53 2022

Date Generated: 12/22/2022 - 21:31:52

Console Errors Warnings Find in File Results

ISE Project Navigator (P-20131013) - D:\assignment\karem_atef\karem_atef.xise - [Design Summary (out of date)]

Design Overview

- Project File: karem_atef.xise
- Module Name: up_3bit_counter
- Target Device: xc3s100e-5vq100
- Product Version: ISE 14.7
- Design Goal: Balanced
- Design Strategy: Xilinx Default (Unlocked)
- Environments: System Settings

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	3	1,920	1%	
Number of 4 input LUTs	2	1,920	1%	
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Number of Slices containing only related logic	2	2	100%	
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Total Number of 4 input LUTs	2	1,920	1%	
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Number of BUFRMULs	1	24	4%	
Average Fanout of Non-Clock Nets	3.00			

Performance Summary

Final Timing Score:	0 [Setup: 0, Hold: 0]	Pinned Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports

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Place and Route Report	Current	Thu Dec 22 21:29:27 2022	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu Dec 22 21:29:29 2022	0	0	6 Infos (6 new)
Bilgen Report					

Secondary Reports

Report Name	Status	Generated
XHM Simulator Log	Out of Date	Thu Dec 22 21:29:53 2022

Date Generated: 12/22/2022 - 21:31:52

Console Errors Warnings Find in File Results

ISE Project Navigator (P-20131013) - D:\assignment\karem_atef\karem_atef.xise - [Design Summary (out of date)]

Design Overview

- Project File: karem_atef.xise
- Module Name: up_3bit_counter
- Target Device: xc3s100e-5vq100
- Product Version: ISE 14.7
- Design Goal: Balanced
- Design Strategy: Xilinx Default (Unlocked)
- Environments: System Settings

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	3	1,920	1%	
Number of 4 input LUTs	2	1,920	1%	
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Total Number of 4 input LUTs	2	1,920	1%	
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Number of BUFRMULs	1	24	4%	
Average Fanout of Non-Clock Nets	3.00			

Performance Summary

Final Timing Score:	0 [Setup: 0, Hold: 0]	Pinned Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Thu Dec 22 21:29:15 2022	0	0	0
Translation Report	Current	Thu Dec 22 21:29:19 2022	0	0	0
Map Report	Current	Thu Dec 22 21:29:22 2022	0	0	2 Infos (2 new)
Place and Route Report	Current	Thu Dec 22 21:29:27 2022	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu Dec 22 21:29:29 2022	0	0	6 Infos (6 new)
Bilgen Report					

Secondary Reports

Report Name	Status	Generated
XHM Simulator Log	Out of Date	Thu Dec 22 21:29:53 2022

Date Generated: 12/22/2022 - 21:31:52

Console Errors Warnings Find in File Results

Test bench Code

The screenshot shows the Xilinx ISE Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. The left sidebar displays a project hierarchy under 'karem_atef' with a sub-project 'xc3s100e-5vq100' and a module 'up_3bitc_testb - behavior (up_3bitc_testb.vhd)'. The main workspace shows the generated VHDL code for the testbench:

```
1 -- NAME : Karem Atef Mohamady SEC : 2 BN : 30
2 --
3 --
4 -- Company:
5 -- Engineer:
6 --
7 -- Create Date: 21:23:31 12/22/2022
8 -- Design Name:
9 -- Module Name: D:/assignment/karem_atef/up_3bitc_testb.vhd
10 -- Project Name: karem_atef
11 --
12 -- Target Device:
13 --
14 --
15 -- VHDL Test Bench Created by ISE for module: up_3bitc_counter
16 --
17 -- Dependencies:
18 --
19 -- Revision:
20 -- Revision 0.01 - File Created
21 -- Additional Comments:
22 --
23 -- Notes:
24 -- This testbench has been automatically generated using types std_logic and
25 -- std_logic_vector for the ports of the unit under test. Xilinx recommends
26 -- that these types always be used for the top-level I/O of a design in order
27 -- to guarantee that the testbench will bind correctly to the post-implementation
28 -- simulation model.
```

The bottom status bar shows the date and time: 12/22/2022, 9:42 PM, and the temperature: 17°C. The taskbar at the bottom includes icons for Start, Design, Files, Libraries, and several open tabs related to the project files.

The screenshot shows the Xilinx ISE Project Navigator interface with the same project structure and workspace as the first screenshot. The main workspace now displays the edited VHDL code for the testbench:

```
27 -- to guarantee that the testbench will bind correctly to the post-implementation
28 -- simulation model.
29
30 LIBRARY ieee;
31 USE ieee.std_logic_1164.ALL;
32
33 ENTITY up_3bitc_testb IS
34 END up_3bitc_testb;
35
36 ARCHITECTURE behavior OF up_3bitc_testb IS
37
38 COMPONENT up_3bitc_counter
39 PORT (
40     clk : IN std_logic;
41     reset : IN std_logic;
42     counter : OUT std_logic_vector(2 downto 0)
43 );
44 END COMPONENT;
45
46
47 signal reset,clk: std_logic;
48 signal counter:std_logic_vector(2 downto 0);
49
50 BEGIN
51
52     uut: up_3bitc_counter PORT MAP (
53         clk => clk,
54         reset => reset,
```

The bottom status bar shows the date and time: 12/22/2022, 9:42 PM, and the temperature: 17°C. The taskbar at the bottom includes icons for Start, Design, Files, Libraries, and several open tabs related to the project files.

ISE Project Navigator (P.20131013) - D:\assignment\karem_atef\karem_atef.xise - [up_3bitc_testb.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View Implementation Simulation

Hierarchy

- karem_atef
 - xc3s100e-5vq100
 - up_3bitc_testb - behavior (up_3bitc)

No Processes Running

Processes: up_3bitc_testb - behavior

- iSim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

```

53     clk => clk,
54     reset => reset,
55     counter => counter
56   );
57
58   -- Clock process definitions
59   clock_process :process
60 begin
61   clk <= '0';
62   wait for 10 ns;
63   clk <= '1';
64   wait for 10 ns;
65 end process;
66
67
68   -- Stimulus process
69   stim_proc: process
70 begin
71
72   reset <= '1';
73   wait for 20 ns;
74   reset <= '0';
75
76   wait;
77
78 end process;
79
80 end behavior;

```

Start Design Files Libraries up_lbt_counter.vhd up_lbt_counter.vhd Design Summary (out of date) up_3bitc_testb.vhd up_3bitc_beh.vhd up_3bitc_beh.vhd up_lbt_counter (RTL) up_lbt_counter (NGC) up_lbt_counter (Tech)

View by Category

Design Objects of Top Level Block

Instances	Pins	Signals	Name	Type	Value
up_3bitc	up_3bitc	up_3bitc	counter_up1	Modulo	COUNTER1

Properties of Instance: counter_up1

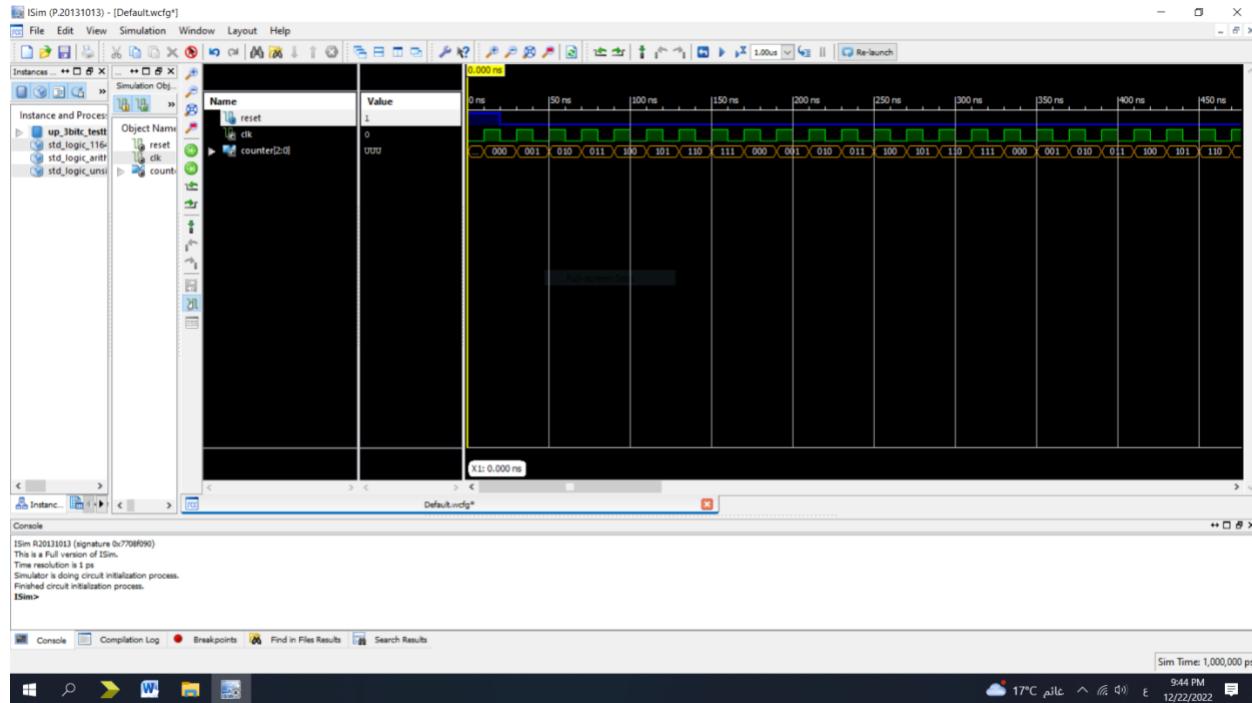
Name	Type	Value
counter_up1	Modulo	COUNTER1

Ln 36 Col 1 VHDL

Console Errors Warnings Find in File Results View by Category

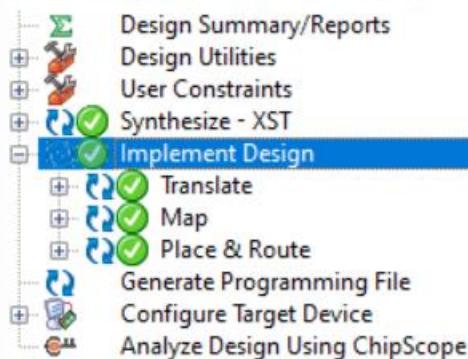
17°C 9:43 PM 12/22/2022

Test Bench Output

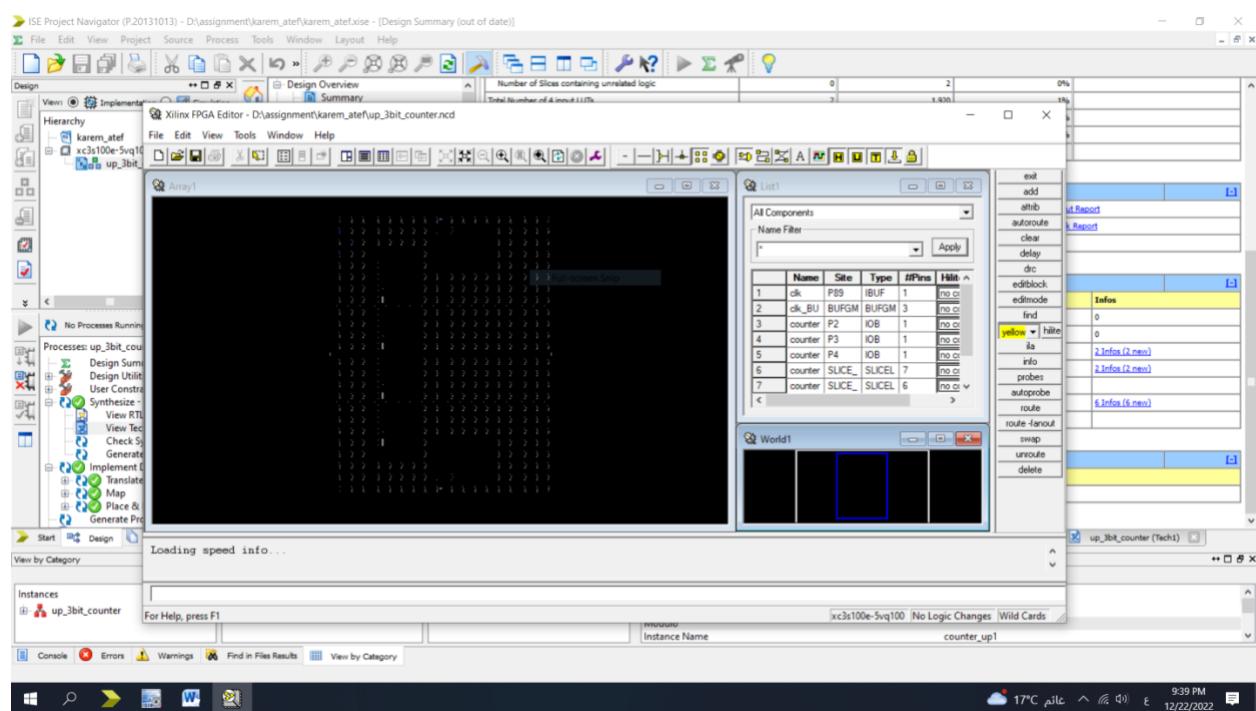


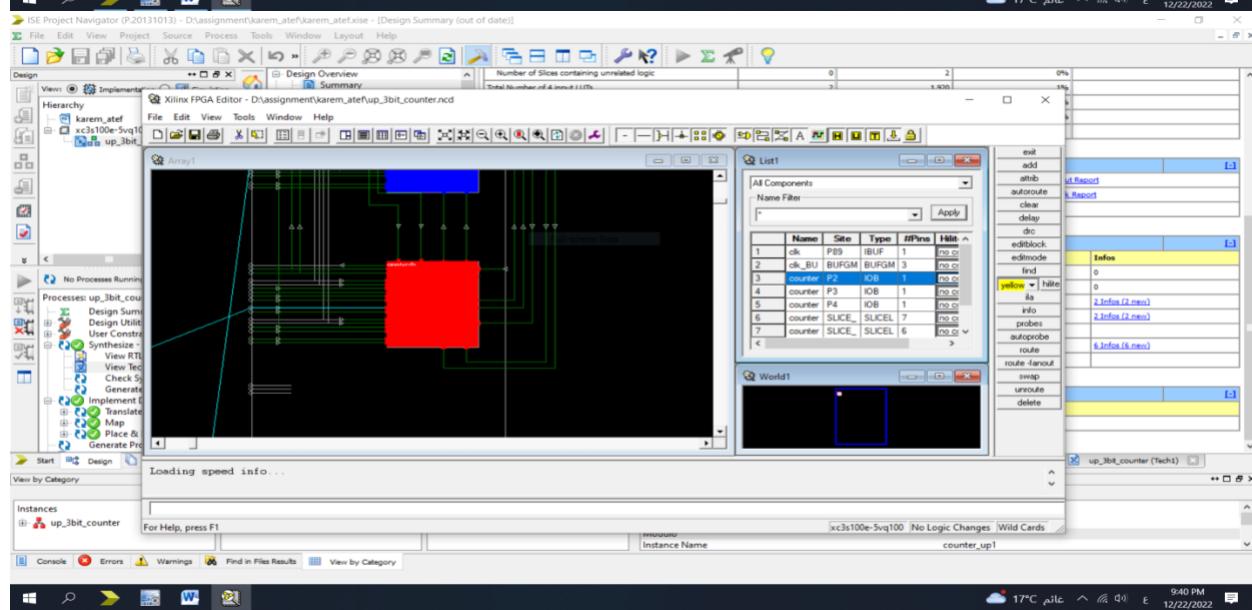
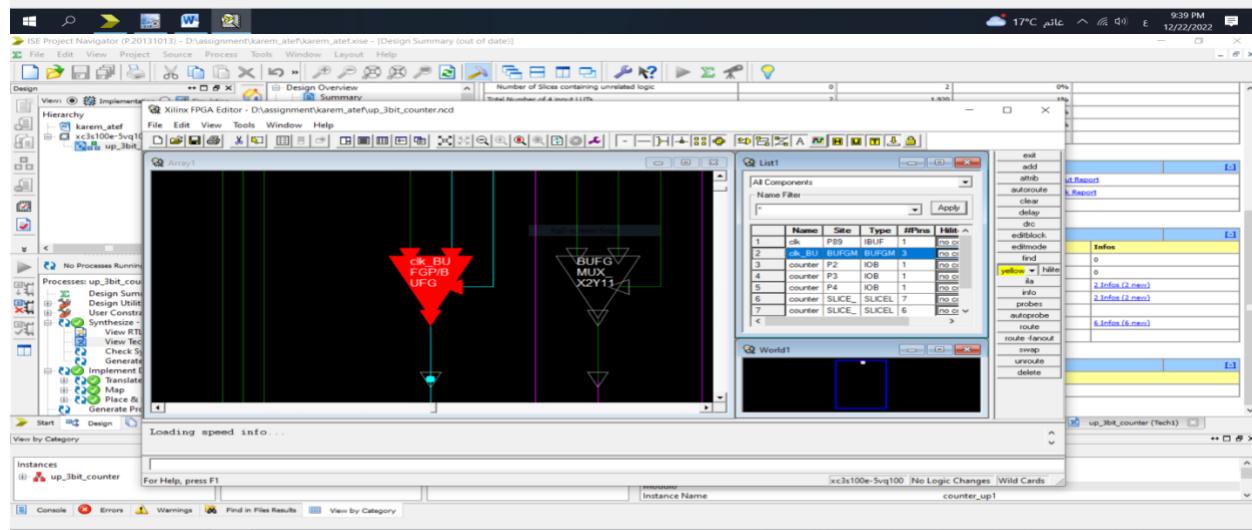
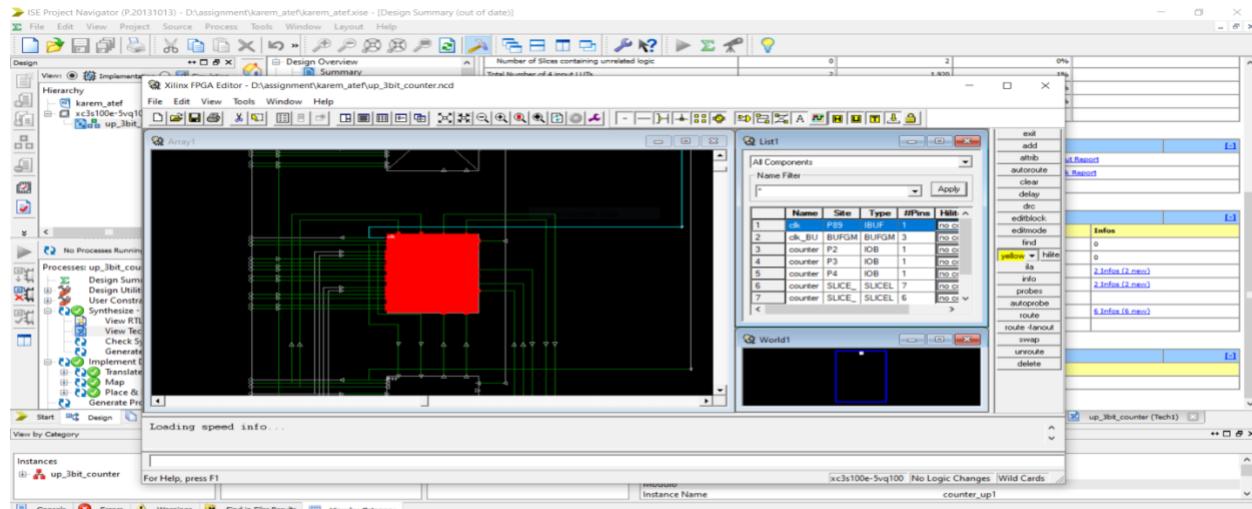
Implement Design (place & Route)

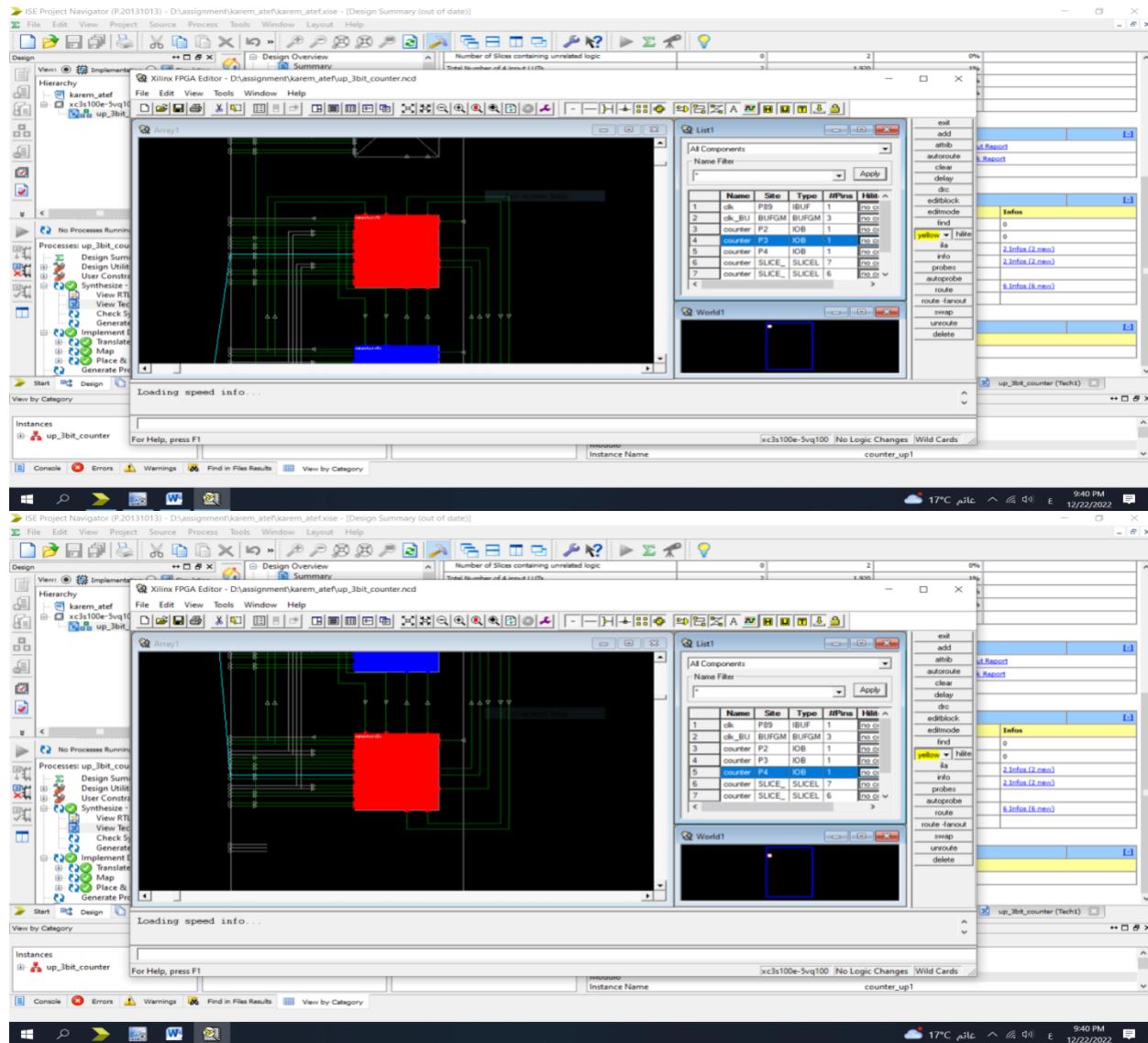
Processes: up_3bit_counter - Behavioral

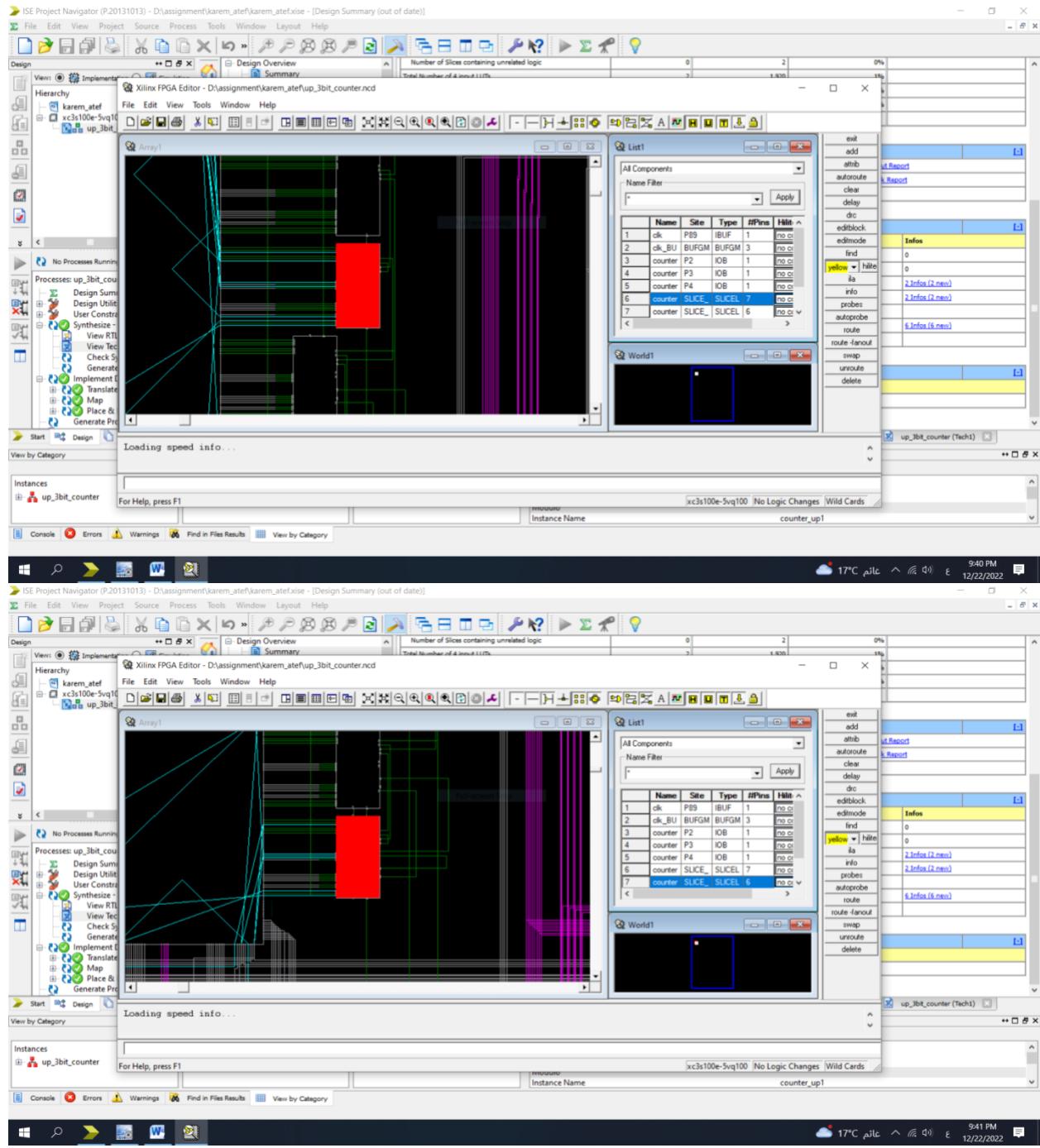


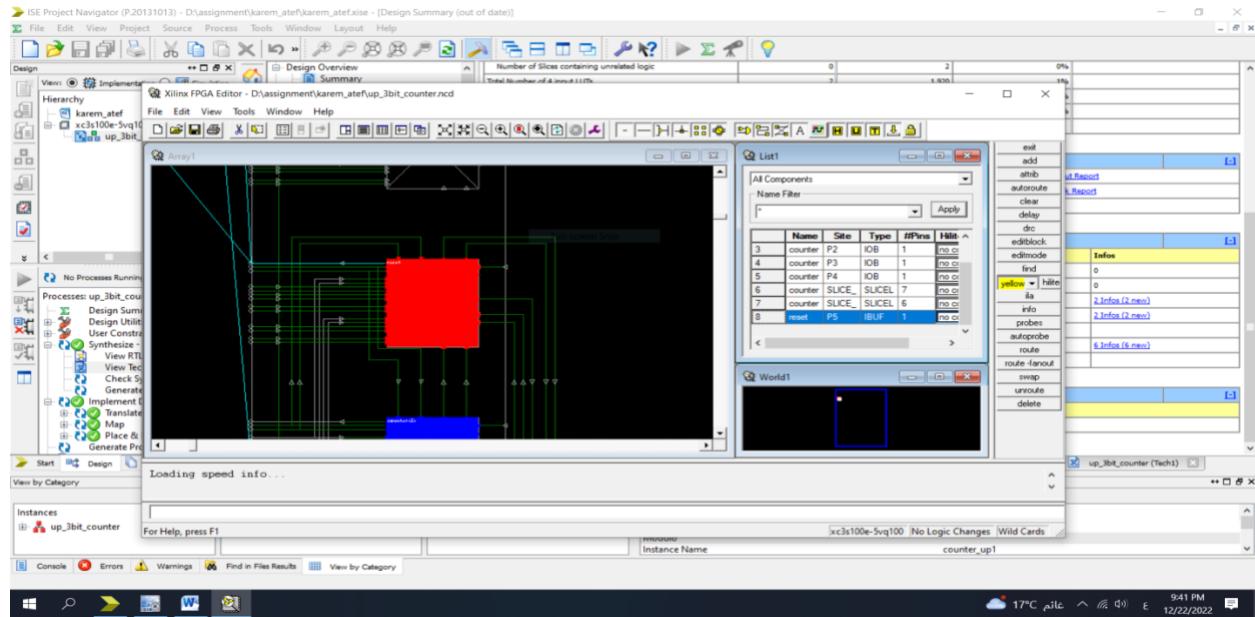
FPGA Editor











Analyze Power Distribution

