



UNIVERSITY OF CALIFORNIA

Marlan and Rosemary Bourns  
College of Engineering

# Bluetooth Audio Transmitter

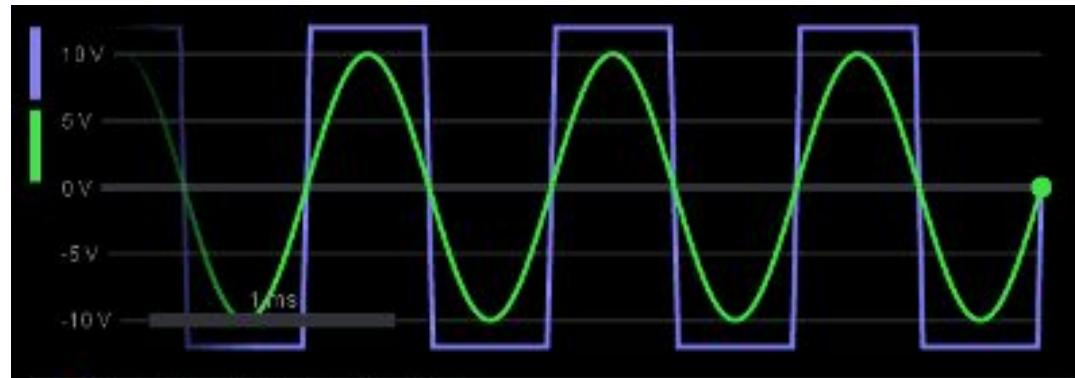
BOURNS HALL

Presented By:

Zohaib Khan, Karen Escareno, Rishi Kodukula

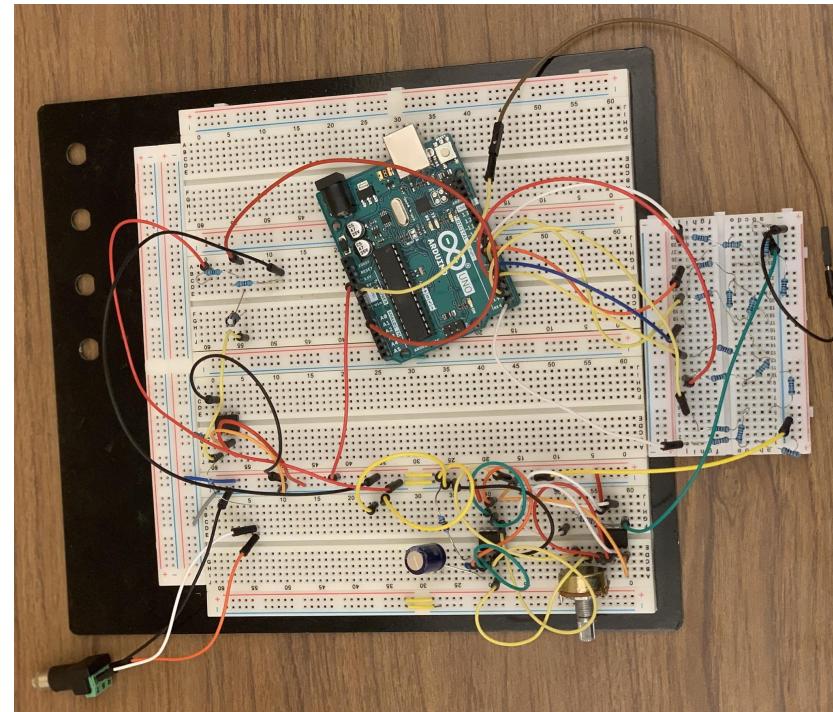
# Concept and Application of the Design

- Design of the system requires an audio signal that will be digitized by the transmitter before being sent to the receiver to output the sound.
- The intended applications for this project is to connect any form of sound through a 3.5mm jack and be able to hear the corresponding real time audio.
- Real-time processes apply to all core concepts of technology, such as digital communication, digital signal processing and real time processing

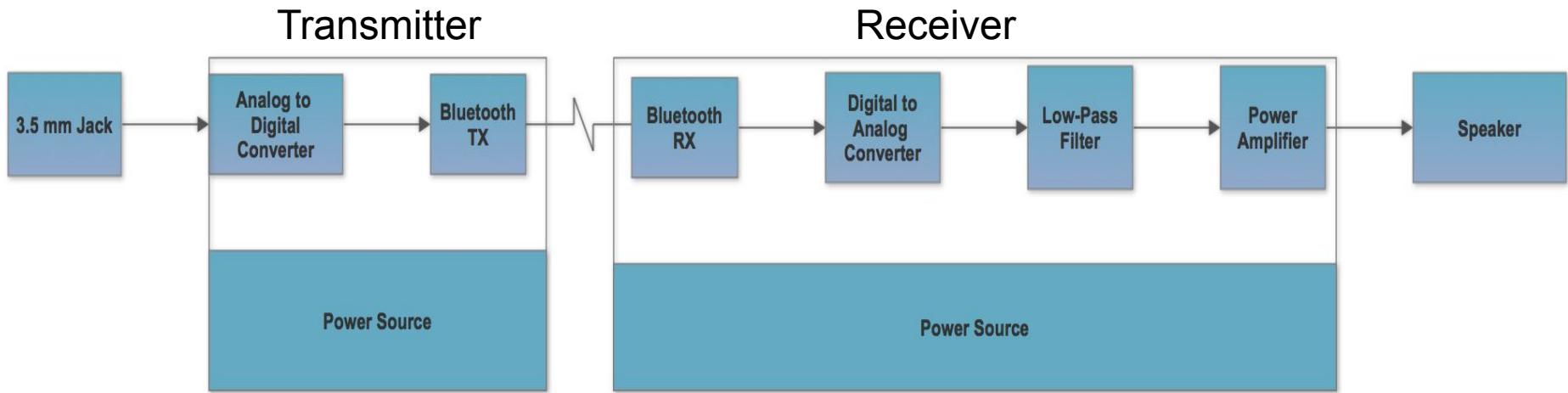


# Technical Design Objectives

- Range: 20 ft +
- Sampling Rate: 40KHZ - 80KHZ
- Accuracy: 5 % Error
- Response Time: Micro-seconds
- Input Frequency (Depends on Signal): 100 HZ to 40 KHZ

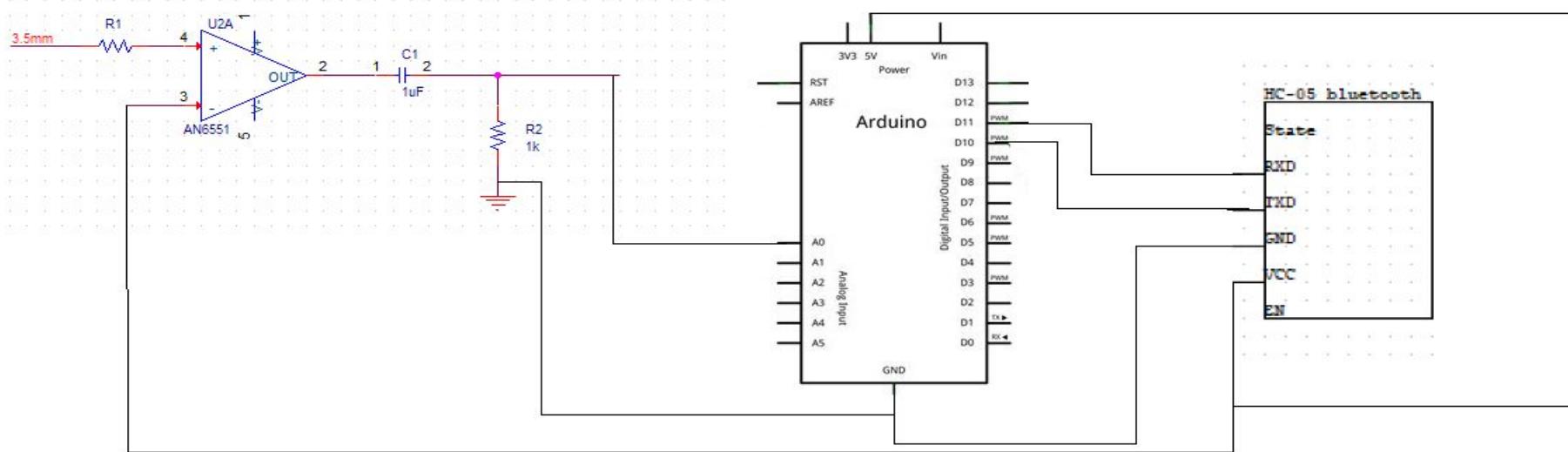


# Final High-Level Design



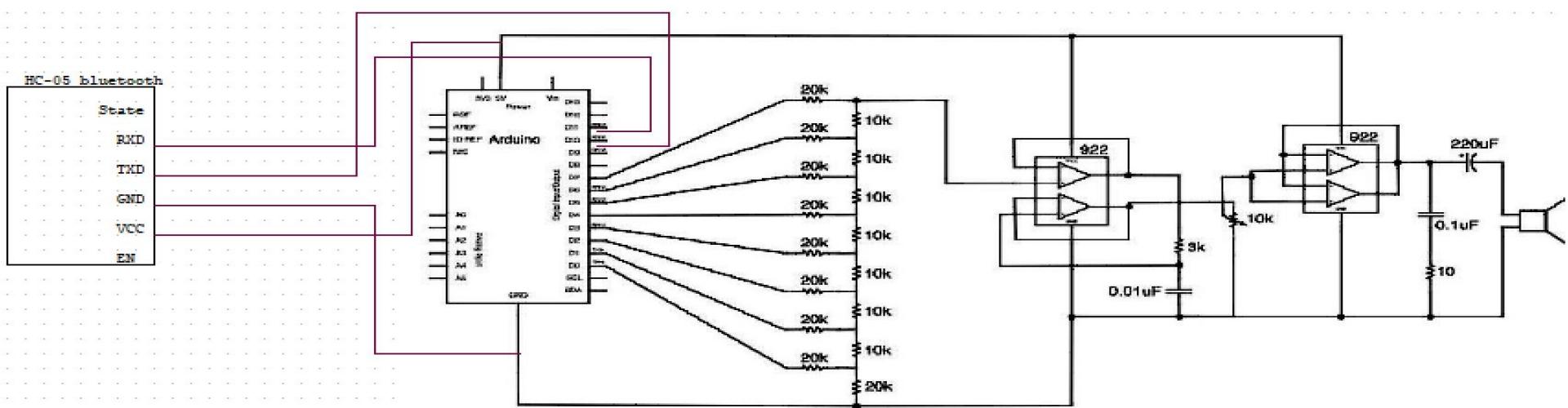
# Schematic

Transmitter:

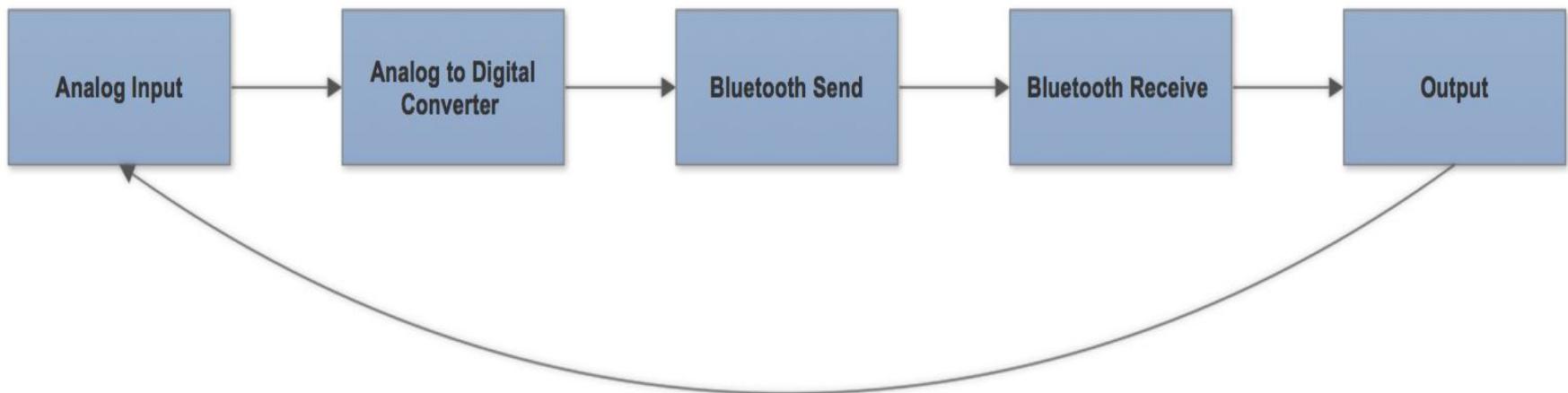


# Schematic

## Receiver:



# Flow Chart of Software



# Technical Challenges

- Challenges mainly consisted of register programming and electrical circuit such as the DAC, Power Amplifier, and Low-Pass Filter.
- We tackled these problems in separate parts. When designing our hardware we made sure the signal (20 KHz- 40Khz) behaved as expected through the specific hardware components.
- For example, the 3.5mm jack outputted a 20Khz sine wave signal on the oscilloscope which was then measured after the DAC to get a 20KHz sine wave signal. The signal then went into a Low-Pass Filter which allowed us to pass lower signals than the cutoff frequency, the Amplifier which amplified the signal and then outputted to the speaker.

```
ADCSRA |= (1 << ADPS2); // 16 prescaler for 76.9 KHz
ADCSRA |= (1 << ADATE); // enable auto trigger
ADCSRA |= (1 << ADIE); // enable interrupts when measurement complete
ADCSRA |= (1 << ADEN); // enable ADC
ADCSRA |= (1 << ADSC); // start ADC measurements
```



# Major Components of the Design and Implementation

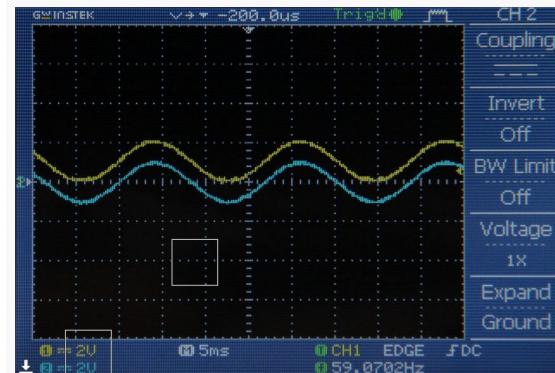
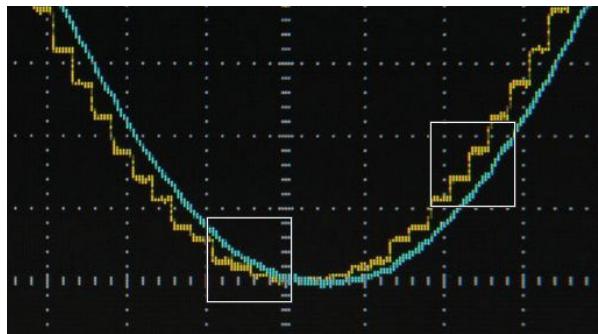
- 3.5 mm jack - Using the TSS9N op amp with a gain of 50, and a cap on A0, we were able to center the wave at 512 (Half of  $2^{10}$  ADC).
- Analog to Digital Converter - Register programming allowed us to manipulate the ADC to run in a free continuous mode and have a sampling rate of 77 KHZ (prescaler of 16).
- Bluetooth (HC05s) - Connected through AT commands. One master and one slave sending 8 bit char values. Baud rate: 115200, UART communication.



Time	Port	Data
14:25:26.348	COM12	-> 0
14:25:26.348	COM12	-> 1
14:25:26.348	COM12	-> 2
14:25:26.348	COM12	-> 3
14:25:26.348	COM12	-> 6
14:25:26.348	COM12	-> 8
14:25:26.348	COM12	-> 12
14:25:26.348	COM12	-> 15
14:25:26.388	COM12	-> 19
14:25:26.388	COM12	-> 24
14:25:26.388	COM12	-> 29
14:25:26.388	COM12	-> 34
14:25:26.388	COM12	-> 40
14:25:26.388	COM12	-> 46
14:25:26.388	COM12	-> 52
14:25:29.628	COM10	-> 0
14:25:29.628	COM10	-> 0
14:25:29.628	COM10	-> 0
14:25:29.628	COM10	-> 1
14:25:29.628	COM10	-> 2
14:25:29.628	COM10	-> 3
14:25:29.628	COM10	-> 6
14:25:29.628	COM10	-> 8
14:25:29.628	COM10	-> 12
14:25:29.628	COM10	-> 15
14:25:29.628	COM10	-> 19
14:25:29.628	COM10	-> 24
14:25:29.668	COM10	-> 29
14:25:29.668	COM10	-> 34
14:25:29.668	COM10	-> 40
14:25:29.668	COM10	-> 46

# Major Components of the Design and Implementation

- Digital to Analog Converter - 8 bit R2R Resistor Ladder can produce 256 different voltage levels. This is connected to each of digital pins 0-7 to each of the 8 junctions in the DAC
- Lowpass Filter - According to Nyquist theorem, one can produce  $\frac{1}{2}$  the signal of a specific sampling rate. If the sampling rate is 30KHZ, the max frequency that can be produced is 15KHZ (upper limit) The cutoff frequency =  $1 / (2\pi RC)$
- Amplifier - TSS9N op amps source 80 amps therefore, adding the two's output as voltage followers, we can source 160 amps of current.



# Design Considerations

## Realistic constraints -

- 16 MHZ clock frequency - this limits ADC sampling rate
- AVR takes 13 clock cycles per conversion
- 8 Bit R2R Resistor Ladder - a resolution of 256 ( $2^8$ ) different voltage levels between 0 and 5v
- Power: 3.3 volts. @ 8GHZ = .004 millamps, resulting in > 1 watt
- Lose of resolution above a sample rate of 15kHz.

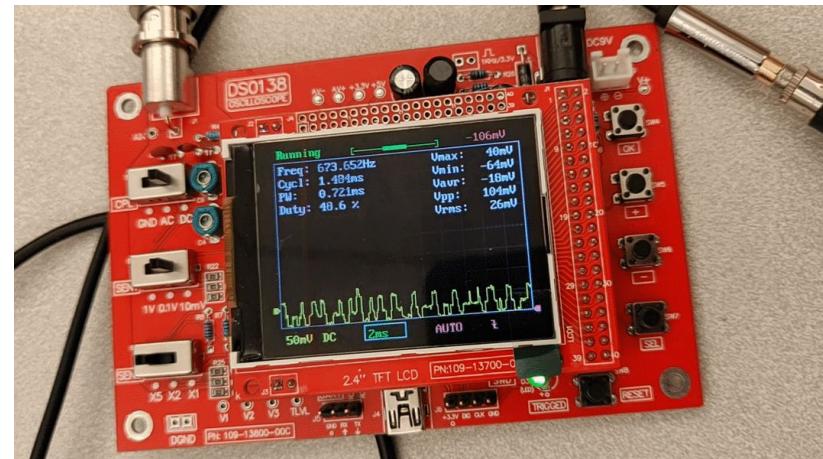
## Industry Standards :

- UART - IEEE 1451.0, Accession # 16375333, Date: October 10, 2016
- Standard for Graphic Symbols - IEEE 315-1975 Date: September 4, 1975
- SPI - IEEE, Accession #17651795 Date: March 26, 2018
- ISO/IEC 9899: Programming Language C. Dec 1999

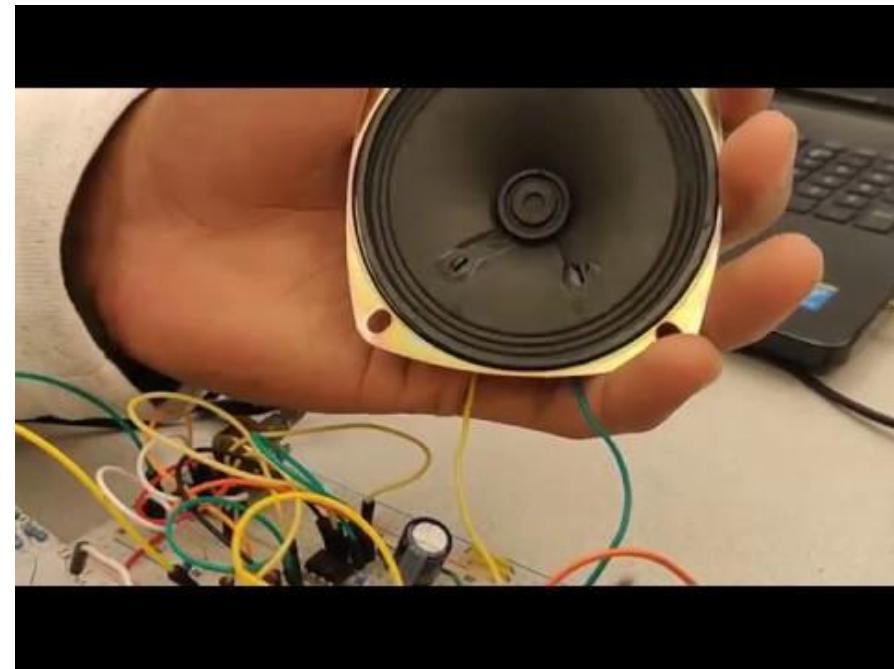
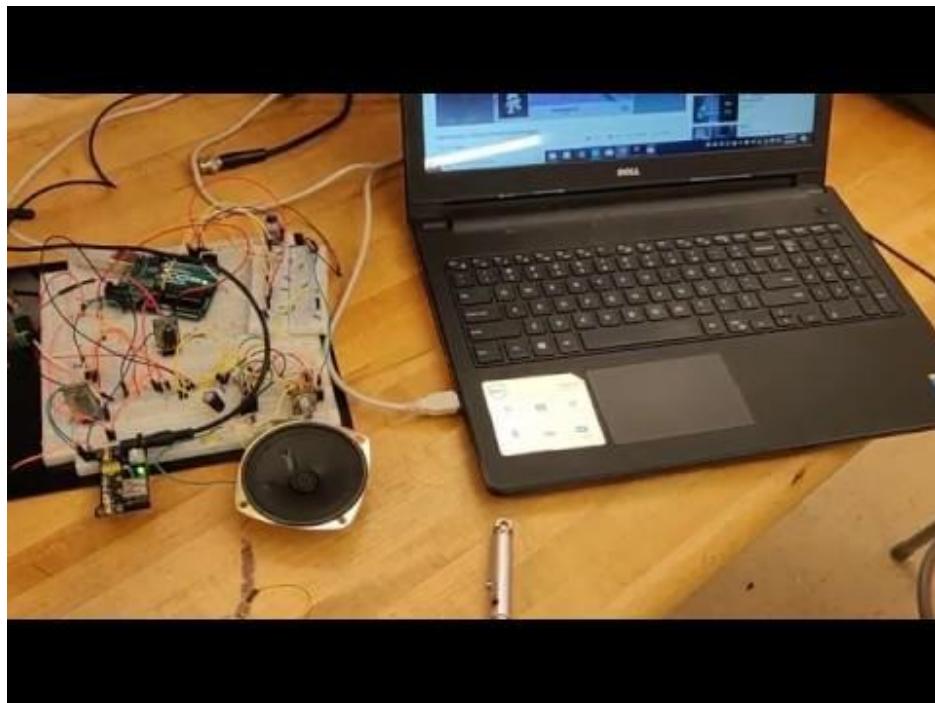
# Test Report

- Our system's primary test equipment was the oscilloscope.
  - We tested our system through digital and analog signals to compare the outcome with the predicted results.
- Test Results:
- Distance between the two system
  - Avg of 25 Ft. (Higher than projected)
- Sent a digitized signal (200 Hz - 40KHZ) signal to the DAC, lowpass, and power amplifier
  - period = (duration of each step) \* (number of steps),  $F = 1/\text{period}$
  - Output 196 Hz. (2 % Error)
- Bluetooth
  - Serial Monitor, Timestamps

```
void fourhundredhertz() {
    for (int t=0;t<100;t++){
        PORTD = sine[t];
        delayMicroseconds(25);
    }
}
```



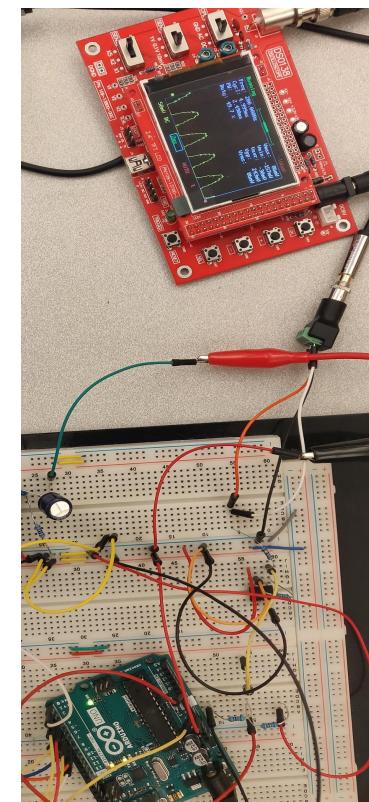
# Demo



# Summary

The purpose of this project was to simulate and create a foundation to develop life long skills we will continue to use. The importance of this project is to further understand and become familiarized with

- Digital signal processing
- Register Programming
- Sampling rates
- Sampling Analog and Digital Signals
- Aliasing & Quantization
- UART, SPI, ADC, DAC
- Debugging
- Peer Communication and Collaboration



# Acknowledgments

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