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Help **ADD INSTRUCTION** 

- The instruction always adds two register values.
- The bus is used exactly two times: Once during instruction fetch and a second time to write the result from the ALU to the Register File and to simultaneously update the CC register.
- The Operand Fetch, Execute, and Store Result phases of instruction execution occur over three consecutive clock cycles.



In the Immediate Mode, the instruction adds one register value and a sign-extended immediate (constant) value.

The bus is used three times. During instruction fetch, it is used twice: once to transfer the address from PC to MAR, and a second time to transfer instruction from MDR to IR. The bus is used a third time to write the result and update the CC register.

ADD uses one additional state—occupied for a single clock cycle—after Instruction Decode to perform these three phases in one cycle.

The CC register is updated since ADD writes the Register File.

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