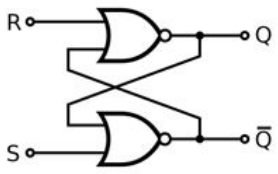
HOMEWORK 1. STORAGE

Consider a latch comprised of NOR rather than NAND gates:



HOMEWORK1 A. STORAGE (1/1 point)

For inputs R = 1 and S = 0, which of the following is true?

- Q = 0 and $\overline{Q}$ = 0
- (•) Q = 0 and $\overline{Q}$ = 1 ✔
- Q = 1 and $\overline{Q}$ = 1
- Q = 1 and $\overline{Q}$ = 0

EXPLANATION

With R = 1, the output of the top NOR gate is forced to 0. The inputs to the bottom NOR gate are both 0, so its output is a 1. So R = 1, S = 0 performs a reset.

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HOMEWORK 1 B. STORAGE (1/1 point)

Which input combination retains the current outputs?

- (•) R = 0 and S = 0. ✔
- R = 0 and S = 1.
- R = 1 and S = 0.
- R = 1 and S = 1.

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EXPLANATION

When the S and R inputs are both 0, feedback maintains the Q and $\overline{Q}$ outputs in a constant state. If S becomes a 1 while R is held at 0, then Q=1, and stays at that logic value when S returns to 0. Similarly, if R becomes a 1 while S is held at 0, then Q=0, and that value is retained when R returns to 0.

Check | Hide Answer

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HOMEWORK 2. STORAGE (1/1 point)

A 2-bit loadable register uses two D flip-flops with load capability that share one LD input and one Clock input. If currently D_1D_0 = 01, LD = 0, and Q_1Q_0 = 10, what will be the new value of Q_1Q_0 when the clock triggers (transitions from 0 to 1)?

- 00
- 01
- 10 ✔
- 11

EXPLANATION

Since LD = 0, the current output of 10 is retained.

Final Check | **Save** | Hide Answer | *You have used 1 of 2 submissions*

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HOMEWORK 3. STORAGE (1/1 point)

Consider the following circuit consisting of a positive edge-triggered D flip-flop and a 4-to-1 mux.

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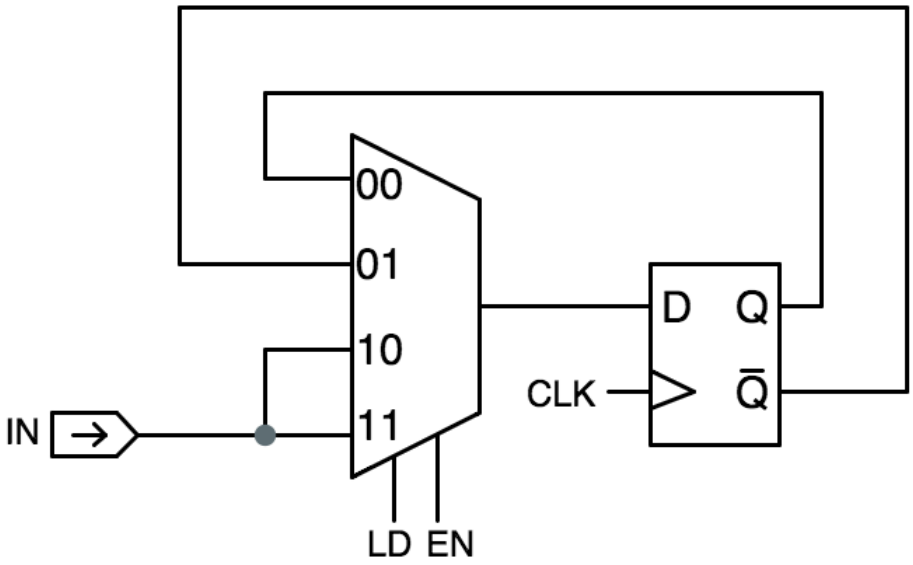

Which of the following statements properly describe the operation of this circuit? [Check all that apply]

- [x] So long as LD = 1, the value of IN will be loaded into the D flip-flop at the next rising edge of the clock. ✔
- [ ] So long as LD = 0, the current value of the flip-flop output will be retained at the next rising edge of the clock.
- [x] When LD = 0 and EN = 1, the output of the flip-flop is inverted from its current value at the next rising edge of the clock. ✔

EXPLANATION

The first statement is true since IN is connected to both mux inputs for which LD = 1. The third statement is true since for those select inputs Q' will pass through the mux and get clocked into the D flip-flop, thereby inverting the output. The second statement is not true for the same reason.

Final Check | **Save** | **Hide Answer** *You have used 1 of 2 submissions*

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