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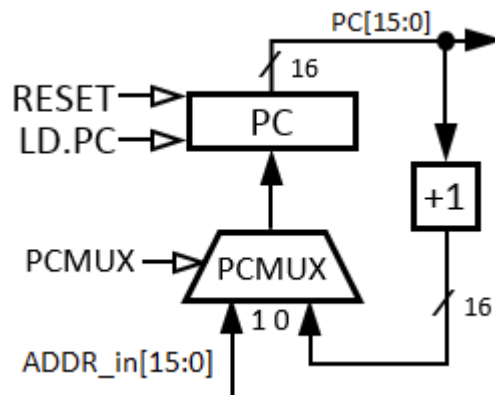
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LAB 7. ISA: Next PC Logic

Design the LC-3 Lite Next PC logic shown in the LC-3 Lite microarchitecture diagram, and test it using the provided test file.

This is the section of the LC-3 Lite we'll be building:



The design comprises the PC register, an incrementer, and some 16-bit muxes.

The PC register is a 16-bit loadable register that is loaded when LD_PC = 1, and otherwise retains its current value. The RESET input causes the PC register to be initialized to 0x3000, the location of the first instruction in the program. Use the PC register you made last lab.

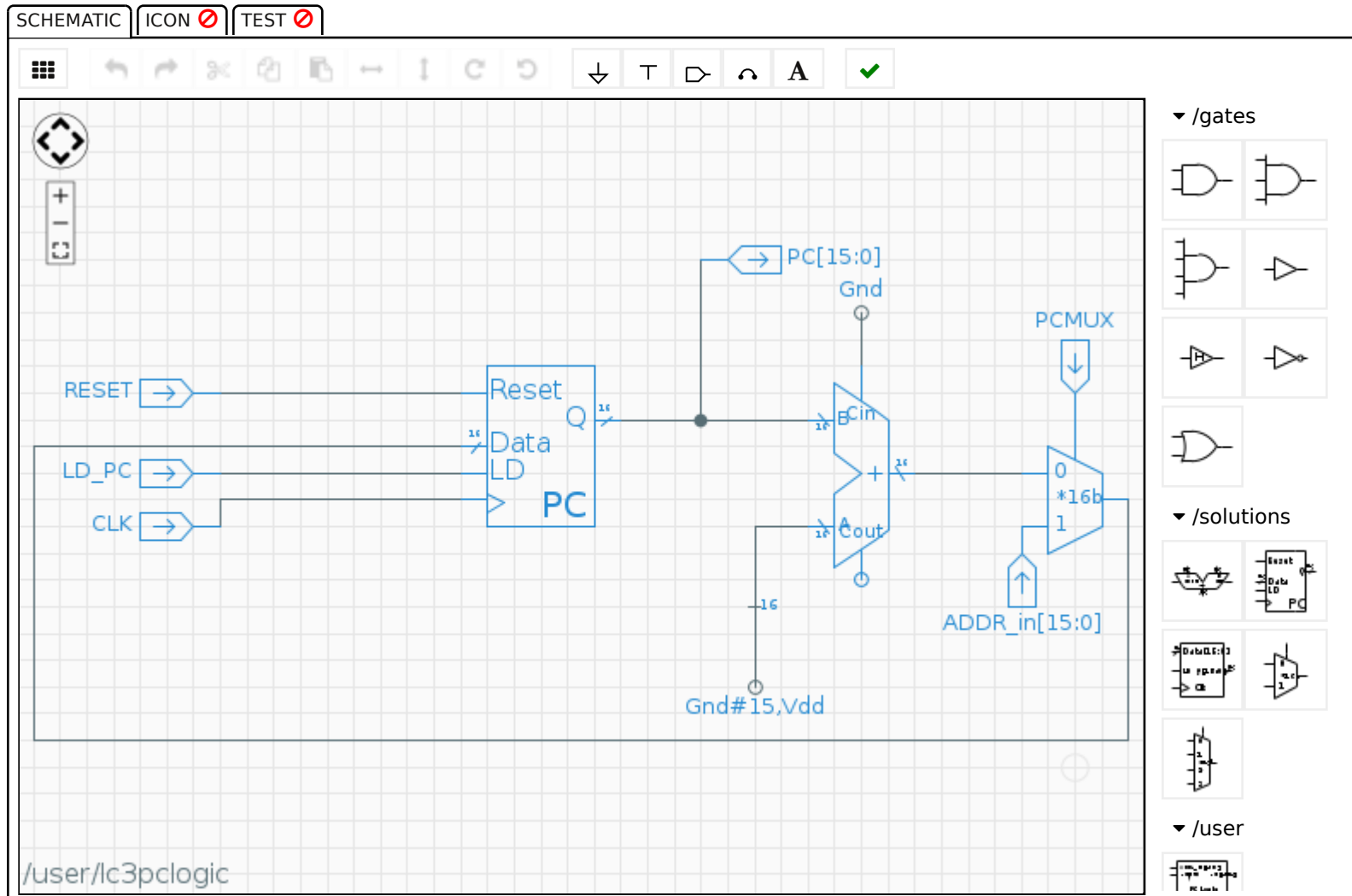
The incrementer is 16-bit adder with one of the inputs set to the value 1, which is achieved by tying bit 0 to the supply voltage and bits 1 through 15 to ground. To pass the incremented PC through the PC mux, the select input PCMUX = 0. When PCMUX = 1, the other mux data input, ADDR_in[15:0], (which will be used for branch instructions) is passed through the PC mux.

Don't forget you can label wires to tie them to ground and vdd. For example, if you double click on a wire and name it: "gnd,vdd,gnd", it would be "010".

After testing and checking, save this as a library component. We will need it in future labs!

LC-3 LITE PC LOGIC (1/1 point)

Module: /user/lc3pclogic



Click component to select, click and drag on background for area select, shift-click and drag on background to pan

[Lecture 2.2.43 \(2015 © MIT EECS\)](#)

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