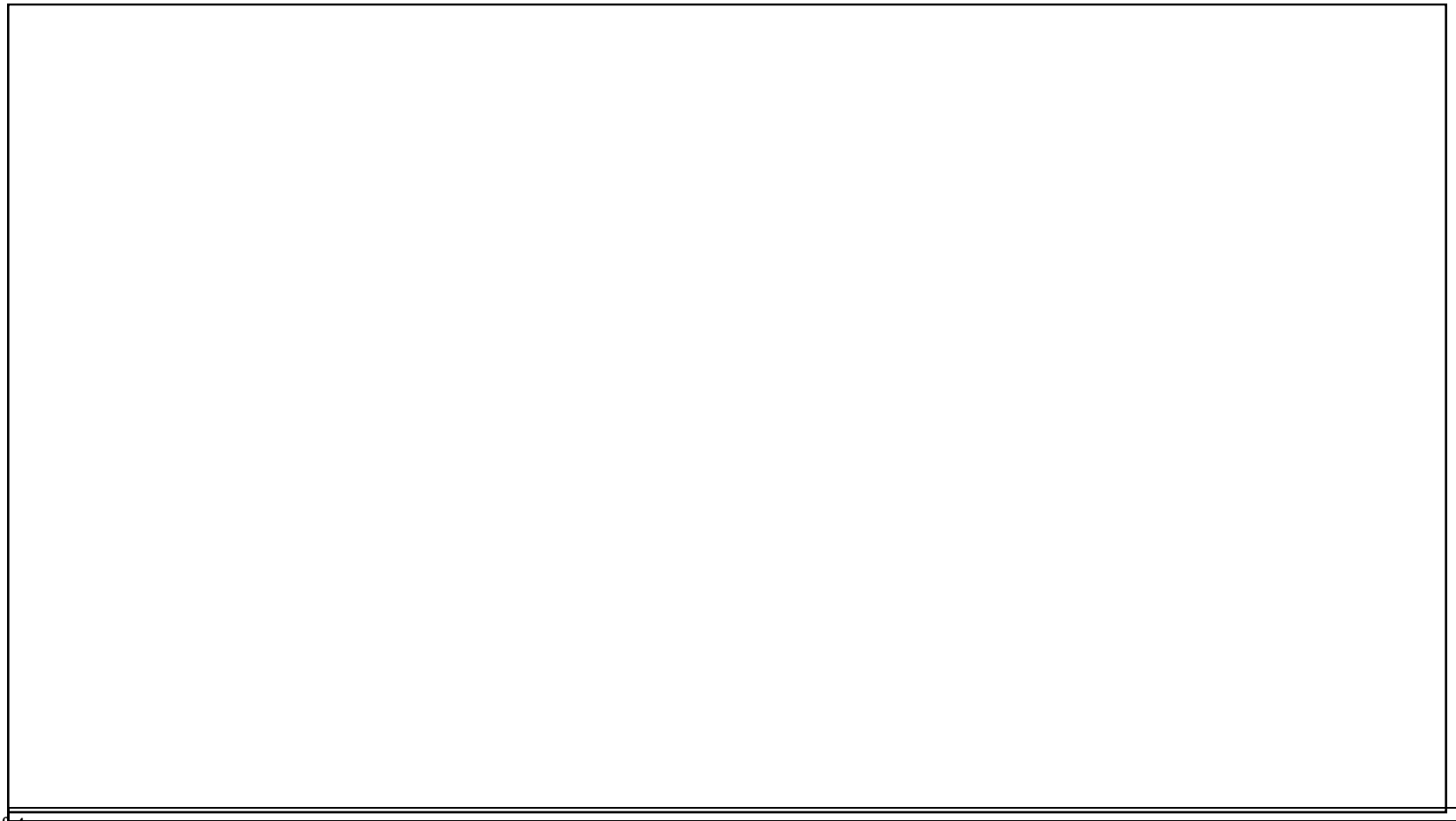
LDR INSTRUCTION



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1. CHECK YOUR UNDERSTANDING (1/1 point)

Which of the following is a true statement regarding the execution of the LC-3 LDR instruction?

- Assuming that the Memory can be read in a single cycle, the instruction requires two cycles of execution beyond the Instruction Decode state.
- During the Evaluate Address phase, the PC is added to the sign-extended immediate value to form the memory address.
- The bus is used exactly four times. ✔
- The CC register is not updated for this instruction since Memory is read.

EXPLANATION

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With a single cycle Memory, three cycles are needed to transfer information between registers. In the first cycle, one of the general-purpose (Register File) registers is read to form the address, which is loaded into MAR. In the second, the MAR register is read to access Memory and the data is placed into MDR. In the third, the data is read from MDR and loaded into the designated general-purpose register while the CC register is simultaneously loaded.

During Evaluate Address, the base register, not the PC, is added to the sign-extended immediate.

The bus is used four times. During instruction fetch, it is used twice: once to transfer the address from PC to MAR, and a second time to transfer the instruction from MDR to IR. The bus is used a third time to send the address to MAR, and a third time to write the result and update the CC register.

The CC register is updated since LDR writes the Register File.

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