OUT-OF-ORDER EXECUTION

4:15 / 4:15 1.0x

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1. CHECK YOUR UNDERSTANDING

Answer the following questions regarding an issue queue entry as described in the video.

1 A. CHECK YOUR UNDERSTANDING (1/1 point)

What is the purpose of the comparator circuits (designated as “=?”)?

- (•) To determine whether the destination register number of the issued instruction matches one or both of the source register numbers for this entry. ✔
- ( ) To determine whether the destination register number of the issued instruction matches the destination register number for this entry.
- ( ) To determine whether an instruction can be removed from the issue queue.
- ( ) To determine which issue queue entry is available for a new instruction.

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EXPLANATION

The comparators ensure that instructions in the queue that have a data dependence with one or more earlier instructions wait until those earlier instructions have issued. Therefore, the comparison is made between the destination register number of the issued instruction and the source register numbers of the queue entry.

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1 B. CHECK YOUR UNDERSTANDING (1/1 point)

What is the difference between the box labeled *SR1* and the one labeled *[SR1]*?

- *SR1* refers to one source register and *[SR1]* to the other source register.
- *SR1* holds the register number for source register 1 while *[SR1]* holds the data associated with source register 1. ✔
- *SR1* and *[SR1]* both hold the data for source register 1. The difference is that the data in *[SR1]* is sent to the ALU.
- *SR1* and *[SR1]* both hold the register number for source register 1. The difference is that *[SR1]* is sent to the ALU.

EXPLANATION

SR1 holds the register number associated with source register 1. It is compared with the *DR* field of the issued instruction to determine if this source register is available.

[SR1] holds the data associated with source register 1. The data is available from the register file if there are no data dependent instructions in the pipeline ahead of this instruction. Otherwise, it may be loaded when a data dependent instruction bypasses the result back to the issue queue.

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DUAL ISSUE QUEUE OPERATION

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