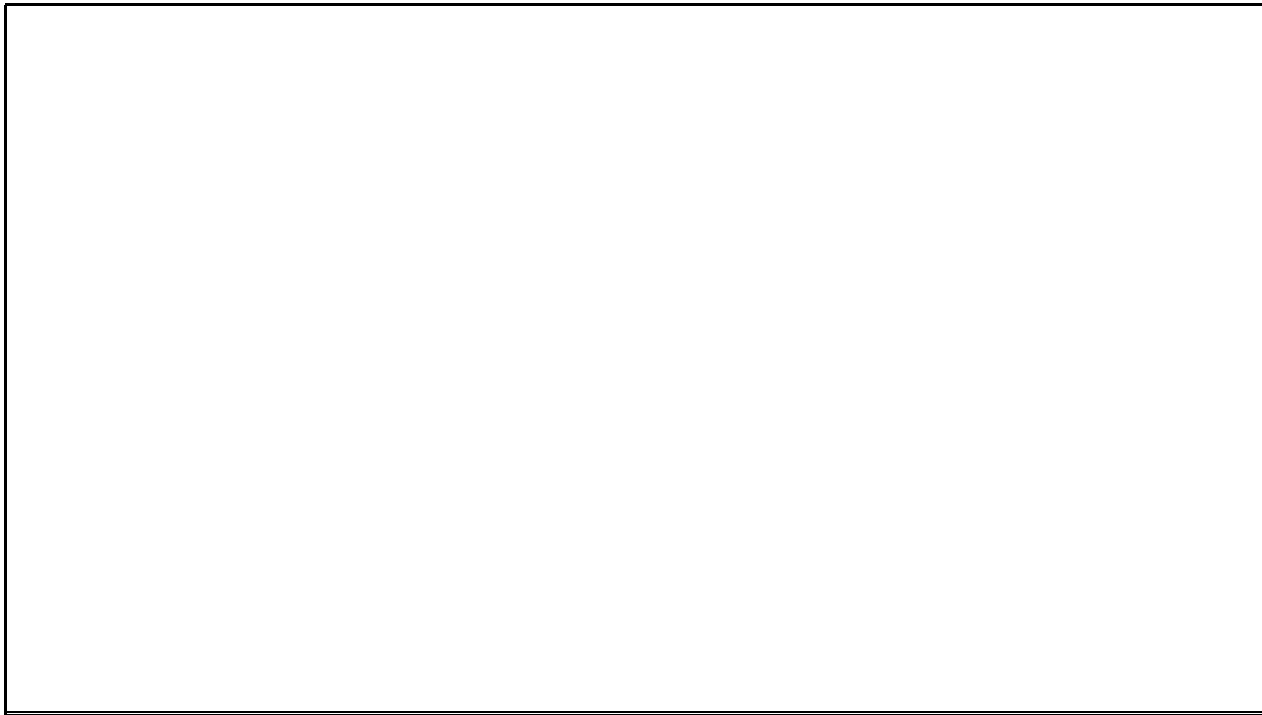




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LC-3 MEMORY-MAPPED I/O HARDWARE



3:01 / 3:01

1.0x

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1. CHECK YOUR UNDERSTANDING (1/1 point)

Which of the following is **NOT** a true statement regarding the reading of the KBDR in the LC-3 memory-mapped I/O hardware?

- ☐ The MAR register is loaded with the address of the KBDR.
- ☒ The KBDR is loaded with the ASCII code contained in the MDR. ✓
- ☐ The MDR is loaded with the data from the INMUX rather than the bus.
- ☐ GateMDR is a 1 to allow the MDR to drive the bus.

EXPLANATION

In order to select the KBDR, its address is loaded into MAR. The KBDR is read by the processor, and not written, so the second statement is false. Instead the MDR is loaded with the value that passes from the KBDR through the INMUX, and then it is sent onto the bus by setting GateMDR to 1.

[Hide Answer](#)*You have used 2 of 2 submissions*[Show Discussion](#)[✎ New Post](#)**2. CHECK YOUR UNDERSTANDING** (1/1 point)

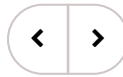
Which of the following is **NOT** a true statement regarding a store to Memory in the LC-3 memory-mapped I/O hardware?

- ☒ The MDR is loaded with the data from the INMUX rather than the bus. ✓
- ☐ The ADDR.CTL.LOGIC recognizes that the address from MAR is for the memory.
- ☐ GateMDR is 0 so that MDR does not drive the bus.
- ☐ It doesn't matter what input to the INMUX is selected to appear at its output.

EXPLANATION

The first statement is false. Since this is a store, the MDR data comes from the bus and not the INMUX. The ADDR.CTL.LOGIC will observe that the address from MAR is for the memory. In order to receive the address and data for the store, GateMDR should be 0. Also, since this is a store, the data from the INMUX is ignored.

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