

Help

BRANCH INSTRUCTION



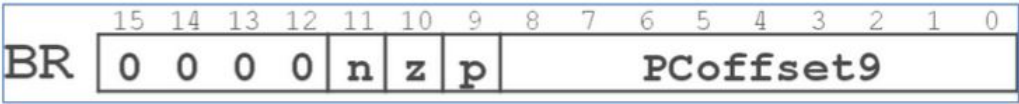
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Consider the LC-3 BR instruction, whose format is as follows:



1 A. CHECK YOUR UNDERSTANDING (1 point possible)

The memory location of the BR instruction is decimal 1000, and the Condition Code is 010. Pick the correct value of the PC for the following value of the BR instruction: 0000010000000111


- ☐ 1000
- ☐ 1001
- ☒ 1007 
- ☐ 1008 

EXPLANATION

The PC is incremented to 1001 during the Instruction Fetch phase of the BR instruction. The branch is taken since the z bit in the branch instruction and the Z bit in the Condition Code are both 1. The sign extended offset of 7 is added to 1001 to form the next PC of 1008.

[Hide Answer](#)*You have used 2 of 2 submissions*[Show Discussion](#)[New Post](#)**1 B. CHECK YOUR UNDERSTANDING** (1/1 point)

The memory location of the BR instruction is decimal 1000, and the Condition Code is 010. Pick the correct value of the PC for the BR instruction: 0000101000000111.

- ☐ 1000
- ☒ 1001 
- ☐ 1007
- ☐ 1008

EXPLANATION

The PC is incremented to 1001 during the Instruction Fetch phase of the BR instruction. The branch is not taken since the n and p bits in the branch instruction are 1 but the N and P bits in the Condition Code are both 0. (The BR is testing for not equal to zero, whereas the result of the last instruction that wrote the register file was zero.) Thus, the incremented value of the PC (1001) is not changed.

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