Help

HOW DO WE MEASURE PERFORMANCE?

9:46 / 9:46 1.0x

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1. CHECK YOUR UNDERSTANDING (1 point possible)

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For the following C statement

```
z = x + y;
```

consider two ways to implement the statement in assembly language:

Code A:

```
LDR R0, R4, #1
LDR R1, R5, #1
ADD R2, R1, R0
STR R2, R6, #1
```

Code B:

```
ADD M[R6+1], M[R5+1], M[R4+1]
```

The single instruction in Code B can read two source operands from memory, add them, and store the result into memory in a single instruction.

The data is arranged in memory such that R4+1 points to x, R5+1 to y, and R6+1 to z. Also, the microarchitecture is designed to execute each instruction in a single clock cycle.

Which of the following statements are true? **[You must check all that apply to earn credit]**

- [x] Code A would have a higher IC than Code B. ✔
- [x] Code A would have a lower CPI than Code B.
- [ ] Code A would require less address calculation hardware than Code B. ✔
- [x] Code A would require the ability to simultaneously read more values from the register file than Code B.

EXPLANATION

The first statement is true since Code A has four instructions compared to one for Code B.

Since the microarchitecture executes all instructions in a single cycle, the CPI for both sequences is 1. Thus, statement two is false.

The third statement is true. Each of the LDR and STR instructions require only one address calculation. The single ADD instruction requires three. Since this instruction is executed in one cycle, we need three copies of the address calculation hardware.

For the fourth statement, the opposite is true. The instructions in Code A require at most two simultaneous reads of the register file (for the ADD and the STR), while the single ADD in Code B requires three: R4, R5, and R6.

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