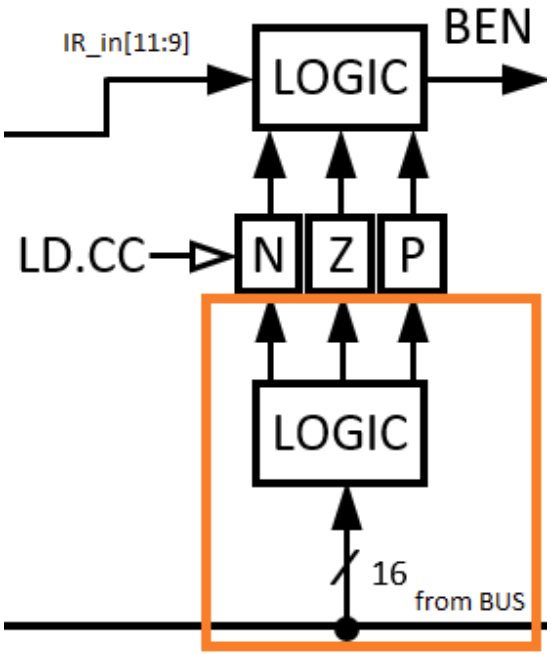
Design the LC-3 Condition Code generation logic and test it using the provided test file.

The area of the LC-3 we are designing is shown here in the red box:



The input to this combinational logic circuit is a 16-bit two's complement value, and the outputs are N, Z, and P, only one of which should be a 1 for any given input value.

N is 1 when the input is a negative number, otherwise 0.

Z is 1 when the input is zero, otherwise it is 0.

P is 1 when the input is a positive number, otherwise it is 0.

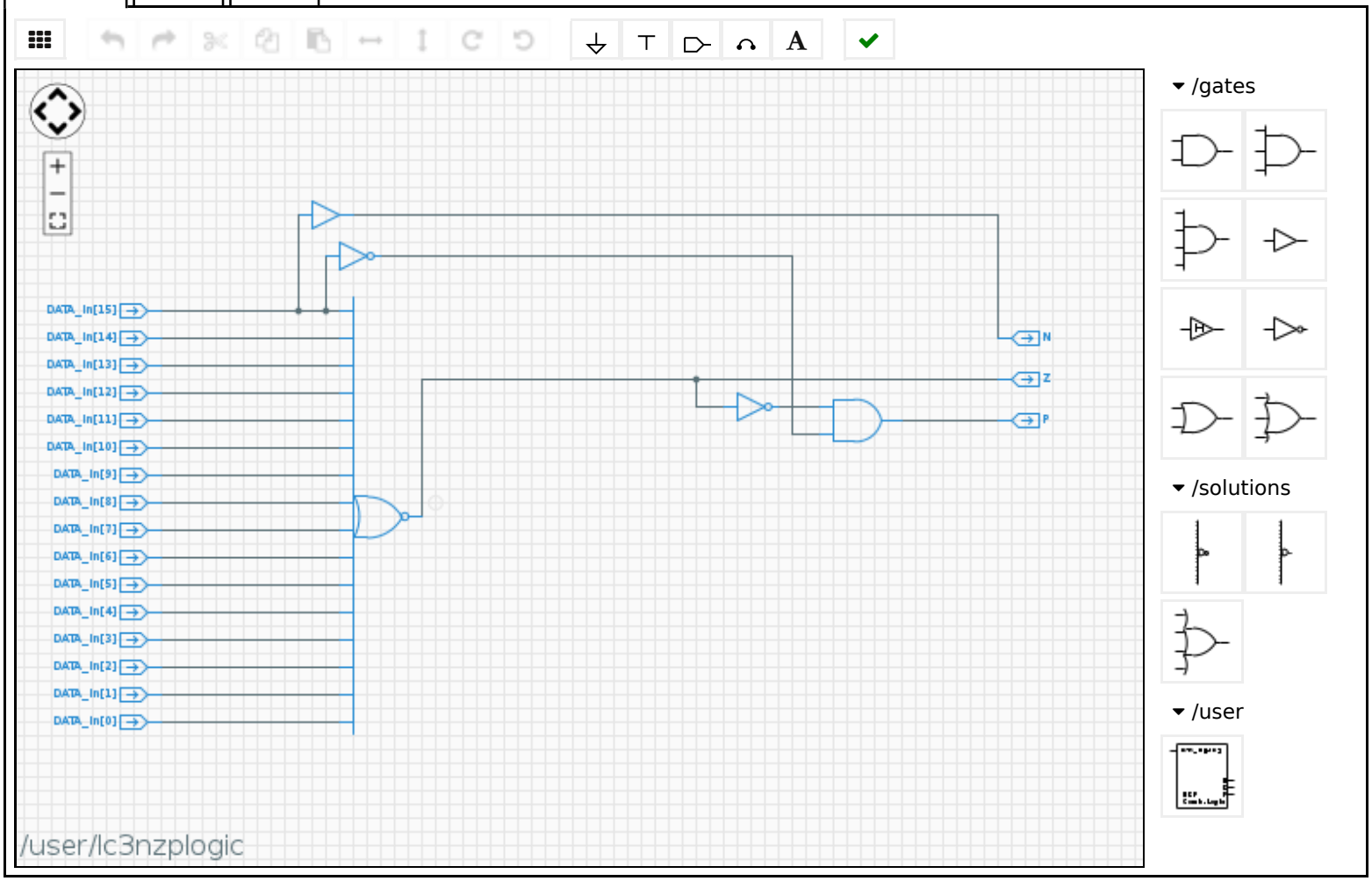
Help

After testing and checking, save this as a library component. We will need it in future labs!

LC-3 LITE CONDITION CODE LOGIC (1/1 point)

Module: /user/lc3nzplogic

SCHEMATIC ICON TEST



Jade 2.2.43 (2015 © MIT EECS)

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