Lab 8: Complete LC-3 Lite

This is it: Here we'll put together the entire LC-3 Lite!

Using your old labs, and the block diagram as a reference, wire up the LC-3 Lite!

We've built a lot of modules already. To finish the LC-3, we need to add:

- IR (the Instruction Register), a 16-bit loadable register
- MAR (Memory Address Register), a 16-bit loadable register
- MDR (Memory Data Register), a 16-bit loadable register
- MDR Multiplexer
- BusOut Multiplexer, a 16-bit 4-to-1 multiplexer
- the Control FSM, which is provided for you. An optional lab (non-graded) allows you to build it too.

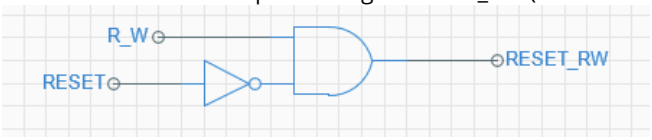
Add each of these circuits to the diagram and hook them up according to the block diagram.

Integrating the Memory

The memory module with the test code is already instantiated on the schematic. Don't delete the contents! We are using a 2-ported version, and will wire one port to be used only for reads, and one port to be used only for writes. Each port has an Address (A), Data (D), Output Enable (OE), and Write Enable (WE) signals. Let's use the top port as the *write port* and the bottom port as the *read port.*

For the write port:

- OE should be hooked up to GND (it will never output a signal)
- WE should be hooked up to the signal RESET_RW (a combination of Reset and Read/Write, from the FSM):



- A should be hooked up to the output of MAR
- D should be hooked up to the output of the MDR

For the read port:

- OE should be hooked up to VDD (it will always output signals)
- WE should be hooked up to GND (it will never write)
- A should be hooked up to the output of MAR

- D should be hooked up to input 0 of the MDRMUX, as on the diagram.

An interesting error sometimes comes up:

> "Node [object Object] is not connected to any output but is an input to the following devices: lc3testmemory"

Help

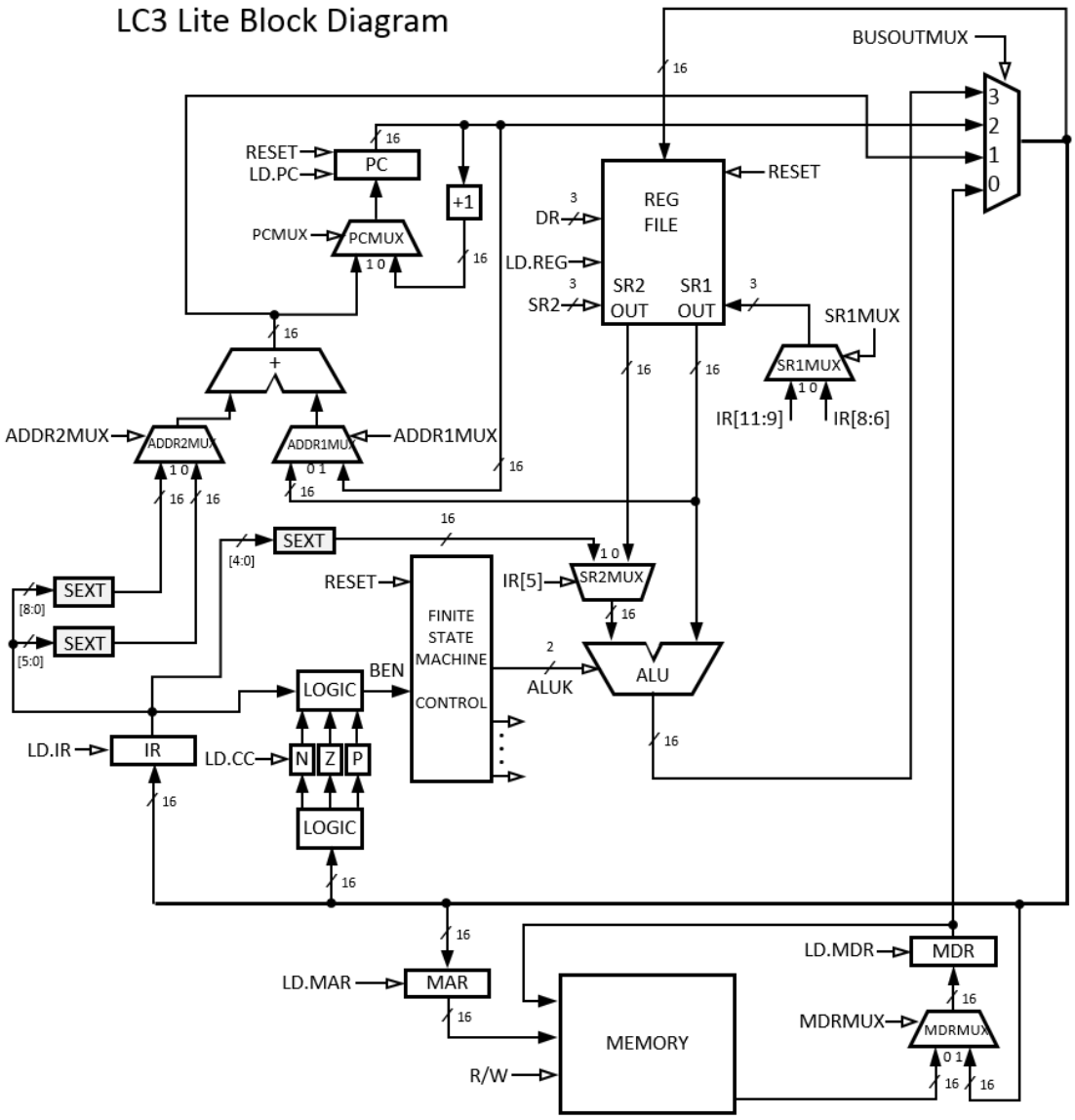
If you see this error, it may be related to the Address ports of the memory and the MAR output. Instead of drawing wires directly from the MAR ouput to the memory Address ports, use a wire stub for the MAR output and name it (i.e. MEMADDR[15:0]), and then use wire stubs (also named the same as the MAR output wire stub) to connect them (wire stubs examples are like the labeled wires hanging off the gates in the RESET_RW picture above).

Remember to load your user modules. Feel free to use your own FSM if so. Label all your wires wider than 1 bit with the correct width to avoid errors. Good luck! If a module doesn't load, please save and try to reload the page!

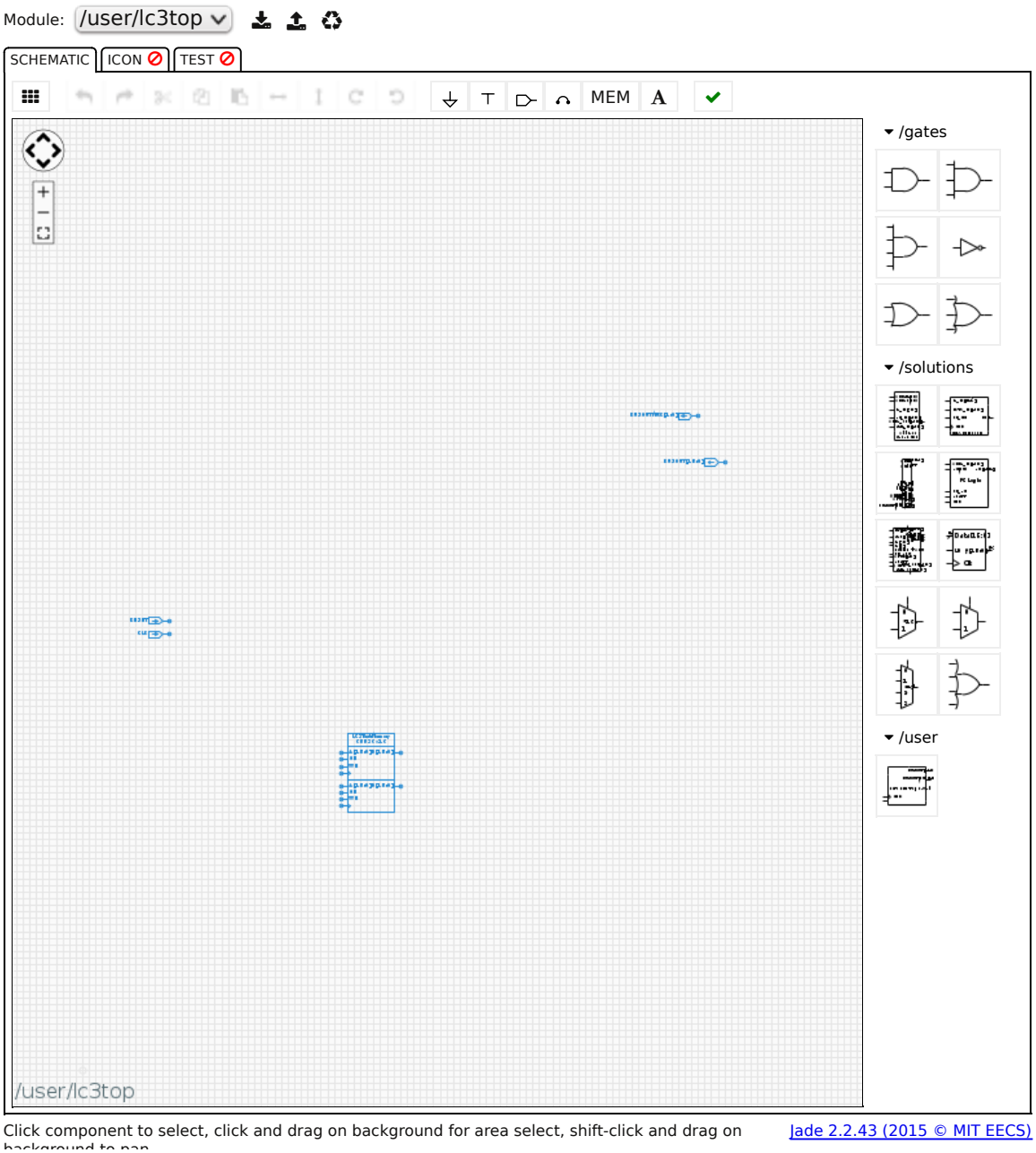
Check and save this module.

Here is the block diagram:

Help



LC-3 LITE (1 point possible)



Error detected:
Circuit does not have a node named "busout[15]".

Circuit does not have a node named "busout[14]".

Circuit does not have a node named "busout[13]".

Circuit does not have a node named "busout[12]".

Circuit does not have a node named "busout[11]".

Circuit does not have a node named "busout[10]".

Circuit does not have a node named "busout[9]".

Circuit does not have a node named "busout[8]".

Circuit does not have a node named "busout[7]".

Circuit does not have a node named "busout[6]".

Circuit does not have a node named "busout[5]".

Circuit does not have a node named "busout[4]".

Circuit does not have a node named "busout[3]".

Circuit does not have a node named "busout[2]".

Circuit does not have a node named "busout[1]".

Circuit does not have a node named "busout[0]".

Circuit does not have a node named "busoutmux[1]".

Circuit does not have a node named "busoutmux[0]".

Help

Check

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