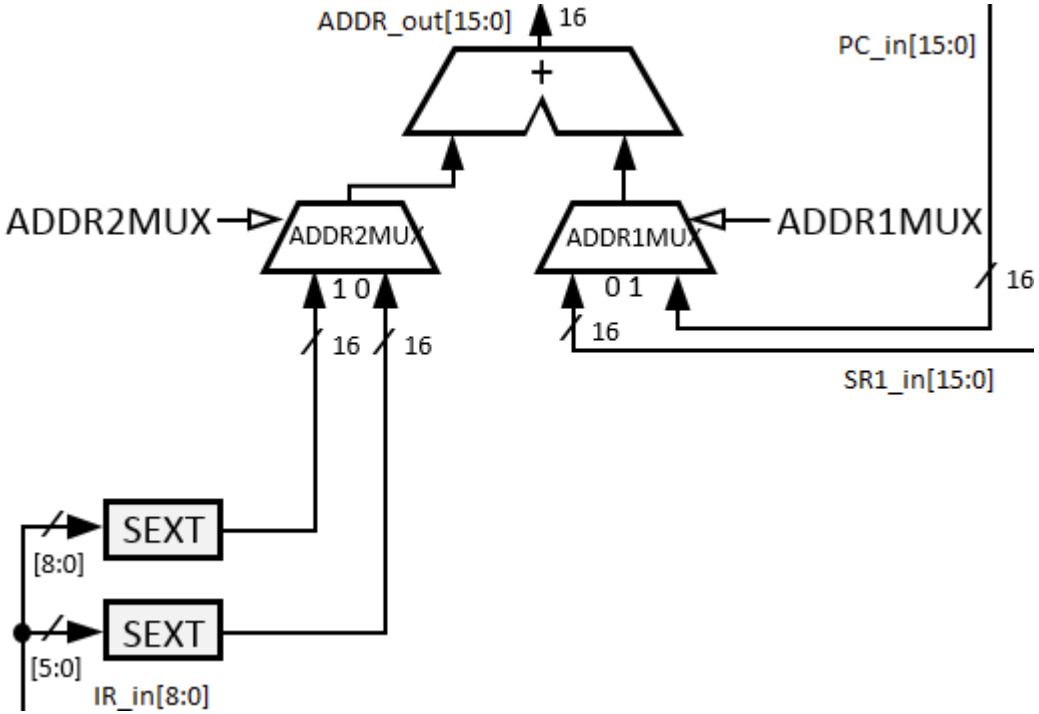
Design the LC-3 Lite Address Generation logic shown in the LC-3 Lite microarchitecture diagram, and test it using the provided test file. The design comprises two sign extension circuits (SEXT), two 2-to-1 muxes (ADDR1 and ADDR2), and a 16-bit adder.

The relevant section from the LC-3 Lite Diagram is shown here:



To pass the register value (SR1_in) through the ADDR1 mux for LDR instructions, the select input ADDR1MUX = 0. When

ADDR1MUX = 1, the other mux data input (the incremented PC for BR instructions) is passed through the mux.

To pass SEXT[5:0] through the ADDR2 mux for LDR instructions, the select input ADDR2MUX = 0. When ADDR2MUX = 1, SEXT[8:0] for BR instructions is passed through the mux.

Help

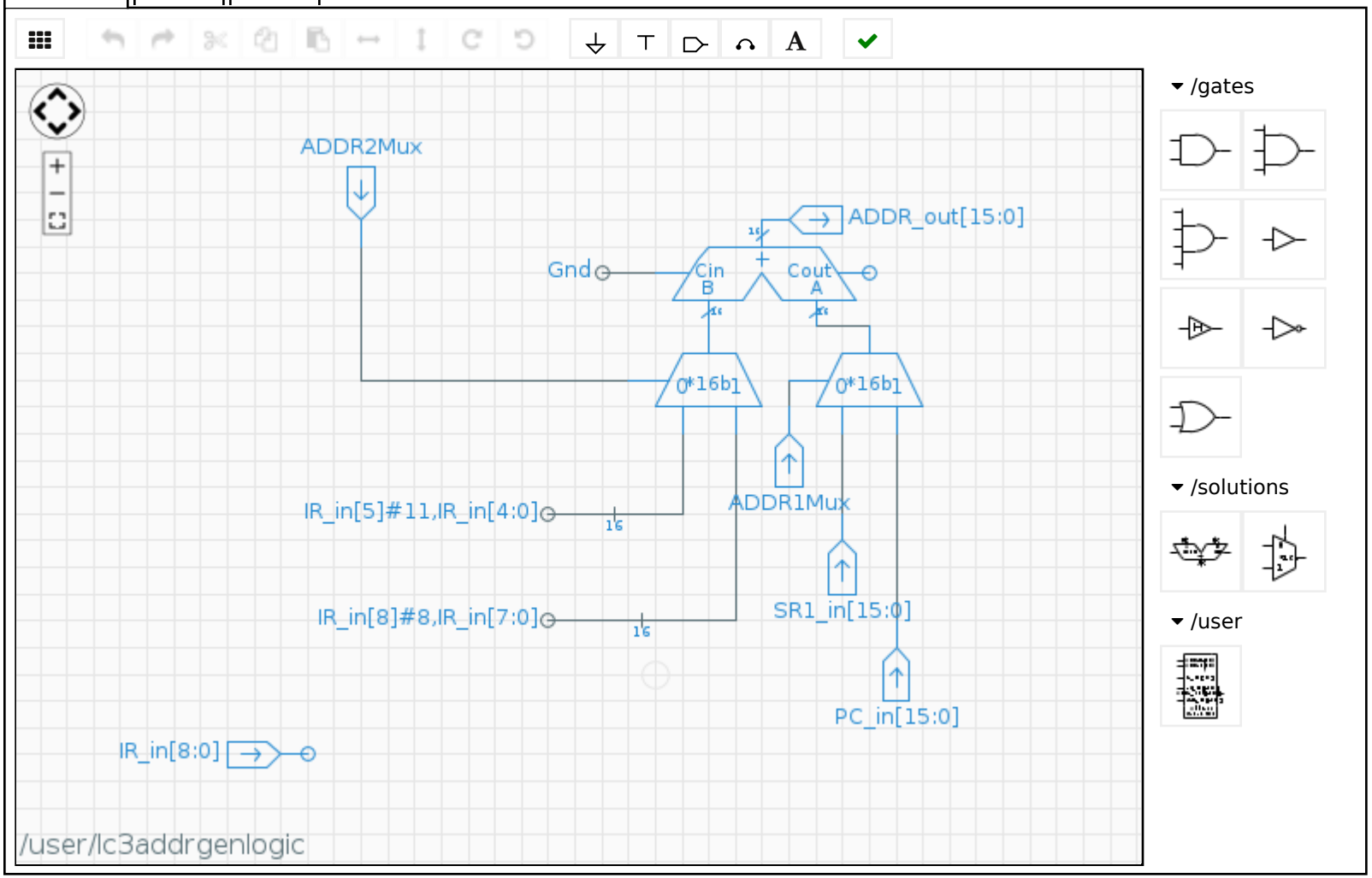
The sign extension circuits are merely wires. For the SEXT[5:0] circuit, bit 5 is replicated ten times; for SEXT[8:0], bit 8 is replicated seven times. Remember how Jade can replicate signals on wires. **Don't rename wires that are attached to the input or output terminals of the circuit!** That confuses Jade and its naming of the terminal (is it the terminal name, or is it this replicated wire name?). If you leave the terminal unattached to a wire, and then just rename the wire hanging off of the component's input or output, then it is clear to the simulator.

Save your design as a library component.

LC-3 LITE ADDRESS GENERATION (1/1 point)

Module: /user/lc3addrgenlogic

SCHEMATIC | ICON | TEST



Jade 2.2.43 (2015 © MIT EECS)

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