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A DIRECT MAPPED CACHE EXAMPLE

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| | 4:01 / 4:01 | 1.0x | | | |
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1. CHECK YOUR UNDERSTANDING

Answer the following questions about the direct-mapped cache example.

1 A. CHECK YOUR UNDERSTANDING (1/1 point)

Was the single cache hit the result of temporal or spatial locality? [You only have one try for this problem]



- ☒ Temporal 
- ☐ Spatial

EXPLANATION

Since the block size was a single word, there was no opportunity to exploit spatial locality. Block 0001 had been previously brought in the cache (the second load), and because the same block was accessed again by the last load, we had a hit due to temporal locality.

[Hide Answer](#)*You have used 1 of 1 submissions*[Show Discussion](#)[New Post](#)**1 B. CHECK YOUR UNDERSTANDING** (1 point possible)

If we implemented the same size cache, but increased the block size to two words, would the second load have been a hit or a miss?

- ☒ A hit, since the word for the second instruction would have been brought in on the miss for the first instruction. 
- ☒ A hit, due to temporal locality (reading the same word again). 
- ☐ A miss, since the second instruction has a different tag than the first instruction.
- ☐ A miss, since the second instruction has a different index than the first instruction.

EXPLANATION

With the same cache size, doubling the block size would cause us to have only two cache entries, 0 and 1. The rightmost bit of the address would be the word offset, the next bit the index, and the remaining two bits the tag.

Doubling the block size would cause the first two words in memory (with values 100 and 110) to be brought into the cache on the first cache miss. Word 0 would be sent to the processor, since the word offset is 0. The second load has the same index (0) and tag (00) as the first, which would result in a hit since we brought that word into memory on the miss for the first instruction. Word 1 would be sent to the processor, since the word offset is 1.

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