LAB 6. Loadable Flip-flop with Set / Reset

In this lab we will construct a loadable flip-flop with set and reset capability.

It's like a loadable flip-flop, but with two additional inputs, SET and RESET. When SET is high (1), the flip-flop will load a 1 on the positive edge of the next CLK signal. When RESET is high (1), the flip-flop will load a 0 on the positive edge of the next CLK signal. The SET and RESET inputs will never both be 1 (this is illegal).

Note that SET and RESET will work even if the input LD_REG is 0. In other words, SET and RESET don't care whether LD_REG is 0 or 1; their operations will take effect either way. This means you will have to add some logic to ensure that flip-flop's input load signal is 1 when SET/RESET are 1, even if the overall circuit input signal LD_REG is 0.

When SET and RESET are both 0, the circuit acts like a normal loadable flip-flop.

Remember to load your "/user/or4" if you use it. The solution for the loadable flip-flop is available in the parts bin.

The icon for this circuit, "/user/srloadablereg", also appears in the parts bin. Don't use that or you'll get a "recursive inclusion of module" error!

Test it, save it, and submit it to edX via the check button. In the next lab, we will construct a special 16-bit register, using this flip-flop.

LOADABLE FLIP-FLOP WITH SET / RESET (1/1 point)

Help

Module: /user/srloadableff

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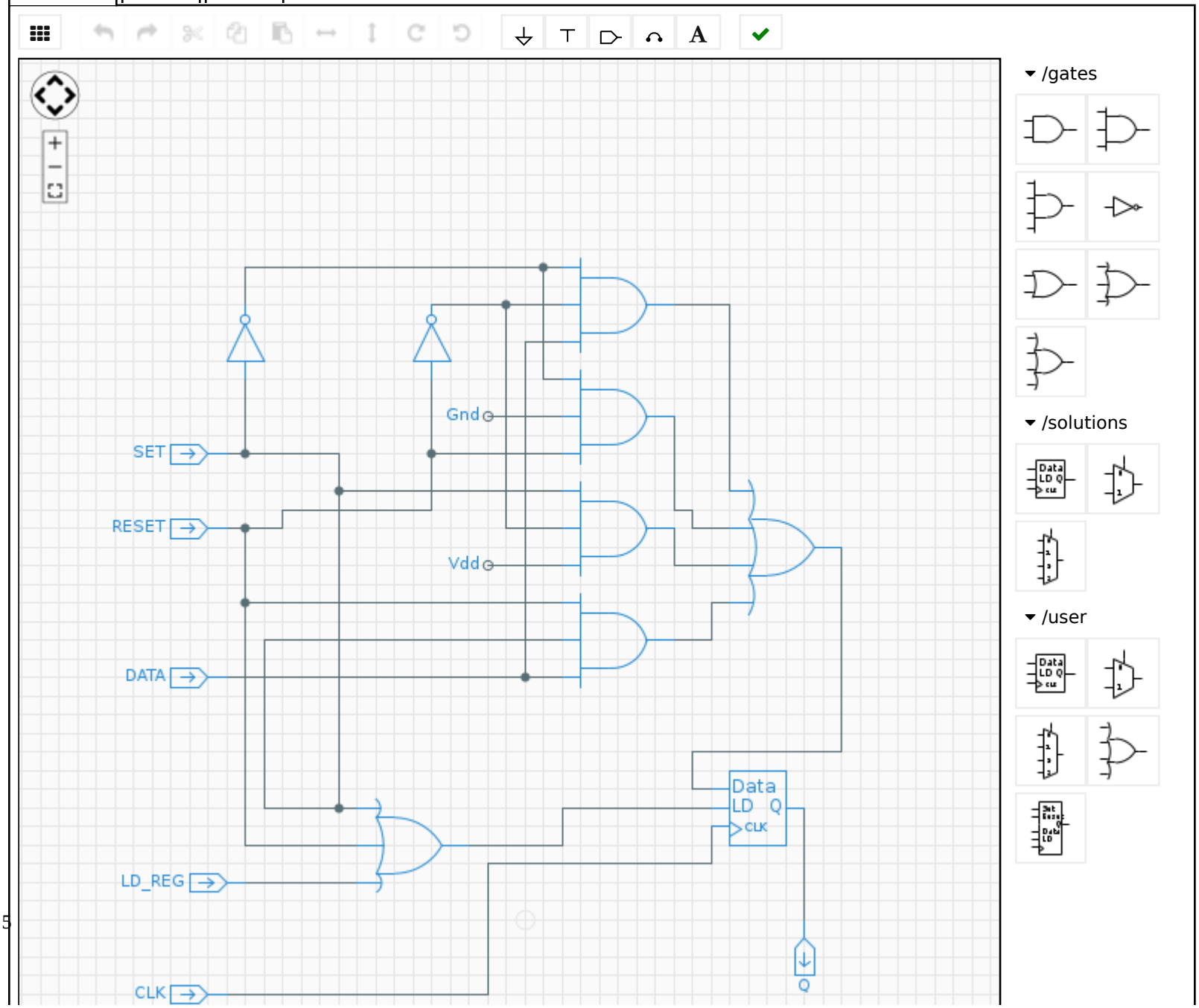

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