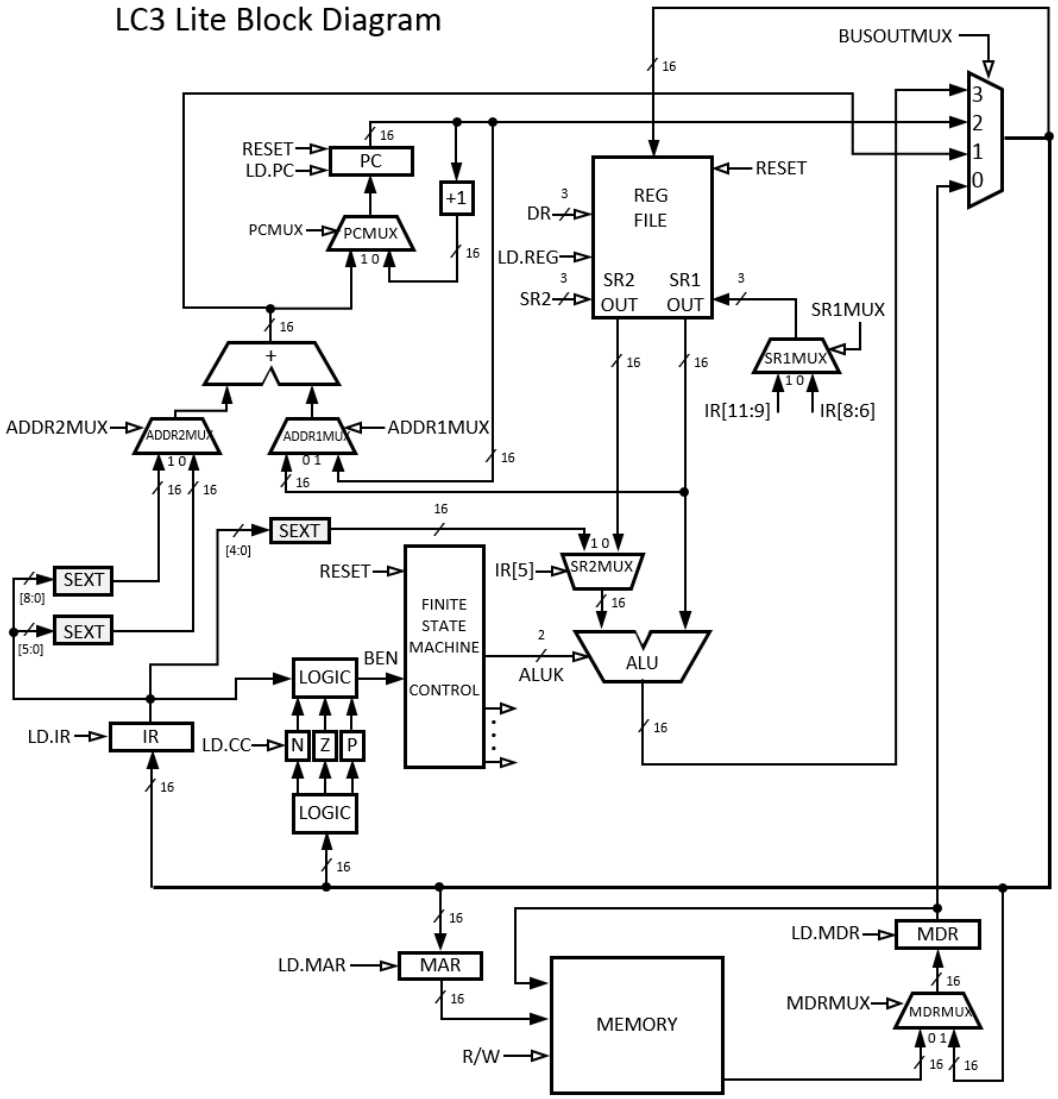
# LC-3 Lite

The LC-3 Lite is a reduced version of the LC-3 that you will implement using Jade. LC-3 Lite supports a subset of the LC-3 instruction set, specifically ADD, AND, NOT, LDR, STR, BR, and TRAP-Halt. The first six instructions operate the same as their full LC-3 counterparts. TRAP-Halt freezes the state of the machine, which occurs when the TRAP instruction (opcode 1111) is encountered, irrespective of the value of the TRAP vector. By freezing the state, register and memory values can be inspected in Jade in order to check for correct operation of the executed program.

Below is a block diagram of the LC-3 Lite microarchitecture that you will implement:



In addition to some repositioning of components and signals, you'll notice a few technical differences from the LC-3 diagram that you saw in the videos:

- A 4-to-1 MUX is used instead of a bus.
- IR[5] controls the SR2MUX.
- The PCMUX has only two inputs since JMP instructions are not supported.
- The ZEXT and MARMUX are removed since only TRAP-Halt is supported.
- The R signal is removed since Memory is accessed in a single cycle.
- The PC, Register File, and FSM Control receive a RESET signal as an input.
- Although we could support memory-mapped I/O in LC-3 Lite, Input and Output are removed due to the inability to receive input from, and send output to, a user in Jade.

The Memory is preloaded with the program to be run. The first program instruction in an LC-3 Lite program is always located at x3000, and the first program data item is always at x4000.

When the machine is powered on, the RESET signal is set to 1. This forces the initialization of the PC to x3000 (the address of the first instruction), register R4 to x4000 (the address of the first data item), and the FSM to state 0 (the first state of instruction fetch). After RESET goes to 0, the hardware begins fetching instructions starting at address x3000 and continues until the TRAP-Halt (opcode 1111) is encountered. This instruction causes the machine to freeze (remain in the Halt state of the FSM) so that register and memory values can be checked in Jade.