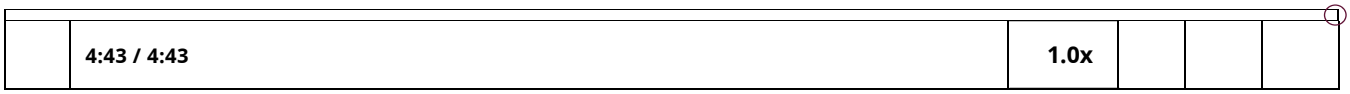
DIRECT MAPPED CACHE



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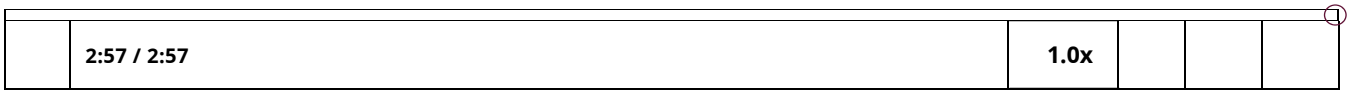
At 2:24, Professor Albonesi says that we have 2^2b bytes in each cache block, while the screen shows, 2^(b+1). What is shown on the screen, 2^(b+1), is correct.

At 2:49, Professor Albonesi says that the total cache capacity is 2^(2b+i), while the screen shows 2^(b+1+i). What is shown on the screen, 2^(b+1+i), is correct.

READING AND WRITING DIRECT MAPPED CACHE

Help



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1. CHECK YOUR UNDERSTANDING (1/1 point)

When reading a cache, the data can be read out while simultaneously checking for a cache hit. However, when writing, we first confirm that we have a cache hit before writing the data. Why is this the case?

- (•) Reading does not change the cache contents, but writing does. For writes, we check that we have the correct memory block before writing, so that we don't overwrite a different memory block. ✔
- ( ) Accessing the tag is faster for cache reads compared to cache writes.
- ( ) Accessing the tag is faster for cache writes compared to cache reads.
- ( ) Accessing the valid bit is faster for cache writes than for cache reads.

EXPLANATION

If we incorrectly read the wrong memory block out of the cache, the contents of the cache are not changed. However, if

we overwrite that block, we have lost its contents.

Accessing the tag and valid bits takes the same time for a read or a write.

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Final Check | **Save** | **Hide Answer** | *You have used 1 of 2 submissions*

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2. CHECK YOUR UNDERSTANDING (5/5 points)

An LC-3 direct mapped cache has 128 blocks, each of which holds 4 bytes (32 bits) of data.

Fill in the following fields related to the cache:

Total cache capacity in bytes?

512

512

Answer: 512

Number of word offset bits?

1

1

Answer: 1

Number of index bits?

7

7

Answer: 7

Number of tag bits?

8

8

Answer: 8

Number of main memory blocks that map to a given cache location?

Help

256

256

Answer: 256

EXPLANATION

The total cache capacity is 128 × 4 = 512 bytes.

Each location holds 32 bits or two LC-3 words. Therefore, we need one word offset bit to select between the two.

With 128 blocks, we need 7 bits to index the cache (2^7 = 128).

The remaining 16 – 7 – 1 = 8 bits of the address are the tag.

With 8 tag bits, then 2^8 = 256 main memory blocks map into a given cache location.

Final Check | **Save** | Hide Answer | *You have used 1 of 2 submissions*

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