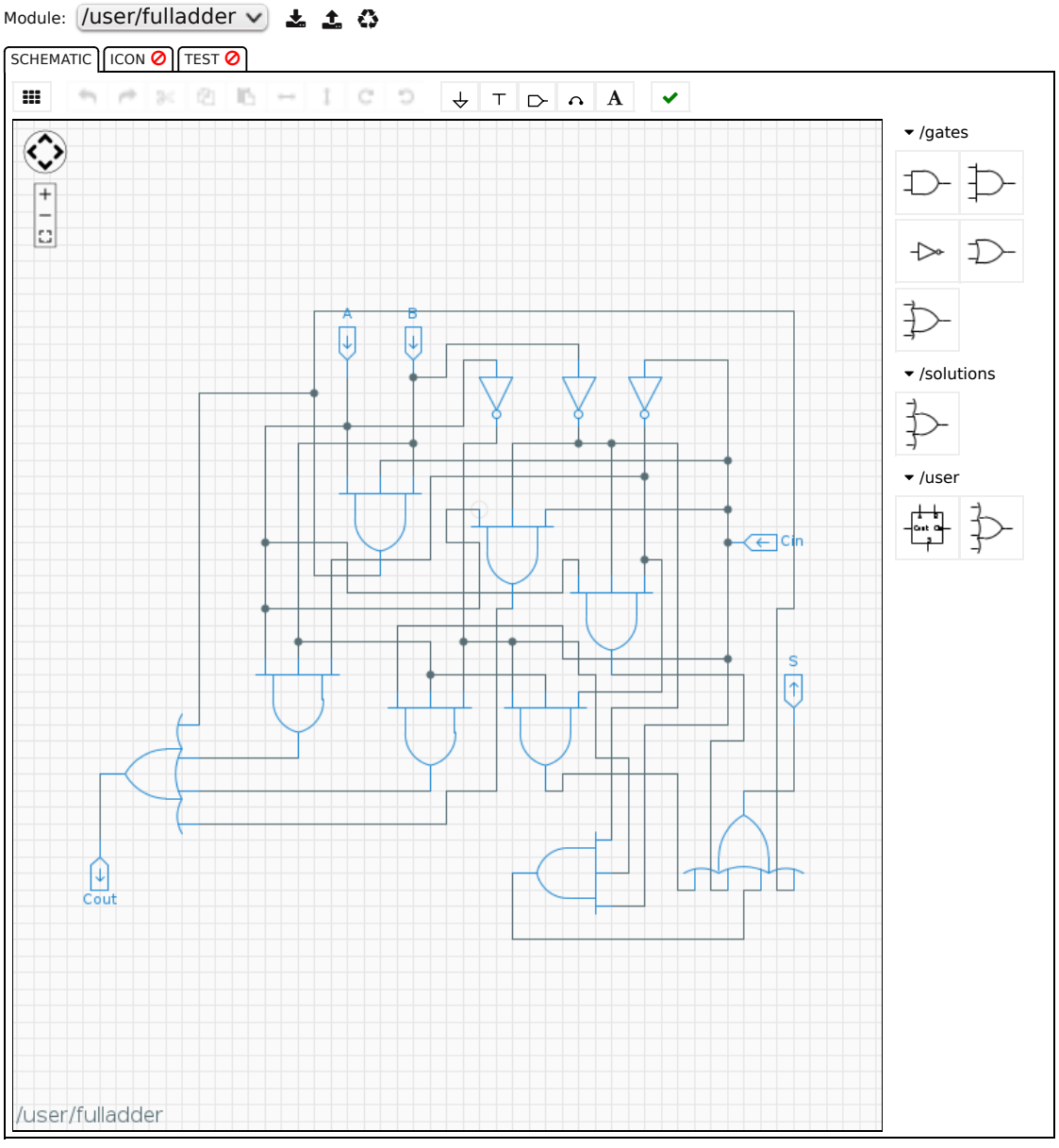
LAB 1. ADDER

Design a Full Adder, using NOT, AND, and OR gates, and test it using the provided test file.

You may want to load your "/user/or4".

After testing and checking, save this as a library component. We will need it in future labs!

FULL ADDER (1/1 point)



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LAB 2. ADDERS

Design a 2-bit adder/subtractor, using two copies of your Full Adder library component, two inverters, and two 2-to-1 Muxes. Your design should have an input signal, ***Subtract,*** that subtracts the inputs when ***Subtract* = 1** and adds them when ***Subtract* = 0**.

The output terminal ***Overflow*** should be connected to the carry out of the MSB. For unsigned integer addition, a 1 on this output indicates that overflow occurred (As discussed in the videos, a carry out of the MSB of 1 does not necessarily indicate that overflow occurred for two's complement integer arithmetic).

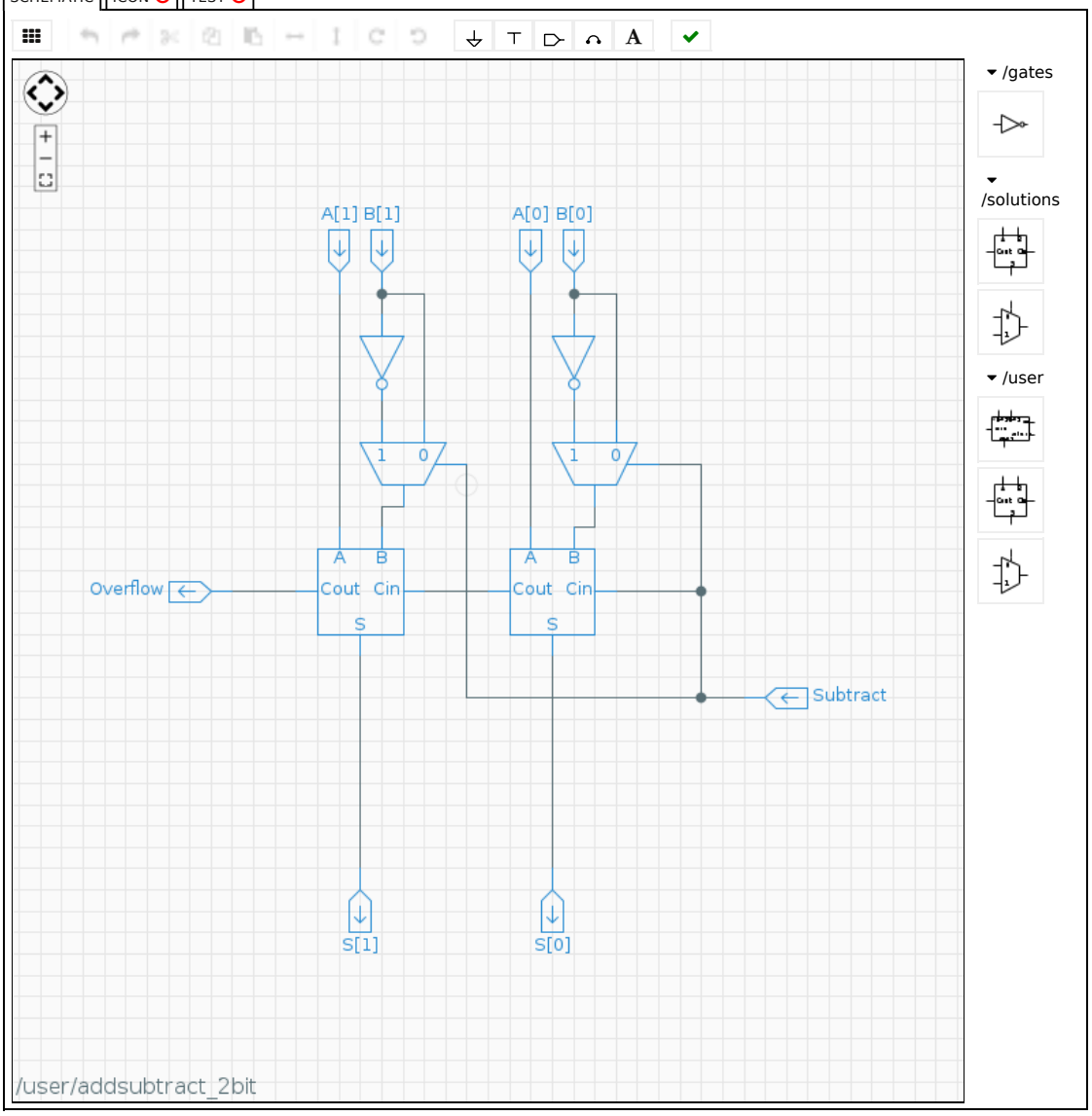
You need to load your "/user/mux2to1" and "/user/fulladder" designs, and "/user/or4" if you used that component.

Test your design using the provided test file. Save it after it passes the tests.

2-BIT ADDER/SUBTRACTOR (1/1 point)

Module: /user/addsubtract_2bit

SCHEMATIC ICON TEST



Click component to select, click and drag on background for area select, shift-click and drag on background to pan

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LAB 3. ADDERS

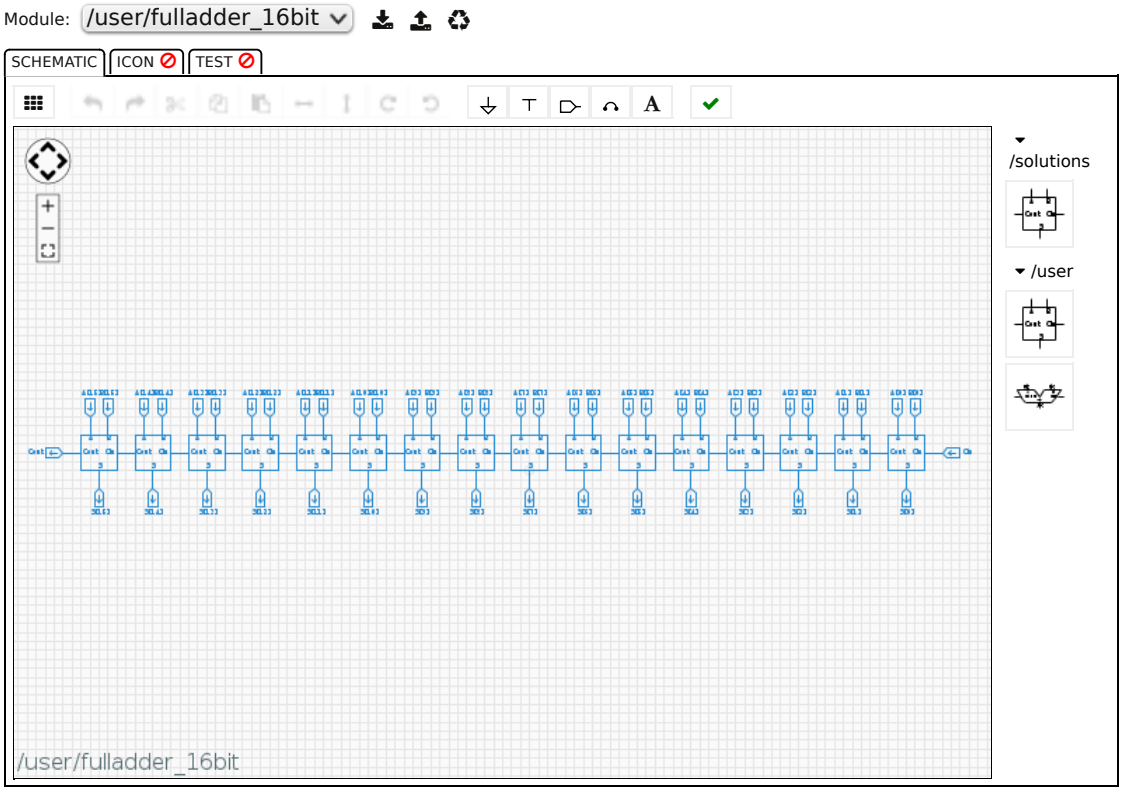
Design a 16-bit Ripple Carry Adder that adds the 16-bit inputs A and B, using 16 copies of your Full Adder library component, and test it using the provided test file.

Don't forget to load your "/user/fulladder" component, and "/user/or4" if you used that component.

After testing and checking, save this as a library component. We will need it in future labs!

16 BIT RIPPLE CARRY ADDER (1/1 point)

Help



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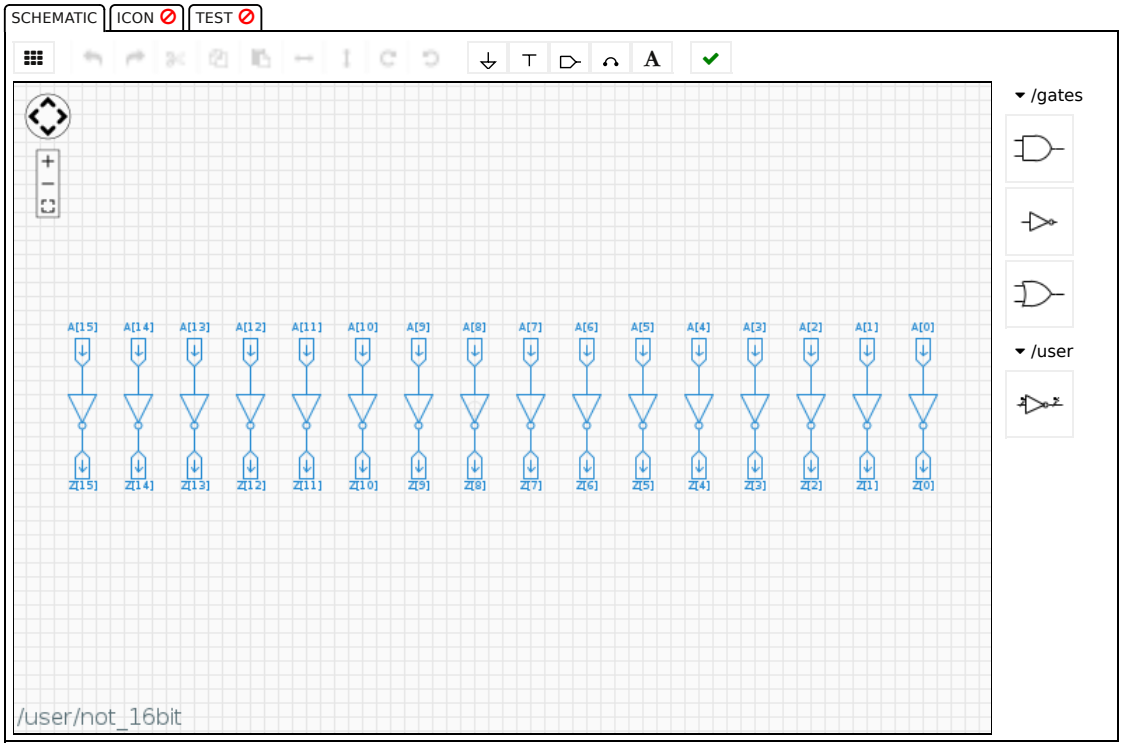
LAB 4. ADDERS

Design a 16-bit **NOT** circuit that inverts the individual bits of the 16-bit input A and test it using the provided test file.

After testing and checking, save this as a library component. We will need it in future labs!

16 BIT NOT (1/1 point)

Module: /user/not_16bit



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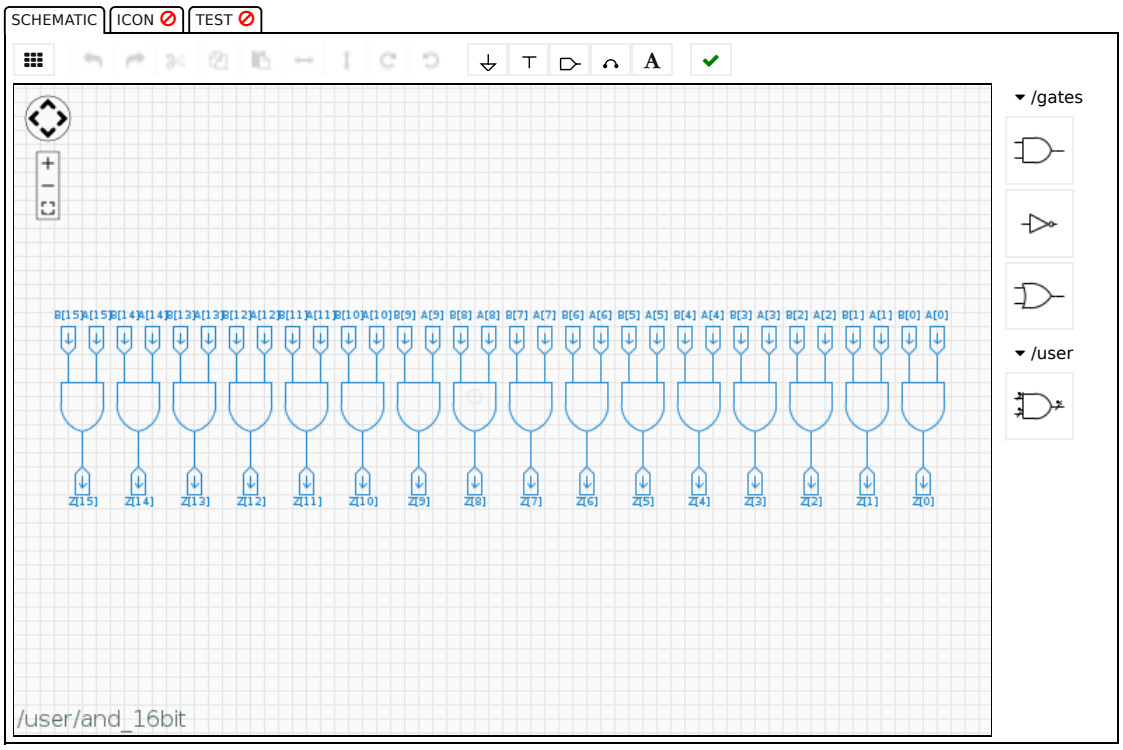
LAB 5. ADDERS

Design a 16-bit AND circuit that ANDs the individual bits of the 16-bit inputs A and B and test it using the provided test file.

After testing and checking, save this as a library component. We will need it in future labs!

16 BIT AND (1/1 point)

Module: /user/and_16bit



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LAB 6. ADDERS

Design an *Arithmetic Logic Unit (ALU)* that performs the Add, NOT, and AND operations on the 16-bit inputs A and B, and also provides the ability to pass A to the output unchanged.

The 16-bit output of the ALU is defined by the 2-bit ALUK input:

ALUK[1]	ALUK[0]	ALU Output
0	0	Addition of A and B
0	1	AND of A and B
1	0	NOT of A
1	1	A (unchanged)

In your design, the inputs A and B should be passed to your previously designed Add, NOT, and AND circuits and the output of those components sent to the appropriate data inputs of a 16-bit 4-to-1 Mux as defined by the above table. The last data input of the Mux should be the input A. The select input for the Mux is the 2-bit ALUK input. Take care to connect ALUK[1] and ALUK[0] to the correct two bits of the select input.

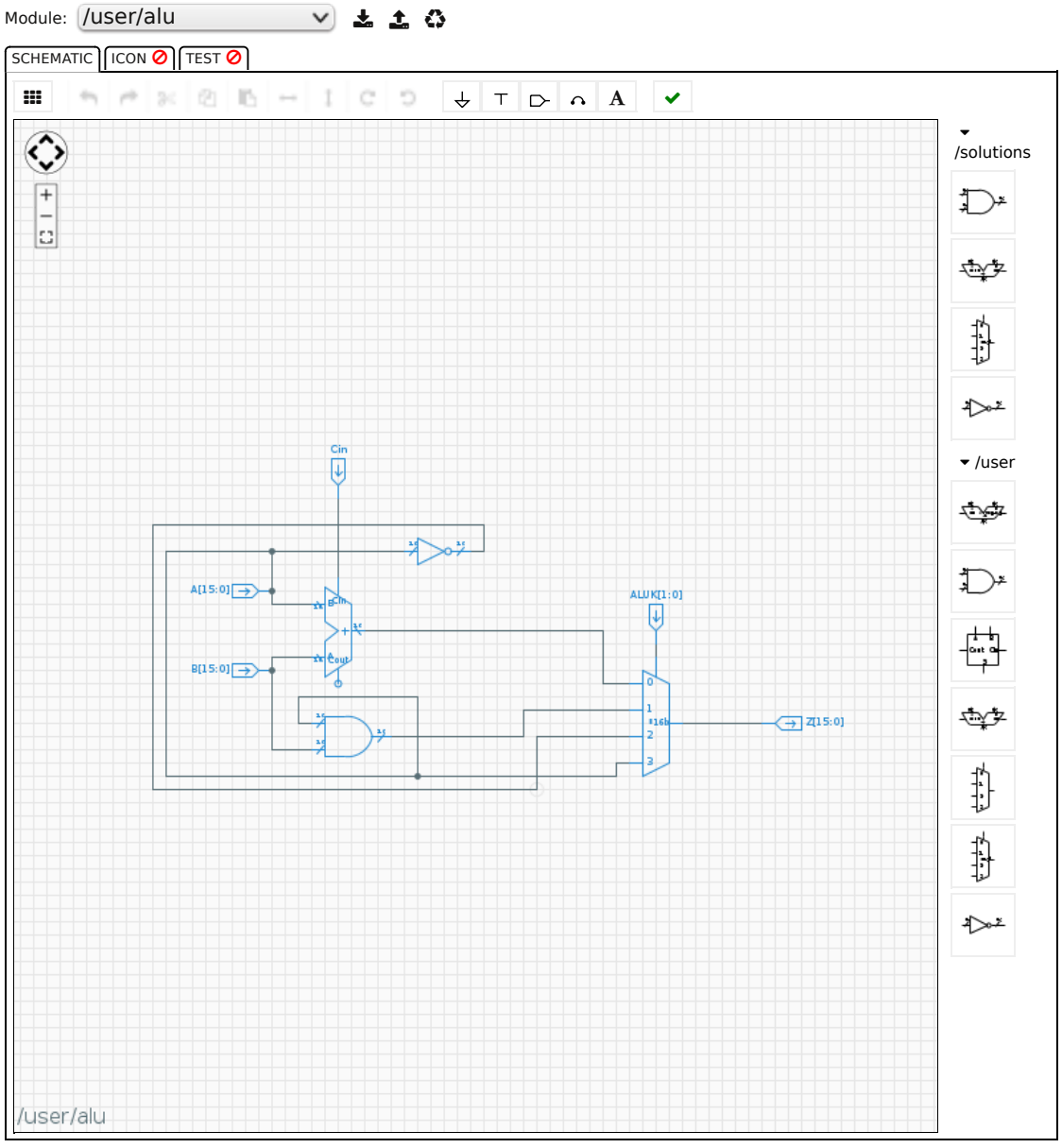
Load your "/user/fulladder", "/user/fulladder_16bit", "/user/and_16bit", "/user/not_16bit", "/user/mux4to1", "/user/mux4to1_16bit" modules first, and "/user/or4" if you used that component.

Test your ALU using the provided test file.

After testing and checking, save this as a library component. We will need it in future labs!

Help

ALU (1/1 point)



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