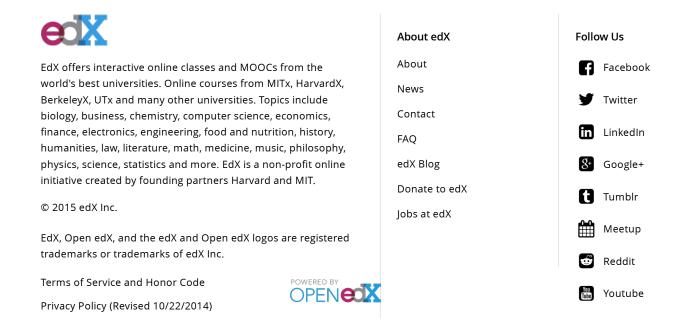
| rseware | Course Info | Discussion | Wiki | Progress | Discussion Guidelines | Resources | Exploring | |
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Recall that a pipelined processor can, in the absence of hazards, achieve a Cycles Per Instruction (CPI) close to 1. What CPI can be achieved in a 2-way superscalar pipeline in the absence of hazards?

1 of 2 05/14/2015 04:49 PM



2 of 2 05/14/2015 04:49 PM