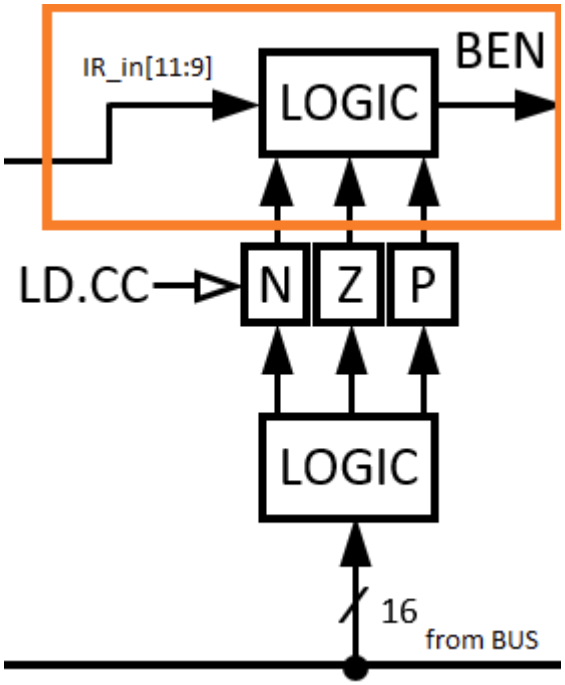
Design the LC-3 BEN logic, and test it using the provided test file.

The area of the LC-3 we are designing is shown here, in red:



The design takes as inputs IR[11:9] and the value of the 3-bit CC (condition codes: N, Z, P) register and generates a single BEN output.

Refer to the BR Instruction Unit video to design this logic.

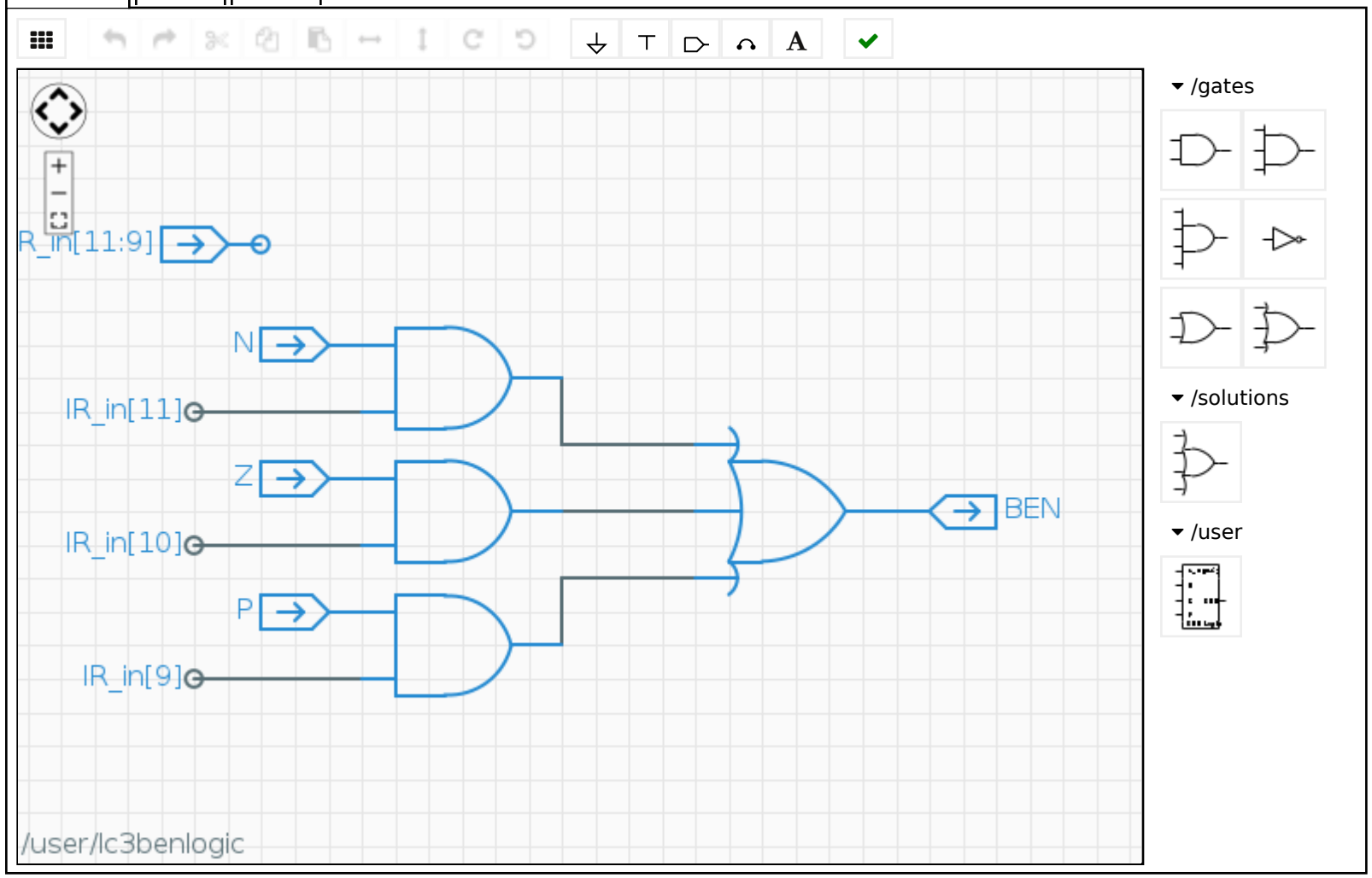
Save your design as a library component.

LC-3 LITE BRANCH ENABLE LOGIC (1/1 point)

Help

Module: /user/lc3benlogic

SCHEMATIC | ICON | TEST



Click component to select, click and drag on background for area select, shift-click and drag on background to pan

Jade 2.2.43 (2015 © MIT EECS)

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Help

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