In this module we will cover the last part of our von Neumann machine – the control unit that orchestrates and synchronizes the operation of the computer. We will discuss the details of the finite state machine that controls the LC-3, walking through the various states it uses to coordinate instruction execution. We will first cover the states related to Instruction Fetch and Decode. To illustrate how the LC-3 controls the processor in the other stages, we will follow the flow of a few example instructions (ADD, LDR, and BR).

By the end of this module you will be able to:

- Explain how the control signals of the LC-3 are generated for the Instruction Fetch and Decode stages and how they control the LC-3 datapath.
- For the LC-3 ADD, LDR, and BR instructions, describe how the FSM orchestrates the flow of data throughout the LC-3 datapath.

INTRODUCING LC-3 CONTROL

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