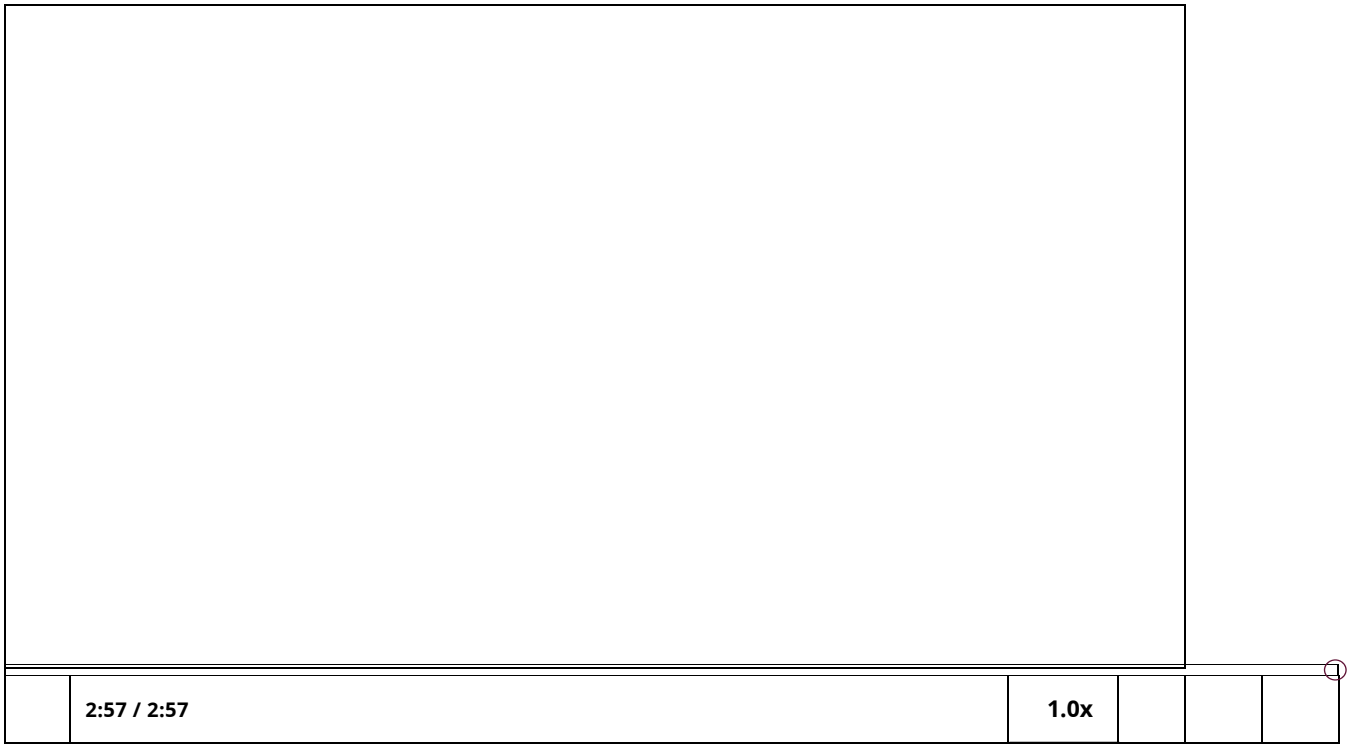
In this module we cover data-level parallelism, which is a form of parallelism that exists when we are performing the same operation on many pieces of data. This type of parallelism is relatively easy to exploit because there are no dependencies between the pieces of data. Processors exploit this via special instructions termed SIMD (single instruction, multiple data) instructions. We'll go into how these instructions work and how a processor pipeline handles them differently than normal instructions.

By the end of this module you will be able to:

- Identify when a loop of instructions has data level parallelism.
- Modify a processor adder to handle SIMD instructions.
- Discuss how a processor exploits instruction-level parallelism (ILP), thread-level parallelism (TLP), and data-level parallelism (DLP) together in order to improve performance.

INTRODUCING DATA LEVEL PARALLELISM



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