edX   **CornellX: ENGRI1210x The Computing Technology Inside Your Smartphone**   🏠 **KarenWest**   ▼

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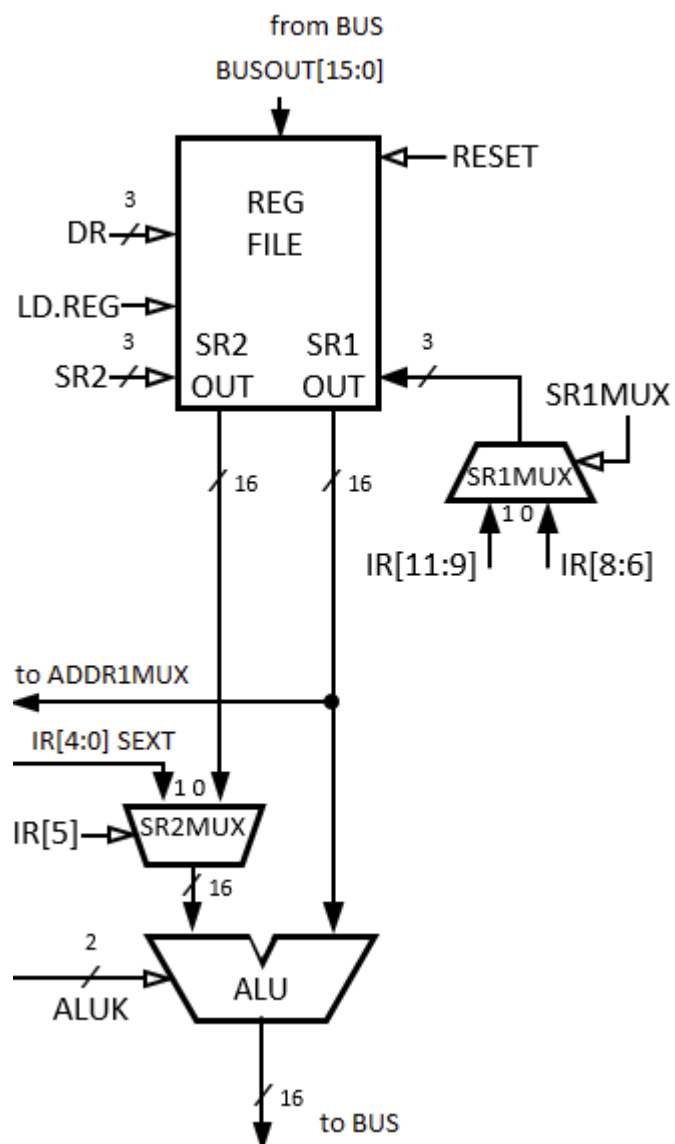
Syllabus   **How to Use Jade**

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Lab 8: Register File and ALU

In this lab, we will combine and test our register file and ALU.

We will be implementing this section of the LC-3 Lite diagram:

from BUS
BUSOUT[15:0]

REG FILE

RESET

3
DR

LD.REG

3
SR2

SR2 OUT   SR1 OUT

3

SR1MUX

SR1MUX
1 0

16   16

IR[11:9]   IR[8:6]

to ADDR1MUX

IR[4:0] SEXT

1 0

IR[5]   SR2MUX

16

2

ALUK   ALU

16
to BUS

Your (or the solution's) register file should be able to be simply dropped in (most of its inputs on the top and left are set up to be in the right places. The ALU can go below the register file, and its input A should receive the output SR1_OUT from the register file (usually needs a horizontal flip to align the terminals). The 2-to-1 muxes are labeled with the correct ports in the
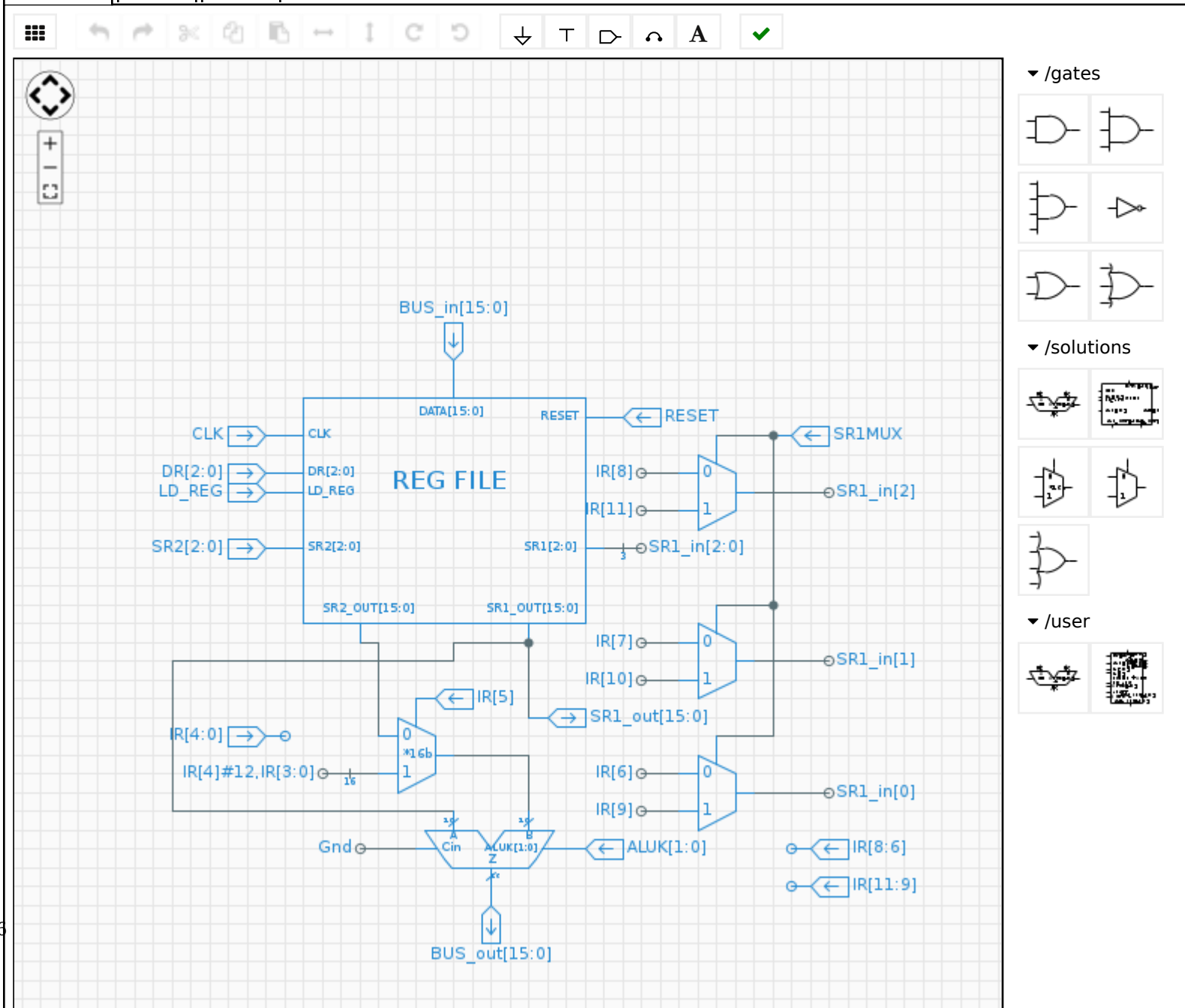
diagram. **Note that the SR1MUX is NOT a 16-bit mux, but rather, a 3-bit mux. You can use 3 copies of the 1-bit mux, and/or use wire names.** You will also have to sign extend the input IR[4:0] to 16 bits.
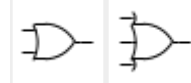
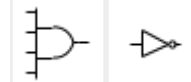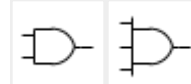**Remember to load your previously built modules!**
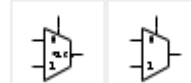
Build, test, and save your design. We're almost there!

LC-3 LITE REGISTER FILE AND ALU (1/1 point)

Module: /user/lc3regalu

SCHEMATIC | ICON ⊘ | TEST ⊘

/gates

/solutions

/user

BUS_in[15:0]

DATA[15:0]   RESET   ← RESET
CLK →   CLK
                                                    ← SR1MUX
DR[2:0] →   DR[2:0]   IR[8]⊙   0
LD_REG →   LD_REG   REG FILE
                                            IR[11]⊙   1   ⊙SR1_in[2]

SR2[2:0] →   SR2[2:0]   SR1[2:0]   ⊙SR1_in[2:0]
                                                    3

SR2_OUT[15:0]   SR1_OUT[15:0]

                                            IR[7]⊙   0
                                            IR[10]⊙   1   ⊙SR1_in[1]

                        ← IR[5]   → SR1_out[15:0]

IR[4:0] →⊙   0
                        *16b
IR[4]#12,IR[3:0]⊙   1
                16   IR[6]⊙   0
                                            IR[9]⊙   1   ⊙SR1_in[0]

                16   16
                A   B
Gnd⊙   Cin   ALUK[1:0]   ← ALUK[1:0]   ⊙← IR[8:6]
                        Z
                        16   ⊙← IR[11:9]

BUS_out[15:0]

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