Microcontrollers within the same family differ by the amount of memory and by the types of I/O modules. All LM3S and TM4C microcontrollers have a Cortex-M processor. There are hundreds of members in this family; some of them are listed in Table 2.11.

Part number	*RAM*	*Flash*	*I/O*	*I/O modules*
LM3S811	8	64	32	PWM
LM3S1968	64	256	52	PWM
LM3S2965	64	256	56	PWM, CAN
LM3S3748	64	128	61	PWM, DMA, USB
LM3S6965	64	256	42	PWM, Ethernet
LM3S8962	64	256	42	PWM, CAN, Ethernet, IEEE1588
LM4F110B2QR	12	32	43	floating point, CAN, DMA
LM4F120H5QR	32	256	43	floating point, CAN, DMA, USB
TM4C123GH6PM	32	256	43	floating point, CAN, DMA, USB, PWM
	KiB	KiB	pins	

Table 2.11. Memory and I/O modules (all have SysTick, RTC, timers, UART, I^2C, SSI, and ADC).

The memory map of TM4C123 is illustrated in Figure 2.18. Although specific for the TM4C123, all ARM®Cortex™-M microcontrollers have similar memory maps. In general, Flash ROM begins at address 0x0000.0000, RAM begins at 0x2000.0000, the peripheral I/O space is from 0x4000.0000 to 0x5FFFF.FFFF, and I/O modules on the private peripheral bus exist from 0xE000.0000 to 0xE00F.FFFF. In particular, the only differences in the memory map for the various 180 members of the LM3S/TM4C family are the ending addresses of the flash and RAM. Having multiple buses means the processor can perform multiple tasks in parallel. The following is some of the tasks that can occur in parallel

ICode bus Fetch opcode from ROM
DCode bus Read constant data from ROM
System bus Read/write data from RAM or I/O, fetch opcode from RAM
PPB Read/write data from internal peripherals like the NVIC
AHB Read/write data from high-speed I/O and parallel ports (M4 only)

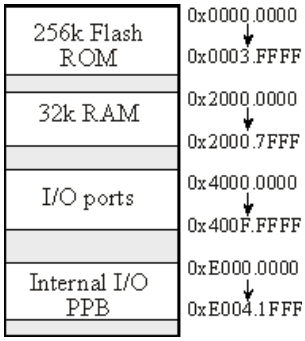

Figure 2.18. Memory map of the TM4C123.