Help

While we're introducing digital circuits, we need digital storage devices, which are essential components used to make registers and memory. The simplest storage device is the **set-reset latch**. One way to build a set-reset latch is shown on the left side of Figure 4.7. If the inputs are *S**=0 and *R**=1, then the *Q* output will be 1. Conversely, if the inputs are *S**=1 and *R**=0, then the *Q* output will be 0. Normally, we leave both the *S** and *R** inputs high. We make the signal *S** go low, then back high to set the latch, making *Q*=1. Conversely, we make the signal *R** go low, then back high to reset the latch, making *Q*=0. If both *S** and *R** are 1, the value on *Q* will be remembered or stored. This latch enters an unpredictable mode when *S** and *R** are simultaneously low.

The **gated D latch** is also shown in Figure 4.7. The front-end circuits take a data input, *D*, and a control signal, *W*, and produce the *S** and *R** commands for the set-reset latch. For example, if *W*=0, then the latch is in its quiescent state, remembering the value on Q that was previously written. However, if *W*=1, then the data input is stored into the latch. In particular, if *D*=1 and *W*=1, then *S**=0 and *R**=1, making *Q*=1. Furthermore, if *D*=0 and *W*=1, then *S**=1 and *R**=0, making *Q*=0. So, to use the gated latch, we first put the data on the *D* input, next we make *W* go high, and then we make *W* go low. This causes the data value to be stored at *Q*. After *W* goes low, the data does not need to exist at the *D* input anymore. If the *D* input changes while *W* is high, then the *Q* output will change correspondingly. However, the last value on the *D* input is remembered or latched when the *W* falls, as shown in Table 4.3.

The **D flip-flop**, shown on the right of Figure 4.7, can also be used to store information. D flip-flops are the basic building block of RAM and registers on the computer. To save information, we first place the digital value we wish to remember on the *D* input, and then give a rising edge to the **clock** input. After the rising edge of the **clock**, the value is available at the *Q* output, and the *D* input is free to change. The operation of the clocked D flip-flop is defined on the right side of Table 4.3. The 74HC374 is an 8-bit D flip-flop, such that all 8 bits are stored on the rising edge of a single clock. The 74HC374 is similar in structure and operation to a register, which is high-speed memory inside the processor. If the gate (*G*) input on the 74HC374 is high, its outputs will be HiZ (floating), and if the gate is low, the outputs will be high or low depending on the stored values on the flip-flop. The D flip-flops are edge-triggered, meaning that changes in the output occur at the rising edge of the input clock.

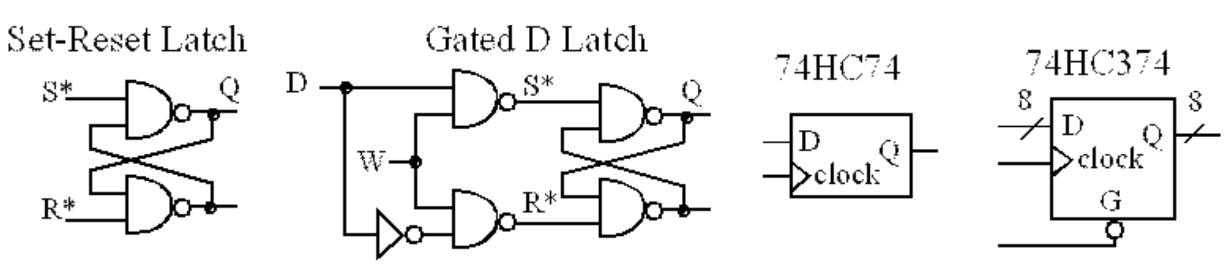

Figure 4.7. Digital storage elements.

D	W	Q		D	clock	Q
0	0	Q_{old}		0	0	Q_{old}

Table 4.3. D flip-flop operation. Q_{old} is the value of the D input at the time of fall of W or rise of clock.