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question on check point 10.1 from PLL video lecture in C10

CHECKPOINT 10.1

How would you change Program 10.1 if your microcontroller had an 8 MHz crystal and you wish to run at 50 MHz?

Here is the answer given to us if we click the button:

Change the specification from 16 MHz to 8 MHz. Change the line
SYSCTL_RCC_R += 0x00000540; // 10101, configure for 16 MHz crystal
to
SYSCTL_RCC_R += 0x00000380; // 01110, configure for 8 MHz crystal
Change the specification from divide by 5 to divide by 8. Change the line
SYSCTL_RCC2_R += (4<<22); // configure for 80 MHz clock
to
SYSCTL_RCC2_R += (7<<22); // configure for 50 MHz clock

```
void PLL_Init(void){
  // 0) Use RCC2
  SYSCTL_RCC2_R |=  0x80000000;  // USERCC2
  // 1) bypass PLL while initializing
  SYSCTL_RCC2_R |=  0x00000800;  // BYPASS2, PLL bypass
  // 2) select the crystal value and oscillator source
  SYSCTL_RCC_R = (SYSCTL_RCC_R &~0x000007C0)   // clear XTAL field, bits 10-6
          + 0x00000540;  // 10101, configure for 16 MHz crystal
  SYSCTL_RCC2_R &= ~0x00000070; // configure for main oscillator source
  // 3) activate PLL by clearing PWRDN
  SYSCTL_RCC2_R &= ~0x00002000;
  // 4) set the desired system divider
  SYSCTL_RCC2_R |= 0x40000000;   // use 400 MHz PLL
  SYSCTL_RCC2_R = (SYSCTL_RCC2_R&~ 0x1FC00000)  // clear system clock divider
          + (4<<22);      // configure for 80 MHz clock
  // 5) wait for the PLL to lock by polling PLLLRIS
  while((SYSCTL_RIS_R&0x00000040)==0){}; // wait for PLLRIS bit
  // 6) enable use of PLL by clearing BYPASS
  SYSCTL_RCC2_R &= ~0x00000800;
}
```
Program 10.1. Activate the LM4F/TM4C with a 16 MHz crystal to run at 80 MHz (C10_PLL.zip).

Here is my question:
To run at 80 MHz, XTAL = 0x15 or 10101 for a 16 MHz crystal in bits 6-10 of SYSCTL_RCC_R,
and the SYSDIV2 (bits 28-22 in SYSCTL_RCC2_R) = (4<<22 to be in those bit locations),
since 400 MHz / (4 + 1) = 80 MHz (with the 400MHz coming from the VCO output).

So to change to an 8MHz crystal, my question is -- why do the XTAL bits change from: 10101 (0x15)
to 01110 (0x0E) for an 8MHz crystal? The comment in the answer says that we are instead dividing by 8
rather than dividing by 5. How does the XTAL value 01110 divide by 8 for the 8MHz crystal? How does
the XTAL value 10101 divide by 5 for the 16MHz crystal?

It was clear the SYSDIV2 bit value had to be 7, to create a clock of 50 MHz.

Thanks for helping me clear this confusion!

c10

Just now by Karen West

the students' answer, *where students collectively construct a single answer*

Click to start off the wiki answer

followup discussions *for lingering questions and comments*

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