Time is an essential element of an embedded system. In this section we introduce the phase-lock-loop (PLL) that allows the software to both utilize an accurate crystal and to select how fast the computer executes.

You have probably already noticed, but in most of the Lab projects the TExaS grader has been activating the PLL so the system runs at 80 MHz. In lab you will not be allowed to modify the PLL because the grader needs to run fast and it needs to know how fast it is running.

VIDEO 10.1. THE PHASE LOCK LOOP (PLL)

Help

C10 1a PLL YouTube

So if I want to operate at low power, maybe I choose a low speed.

If I want to operate at a higher speed, then I'm

going to be draining the battery faster.

So I'm gonna be consuming the power faster.

So by appropriately choosing that operating point,

you can run the system in the most efficient way.

9:34 / 9:34 | 1.0x

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