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9-PPS&&NMEA#1AB
10-USB2.0_1&&2#1-HUB
11-NC
12-MIPI-CSI CON1
13-CODEC CON
14-EEPROM-1A
15-EEPROM-1B
16-RGMII TO 3V3 LEVEL-1A
17-NC
18-3.3V&&1.8V#1&&2
19-USB2.0_1&&2#1-DEBUG
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36-PLL1A&&1B
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54-ORIN-2B
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57-SD&&UFS#4
58-ORIN CANX2&&FAN#4
59-RGMII TO3V3 LEVEL-2B
60-NC
61-NC
62-NC
63-NC
64-XFI3 MUX-SYSTEM
65-XFI2 MUX-GATEWAY
66-NC
67-MCU-BAKA CON
68-IMU CON
69-CAN CONNECTOR
70-MCU-1
71-TJA1101B-1
72-88Q2112-100T1-1
73-MCU#1_CANX6
74-FT4232HL&&USB MUX-1
75-NC
76-MCU-2
77-TJA1101B-2
78-88Q2112-100T1-2
79-MCU#2_CANX6
80-FT4232HL&&USB MUX-2
81-88Q2112-100T1-1
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83-DATA BOX CON
84-6113X2 CON-1 SYSTEM
85-DEBUG BOARD CON X2
86-PCIE SW CON
87-6113X2 CON-2-GATEWAY
88-88Q2112-P5-S1
89-88Q2112-P6-S2
90-88Q2112-P7-R1
91-88Q2112-P8-R2
92-88Q2112-P5-S1-2
93-88Q2112-P6-S2-2
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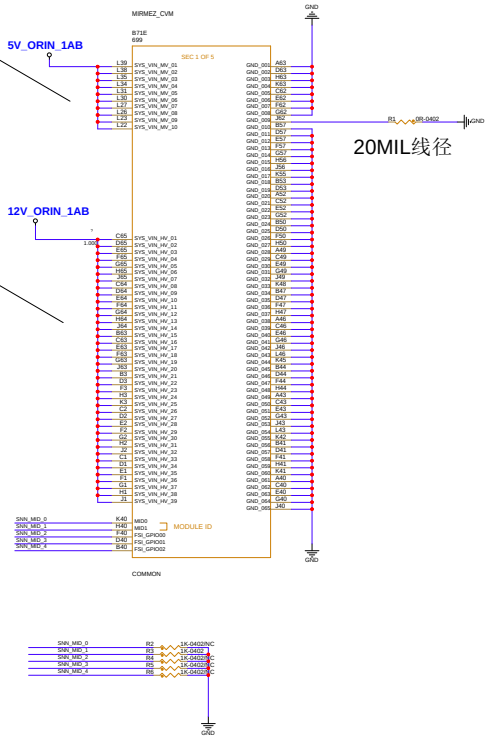
CVM CONNECTOR 1/3

5V-6A

12V-10A



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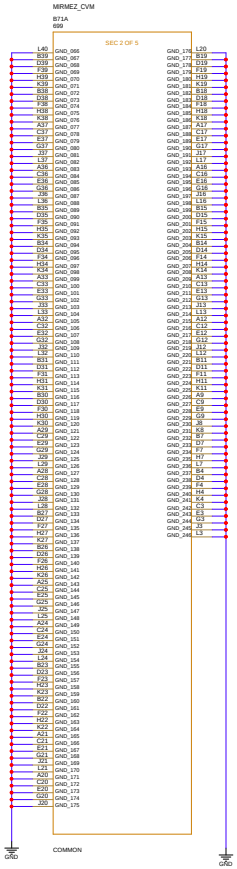
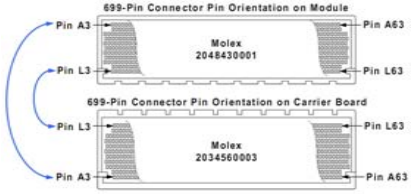
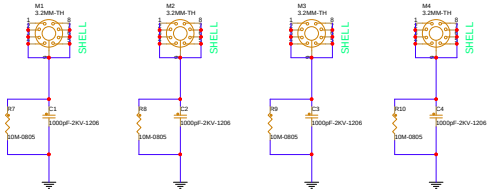
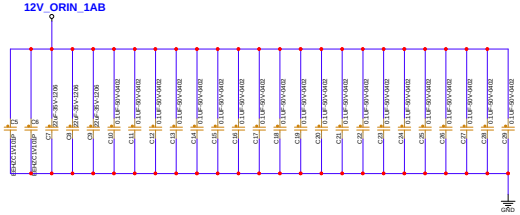


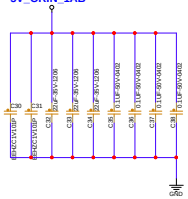
IDDMAX	VIN Imax [SYS_VIN_HV]		5.4	A	Software limited. IDDMAX (HV/MV current) reflects EDPp based on a 6 uS moving window.
	VIN Imax [SYS_VIN_MV]		6.0	A	5.4A is for VIN [20V] on SYS_VIN_HV. 6.0A is for VIN [5V] on SYS_VIN_MV. Actual IDDMAX is dependent on VIN (VINMIN)

Make sure the CVM connector symbol follow the mirrored pin orientation in design guide chapter 3.0.









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CVM CONNECTOR 2/3

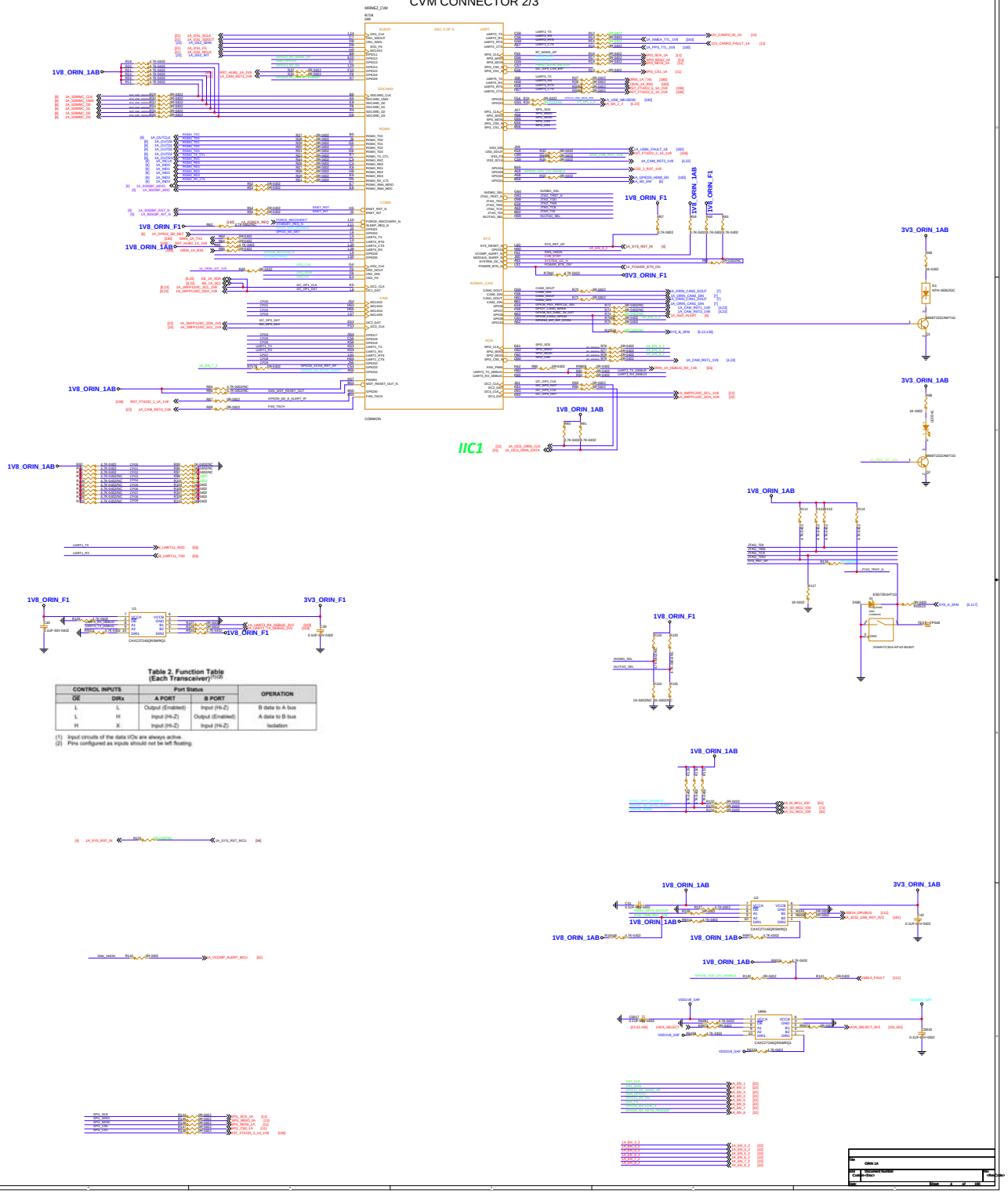
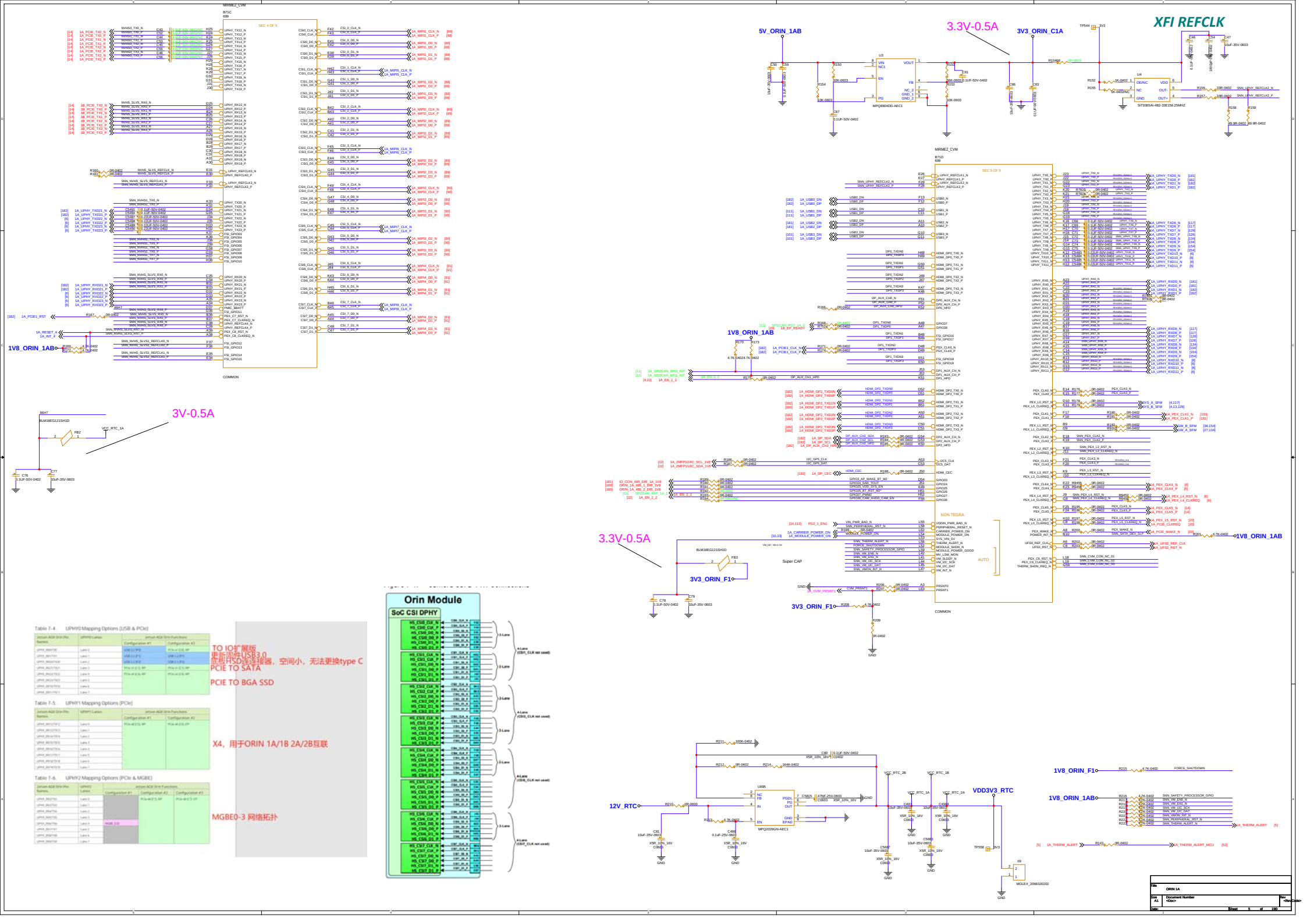


Table 2. Function Table
(Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
OE	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.


XFI REFCLK
5V_ORIN_1AB
3.3V-0.5A
3V3_ORIN_C1A
MIRMEZ_CVM
COMMON
1V8_ORIN_1AB
3V-0.5A
3V3_ORIN_F1
NON TEGRA
Super Cap
12V_RTC
VDD3V3_RTC
Orin Module
SoC CSI DPHY
TO IO扩展版
更新固件让USB3.0
底板HSD连接接器，空间小，无法更换type C
PCIE TO SATA
PCIE TO BGA SSD
X4，用于ORIN 1A/1B 2A/2B互联
MGBE0-3 网络拓扑

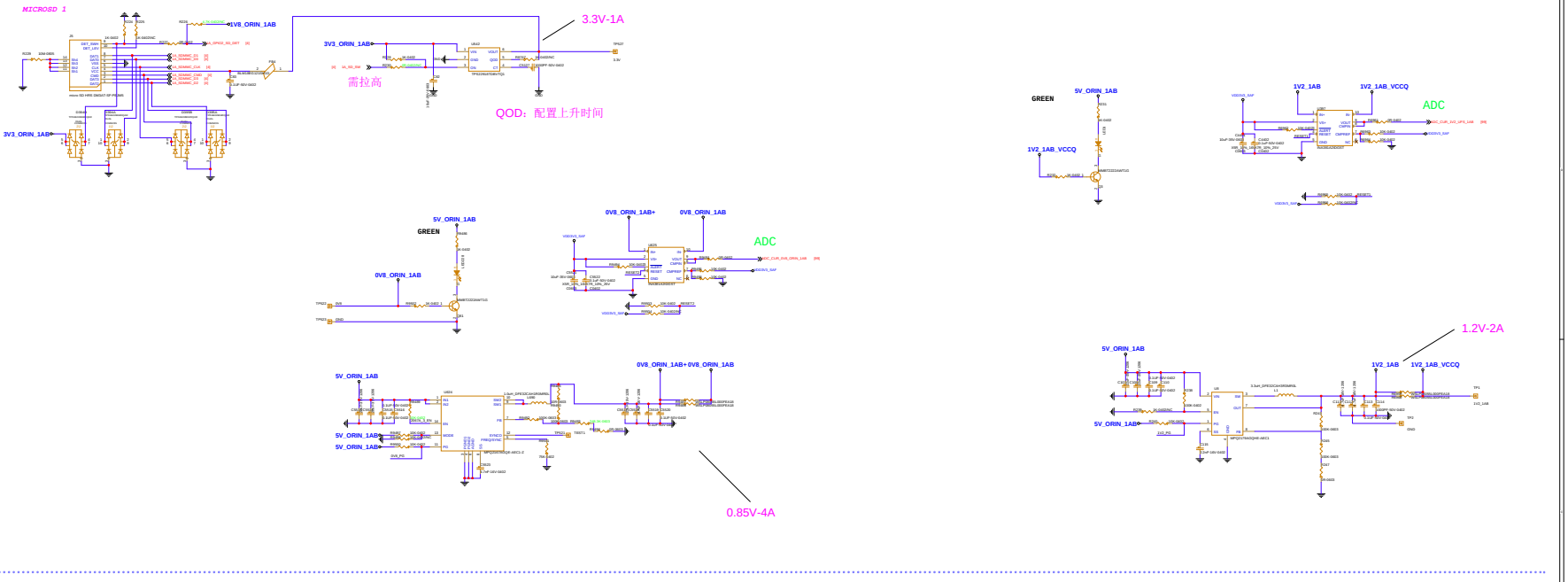
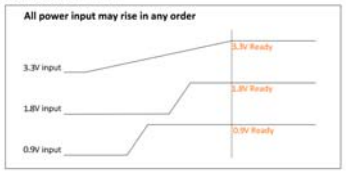
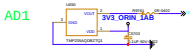
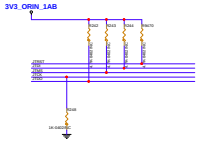


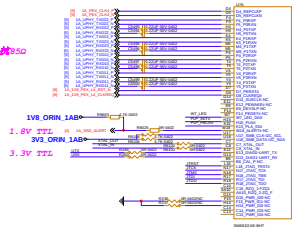
Figure 1: Power-on Sequence Requirements

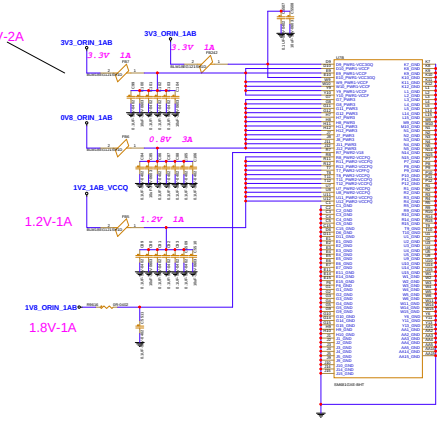


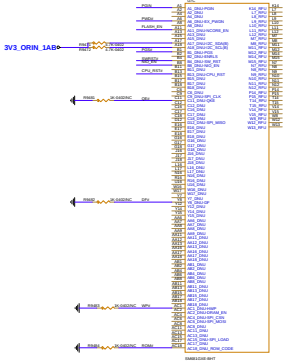
FerriSSD Part #	Max Point A 3.3V current (mA)	Max Point B 1.8V current (mA)	Max Point C 0.9V current (mA)
SM681GXC AG	200	400	1500
SM681GXD AG	300	400	1500
SM681GXE AG	400	500	1500
SM681GXF AG	700	600	1500





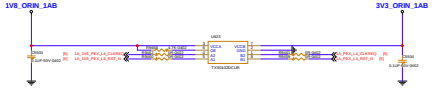


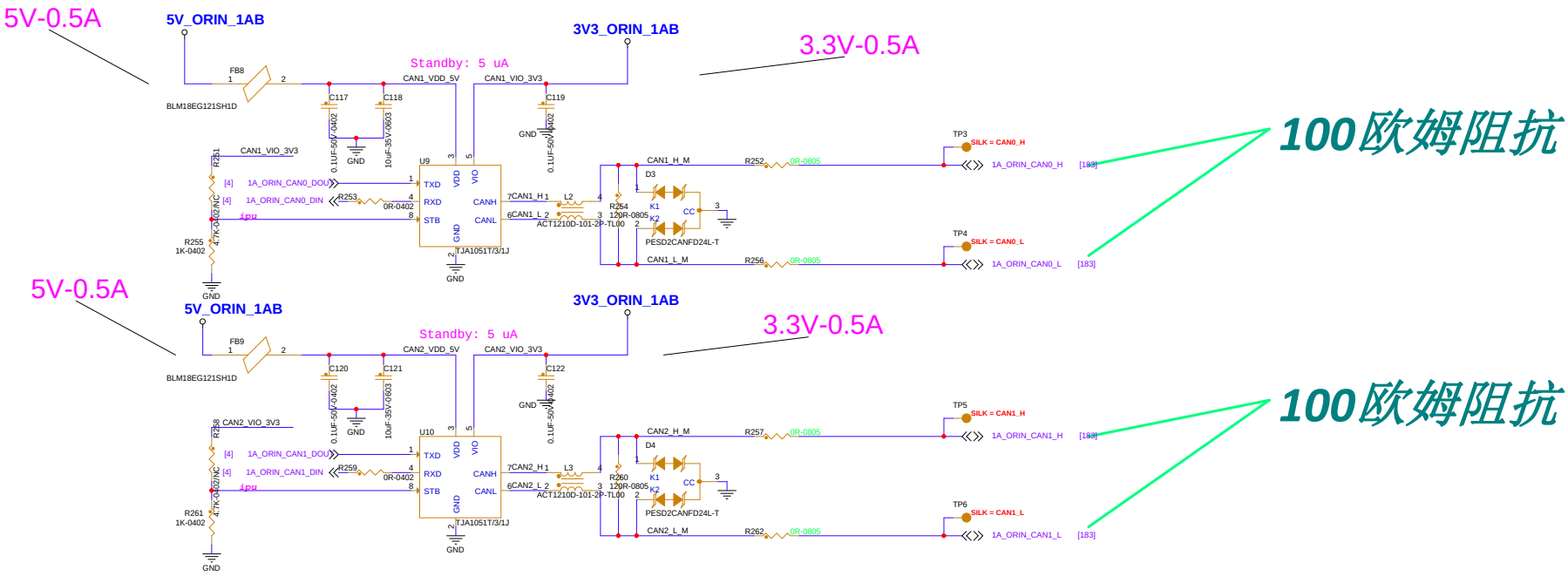




Reserved for PLP电路

异常状态指示灯





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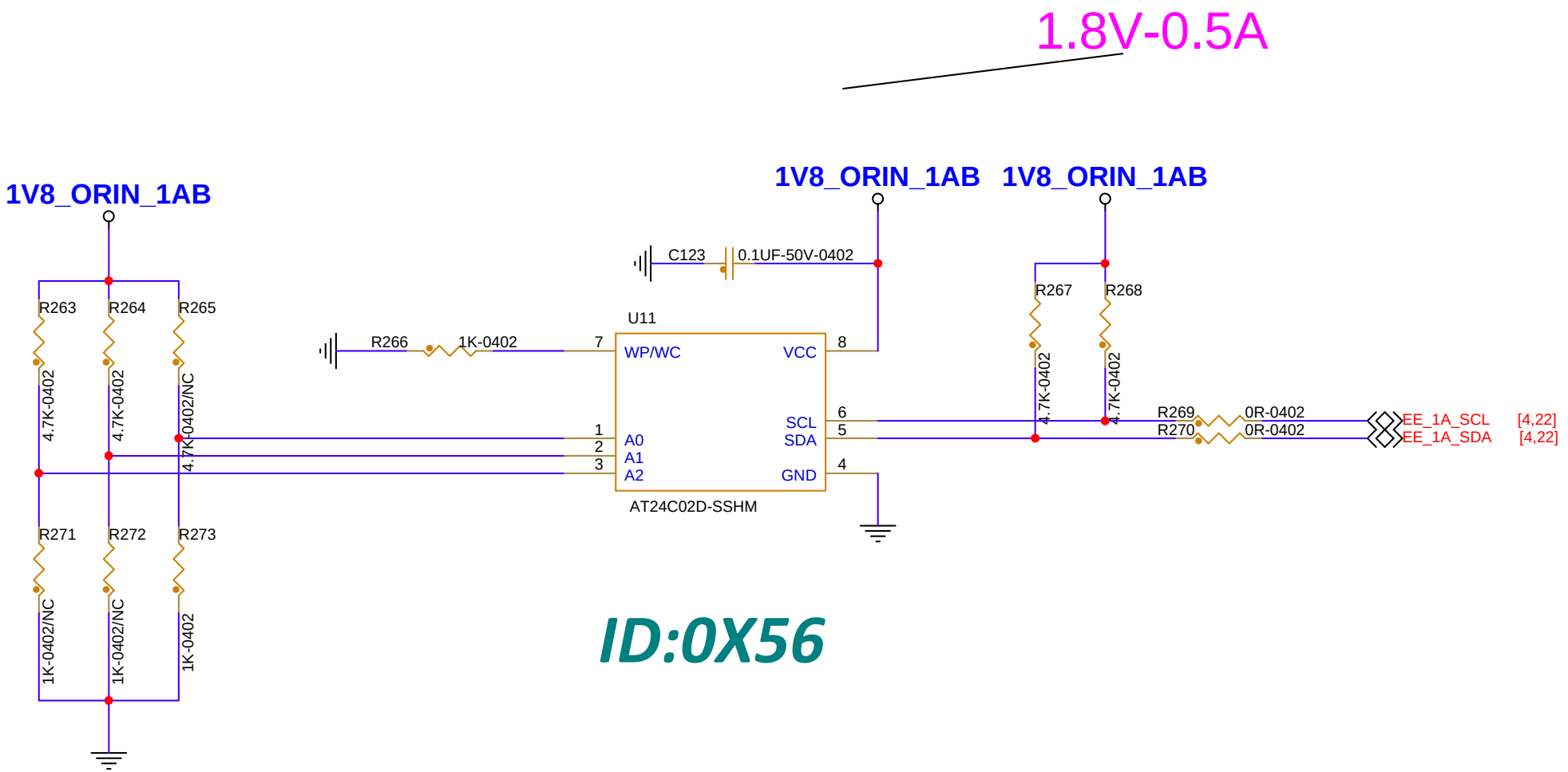

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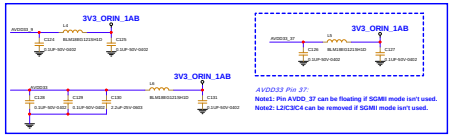
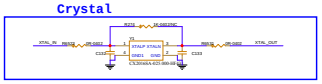
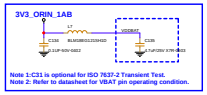
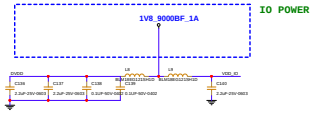
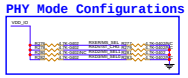
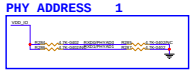


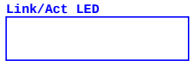


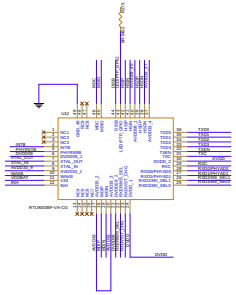






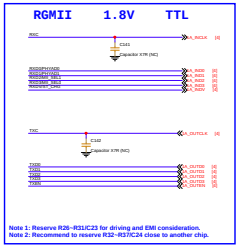


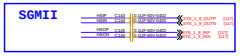


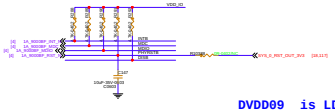


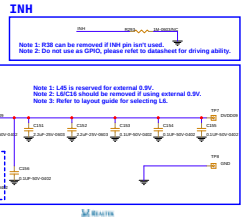
OUT

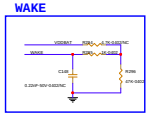
IN











RGMII to SGMII (PHY side@1000Mbps):

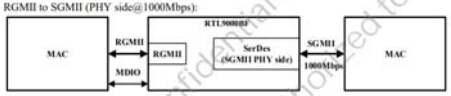


Figure 56 RGMII to SGMII Bridge Mode: PHY side, 1000Mbps.

9.2.55. RG_Config (RG App Configure Register, Page 0xa47, Reg 0x17)

Table 80 RG_Config (RG APP Configure Register, Page 0xa47, Reg 0x17)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	000000000000	Reserved.
3:0	rg_application_cfg	RW	0000	0: xMII (MII/RMII/RGMII) => 100Base-T1. 1: SGMII (PHY side) => 100Base-T1. 2: RGMII to SGMII (PHY side@100Mbps) 3: RGMII to SGMII (PHY side@1000Mbps) 4: RGMII to SGMII (MAC side)

9.2.56. SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

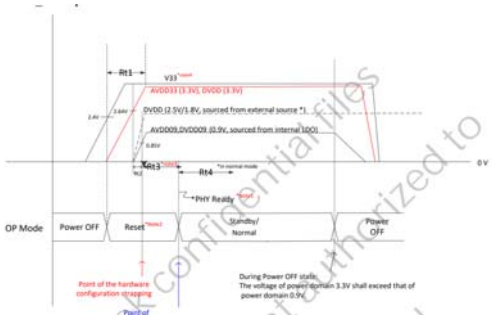
Table 81 SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Bit	Name	Type	Default	Description
15:10	RSVD	RW	011100	Reserved. Used internally; WRITE is not allowed.
9:8	SGMII_mode	RW	00	00: Enable SGMII Auto-Negotiation 01: Enable SGMII Force mode
7:0	RSVD	RW	0x80	Reserved. Used internally; WRITE is not allowed.

9.2.57. SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Table 82 SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Bit	Name	Type	Default	Description
15:1	RSVD	RW	000000000000001	Reserved. Used internally; WRITE is not allowed.
0	SGMII_rst	RW	1	To reset the SGMII, please write this bit to 0 first then write back to 1.



9.2.40. RGTR (RGMII Timing Control Register, Address 0xd082)

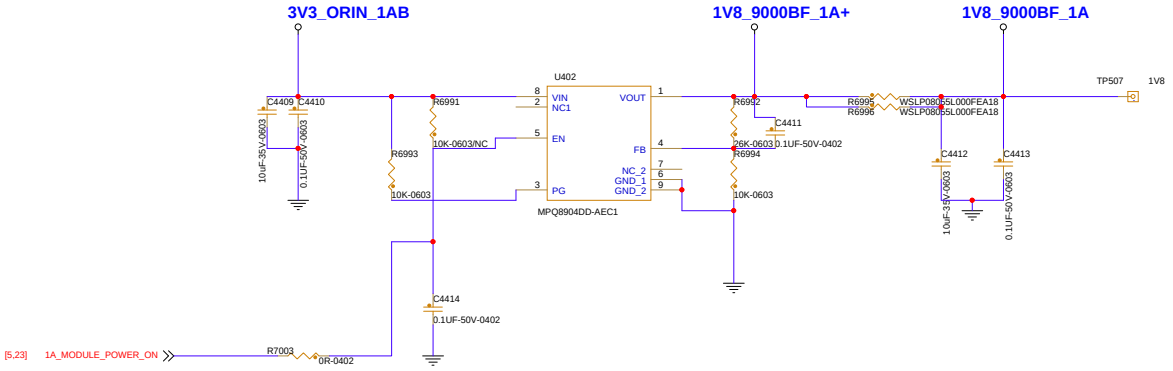
Table 65 RGTR (RGMII Timing Control Register, Address 0xd082)

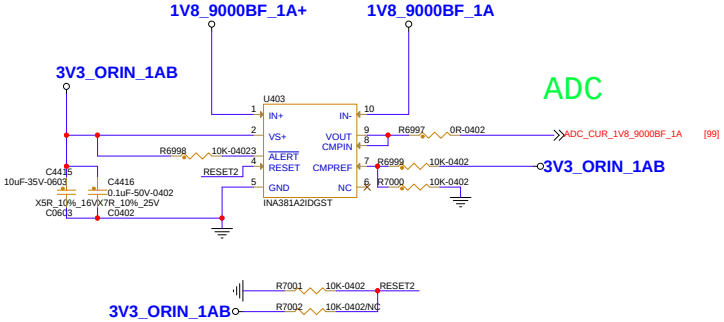
Bit	Name	Type	Default	Description
15	RSVD	RO	0	Reserved.
14	RGMII_Mode	RW	Depends	1: PHY is operating in RGMII mode Decided by hardware configuration, WRITE is not allowed.
13:11	RSVD	RW	000	Reserved. Used internally; WRITE is not allowed.
10	TXC_inv	RW	0	1: Inverse the TXC waveform *Note that if this bit is set to 1, the bit[9:8] RGMII_TXC_timing should be set to 2'b10*
9:8	RGMII_TXC_timing	RW	00	Add the delay for TXC latching TXD; 4ns per level. The timing requirement please refers to section 11.11.5.
7:4	RSVD	RW	0001	Reserved. Used internally; WRITE is not allowed.
3:0	RGMII_RXC_timing	RW	0000	Add the delay for RXC latching RXD, can be set from 0-9, 4ns per level. The timing requirement please refers to section 11.11.5.

*Issue a Software Reset (Reg 0 bit[15] = 1) after the any adjustment above.

DVDD 1.8V

1.8V-0.5A





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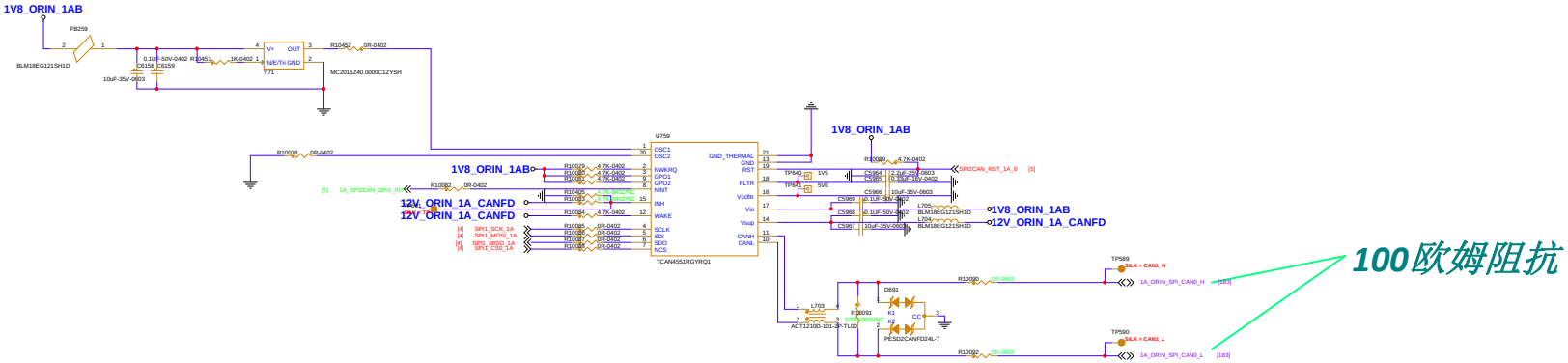

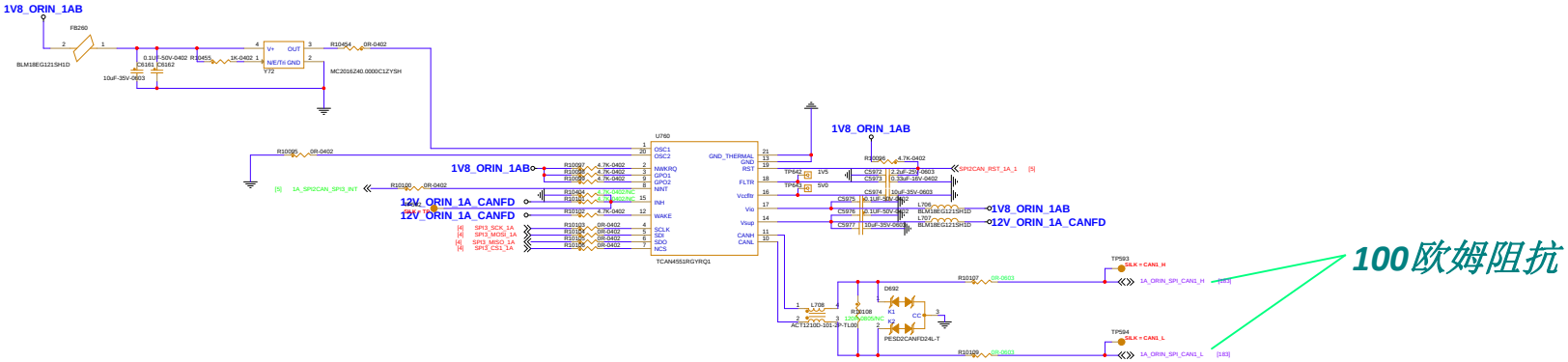

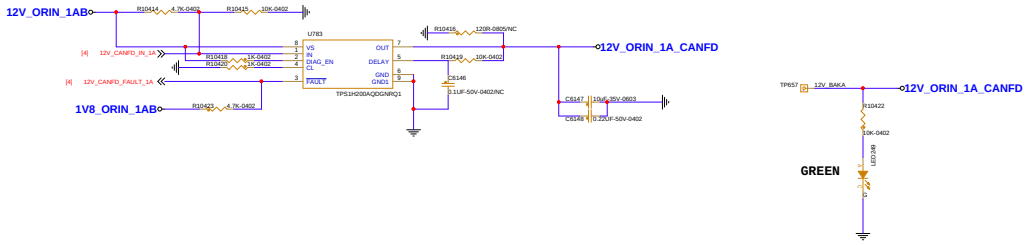

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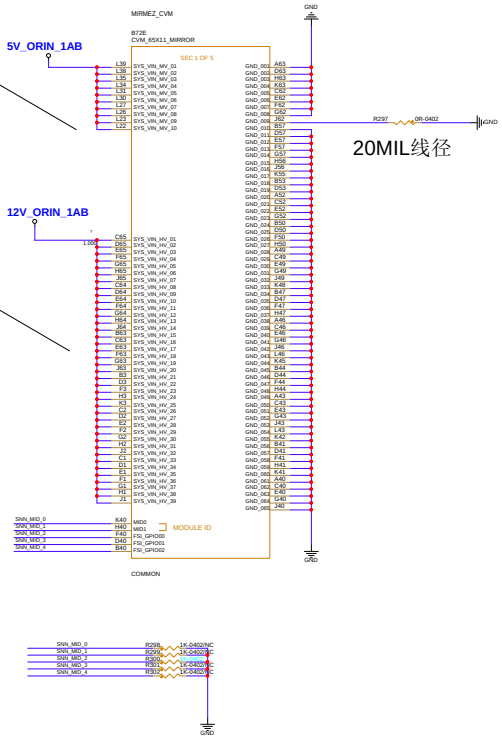
CVM CONNECTOR 1/3

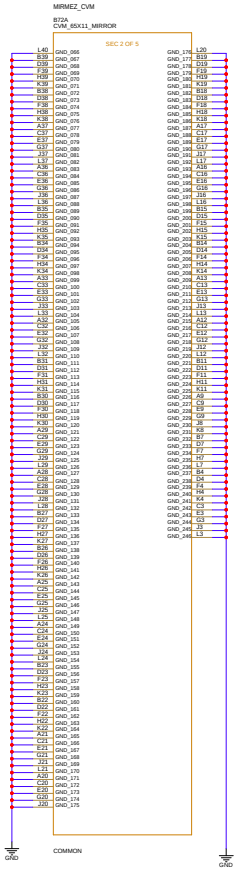
5V-6A

5V_ORIN_1AB

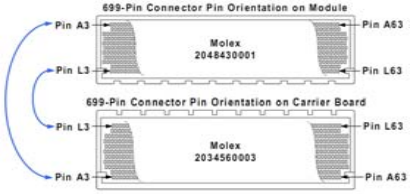
12V-10A

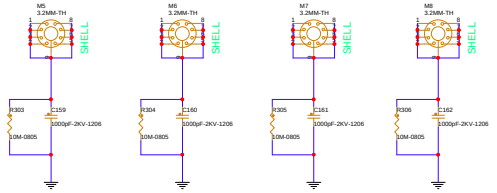
12V_ORIN_1AB

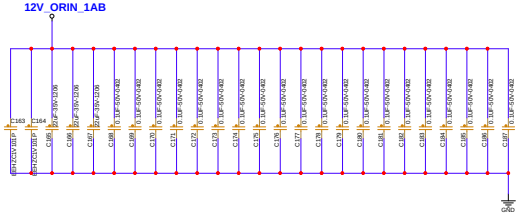


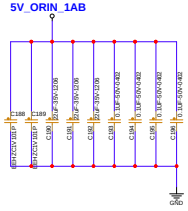


Make sure the CVM connector symbol follow the mirrored pin orientation in design guide chapter 3.0.









Title	ORIN 1B		
Size D	Document Number <Doc>		Rev <RevCode>
Date:		Sheet 12 of 190	

CVM CONNECTOR 2/3

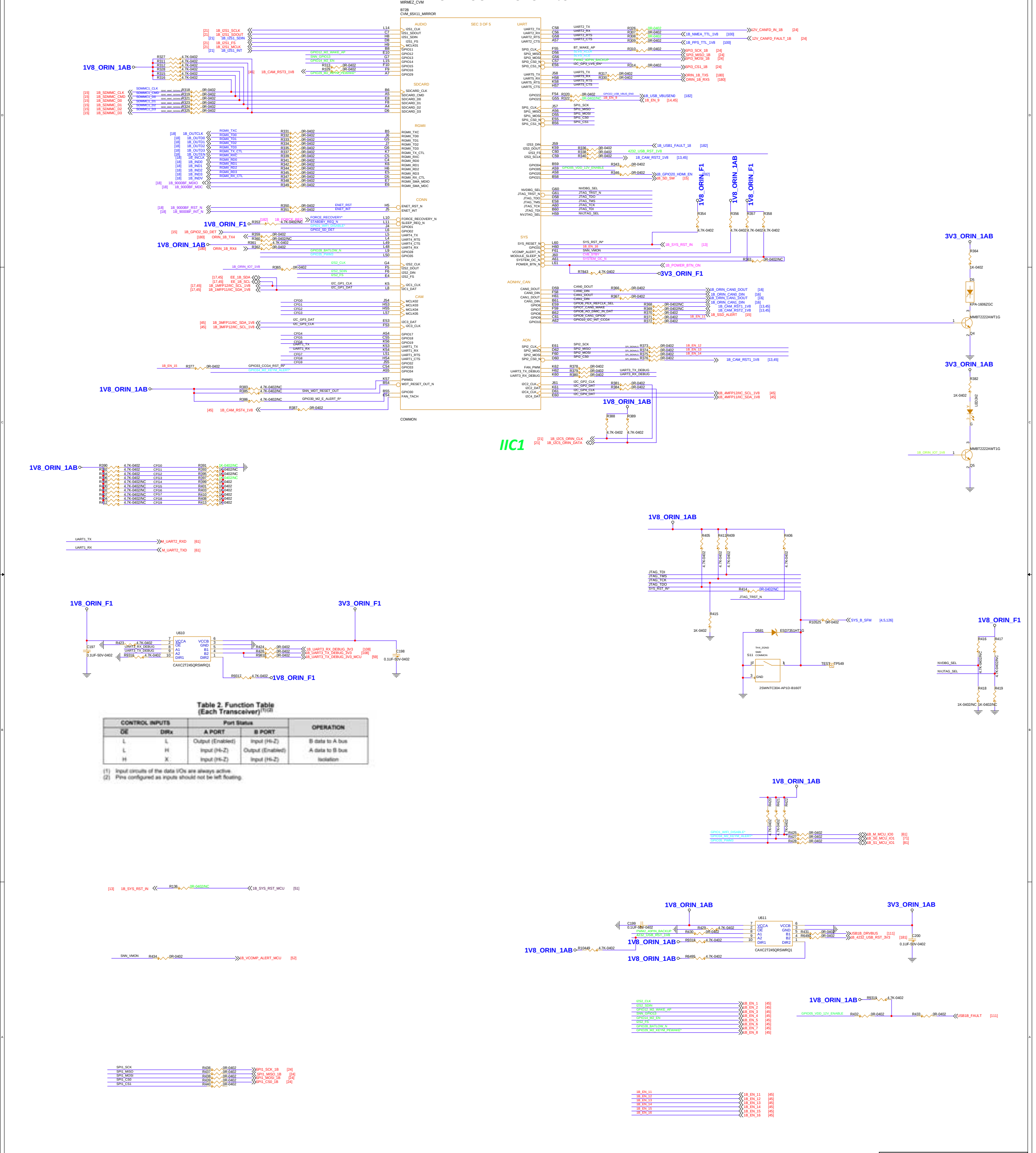
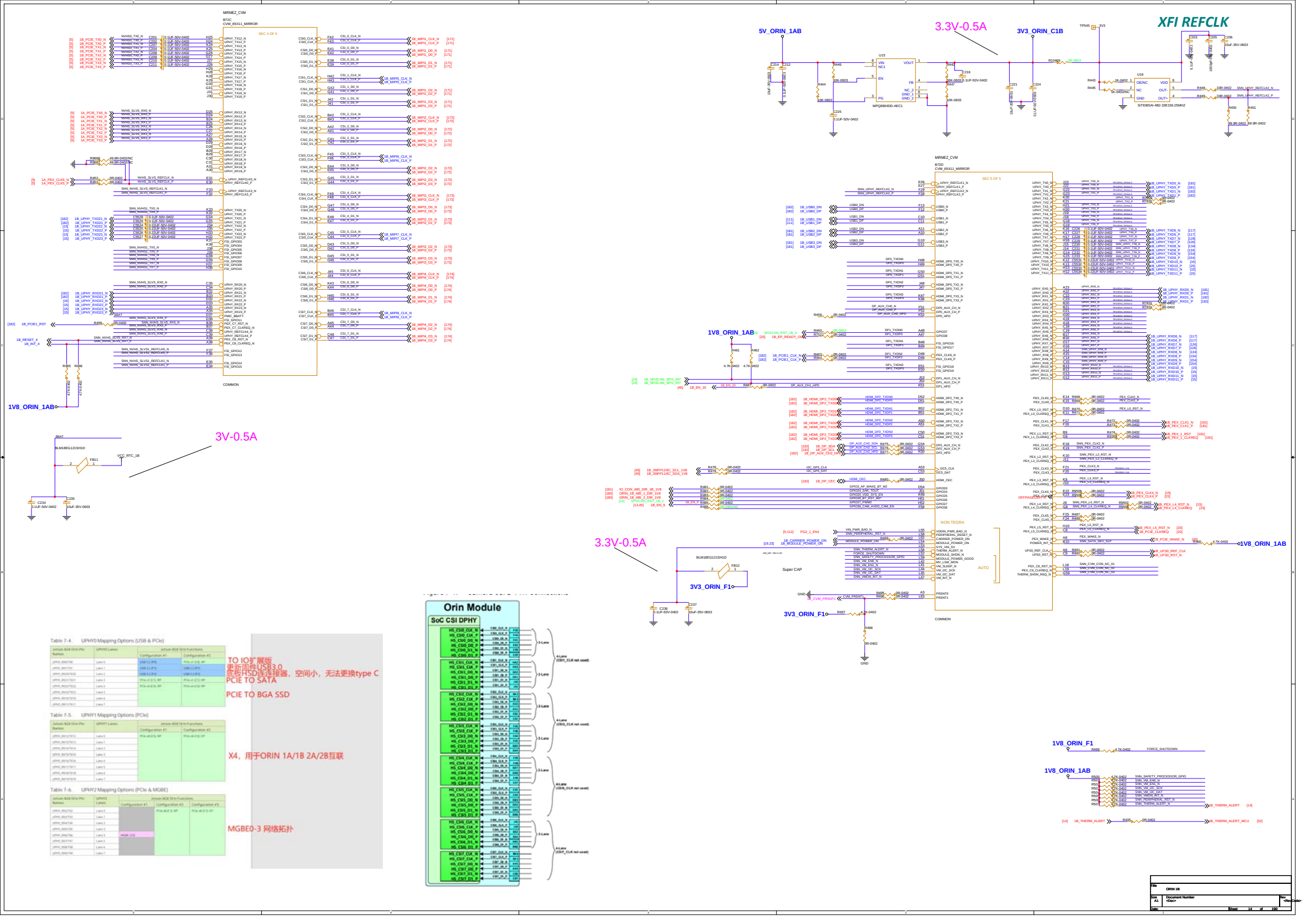


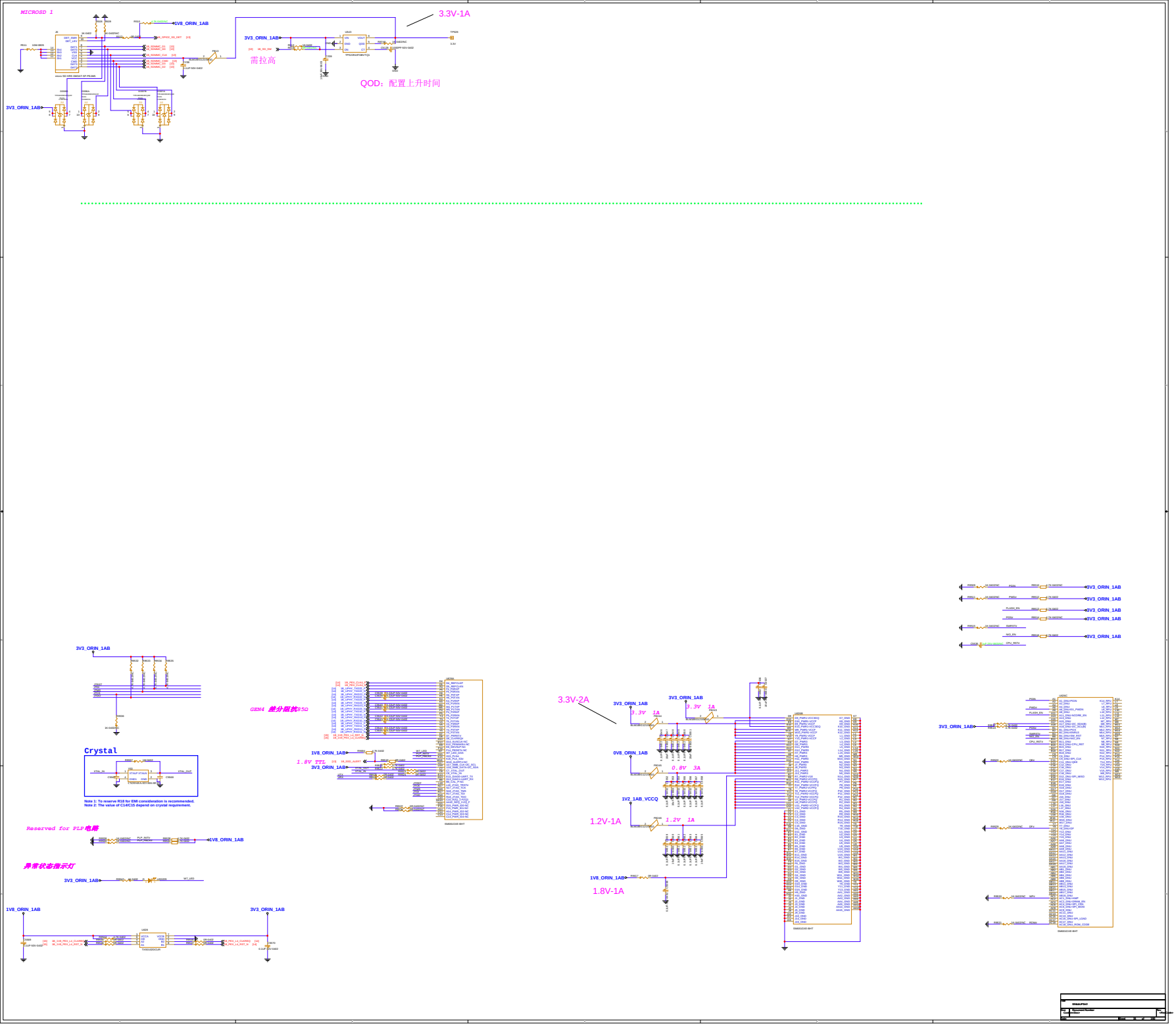
Table 2. Function Table (Each Transceiver)[(1)(2)]

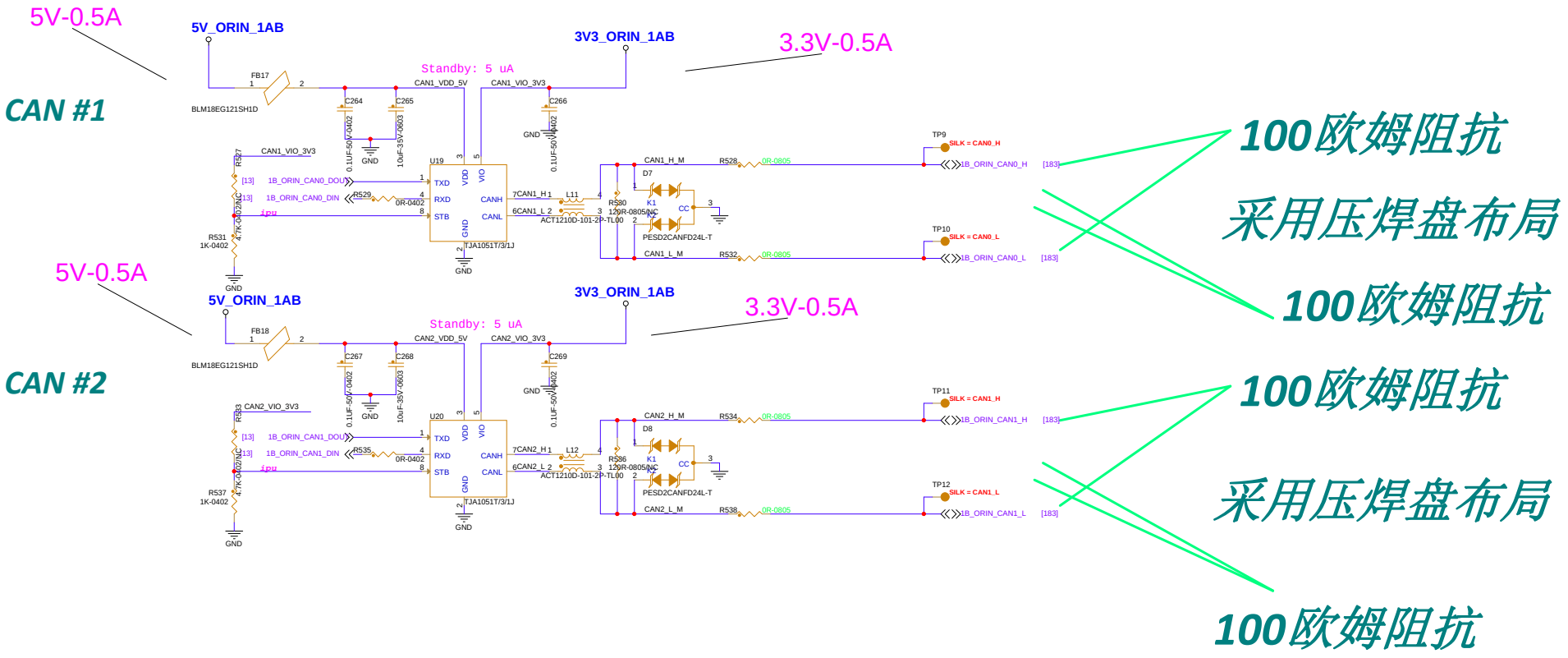
CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

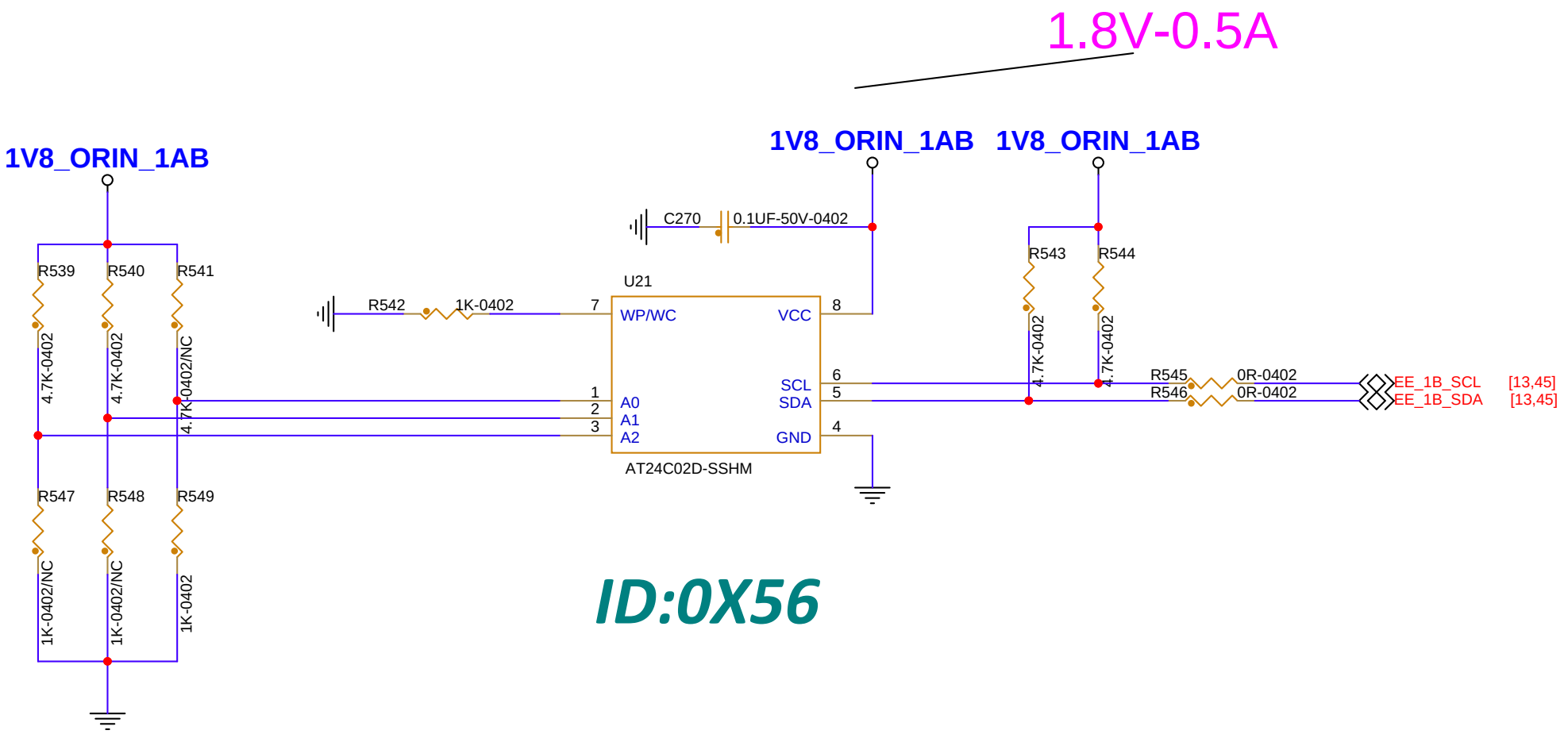
Title: ORIN 1B		
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date:	Sheet 13 of 190	


XFI REFCLK
5V_ORIN_1AB
3.3V-0.5A
3V3_ORIN_C1B
1V8_ORIN_1AB
3V3_ORIN_F1
3V-0.5A
MIRMEZ_CVM
B72C
CVM_65X11_MIRROR
SEC 4 OF 5
SEC 5 OF 5
COMMON
NON TEGRA
Super CAP
AUTO
TO IO扩展板
更新固件USB3.0
底板HSD连接接器，空间小，无法更换type C
PCIE TO SATA
PCIE TO BGA SSD
X4，用于ORIN 1A/1B 2A/2B互联
MGBE0-3 网络拓扑
Orin Module
SoC CSI DPHY
ORIN 1B

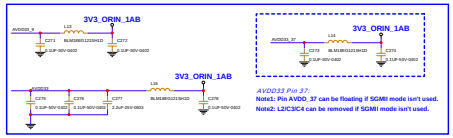

MICROSD 1
1V8_ORIN_1AB
3V3_ORIN_1AB
3.3V-1A
需拉高
QOD：配置上升时间
Crystal
Reserved for PLP电路
异常状态指示灯
GEN4 差分阻抗85Ω
3.3V-2A
1.2V-1A
1.8V-1A
0V8_ORIN_1AB
1V2_1AB_VCCQ
1.8V TTL



Title	ORIN CANX2&&FAN#2	
Size C	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 16 of 190	



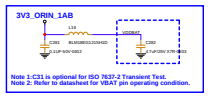
Title: NC		
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date:	Sheet 17 of 190	

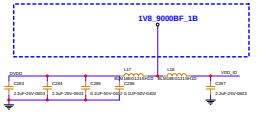


Note1: R1/R2/R3 are used to select different VDD_IO supply source, and it depends on customer requirement.

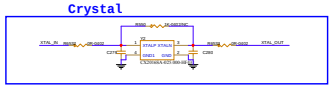
Note2: When using 1.8/2.5V for DVDD, the capacitors can use 6.3V.

Note 3: C31/C22 can be removed if RGMII mode isn't used.





Crystal



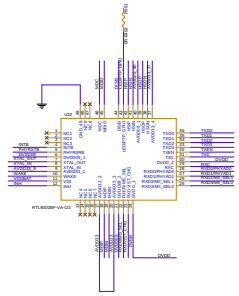
Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

PHY Mode Configurations

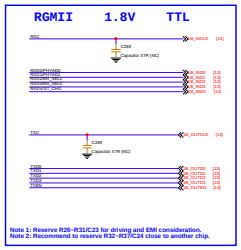
Note 1:
(1) ST_CHG Pull-High (Low) for AUTO (HOST Command) mode.
(2) MS_SEL Pull-High (Low) for Master (Slave) mode.
(3) MII_SEL[1:0]=12 RGMII

PHY ADDRESS 1

Link/Act LED

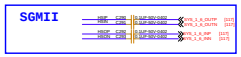


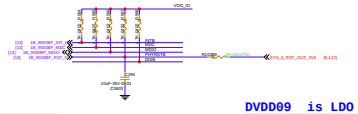
RGMII 1.8V TTL



Note 1: Reserve R26~R31/C23 for driving and EMI consideration.
Note 2: Recommend to reserve R32~R37/C24 close to another chip.

SGMII

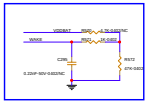




INH

Note 1: R38 can be removed if INH pin isn't used.
Note 2: Do not use as GPIO, please refet to datasheet for driving ability.

WAKE



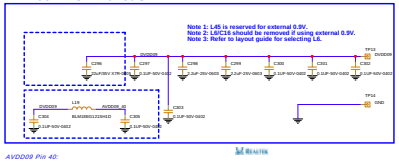
WAKE Pin 10:

Note 1: C34/R52/R53 are used as filter to protect WAKE pin from DPI/Transient noise by OPEN TC12.

Note 2: Default setting of WAKE pin is rising edge active, R54 pull-low resistor should be considered if user can't guarantee proper LOW level on this pin.

Note 3: Refer to datasheet for VIH/VIL level information, and a proper filter may be necessary to avoid any false event on WAKE pin.

DVDD09 is LDO out.



AVDD09 Pin 40:

Note1: Pin AVDD09_40 can be floating if SGMII mode isn't used.

Note2: L7/C18/C19 can be removed if SGMII mode isn't used.

RGMII to SGMII (PHY side@1000Mbps):

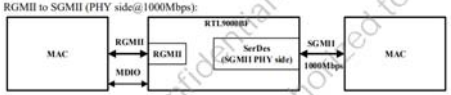


Figure 56 RGMII to SGMII Bridge Mode: PHY side, 1000Mbps.

9.2.55. RG_Config (RG App Configure Register, Page 0xa47, Reg 0x17)

Table 80 RG_Config (RG APP Configure Register, Page 0xa47, Reg 0x17)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	000000000000	Reserved.
3:0	rg_application_cfg	RW	0000	0: xMII (MII/RMII/RGMII) => 100Base-T1. 1: SGMII (PHY side) => 100Base-T1. 2: RGMII to SGMII (PHY side@1000Mbps) 3: RGMII to SGMII (PHY side@1000Mbps) 4: RGMII to SGMII (MAC side)

9.2.56. SGMIICR1 (SGMII Control Register 1, Address 0xce04)

Table 81 SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Bit	Name	Type	Default	Description
15:10	RSVD	RW	011100	Reserved. Used internally; WRITE is not allowed.
9:8	SGMII_mode	RW	00	00: Enable SGMII Auto-Negotiation 01: Enable SGMII Force mode
7:0	RSVD	RW	0x80	Reserved. Used internally; WRITE is not allowed.

9.2.57. SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Table 82 SGMIICR2 (SGMII Control Register 2, Address 0xce00)

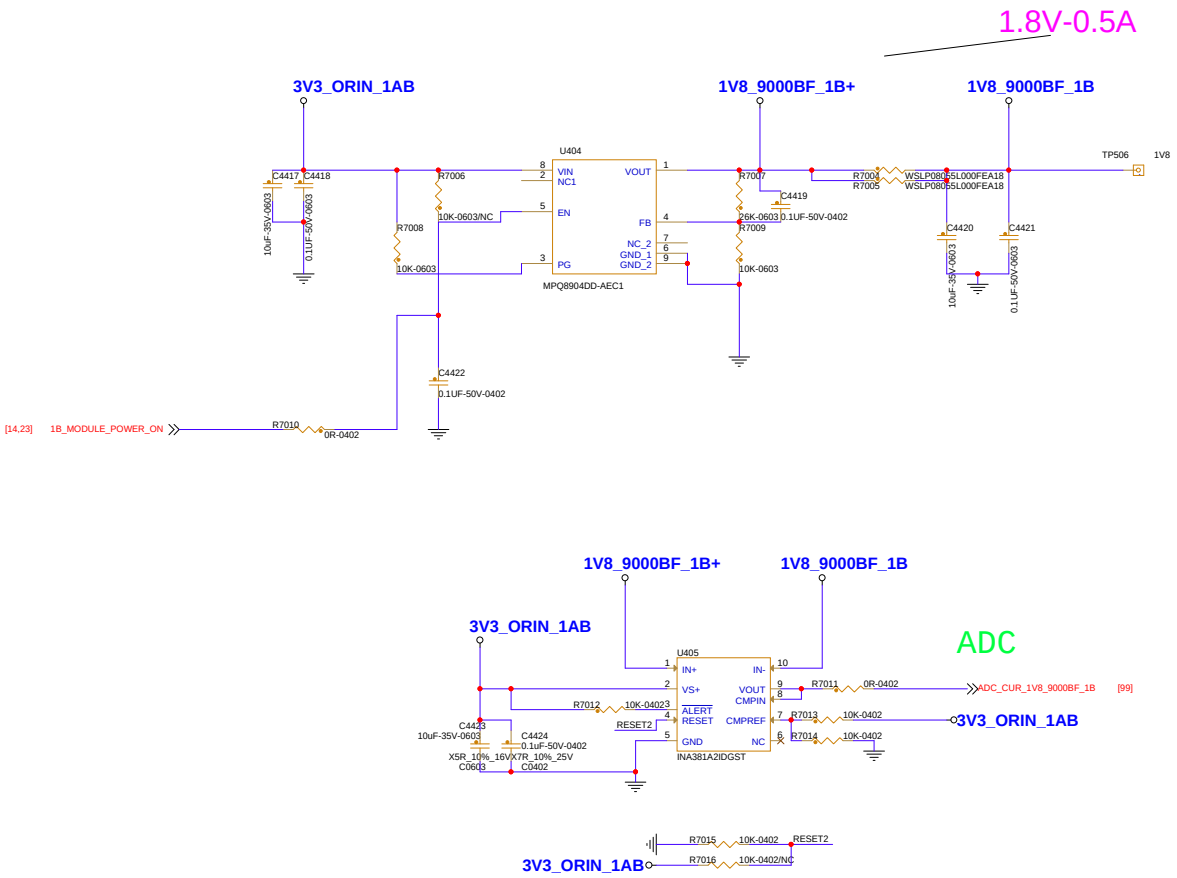
Bit	Name	Type	Default	Description
15:1	RSVD	RW	000000000000001	Reserved. Used internally; WRITE is not allowed.
0	SGMII_rst	RW	1	To reset the SGMII, please write this bit to 0 first then write back to 1.

9.2.40. RGTR (RGMII Timing Control Register, Address 0xd082)

Table 65. RGTR (RGMII Timing Control Register, Address 0xd082)

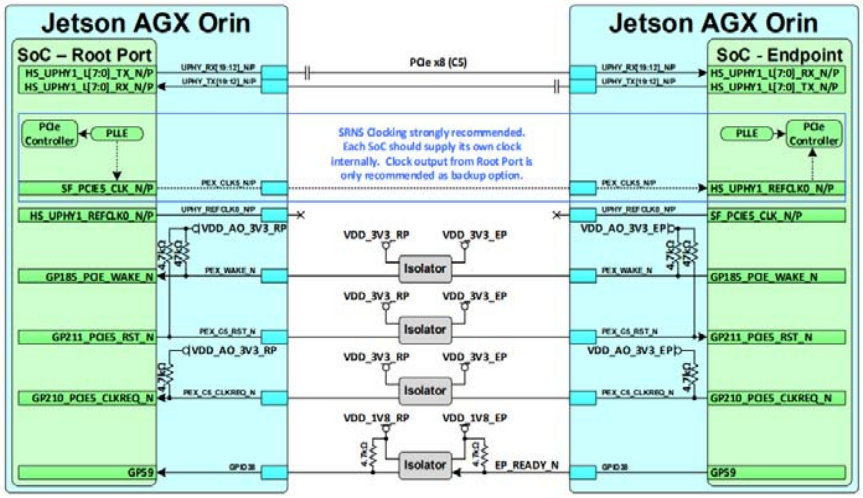
Bit	Name	Type	Default	Description
15	RSVD	RO	* 0	Reserved.
14	RGMII_Mode	RW	Depends	1: PHY is operating in RGMII mode Decided by hardware configuration, WRITE is not allowed.
13:11	RSVD	RW	000	Reserved. Used internally; WRITE is not allowed.
10	TXC_inv*	RW	0	1: Inverse the TXC waveform *Note that if this bit is set to 1, the bit[9:8] RGMII_TXC_timing should be set to 2'b10*
9:8	RGMII_TXC_timing*	RW	00	Add the delay for TXC latching TXD; 4ns per level The timing requirement please refers to section 11.11.5.
7:4	RSVD	RW	0001	Reserved. Used internally; WRITE is not allowed.
3:0	RGMII_RXC_timing*	RW	0000	Add the delay for RXC latching RXD, can be set from 0~9, 4ns per level The timing requirement please refers to section 11.11.5.

*Issue a Software Reset (Reg 0 bit[15] = 1) after the any adjustment above.



Title	NC	
Size C	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 19 of 190	

Figure 6-4. PCIe Jetson AGX Orin RP to Jetson AGX Orin EP connection Example



8.4 器件功能模式

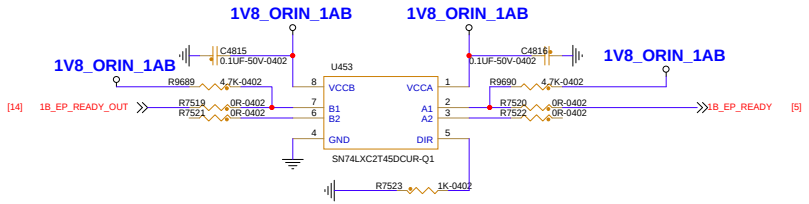
表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

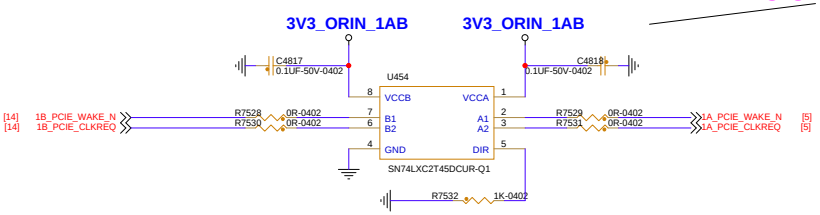
ORIN-1B TO 1A
1A:RC 1B:EP

1.8V-0.5A



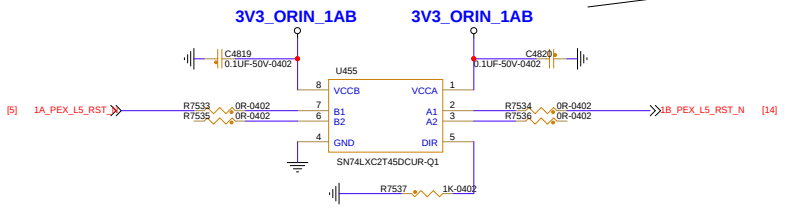
ORIN-1B TO 1A
1A:RC 1B:EP

3.3V-0.5A



ORIN-1A TO 1B
1A:RC 1B:EP

3.3V-0.5A



Title	NC	
Size C	Document Number <Doc>	Rev <RevCode>
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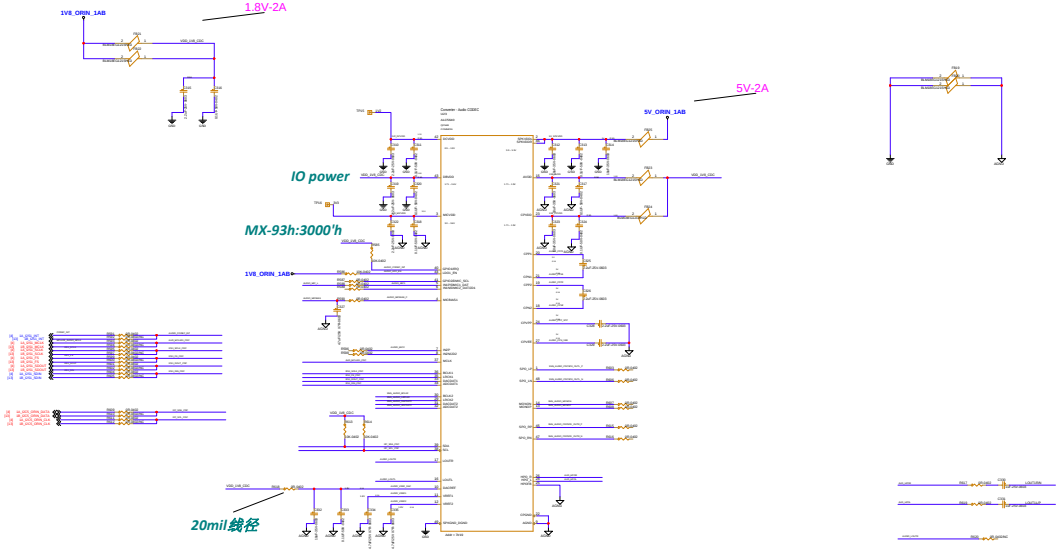
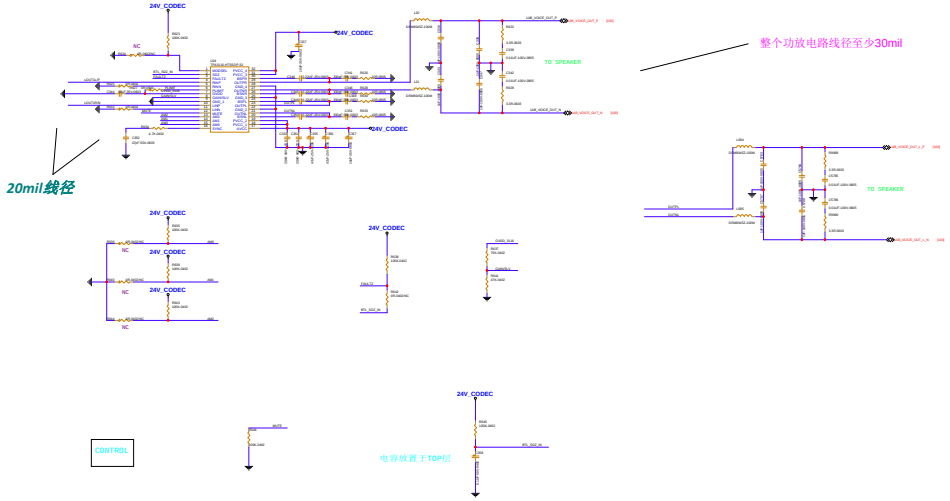
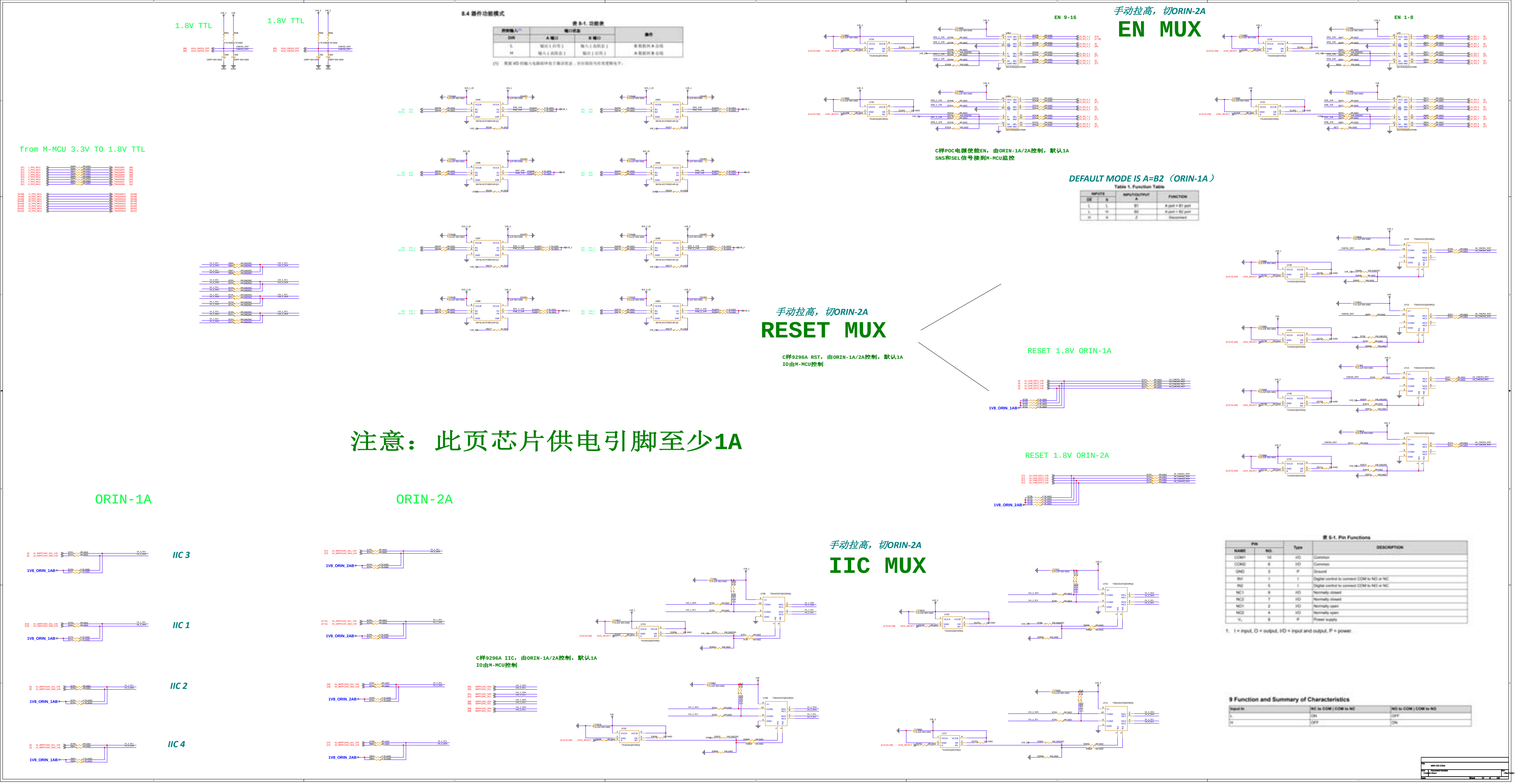
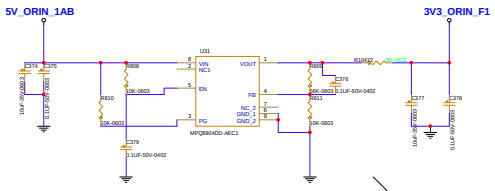


功放改为12V输入

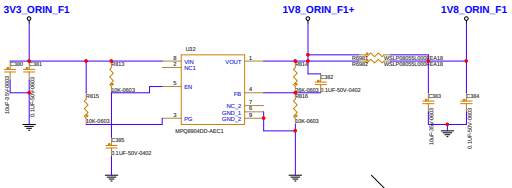


整个功放电路线径至少30mil

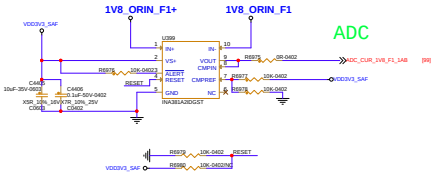

1.8V TTL
1.8V TTL
8.4 器件功能模式
from M-MCU 3.3V TO 1.8V TTL
手动拉高，切ORIN-2A
EN MUX
EN 9-16
EN 1-8
C样POC电源使能EN，由ORIN-1A/2A控制，默认1A
SNS和SEL信号接到M-MCU监控
DEFAULT MODE IS A=B2（ORIN-1A）
Table 1. Function Table
手动拉高，切ORIN-2A
RESET MUX
C样9296A RST，由ORIN-1A/2A控制，默认1A
IO由M-MCU控制
RESET 1.8V ORIN-1A
1V8_ORIN_1AB
RESET 1.8V ORIN-2A
1V8_ORIN_2AB
注意：此页芯片供电引脚至少1A
ORIN-1A
ORIN-2A
IIC 3
IIC 1
IIC 2
IIC 4
1V8_ORIN_1AB
1V8_ORIN_2AB
手动拉高，切ORIN-2A
IIC MUX
C样9296A IIC，由ORIN-1A/2A控制，默认1A
IO由M-MCU控制
表 5-1. Pin Functions
9 Function and Summary of Characteristics



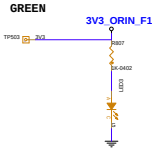
3.3V-0.5A



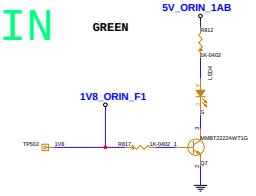
1.8V-0.5A

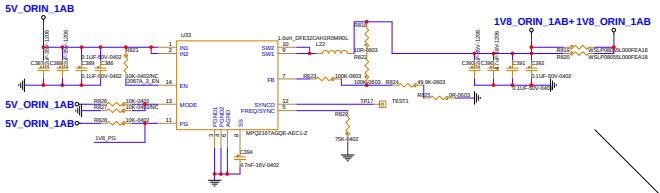


3.3V ORIN



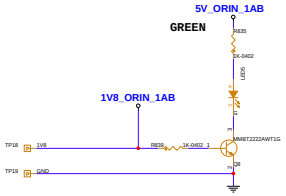
1.8V ORIN

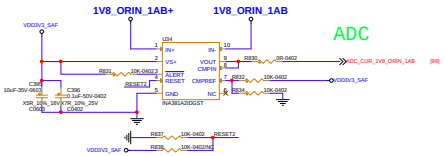


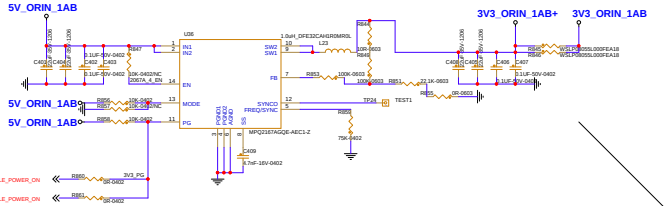


F=2.1MHZ
FCCM MODE

1.8V-4A

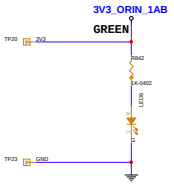


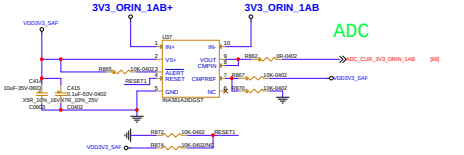




F=2.1MHZ
FCCM MODE

3.3V-4A





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Size	Document Number	Rev
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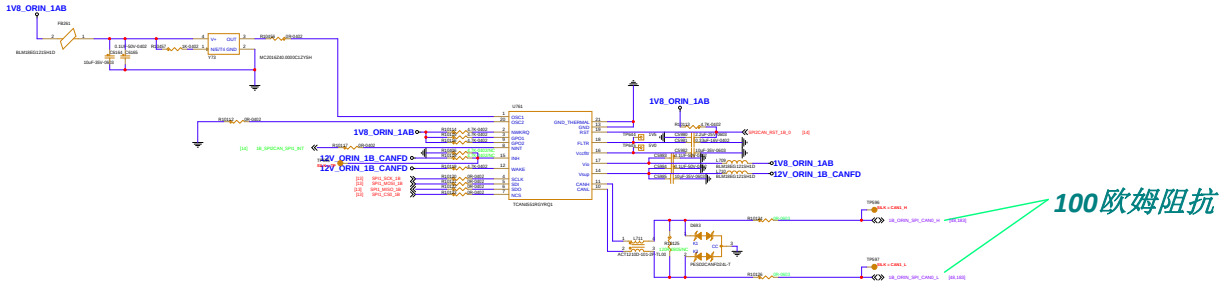
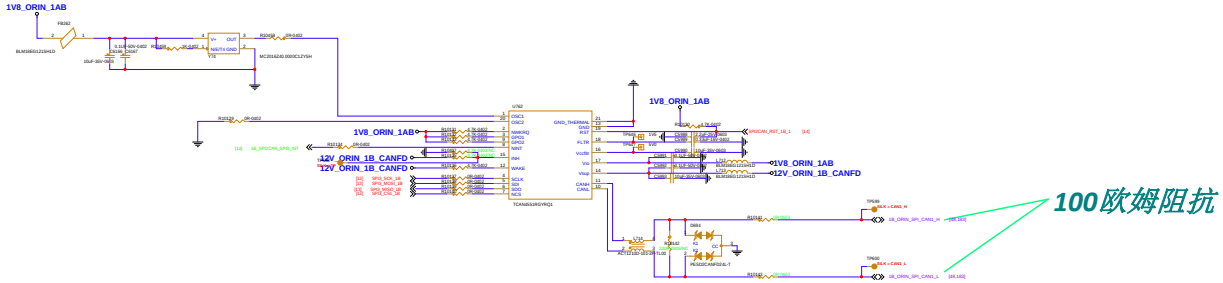
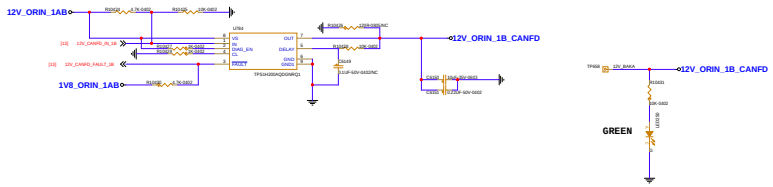

1V8_ORIN_1AB
12V_ORIN_1B_CANFD
100欧姆阻抗


1V8_ORIN_1AB
12V_ORIN_1B_CANFD
100欧姆阻抗


12V_ORIN_1AB
1V8_ORIN_1AB
12V_ORIN_1B_CANFD
GREEN

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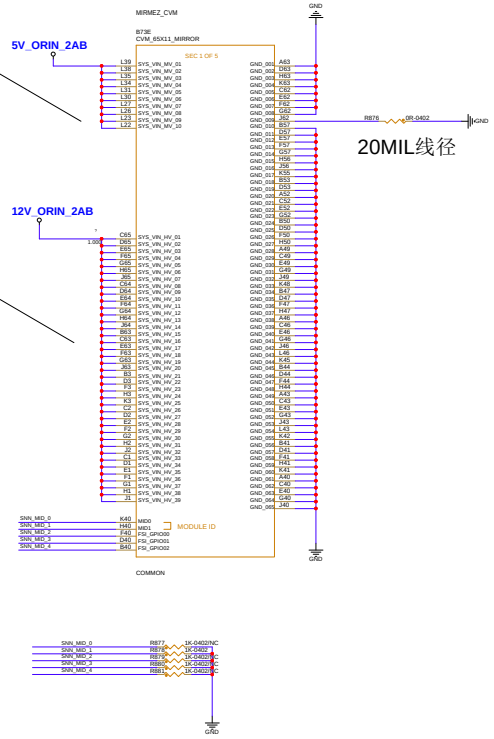
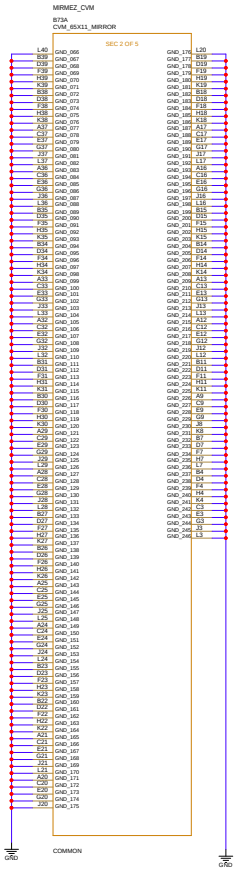
CVM CONNECTOR 1/3

5V-6A

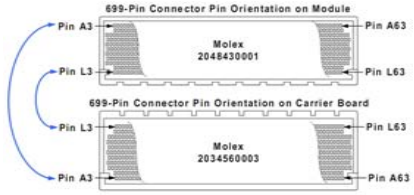
12V-10A

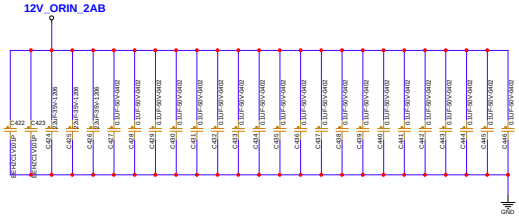


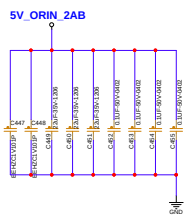
20MIL线径

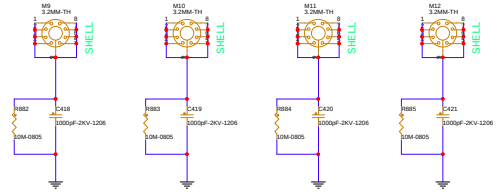


Make sure the CVM connector symbol follow the mirrored pin orientation in design guide chapter 3.0.









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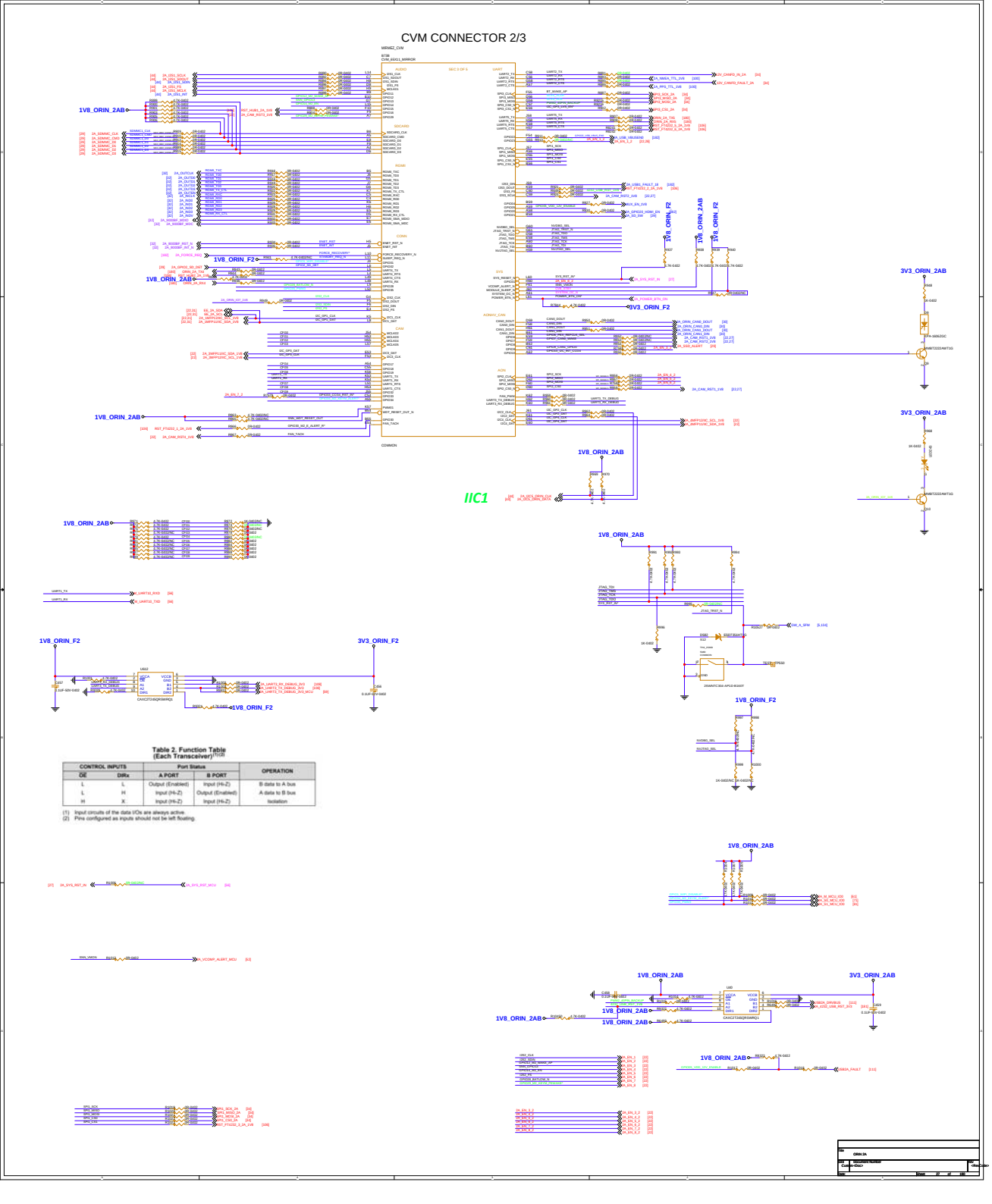
CVM CONNECTOR 2/3



IIC1

Table 2. Function Table
(Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
OE	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

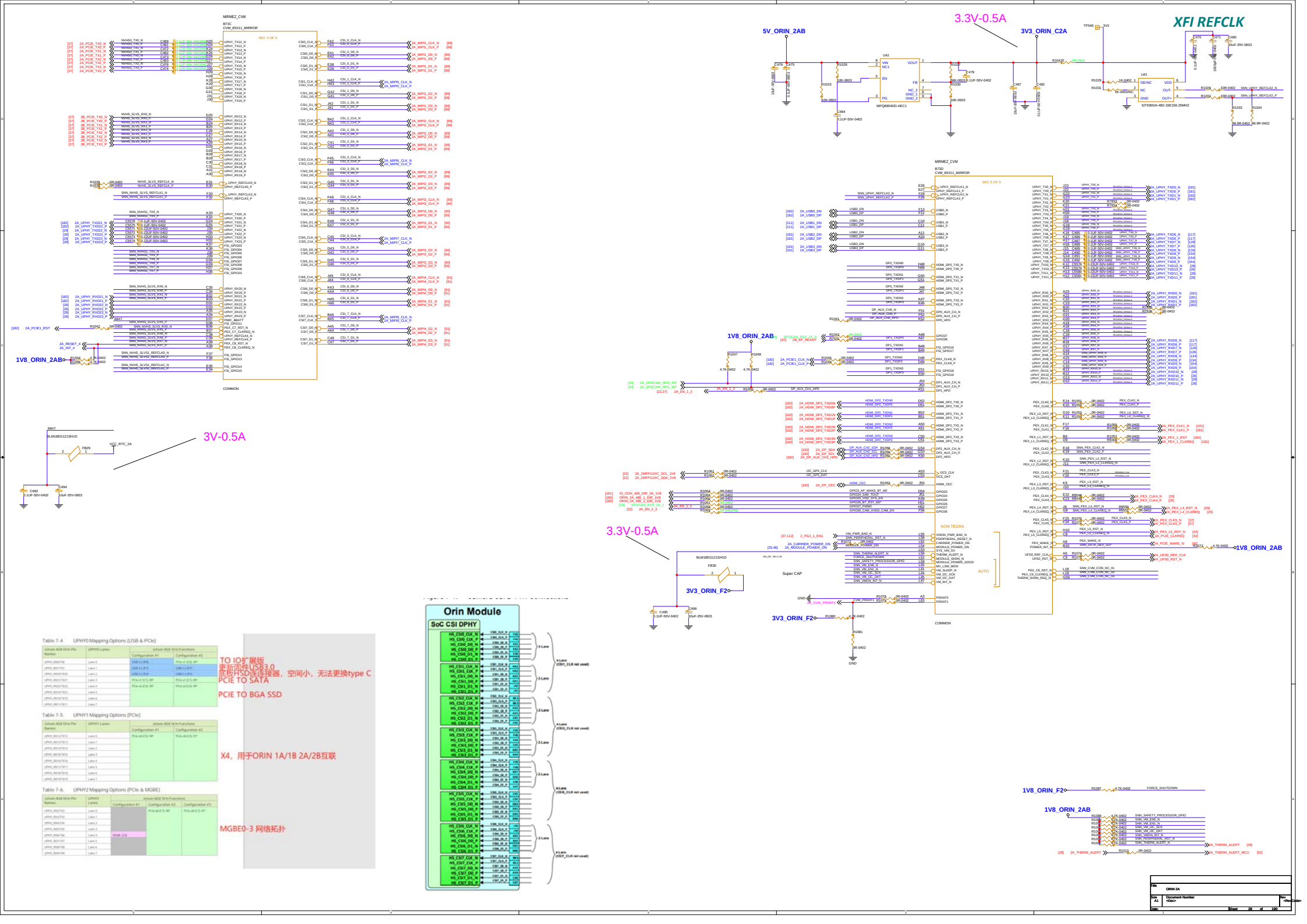


Table 7-4. UPHY0 Mapping Options (USB & PCIe)

Jetson AGX Orin Pin Names	UPHY0 Lanes	Jetson AGX Orin Functions	
		Configuration #1	Configuration #2
UPHY_RX0/TX0	Lane 0	USB 3.2 (P3)	PCIe x1 (C5) MP
UPHY_RX1/TX1	Lane 1	USB 3.2 (P1)	USB 3.2 (P1)
UPHY_RX2/TX2	Lane 2	USB 3.2 (P2)	USB 3.2 (P2)
UPHY_RX3/TX3	Lane 3	PCIe x1 (C1) MP	PCIe x1 (C1) MP
UPHY_RX4/TX4	Lane 4	PCIe x4 (C4) MP	PCIe x4 (C4) MP
UPHY_RX5/TX5	Lane 5		
UPHY_RX6/TX6	Lane 6		
UPHY_RX7/TX7	Lane 7		

Table 7-5. UPHY1 Mapping Options (PCIe)

Jetson AGX Orin Pin Names	UPHY1 Lanes	Jetson AGX Orin Functions	
		Configuration #1	Configuration #2
UPHY_RX0/TX0	Lane 0	PCIe x8 (C5) MP	PCIe x8 (C5) EP
UPHY_RX1/TX1	Lane 1		
UPHY_RX2/TX2	Lane 2		
UPHY_RX3/TX3	Lane 3		
UPHY_RX4/TX4	Lane 4		
UPHY_RX5/TX5	Lane 5		
UPHY_RX6/TX6	Lane 6		
UPHY_RX7/TX7	Lane 7		

Table 7-6. UPHY2 Mapping Options (PCIe & MGBE)

Jetson AGX Orin Pin Names	UPHY2 Lanes	Jetson AGX Orin Functions		
		Configuration #1	Configuration #2	Configuration #3
UPHY_RX0/TX0	Lane 0	PCIe x8 (C7) MP	PCIe x8 (C7) EP	
UPHY_RX1/TX1	Lane 1			
UPHY_RX2/TX2	Lane 2			
UPHY_RX3/TX3	Lane 3			
UPHY_RX4/TX4	Lane 4	MGBE 2.5G		
UPHY_RX5/TX5	Lane 5			
UPHY_RX6/TX6	Lane 6			
UPHY_RX7/TX7	Lane 7			

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MICROSD 1

3V3_ORIN_2AB

1V8_ORIN_2AB

需拉高

3.3V-1A

QOD：配置上升时间

5V_ORIN_2AB

GREEN

1V2_2AB_VCCQ

1V2_2AB

1V2_2AB_VCCQ

ADC

0.85V carrier
3.2A L=0.57UH
C=18UF
F=2.1MHZ
FCCM MODE

0V8_ORIN_2AB

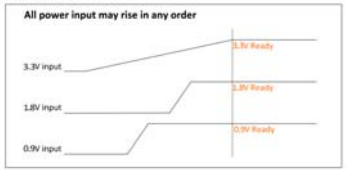
0V8_ORIN_2AB+

F=2.4MHZ
FCCM MODE
2A(2A计算) 1.2V
L=2.64UH C=7.33UF

1.2V-2A

0.85V-4A

Figure 1: Power-on Sequence Requirements



FerriSSD Part #	Max Point A 3.3V current (mA)	Max Point B 1.8V current (mA)	Max Point C 0.9V current (mA)
SM681GXC AG	200	400	1500
SM681GXD AG	300	400	1500
SM681GXE AG	400	500	1500
SM681GXF AG	700	600	1500

3V3_ORIN_2AB

Crystal

Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

Reserved for PLP电路

1V8_ORIN_2AB

异常状态指示灯

3V3_ORIN_2AB

1V8_ORIN_2AB

3V3_ORIN_2AB

GEN4 差分眼放95Ω

1V8_ORIN_2AB
1.8V TTL
3V3_ORIN_2AB
3.3V TTL

3.3V-2A

3V3_ORIN_2AB
3.3V 1A

0V8_ORIN_2AB
0.8V 3A

1V2_2AB_VCCQ
1.2V 1A

1.2V-1A

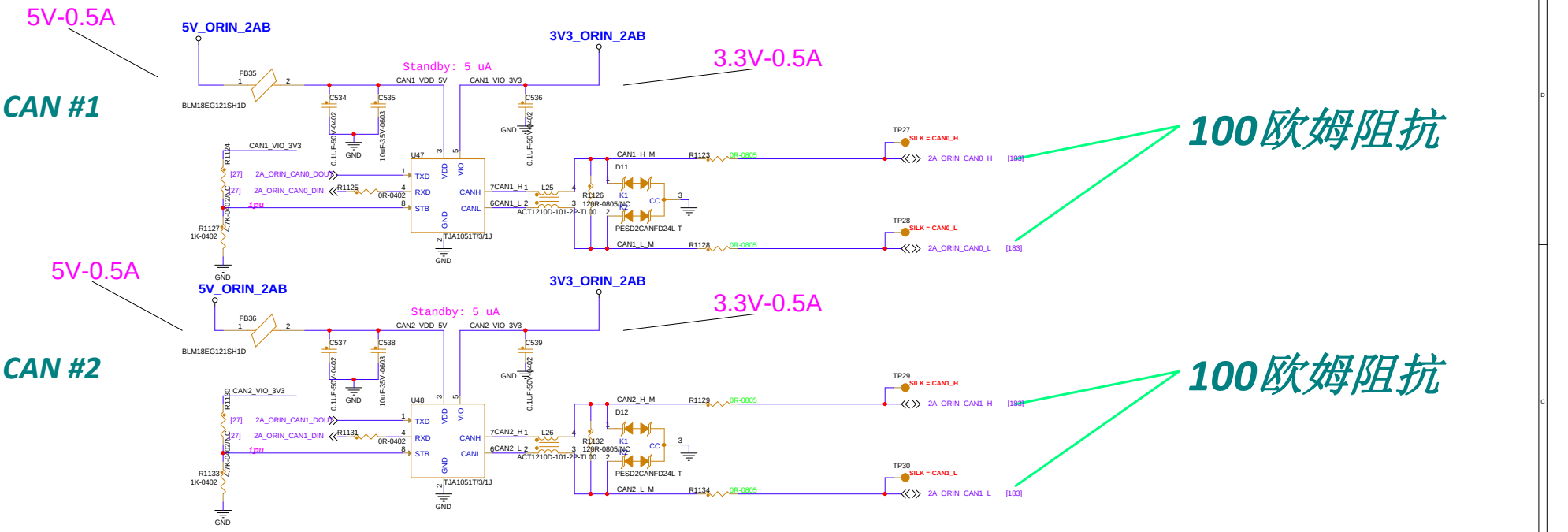
1V8_ORIN_2AB

1.8V-1A

3V3_ORIN_2AB

3V3_ORIN_2AB

3V3_ORIN_2AB



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Size C	Document Number <Doc>	Rev <RevCode>
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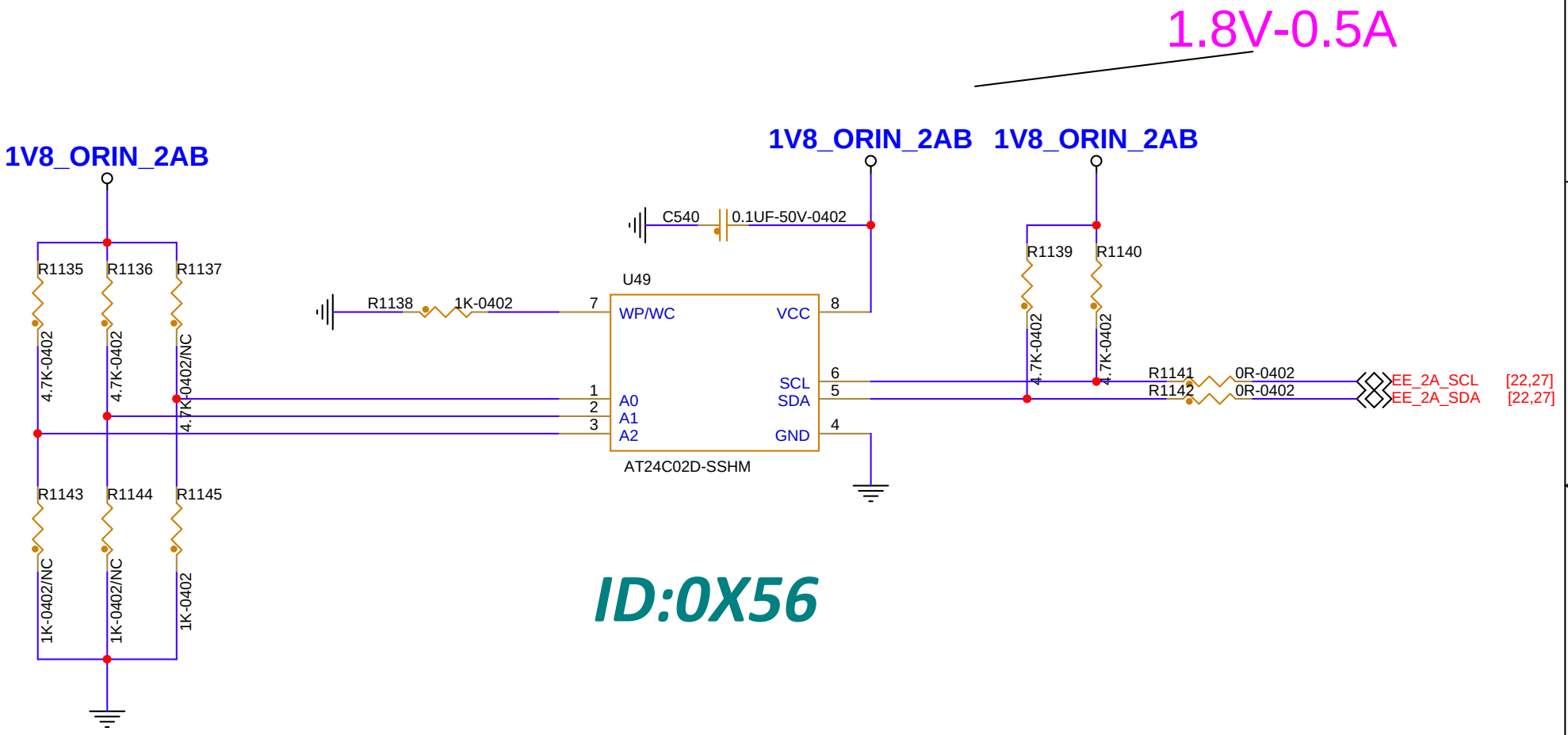

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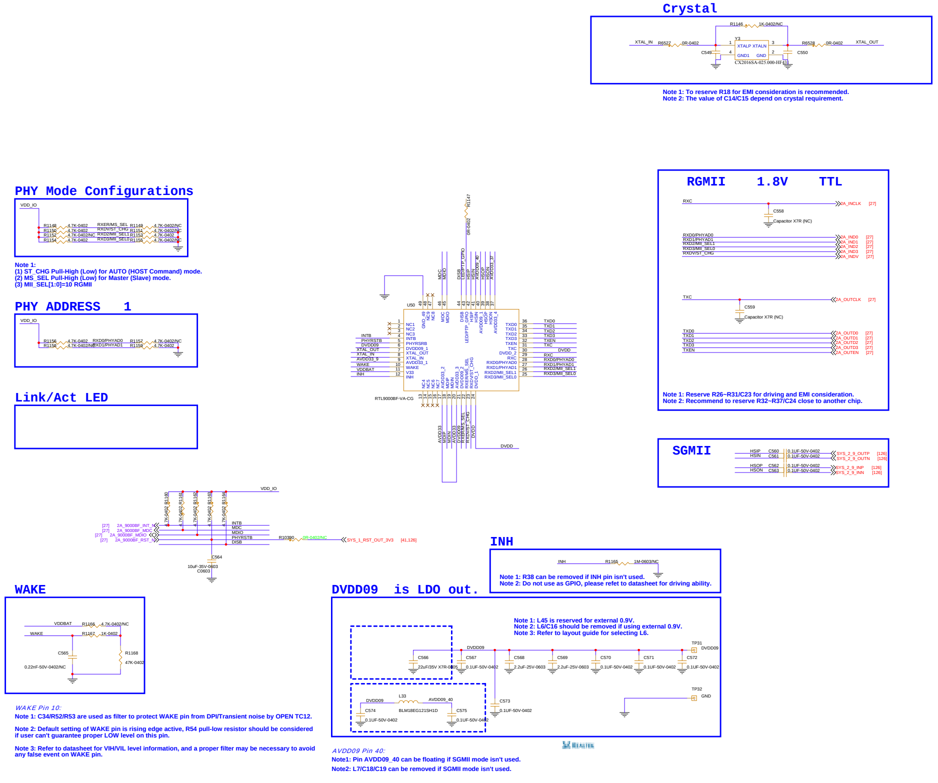
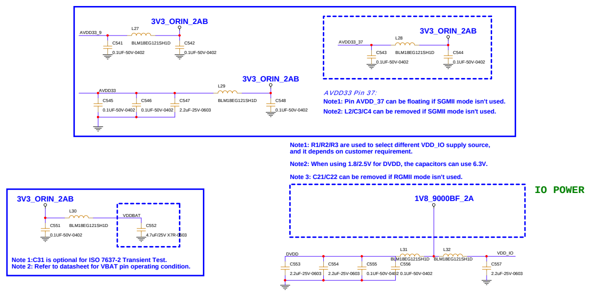


Crystal
XTAL_IN R6527 0R-0402
R1146 1K-0402/NC
Y3 XTALP XTALN GND1 GND
CX2016SA-025.000-HF431
C549 C550
R6528 0R-0402 XTAL_OUT
Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.
PHY Mode Configurations
VDD_IO
R1148 4.7K-0402 RXER/MS_SEL R1149 4.7K-0402/NC
R1150 4.7K-0402 RXDV/ST_CHG R1151 4.7K-0402/NC
R1152 4.7K-0402/NC RXD2/MII_SEL1 R1153 4.7K-0402
R1154 4.7K-0402 RXD3/MII_SEL0 R1155 4.7K-0402/NC
Note 1:
(1) ST_CHG Pull-High (Low) for AUTO (HOST Command) mode.
(2) MS_SEL Pull-High (Low) for Master (Slave) mode.
(3) MII_SEL[1:0]=10 RGMII
PHY ADDRESS 1
VDD_IO
R1156 4.7K-0402 RXD0/PHYAD0 R1157 4.7K-0402/NC
R1158 4.7K-0402/NC RXD1/PHYAD1 R1159 4.7K-0402
Link/Act LED
RTL9000BF-VA-CG
RGMII 1.8V TTL
RXC 2A_INCLK [27]
C558 Capacitor X7R (NC)
RXD0/PHYAD0 2A_IND0 [27]
RXD1/PHYAD1 2A_IND1 [27]
RXD2/MII_SEL1 2A_IND2 [27]
RXD3/MII_SEL0 2A_IND3 [27]
RXDV/ST_CHG 2A_INDV [27]
TXC 2A_OUTCLK [27]
C559 Capacitor X7R (NC)
TXD0 2A_OUTD0 [27]
TXD1 2A_OUTD1 [27]
TXD2 2A_OUTD2 [27]
TXD3 2A_OUTD3 [27]
TXEN 2A_OUTEN [27]
Note 1: Reserve R26~R31/C23 for driving and EMI consideration.
Note 2: Recommend to reserve R32~R37/C24 close to another chip.
SGMII
HSIP C560 0.1UF-50V-0402 SYS_2_9_OUTP [126]
HSIN C561 0.1UF-50V-0402 SYS_2_9_OUTN [126]
HSOP C562 0.1UF-50V-0402 SYS_2_9_INP [126]
HSON C563 0.1UF-50V-0402 SYS_2_9_INN [126]
VDD_IO
R1160 R1161 R1162 R1163 R1164 4.7K-0402
[27] 2A_9000BF_INT_N INTB
[27] 2A_9000BF_MDC MDC
[27] 2A_9000BF_MDIO MDIO
[27] 2A_9000BF_RST_N PHYRSTB
DISB
R10390 0R-0402/NC SYS_1_RST_OUT_3V3 [41,126]
C564 10uF-35V-0603 C0603
INH
INH R1165 1M-0603/NC
Note 1: R38 can be removed if INH pin isn't used.
Note 2: Do not use as GPIO, please refet to datasheet for driving ability.
WAKE
VDDBAT R1166 4.7K-0402/NC
WAKE R1167 1K-0402
C565 0.22nF-50V-0402/NC
R1168 47K-0402
WAKE Pin 10:
Note 1: C34/R52/R53 are used as filter to protect WAKE pin from DPI/Transient noise by OPEN TC12.
Note 2: Default setting of WAKE pin is rising edge active, R54 pull-low resistor should be considered if user can't guarantee proper LOW level on this pin.
Note 3: Refer to datasheet for VIH/VIL level information, and a proper filter may be necessary to avoid any false event on WAKE pin.
DVDD09 is LDO out.
Note 1: L45 is reserved for external 0.9V.
Note 2: L6/C16 should be removed if using external 0.9V.
Note 3: Refer to layout guide for selecting L6.
DVDD09
C566 22uF/35V X7R-0805
C567 0.1UF-50V-0402
C568 2.2uF-25V-0603
C569 2.2uF-25V-0603
C570 0.1UF-50V-0402
C571 0.1UF-50V-0402
C572 0.1UF-50V-0402
TP31 DVDD09
TP32 GND
DVDD09 L33 AVDD09_40
BLM18EG121SH1D
C574 0.1UF-50V-0402
C575 0.1UF-50V-0402
C573 0.1UF-50V-0402
AVDD09 Pin 40:
Note1: Pin AVDD09_40 can be floating if SGMII mode isn't used.
Note2: L7/C18/C19 can be removed if SGMII mode isn't used.



3V3_ORIN_2AB
AVDD33_9 L27 BLM18EG121SH1D
C541 0.1UF-50V-0402
C542 0.1UF-50V-0402
AVDD33_37 L28 BLM18EG121SH1D
C543 0.1UF-50V-0402
C544 0.1UF-50V-0402
AVDD33 L29 BLM18EG121SH1D
C545 0.1UF-50V-0402
C546 0.1UF-50V-0402
C547 2.2uF-25V-0603
C548 0.1UF-50V-0402
AVDD33 Pin 37:
Note1: Pin AVDD_37 can be floating if SGMII mode isn't used.
Note2: L2/C3/C4 can be removed if SGMII mode isn't used.
Note1: R1/R2/R3 are used to select different VDD_IO supply source, and it depends on customer requirement.
Note2: When using 1.8/2.5V for DVDD, the capacitors can use 6.3V.
Note 3: C21/C22 can be removed if RGMII mode isn't used.
3V3_ORIN_2AB
L30 BLM18EG121SH1D
VDDBAT
C551 0.1UF-50V-0402
C552 4.7uF/25V X7R-0603
Note 1:C31 is optional for ISO 7637-2 Transient Test.
Note 2: Refer to datasheet for VBAT pin operating condition.
IO POWER
1V8_9000BF_2A
DVDD L31 BLM18EG121SH1D L32 BLM18EG121SH1D VDD_IO
C553 2.2uF-25V-0603
C554 2.2uF-25V-0603
C555 0.1UF-50V-0402
C556 0.1UF-50V-0402
C557 2.2uF-25V-0603

RGMII to SGMII (PHY side@1000Mbps):

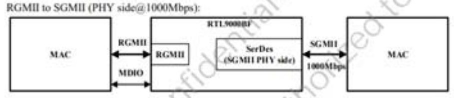


Figure 56 RGMII to SGMII Bridge Mode: PHY side, 1000Mbps.

9.2.55. RG_Config (RG App Configure Register, Page 0xa47, Reg 0x17)

Table 80 RG_Config (RG APP Configure Register, Page 0xa47, Reg 0x17)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	000000000000	Reserved.
3:0	rg_application_cfg	RW	0000	0: xMII (MII/RMII/RGMII) => 100Base-T1. 1: SGMII (PHY side) => 100Base-T1. 2: RGMII to SGMII (PHY side@100Mbps) 3: RGMII to SGMII (PHY side@1000Mbps) 4: RGMII to SGMII (MAC side)

9.2.56. SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Table 81 SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Bit	Name	Type	Default	Description
15:10	RSVD	RW	011100	Reserved. Used internally; WRITE is not allowed.
9:8	SGMII_mode	RW	00	00: Enable SGMII Auto-Negotiation 01: Enable SGMII Force mode
7:0	RSVD	RW	0x80	Reserved. Used internally; WRITE is not allowed.

9.2.57. SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Table 82 SGMIICR2 (SGMII Control Register 2, Address 0xce00)

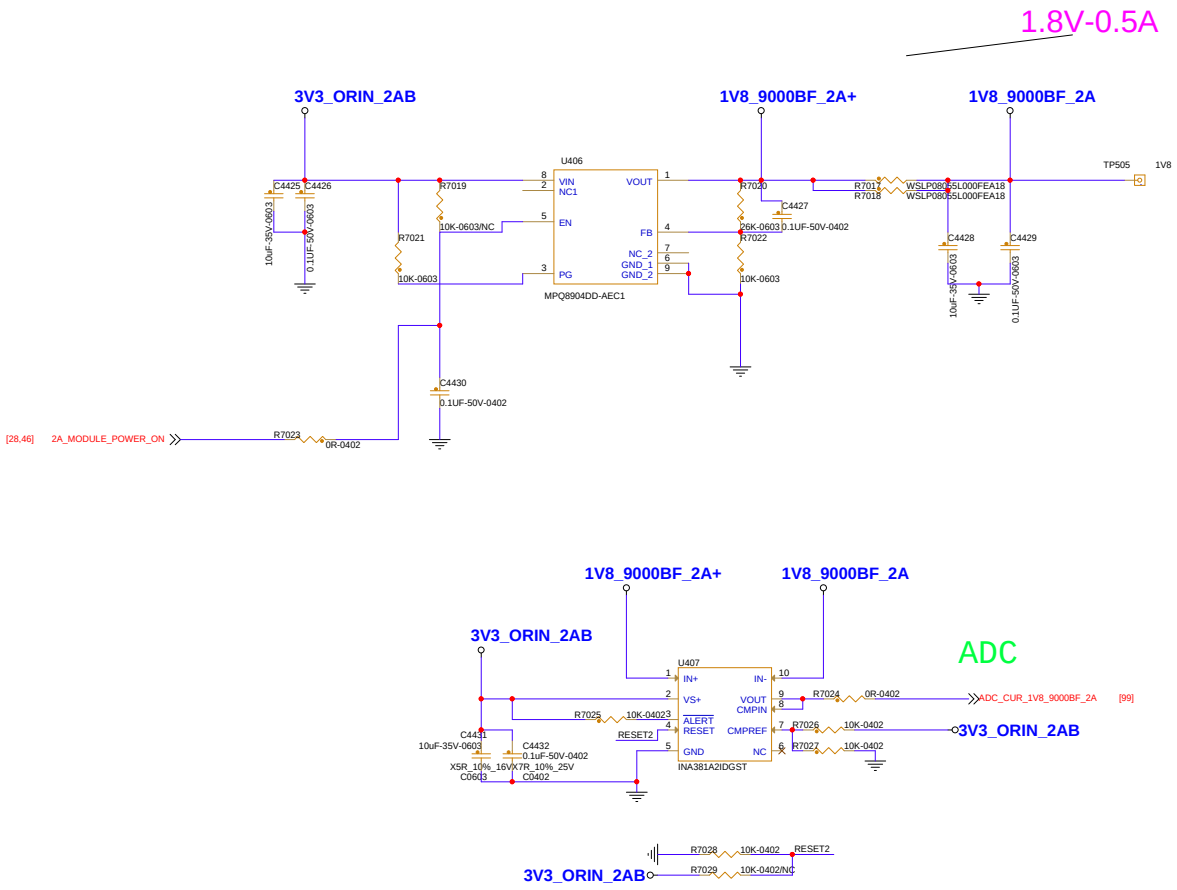
Bit	Name	Type	Default	Description
15:1	RSVD	RW	000000000000001	Reserved. Used internally; WRITE is not allowed.
0	SGMII_rst	RW	1	To reset the SGMII, please write this bit to 0 first then write back to 1.

9.2.40. RGTR (RGMII Timing Control Register, Address 0xd082)

Table 65. RGTR (RGMII Timing Control Register, Address 0xd082)

Bit	Name	Type	Default	Description
15	RSVD	RO	0	Reserved.
14	RGMII Mode	RW	Depends	1: PHY is operating in RGMII mode Decided by hardware configuration, WRITE is not allowed.
13:11	RSVD	RW	000	Reserved. Used internally; WRITE is not allowed.
10	TXC_inv*	RW	0	1: Inverse the TXC waveform *Note that if this bit is set to 1, the bit[9:8] RGMII_TXC_timing should be set to 2'b 10*
9:8	RGMII_TXC_timing*	RW	00	Add the delay for TXC latching TXD; 4ns per level The timing requirement please refers to section 11.11.5.
7:4	RSVD	RW	0001	Reserved. Used internally; WRITE is not allowed.
3:0	RGMII_RXC_timing*	RW	0000	Add the delay for RXC latching RXD, can be set from 0-9; 4ns per level The timing requirement please refers to section 11.11.5.

Issue a Software Reset (Reg 0 bit[15]=1) after the any adjustment above.



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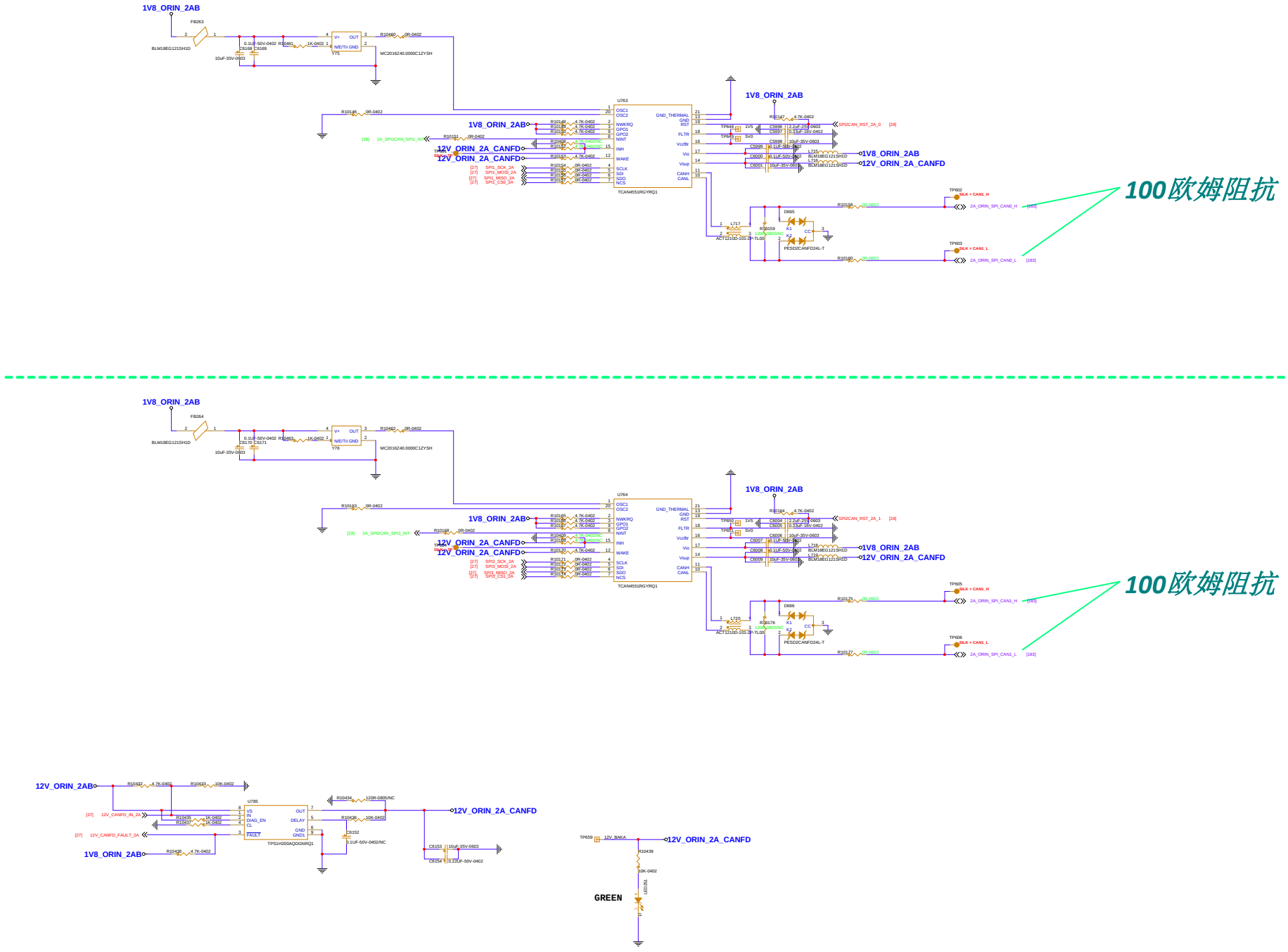
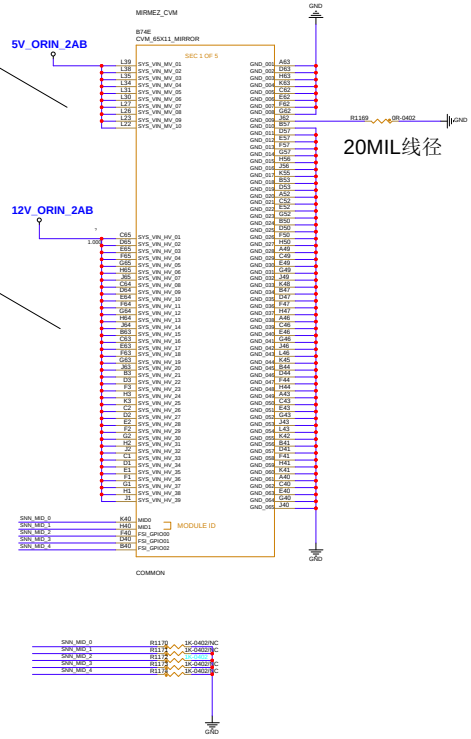

1V8_ORIN_2AB
12V_ORIN_2A_CANFD
100欧姆阻抗
100欧姆阻抗
12V_ORIN_2AB
GREEN

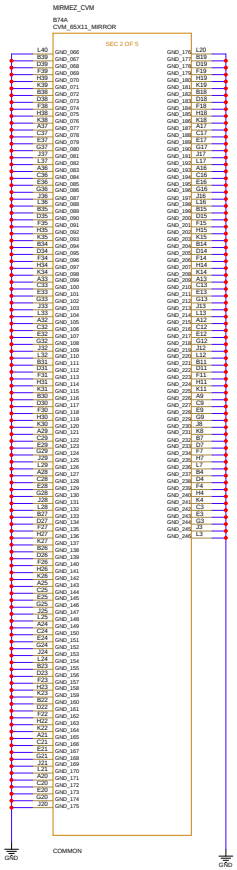
CVM CONNECTOR 1/3

5V-6A

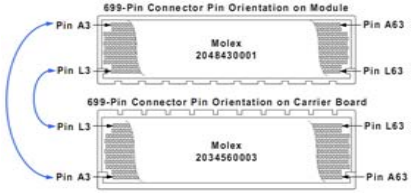
12V-10A

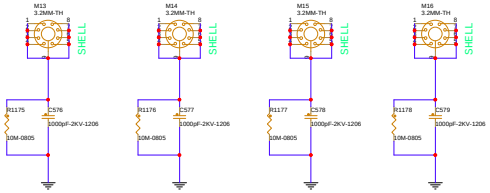


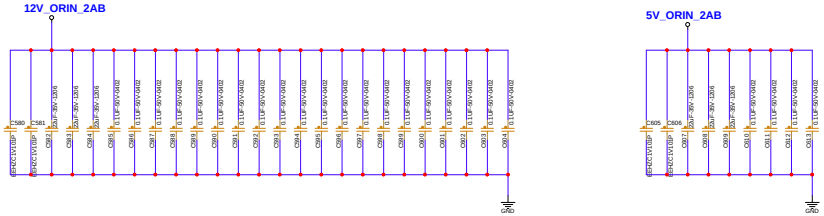
20MIL线径



Make sure the CVM connector symbol follow the mirrored pin orientation in design guide chapter 3.0.







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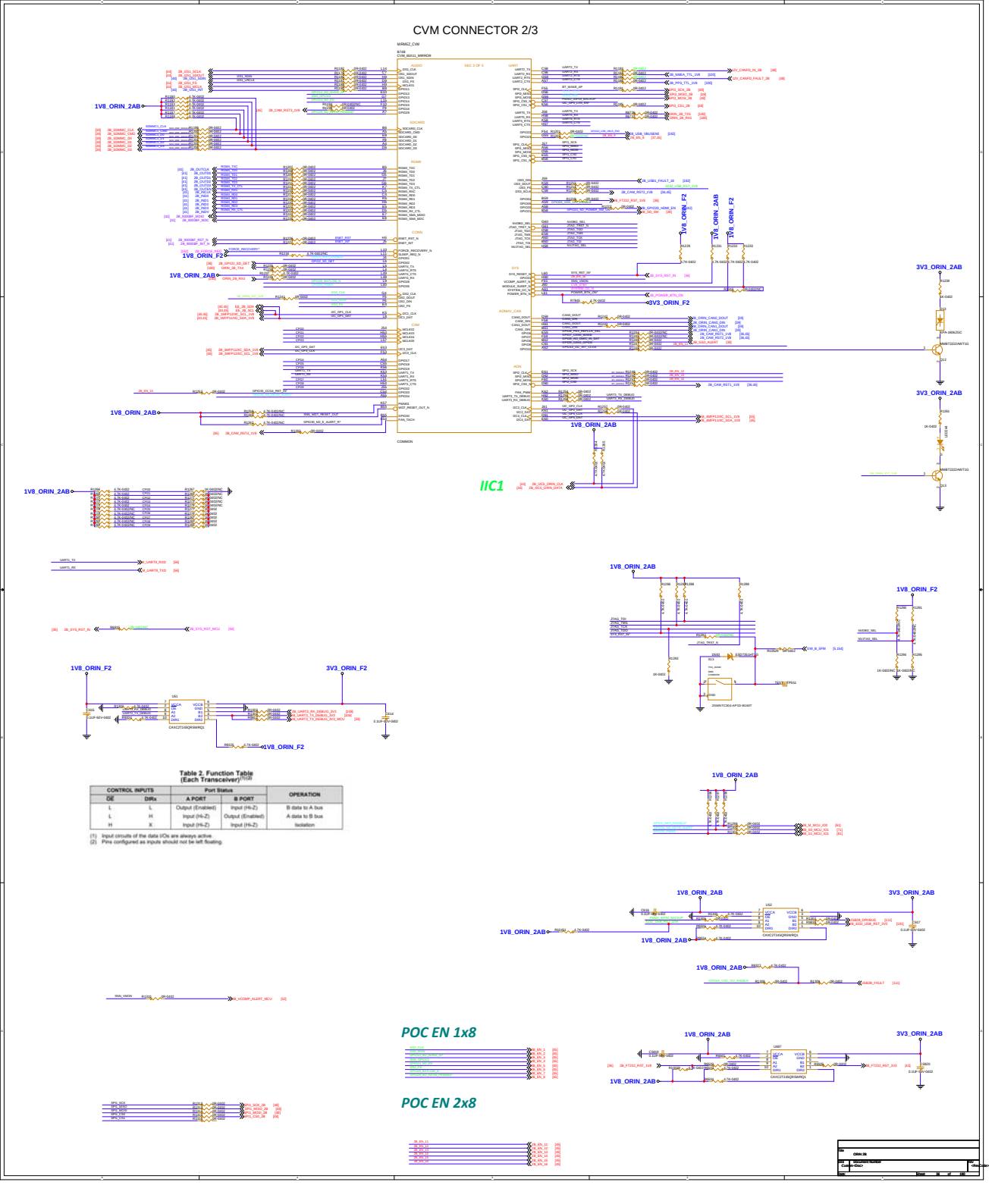
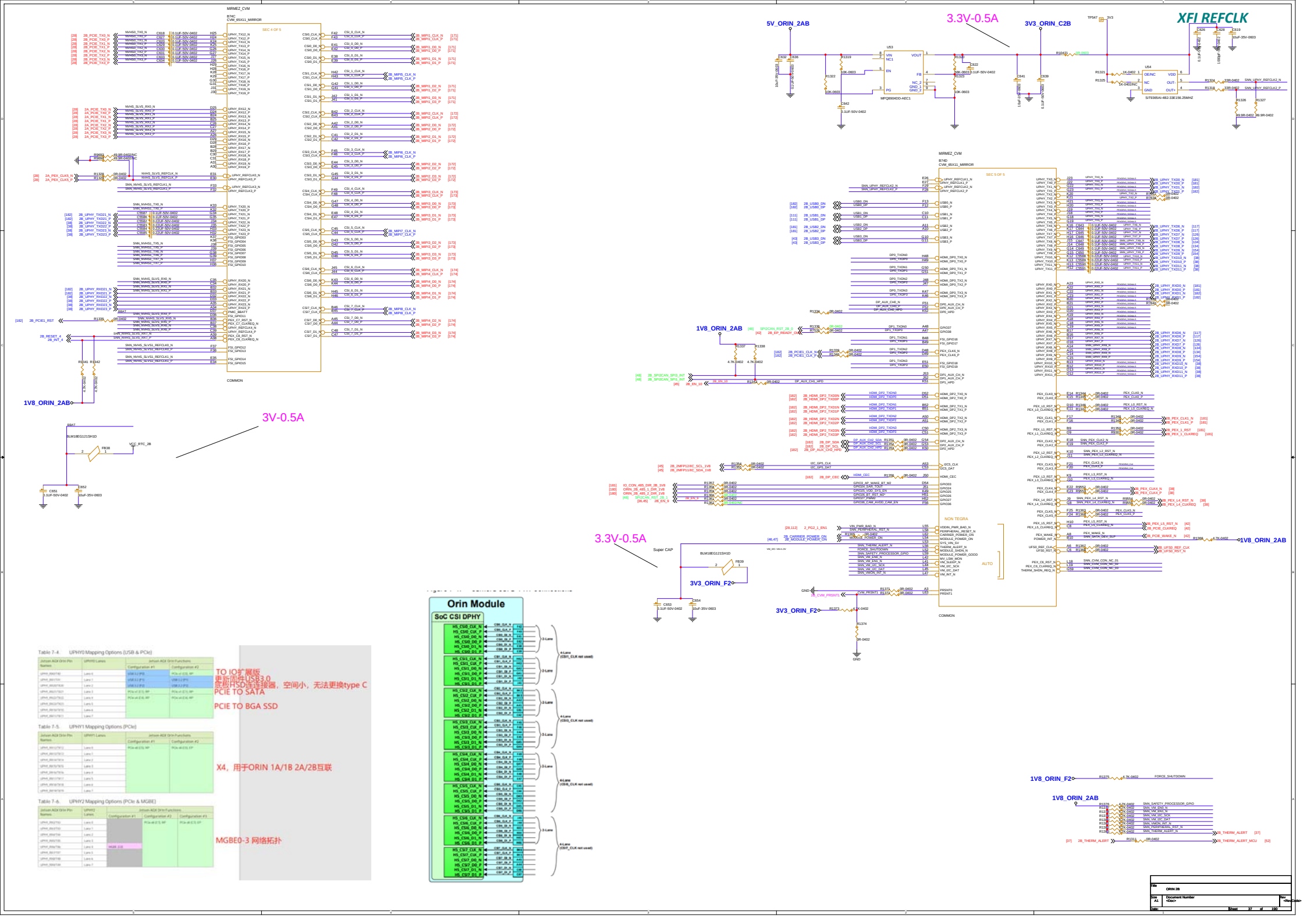
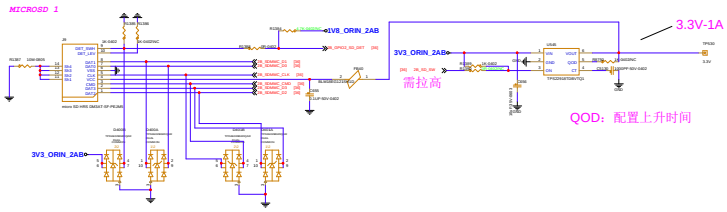
Size: D	Document Number: <Doc>
Rev:	<RevCode>
Date:	Sheet 35 of 190

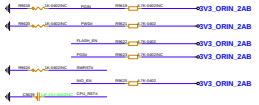
CVM CONNECTOR 2/3

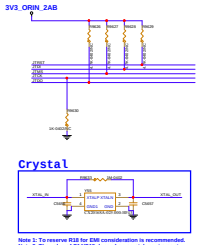


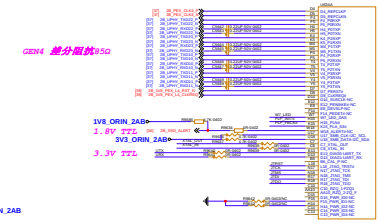

MIRME2_CVM
B74C
CVM_65X11_MIRROR
SEC 4 OF 5
COMMON
5V_ORIN_2AB
3.3V-0.5A
3V3_ORIN_C2B
XFI REFCLK
MP8904DD-AEC1
SiT9365AI-482-33E156.25MHZ
MIRME2_CVM
B74D
CVM_65X11_MIRROR
SEC 5 OF 5
1V8_ORIN_2AB
3V3_ORIN_F2
Super CAP
BLM18EG121SH1D
NON TEGRA
AUTO
COMMON
1V8_ORIN_F2
1V8_ORIN_2AB
Orin Module
SoC CSI DPHY
TO IO扩展版
更新固件让USB3.0
底板HSD连接接器，空间小，无法更接type C
PCIE TO SATA
PCIE TO BGA SSD
X4，用于ORIN 1A/1B 2A/2B互联
MGBE0-3 网络拓扑

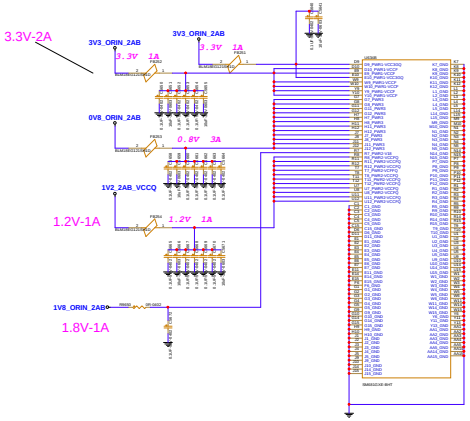

MICROSD 1
1V8_ORIN_2AB
3V3_ORIN_2AB
3.3V-1A
需拉高
QOD：配置上升时间

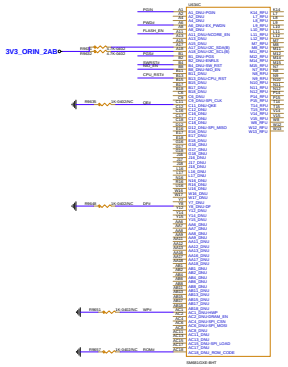

AD1
3V3_ORIN_2AB

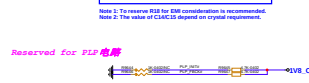

3V3_ORIN_2AB
3V3_ORIN_2AB
3V3_ORIN_2AB
3V3_ORIN_2AB
3V3_ORIN_2AB


3V3_ORIN_2AB
Crystal
Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

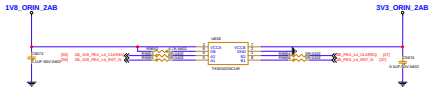

GEN4 差分阻抗85Ω
1V8_ORIN_2AB
1.8V TTL
3V3_ORIN_2AB
3.3V TTL

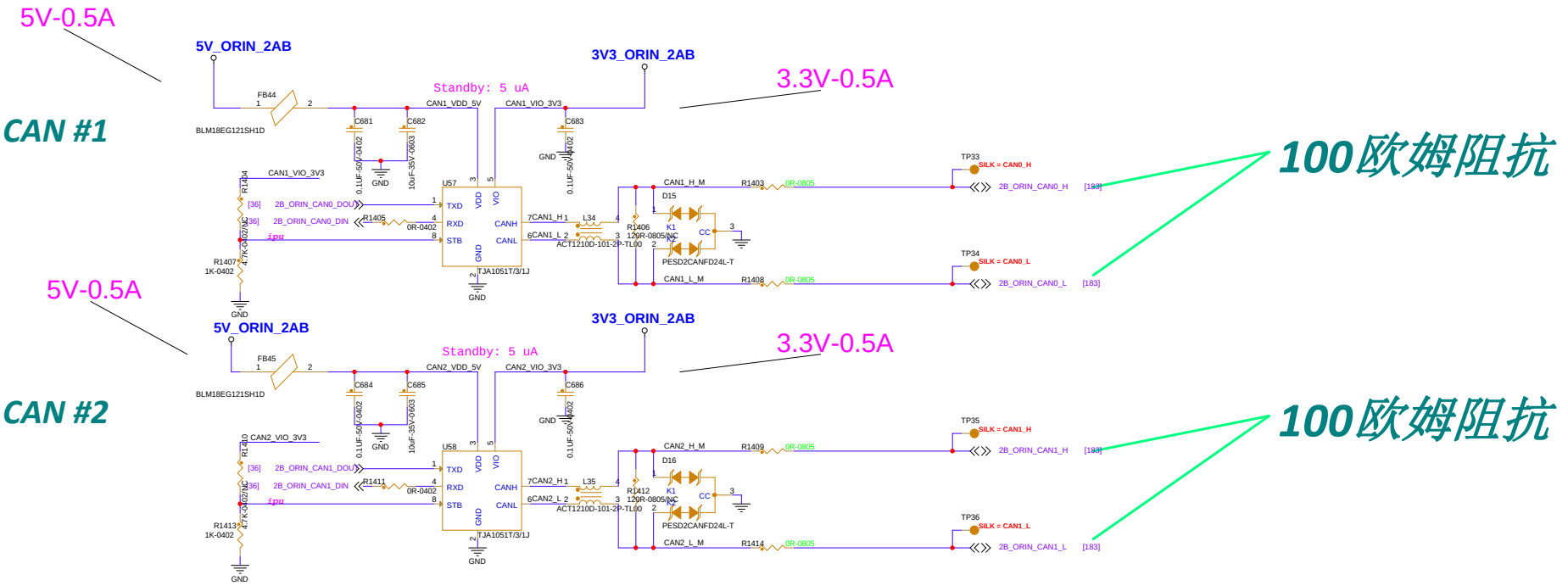

3.3V-2A
3V3_ORIN_2AB
3.3V 1A
3V3_ORIN_2AB
3.3V 1A
0V8_ORIN_2AB
0.8V 3A
1V2_2AB_VCCQ
1.2V-1A
1.2V 1A
1V8_ORIN_2AB
1.8V-1A


3V3_ORIN_2AB


Reserved for PLP电路
1V8_ORIN_2AB


异常状态指示灯
3V3_ORIN_2AB


1V8_ORIN_2AB
3V3_ORIN_2AB



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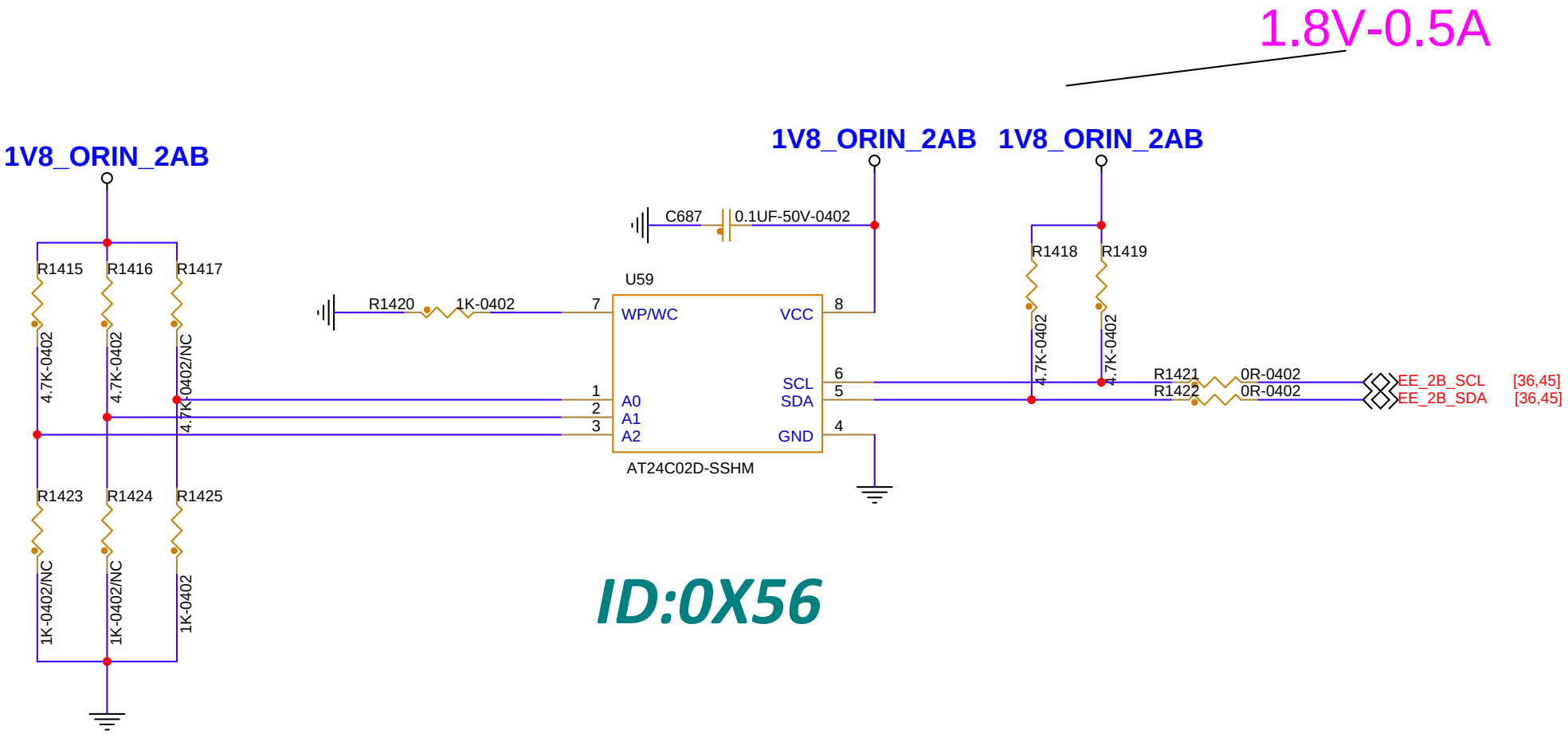


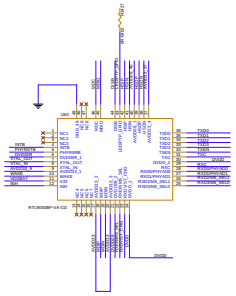
Title: NC		
Size: A	Document Number: <Doc>	Rev: <RevCode>
Date:	Sheet 40 of 190	

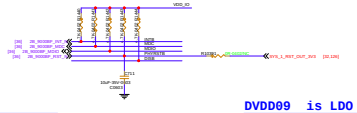
PHY Mode Configurations

Note 1:
(1) ST_CHG Pull-High (Low) for AUTO (HOST Command) mode.
(2) MS_SEL Pull-High (Low) for Master (Slave) mode.
(3) MII_SEL[1:0]=10 RGMII

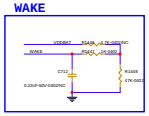
PHY ADDRESS 1

Link/Act LED





WAKE



WAKE Pin 10:

Note 1: C54/R52/R53 are used as filter to protect WAKE pin from DPI/Transient noise by OPEN TC12.

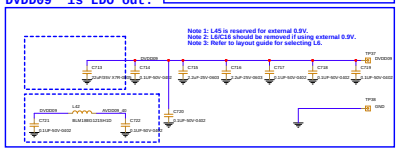
Note 2: Default setting of WAKE pin is rising edge active, R54 pull-low resistor should be considered if user can't guarantee proper LOW level on this pin.

Note 3: Refer to datasheet for VIH/VIL level information, and a proper filter may be necessary to avoid any false event on WAKE pin.

INH

Note 1: R38 can be removed if INH pin isn't used.
Note 2: Do not use as GPIO, please refet to datasheet for driving ability.

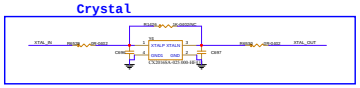
DVDD09 is LDO out.



AVDD09 Pin 40:

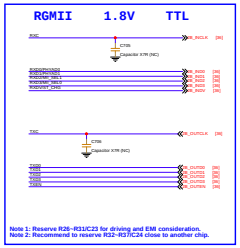
Note1: Pin AVDD09_40 can be floating if SGMII mode isn't used.
Note2: L7/C18/C19 can be removed if SGMII mode isn't used.

Crystal



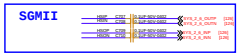
Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

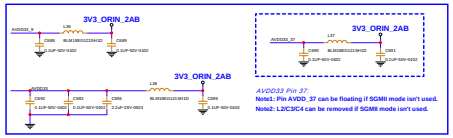
RGMII 1.8V TTL



Note 1: Reserve R26~R31/C23 for driving and EMI consideration.
Note 2: Recommend to reserve R32~R37/C24 close to another chip.

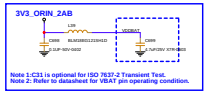
SGMII





AVDD33 Pin 37:

Note1: Pin AVDD_37 can be floating if SGMII mode isn't used.
Note2: L2/C3/C4 can be removed if SGMII mode isn't used.



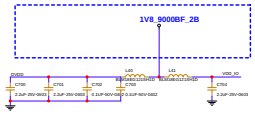
Note 1:C31 is optional for ISO 7637-2 Transient Test.
Note 2: Refer to datasheet for VBAT pin operating condition.

Note1: R1/R2/R3 are used to select different VDD_IO supply source, and it depends on customer requirement.

Note2: When using 1.8/2.5V for DVDD, the capacitors can use 6.3V.

Note 3: C21/C22 can be removed if RGMII mode isn't used.

IO POWER



RGMII to SGMII (PHY side@1000Mbps):

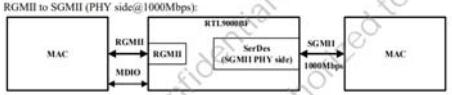


Figure 56 RGMII to SGMII Bridge Mode: PHY side, 1000Mbps.

9.2.55. RG_Config (RG App Configure Register, Page 0xa47, Reg 0x17)

Table 80 RG_Config (RG APP Configure Register, Page 0xa47, Reg 0x17)

Bit	Name	Type	Default	Description
15:4	RSVD	RO	000000000000	Reserved.
3:0	rg_application_cfg	RW	0000	0: xMII (MII/RMII/RGMII) => 100Base-T1. 1: SGMII (PHY side) => 100Base-T1. 2: RGMII to SGMII (PHY side@100Mbps) 3: RGMII to SGMII (PHY side@1000Mbps) 4: RGMII to SGMII (MAC side)

9.2.56. SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Table 81 SGMIICR1 (SGMII Control Register 1, Address 0xcc04)

Bit	Name	Type	Default	Description
15:10	RSVD	RW	011100	Reserved. Used internally; WRITE is not allowed.
9:8	SGMII_mode	RW	00	00: Enable SGMII Auto-Negotiation 01: Enable SGMII Force mode
7:0	RSVD	RW	0x80	Reserved. Used internally; WRITE is not allowed.

9.2.57. SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Table 82 SGMIICR2 (SGMII Control Register 2, Address 0xce00)

Bit	Name	Type	Default	Description
15:1	RSVD	RW	000000000000001	Reserved. Used internally; WRITE is not allowed.
0	SGMII_rst	RW	1	To reset the SGMII, please write this bit to 0 first then write back to 1.

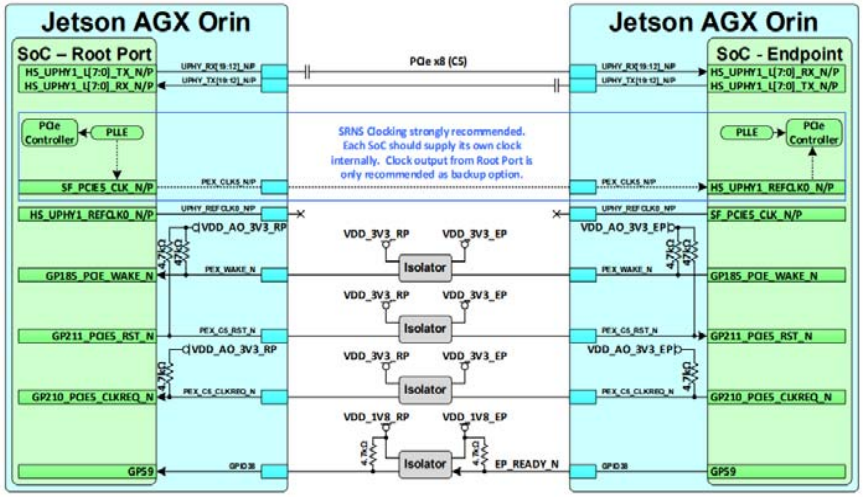
9.2.40. RGTR (RGMII Timing Control Register, Address 0xd082)

Table 65 RGTR (RGMII Timing Control Register, Address 0xd082)

Bit	Name	Type	Default	Description
15	RSVD	RO	0	Reserved.
14	RGMII_Mode	RW	Depends	1: PHY is operating in RGMII mode Decided by hardware configuration, WRITE is not allowed.
13:11	RSVD	RW	000	Reserved. Used internally; WRITE is not allowed.
10	TXC_inv*	RW	0	1: Invert the TXC waveform *Note that if this bit is set to 1, the bit[9:8] RGMII_TXC_timing should be set to 2'b10*
9:8	RGMII_TXC_timing*	RW	00	Add the delay for TXC latching TXD, 4ns per level The timing requirement please refers to section 11.11.5.
7:4	RSVD	RW	0001	Reserved. Used internally; WRITE is not allowed.
3:0	RGMII_RXC_timing*	RW	0000	Add the delay for RXC latching RXD, can be set from 0~9, 4ns per level The timing requirement please refers to section 11.11.5.

*Issue a Software Reset (Reg 0 bit[15] =1) after the any adjustment above.

Figure 6-4. PCIe Jetson AGX Orin RP to Jetson AGX Orin EP connection Example



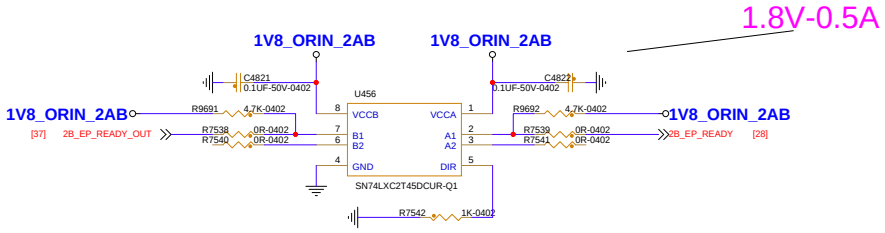
8.4 器件功能模式

表 8-1. 功能表

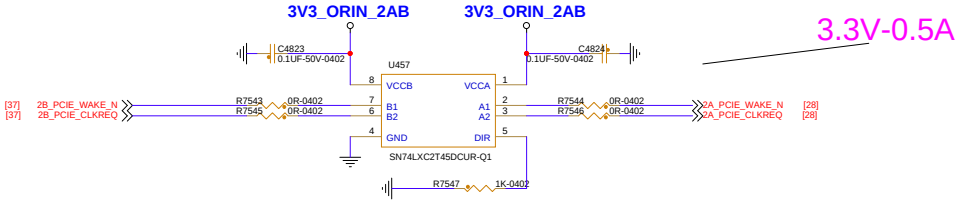
控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

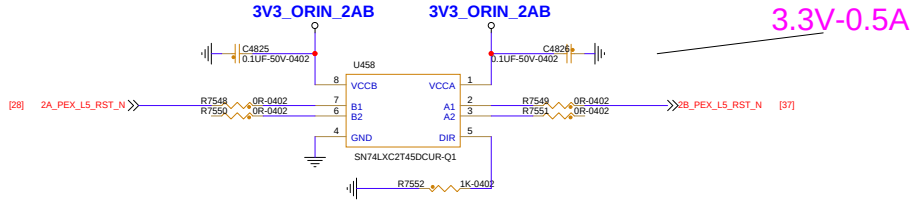
ORIN-2B TO 2A
2A:RC 2B:EP



ORIN-2B TO 2A
2A:RC 2B:EP



ORIN-2A TO 2B
2A:RC 2B:EP



Title	PLL 1A&&1B	
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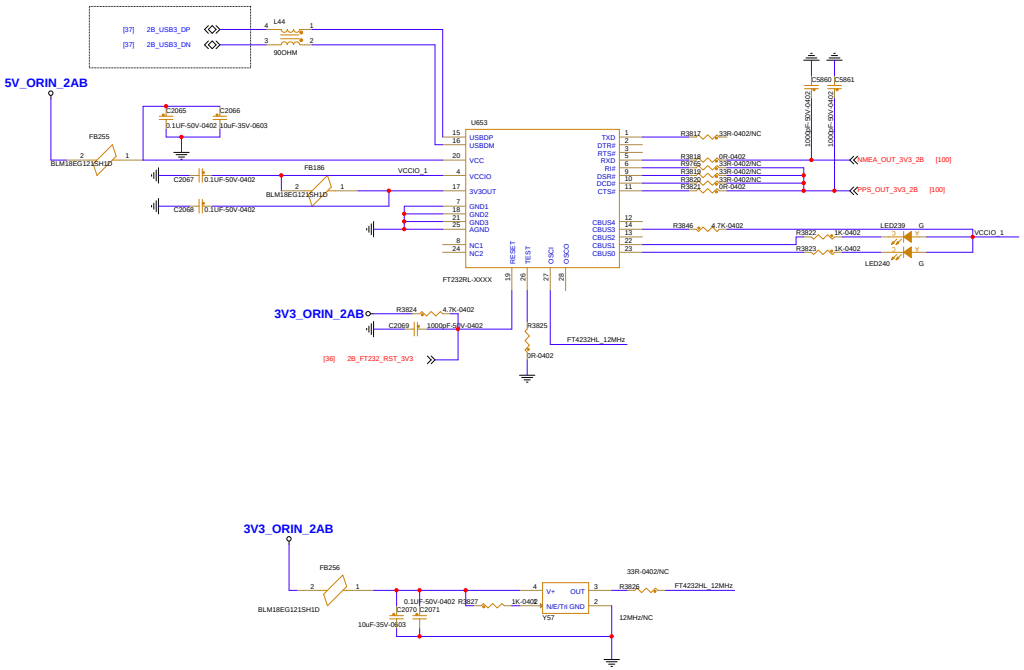
Route length
difference : ±1mm
Route diff pair
impedance : 90Ω



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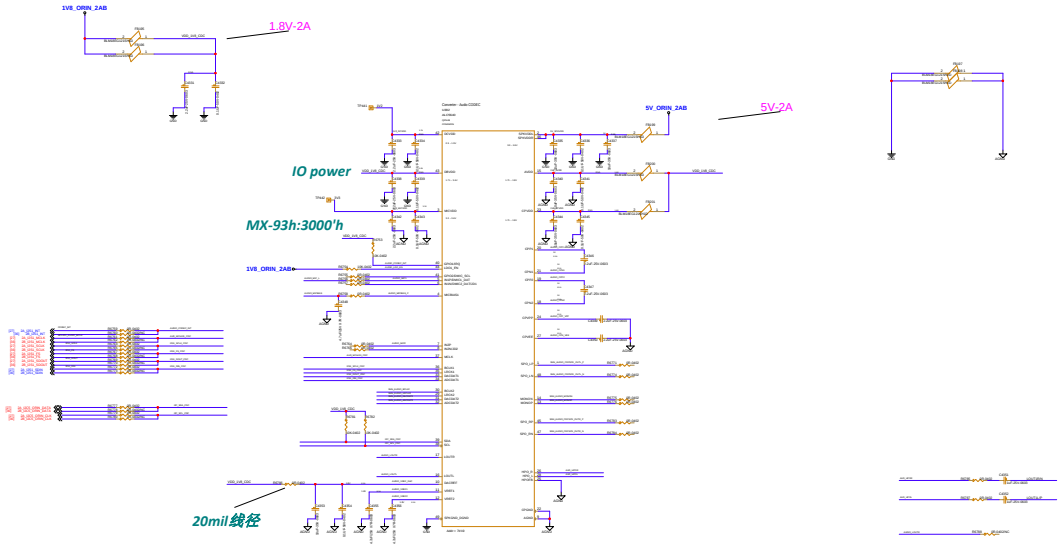
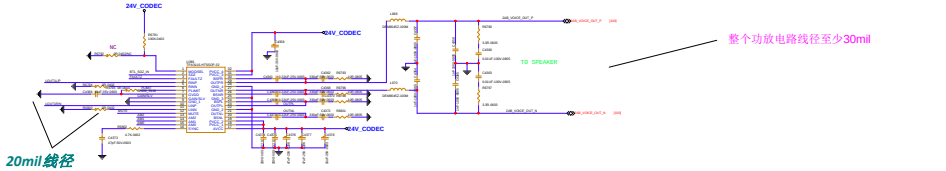
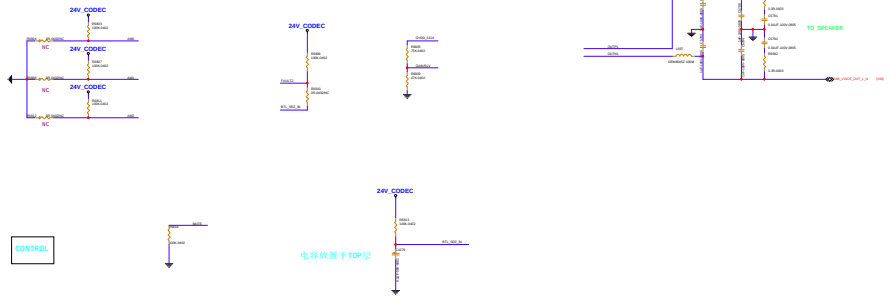
Size	Document Number		Rev
Custom	<Doc>		<RevCode>
Date:		Sheet 43 of 190	


1V8_ORN_2AB
1.8V-2A
5V_ORN_2AB
5V-2A
IO power
MX-93h:3000'h
20mil线径

功放改为12V输入


24V_CODEC
TO_SPEAKER
整个功放电路线径至少30mil
20mil线径


24V_CODEC
NC
TO_SPEAKER
CONTROL
电容放置于TOP层

8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并保持为有效逻辑电平。

1.8V TTL

1.8V TTL

from M-MCU 1.8V TTL

EN MUX

手动拉高，切ORIN-2B

C种POC电源使能EN，由ORIN-1B/2B控制，默认1B
SNS和SEL信号接到M-MCU监控

DEFAULT MODE IS A=B2（ORIN-1B）

Table 1. Function Table

INPUTS		INPUT/OUTPUT	FUNCTION
OE	B	A	
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

RESET MUX

手动拉高，切ORIN-2B

C种9296A RST，由ORIN-1B/2B控制，默认1B
IO由M-MCU控制

1V8_ORIN_1AB

1V8_ORIN_2AB

注意：此页芯片供电引脚至少1A

ORIN-1B

ORIN-2B

IIC 3

IIC 1

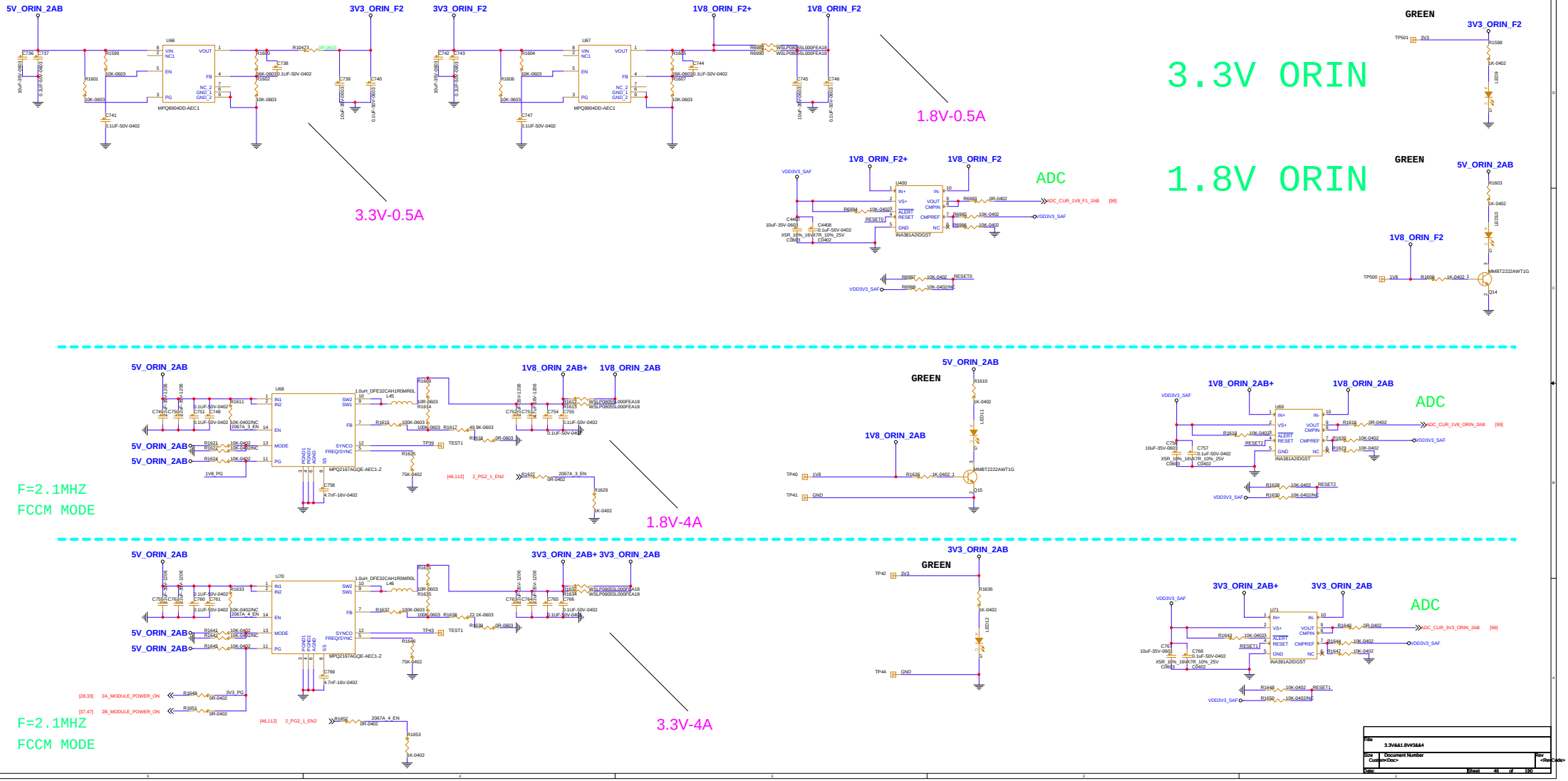
IIC 2

IIC 4

C种9296A IIC，由ORIN-1A/2A控制，默认1A
IO由M-MCU控制

IIC MUX

手动拉高，切ORIN-2B



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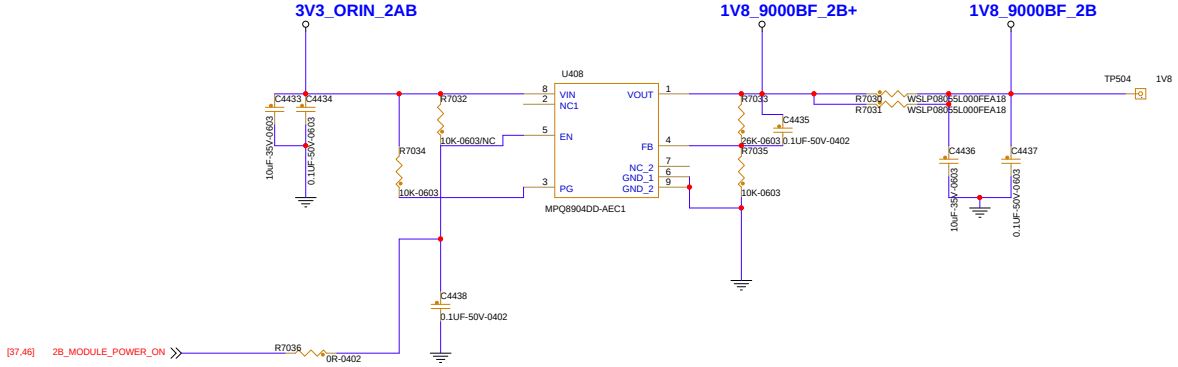
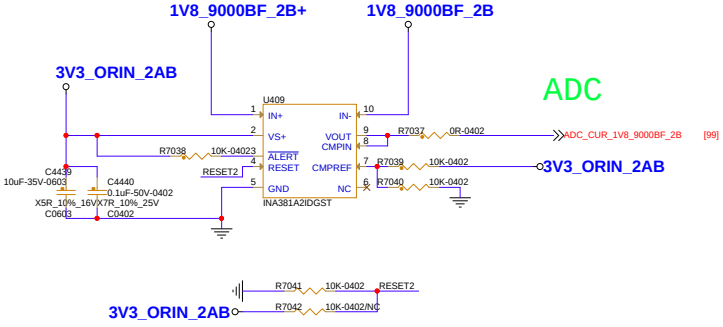
Size	Document Number
Custom	<Doc>
Rev	<RevCode>
Date:	Sheet 46 of 190

1.8V-0.5A





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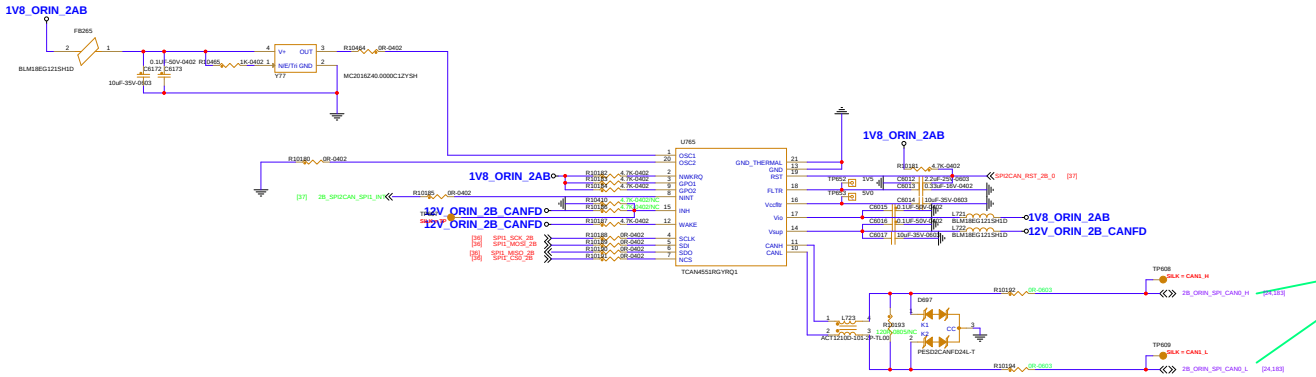

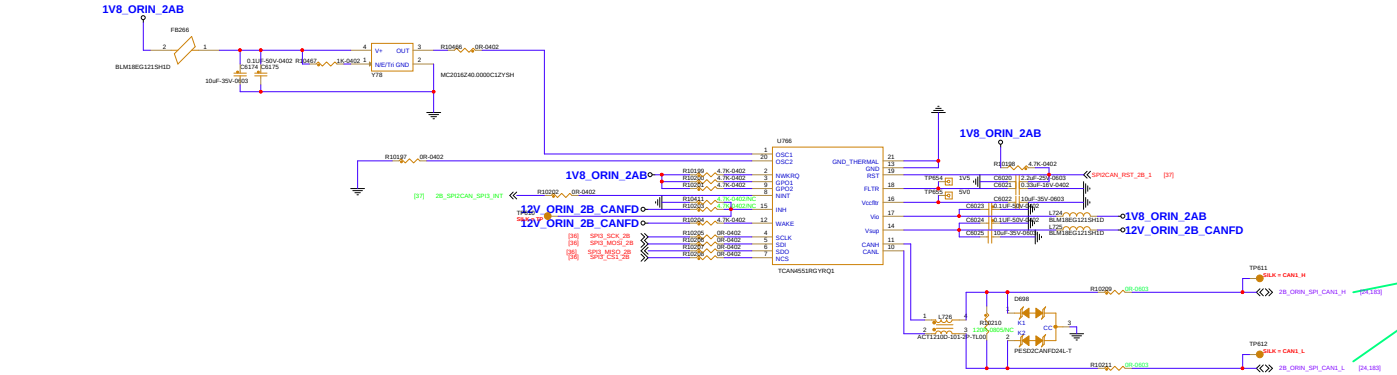

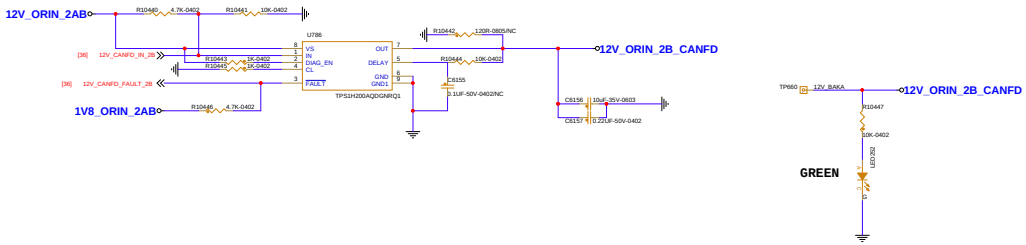

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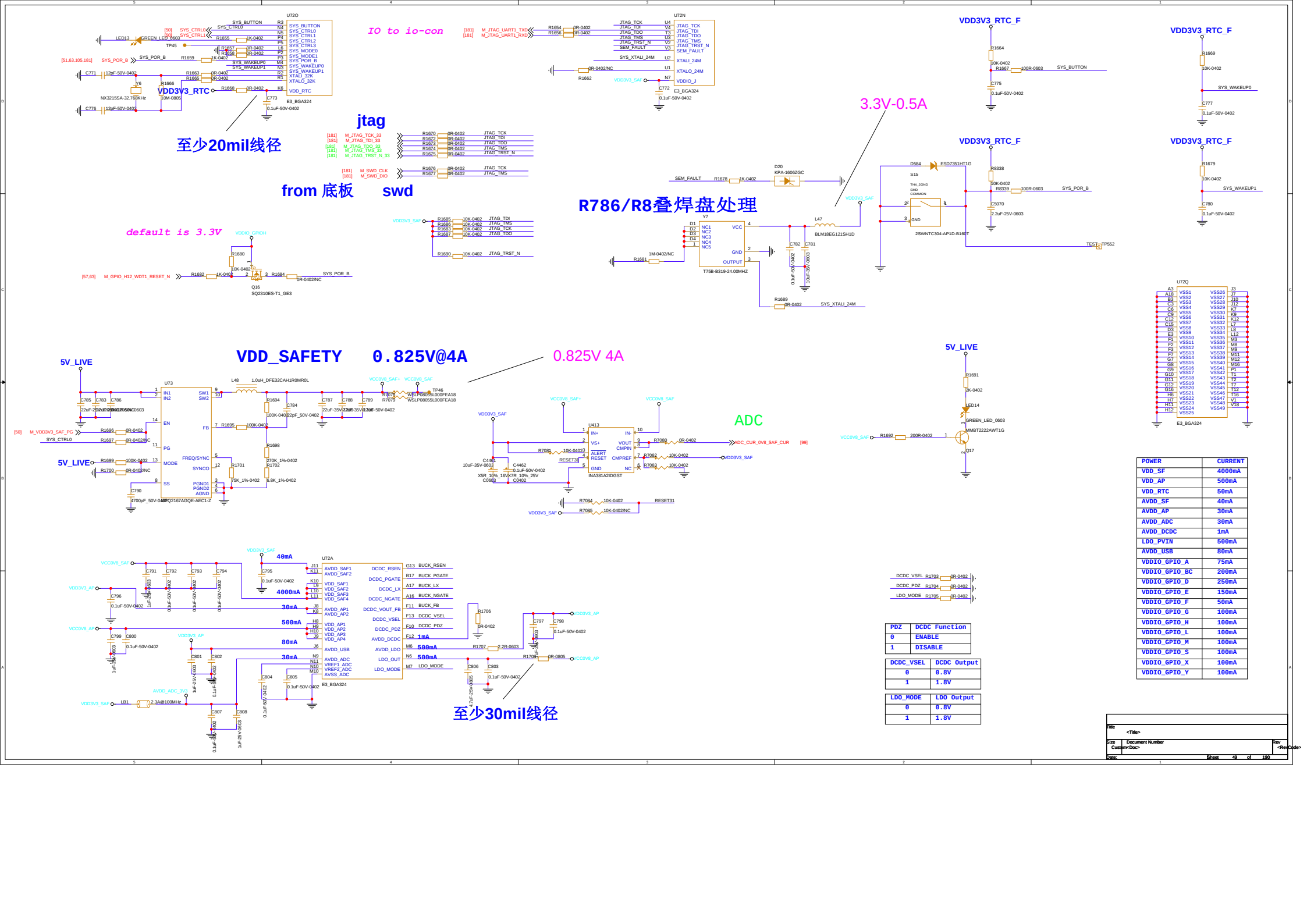

POWER	CURRENT
VDD_SF	4000mA
VDD_AP	500mA
VDD_RTC	50mA
AVDD_SF	40mA
AVDD_AP	30mA
AVDD_ADC	30mA
AVDD_DCDC	1mA
LDO_PVIN	500mA
AVDD_USB	80mA
VDDIO_GPIO_A	75mA
VDDIO_GPIO_BC	200mA
VDDIO_GPIO_D	250mA
VDDIO_GPIO_E	150mA
VDDIO_GPIO_F	50mA
VDDIO_GPIO_G	100mA
VDDIO_GPIO_H	100mA
VDDIO_GPIO_L	100mA
VDDIO_GPIO_M	100mA
VDDIO_GPIO_S	100mA
VDDIO_GPIO_X	100mA
VDDIO_GPIO_Y	100mA

PDZ	DCDC Function
0	ENABLE
1	DISABLE

DCDC_VSEL	DCDC Output
0	0.8V
1	1.8V

LDO_MODE	LDO Output
0	0.8V
1	1.8V

Title	<Title>
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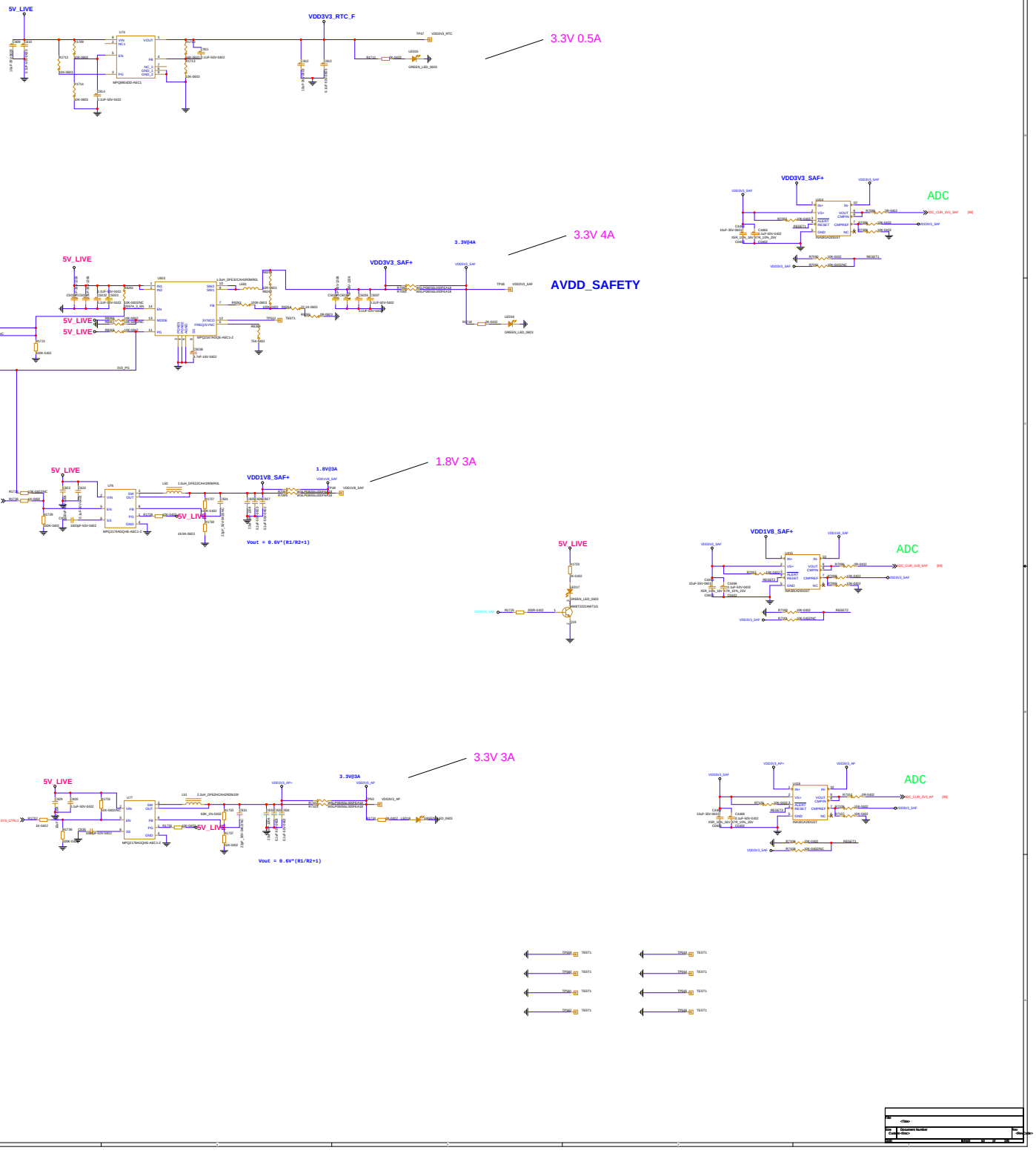

5V_LIVE
VDD3V3_RTC_F
3.3V 0.5A
VDD3V3_SAF+
3.3V 4A
AVDD_SAFETY
F=2.1MHZ
FCCM MODE
VDD1V8_SAF+
1.8V 3A
Vout = 0.6V*(R1/R2+1)
VDD3V3_AP+
3.3V@3A
ADC

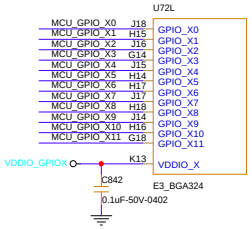
Typical Current Consumption

Operation	HL-T Current (mA)	HS-T Current (mA)
SDR Read 50 MHz	10	10
DDR Read (HyperBus)	75 (166 MHz)	156 (200 MHz)
Program	50	50
Erase	50	50
Standby (HS-T)	0.014	0.011
Deep Power Down (HS-T)	0.0022	0.0013

default is 1.8V

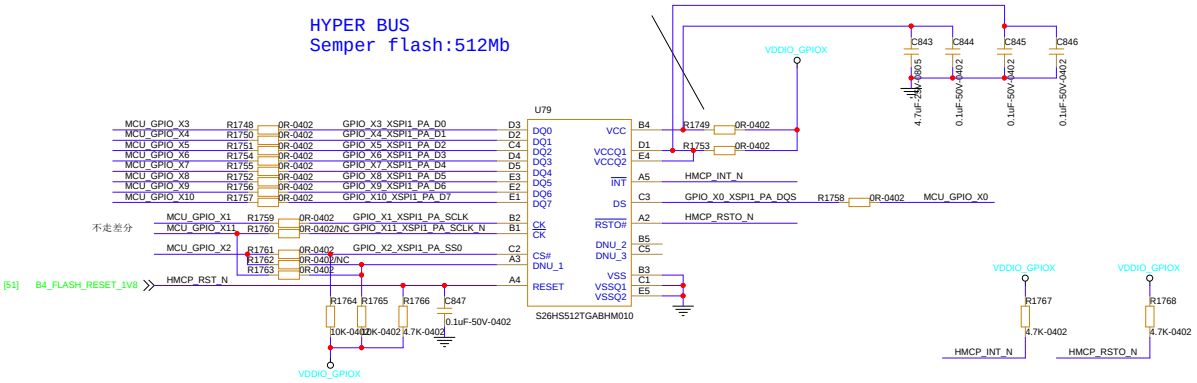
1A

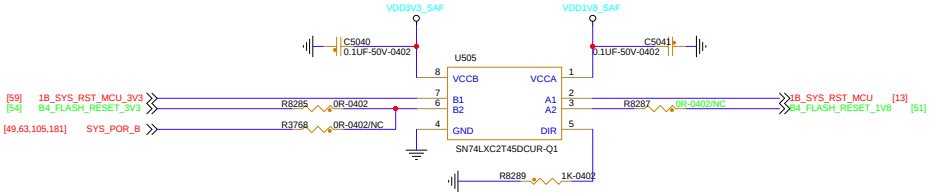
至少20mil线径



至少20mil线径 1.5A

HYPER BUS
Semper flash:512Mb





Deault:S76HS512TC0BHB010 1.8V

S76HS512TC0BHB010 1.8V
S76HL512TC0BHB010 3.3V

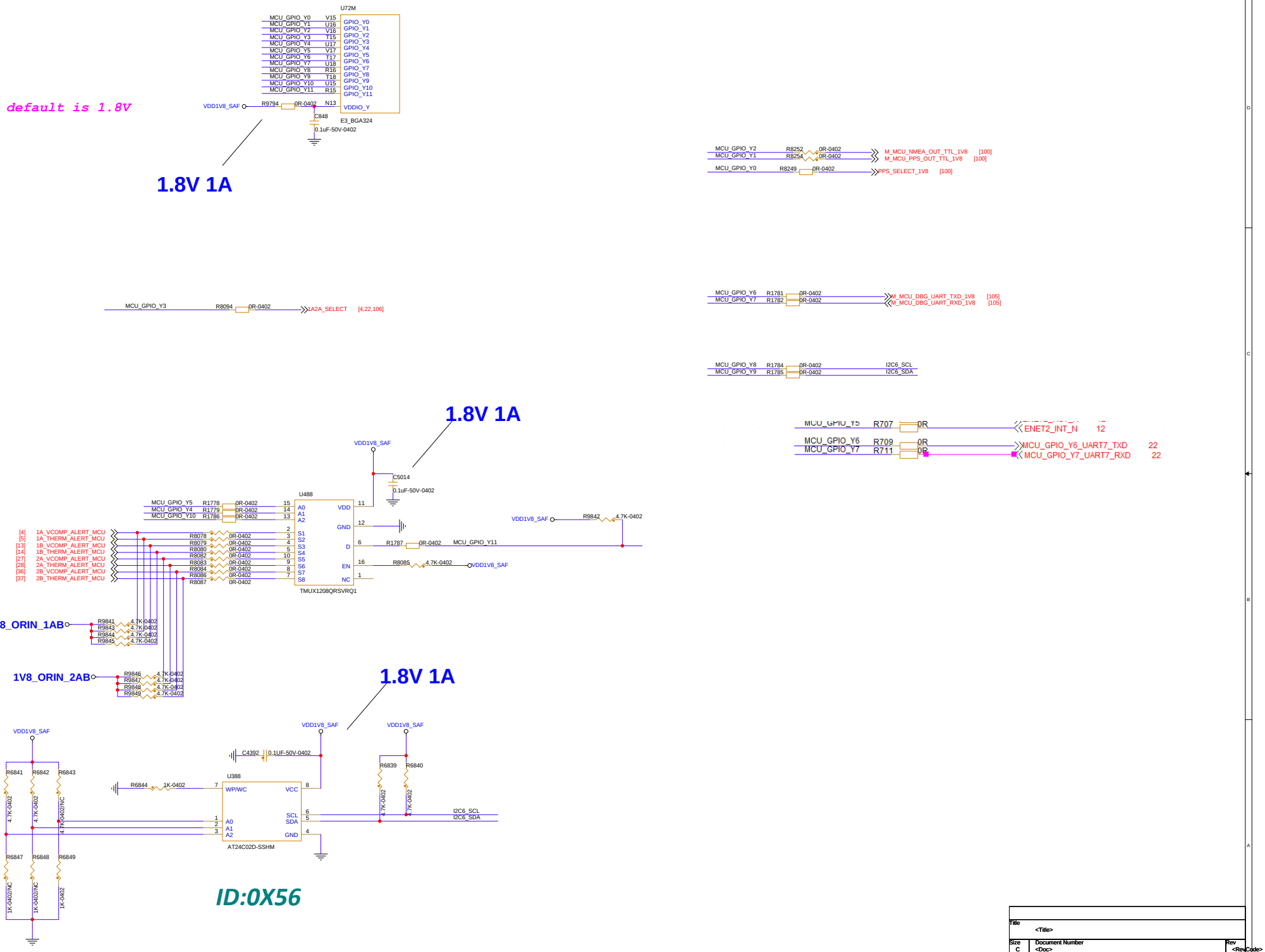
MT35XU256ABA1G12-0AUT 1.8V

8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。


U72M
MCU_GPIO_Y0 V15 GPIO_Y0
MCU_GPIO_Y1 U16 GPIO_Y1
MCU_GPIO_Y2 V16 GPIO_Y2
MCU_GPIO_Y3 T15 GPIO_Y3
MCU_GPIO_Y4 U17 GPIO_Y4
MCU_GPIO_Y5 V17 GPIO_Y5
MCU_GPIO_Y6 T17 GPIO_Y6
MCU_GPIO_Y7 U18 GPIO_Y7
MCU_GPIO_Y8 R16 GPIO_Y8
MCU_GPIO_Y9 T18 GPIO_Y9
MCU_GPIO_Y10 U15 GPIO_Y10
MCU_GPIO_Y11 R15 GPIO_Y11
VDDIO_Y
E3_BGA324
default is 1.8V
VDD1V8_SAF
R9794 0R-0402
C848 0.1uF-50V-0402
1.8V 1A
MCU_GPIO_Y2 R8252 0R-0402 M_MCU_NMEA_OUT_TTL_1V8 [100]
MCU_GPIO_Y1 R8254 0R-0402 M_MCU_PPS_OUT_TTL_1V8 [100]
MCU_GPIO_Y0 R8249 0R-0402 PPS_SELECT_1V8 [100]
MCU_GPIO_Y3 R8094 0R-0402 1A2A_SELECT [4,22,106]
MCU_GPIO_Y6 R1781 0R-0402 M_MCU_DBG_UART_TXD_1V8 [105]
MCU_GPIO_Y7 R1782 0R-0402 M_MCU_DBG_UART_RXD_1V8 [105]
MCU_GPIO_Y8 R1784 0R-0402 I2C6_SCL
MCU_GPIO_Y9 R1785 0R-0402 I2C6_SDA
1.8V 1A
MCU_GPIO_Y5 R707 0R ENET2_INT_N 12
MCU_GPIO_Y6 R709 0R MCU_GPIO_Y6_UART7_TXD 22
MCU_GPIO_Y7 R711 0R MCU_GPIO_Y7_UART7_RXD 22
VDD1V8_SAF
C5014 0.1uF-50V-0402
U488
MCU_GPIO_Y5 R1778 0R-0402
MCU_GPIO_Y4 R1779 0R-0402
MCU_GPIO_Y10 R1786 0R-0402
A0 A1 A2 VDD GND D EN NC
S1 S2 S3 S4 S5 S6 S7 S8
TMUX1208QRSVRQ1
[4] 1A_VCOMP_ALERT_MCU R8078 0R-0402
[5] 1A_THERM_ALERT_MCU R8079 0R-0402
[13] 1B_VCOMP_ALERT_MCU R8080 0R-0402
[14] 1B_THERM_ALERT_MCU R8082 0R-0402
[27] 2A_VCOMP_ALERT_MCU R8083 0R-0402
[28] 2A_THERM_ALERT_MCU R8084 0R-0402
[36] 2B_VCOMP_ALERT_MCU R8086 0R-0402
[37] 2B_THERM_ALERT_MCU R8087 0R-0402
VDD1V8_SAF R9842 4.7K-0402
R1787 0R-0402 MCU_GPIO_Y11
R8085 4.7K-0402 VDD1V8_SAF
1V8_ORIN_1AB
R9841 R9843 R9844 R9845 4.7K-0402
1V8_ORIN_2AB
R9846 R9847 R9848 R9849 4.7K-0402
1.8V 1A
VDD1V8_SAF
C4392 0.1UF-50V-0402
R6844 1K-0402
U388
WP/WC VCC SCL SDA A0 A1 A2 GND
AT24C02D-SSHM
R6841 R6842 R6843 4.7K-0402 4.7K-0402 4.7K-0402/NC
R6847 R6848 R6849 1K-0402/NC 1K-0402/NC 1K-0402
R6839 R6840 4.7K-0402
I2C6_SCL
I2C6_SDA
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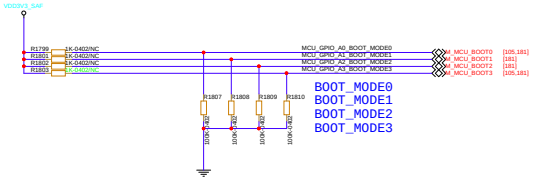
<Doc>
Rev
<RevCode>
Date:
Sheet 52 of 190

default mode is FLASH BOOT



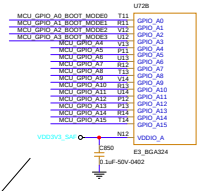
备份

使用网口OTA的话，BOOTSTRAP pin只要不是USB MODE即可

Table 6.1: Boot Mode

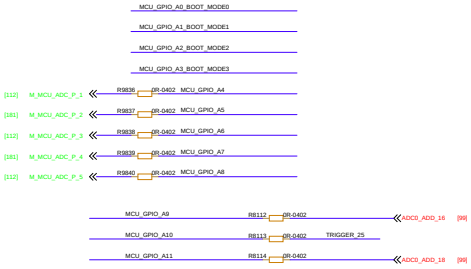
Boot Mode	Description	Notes
1110	User JTAG Mode	In this mode,Boot ROM lockout Semidrive confidential information then configure core into ARM mode, disable MPU then enable JTAG. This mode available on Development mode only
0000	XSPI1 NOR/Hyper Flash	-
0001	XSPI1 NAND Flash	-
0010	eMMC1	-
0011	SD1	-
0100	SD2	-
0101	XSPI Slave Port	Boot from XSPI slave interface
1000	USB Boot	-

default is 3.3V

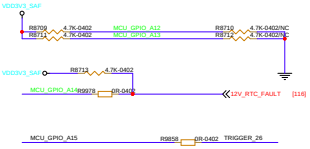


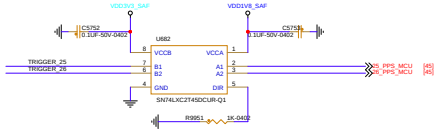
3.3V 1A

5个模拟IO



M-MCU ID:0X03





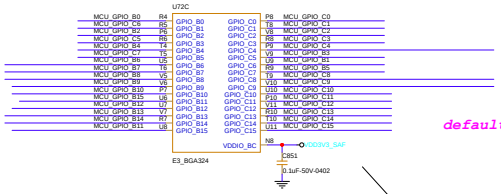
8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

16个模拟IO



default is 3.3V

E D L不支持trg

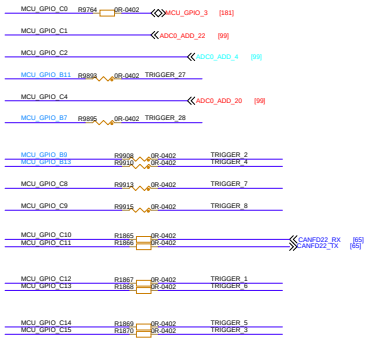
8.4 器件功能模式

表 8-1. 功能表

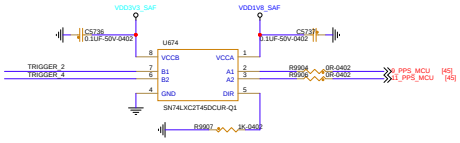
控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

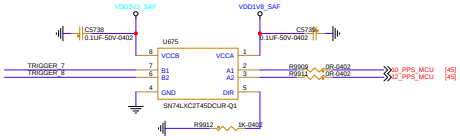
(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

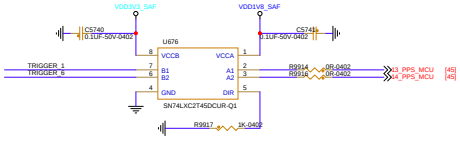
3.3V 1A

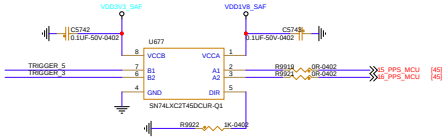


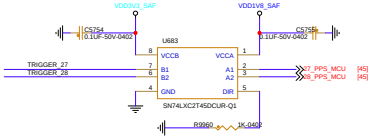
CANFD 22

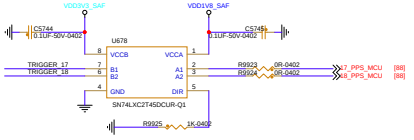


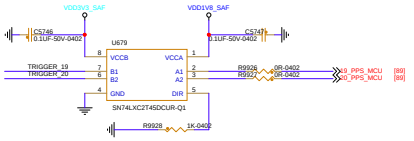


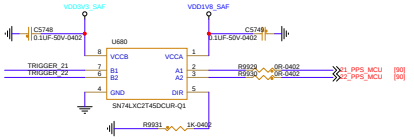


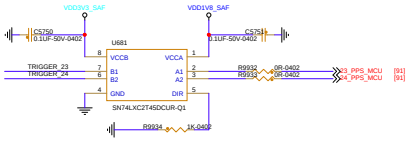


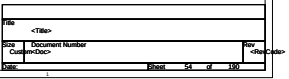




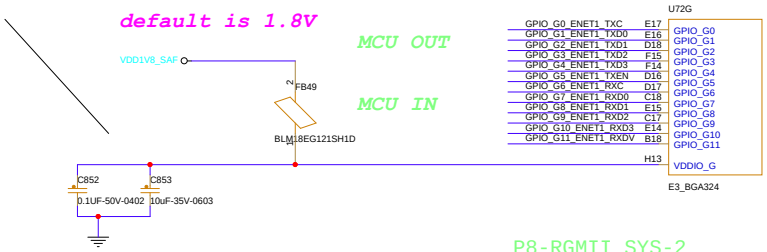








1.8V 1A



P8-RGMII SYS-2

MCU OUT

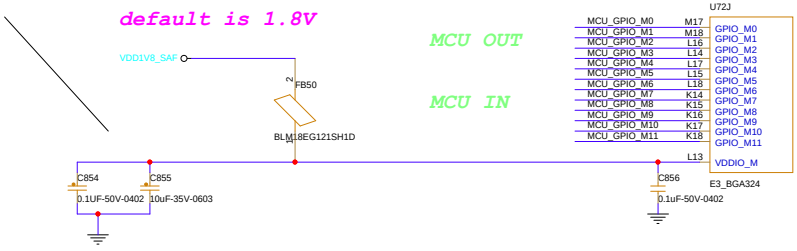
MCU IN

GPIO_G0_ENET1_TXC	SYS_2_MII3_RXCLK	[126]
GPIO_G1_ENET1_TXD0	SYS_2_MII3_RXD0	[126]
GPIO_G2_ENET1_TXD1	SYS_2_MII3_RXD1	[126]
GPIO_G3_ENET1_TXD2	SYS_2_MII3_RXD2	[126]
GPIO_G4_ENET1_TXD3	SYS_2_MII3_RXD3	[126]
GPIO_G5_ENET1_TXEN	SYS_2_MII3_RXDV	[126]
GPIO_G6_ENET1_RXC	SYS_2_MII3_TXCLK	[126]
GPIO_G7_ENET1_RXD0	SYS_2_MII3_TXD0	[126]
GPIO_G8_ENET1_RXD1	SYS_2_MII3_TXD1	[126]
GPIO_G9_ENET1_RXD2	SYS_2_MII3_TXD2	[126]
GPIO_G10_ENET1_RXD3	SYS_2_MII3_TXD3	[126]
GPIO_G11_ENET1_RXDV	SYS_2_MII3_TXEN	[126]

89586 IN

89586 OUT

1.8V 1A



P8-RGMII SYS-1

MCU OUT

MCU IN

MCU_GPIO_M0	GPIO_M0_ENET2_TXC	MII3_RXCLK	[117]
MCU_GPIO_M1	GPIO_M1_ENET2_TXD0	MII3_RXD0	[117]
MCU_GPIO_M2	GPIO_M2_ENET2_TXD1	MII3_RXD1	[117]
MCU_GPIO_M3	GPIO_M3_ENET2_TXD2	MII3_RXD2	[117]
MCU_GPIO_M4	GPIO_M4_ENET2_TXD3	MII3_RXD3	[117]
MCU_GPIO_M5	GPIO_M5_ENET2_TXEN	MII3_RXDV	[117]
MCU_GPIO_M6	GPIO_M6_ENET2_RXC	MII3_TXCLK	[117]
MCU_GPIO_M7	GPIO_M7_ENET2_RXD0	MII3_TXD0	[117]
MCU_GPIO_M8	GPIO_M8_ENET2_RXD1	MII3_TXD1	[117]
MCU_GPIO_M9	GPIO_M9_ENET2_RXD2	MII3_TXD2	[117]
MCU_GPIO_M10	GPIO_M10_ENET2_RXD3	MII3_TXD3	[117]
MCU_GPIO_M11	GPIO_M11_ENET2_RXDV	MII3_TXEN	[117]

89586 IN

89586 OUT

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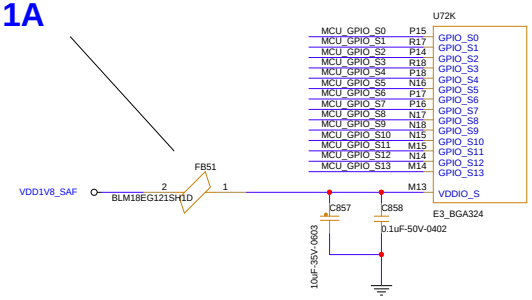
1.8V 1A

default is 1.8V

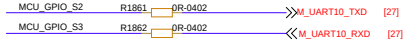


UART4:NMEA/PPS IN
UART5:NMEA/PPS OUT
UART7:DEBUG
UART10:SAFETY TO ORIN 2A
UART11:SAFETY TO ORIN 1A
UART9:SAFETY TO ORIN 2B
UART2:AP TO ORIN 1B
UART3 :M-MCU TO S1-MCU UART10
UART6 :M-MCU TO S2-MCU UART10
UART8 :M-MCU TO ORIN-1A DEBUG LOGGER
UART16:MCU TO ORIN 1B DEBUG UART LOGGER
UART15:MCU TO ORIN 2A DEBUG UART LOGGER
UART14:MCU TO ORIN 2B DEBUG UART LOGGER

1.8V TTL uart11 txd
uart11 rxd

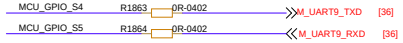
TO ORIN 1A

1.8V TTL uart10 txd
uart10 rxd

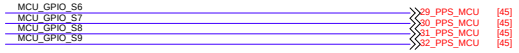


TO ORIN 2A

1.8V TTL uart9 txd
uart9 rxd



TO ORIN 2B



RESET TO ORIN x3

ORIN 1A DEBUG logger UART8-RXD

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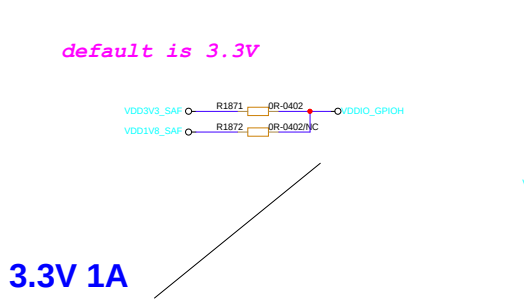
8.4 器件功能模式



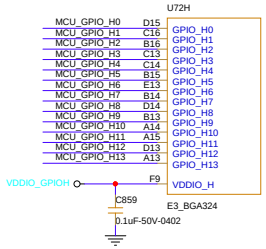
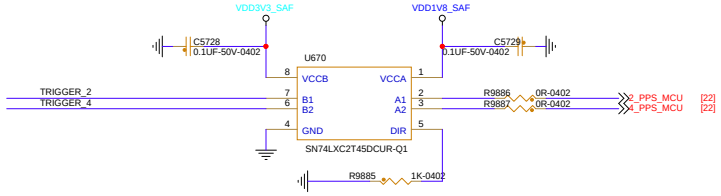
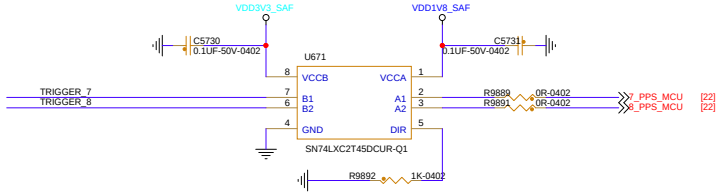


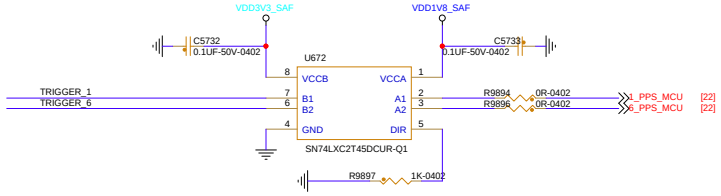
表 8-1. 功能表

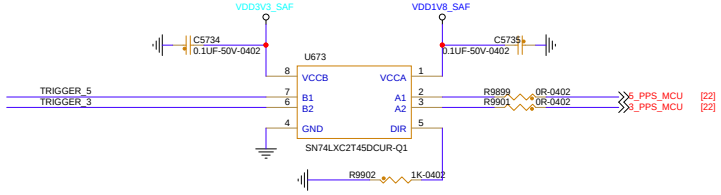
控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

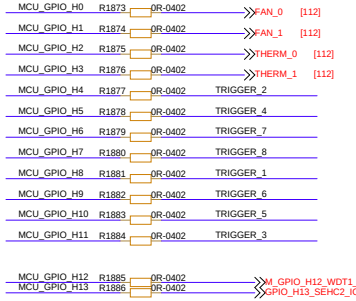
(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。











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Size C	Document Number <Doc>		Rev <RevCode>
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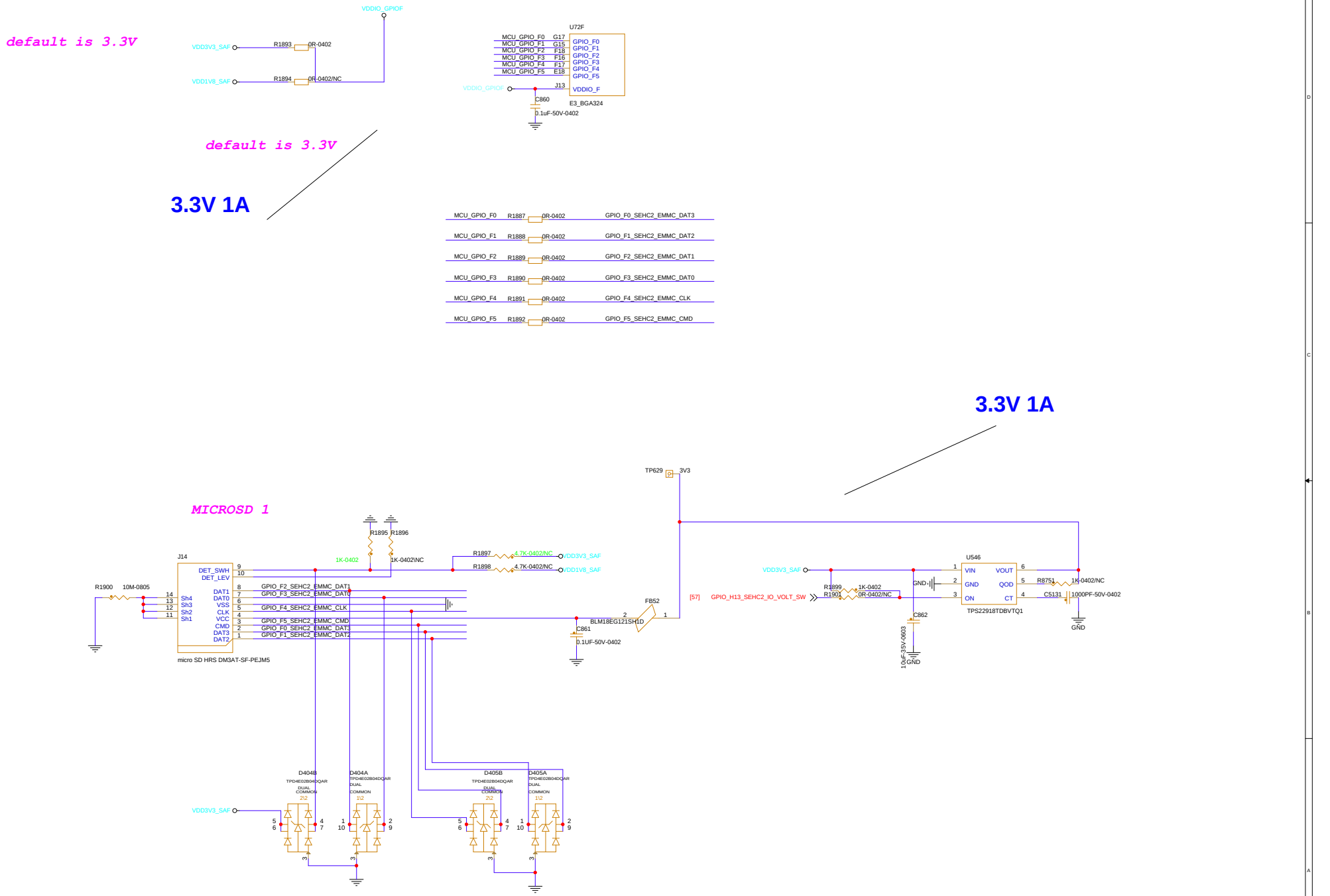

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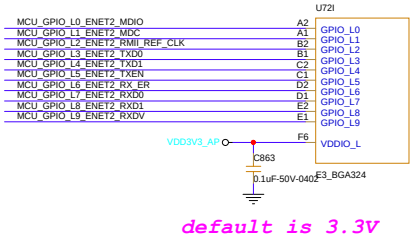
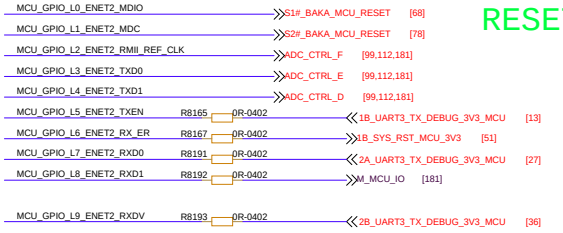


default is 3.3V

3.3V 1A



RESET TO S-MCU x2

UART16:MCU TO ORIN 1B DEBUG UART LOGGER
RESET TO ORIN x1
UART15:MCU TO ORIN 2A DEBUG UART LOGGER
UART14:MCU TO ORIN 2B DEBUG UART LOGGER

UART4:DEBUG
UART5:NMEA/PPS OUT
UART7:NMEA/PPS IN
UART10:SAFETY TO ORIN 2A
UART11:SAFETY TO ORIN 1A
UART9:SAFETY TO ORIN 2B
UART2:AP TO ORIN 1B
UART3 :M-MCU TO S1-MCU UART10
UART6 :M-MCU TO S2-MCU UART10
UART8 :M-MCU TO ORIN-1A DEBUG LOGGER
UART16:MCU TO ORIN 1B DEBUG UART LOGGER
UART15:MCU TO ORIN 2A DEBUG UART LOGGER
UART14:MCU TO ORIN 2B DEBUG UART LOGGER

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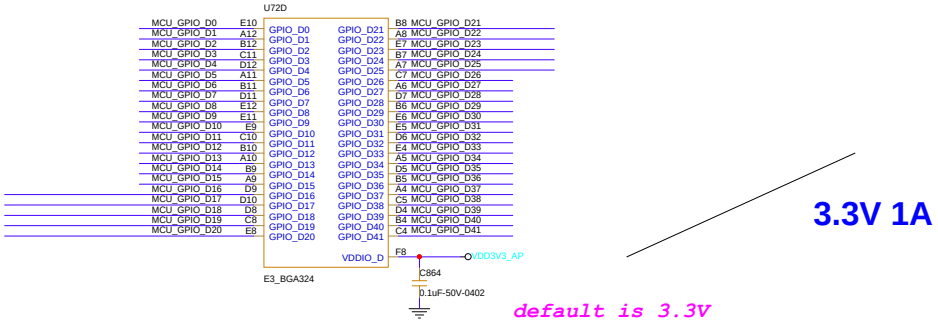

CANFD X21

MCU_GPIO_D0	R1797	0R-0402	CANFD1_RX	CANFD1_RX	[64]
MCU_GPIO_D1	R1798	0R-0402	CANFD1_TX	CANFD1_TX	[64]
MCU_GPIO_D2	R1800	0R-0402	CANFD2_RX	CANFD2_RX	[64]
MCU_GPIO_D3	R1804	0R-0402	CANFD2_TX	CANFD2_TX	[64]
MCU_GPIO_D4	R1805	0R-0402	CANFD3_RX	CANFD3_RX	[64]
MCU_GPIO_D5	R1806	0R-0402	CANFD3_TX	CANFD3_TX	[64]
MCU_GPIO_D6	R1811	0R-0402	CANFD4_RX	CANFD4_RX	[64]
MCU_GPIO_D7	R1812	0R-0402	CANFD4_TX	CANFD4_TX	[64]
MCU_GPIO_D8	R1813	0R-0402	CANFD5_RX	CANFD5_RX	[64]
MCU_GPIO_D9	R1814	0R-0402	CANFD5_TX	CANFD5_TX	[64]
MCU_GPIO_D10	R1817	0R-0402	CANFD6_RX	CANFD6_RX	[64]
MCU_GPIO_D11	R1820	0R-0402	CANFD6_TX	CANFD6_TX	[64]
MCU_GPIO_D12	R1825	0R-0402	CANFD7_RX	CANFD7_RX	[64]
MCU_GPIO_D13	R1826	0R-0402	CANFD7_TX	CANFD7_TX	[64]
MCU_GPIO_D14	R1827	0R-0402	CANFD8_RX	CANFD8_RX	[64]
MCU_GPIO_D15	R1828	0R-0402	CANFD8_TX	CANFD8_TX	[64]
MCU_GPIO_D16	R1831	0R-0402	CANFD9_RX	CANFD9_RX	[64]
MCU_GPIO_D17	R1832	0R-0402	CANFD9_TX	CANFD9_TX	[64]
MCU_GPIO_D18	R1833	0R-0402	CANFD10_RX	CANFD10_RX	[64]
MCU_GPIO_D19	R1834	0R-0402	CANFD10_TX	CANFD10_TX	[64]
MCU_GPIO_D20	R1835	0R-0402	CANFD11_RX	CANFD11_RX	[64]
MCU_GPIO_D21	R1836	0R-0402	CANFD11_TX	CANFD11_TX	[64]
MCU_GPIO_D22	R1837	0R-0402	CANFD12_RX	CANFD12_RX	[64]
MCU_GPIO_D23	R1838	0R-0402	CANFD12_TX	CANFD12_TX	[64]
MCU_GPIO_D24	R1839	0R-0402	CANFD13_RX	CANFD13_RX	[65]
MCU_GPIO_D25	R1840	0R-0402	CANFD13_TX	CANFD13_TX	[65]
MCU_GPIO_D26	R1841	0R-0402	CANFD14_RX	CANFD14_RX	[65]
MCU_GPIO_D27	R1842	0R-0402	CANFD14_TX	CANFD14_TX	[65]
MCU_GPIO_D28	R1843	0R-0402	CANFD15_RX	CANFD15_RX	[65]
MCU_GPIO_D29	R1844	0R-0402	CANFD15_TX	CANFD15_TX	[65]
MCU_GPIO_D30	R1845	0R-0402	CANFD16_RX	CANFD16_RX	[65]
MCU_GPIO_D31	R1846	0R-0402	CANFD16_TX	CANFD16_TX	[65]
MCU_GPIO_D32	R1849	0R-0402	CANFD17_RX	CANFD17_RX	[65]
MCU_GPIO_D33	R1850	0R-0402	CANFD17_TX	CANFD17_TX	[65]
MCU_GPIO_D34	R1851	0R-0402	CANFD18_RX	CANFD18_RX	[65]
MCU_GPIO_D35	R1852	0R-0402	CANFD18_TX	CANFD18_TX	[65]
MCU_GPIO_D36	R1853	0R-0402	CANFD19_RX	CANFD19_RX	[65]
MCU_GPIO_D37	R1854	0R-0402	CANFD19_TX	CANFD19_TX	[65]
MCU_GPIO_D38	R1855	0R-0402	CANFD20_RX	CANFD20_RX	[65]
MCU_GPIO_D39	R1856	0R-0402	CANFD20_TX	CANFD20_TX	[65]
MCU_GPIO_D40	R1857	0R-0402	CANFD21_RX	CANFD21_RX	[65]
MCU_GPIO_D41	R1858	0R-0402	CANFD21_TX	CANFD21_TX	[65]

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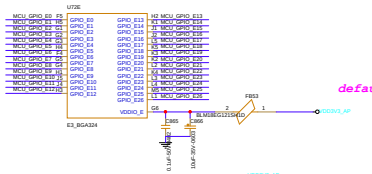
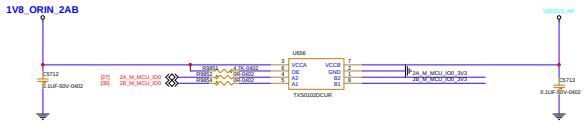
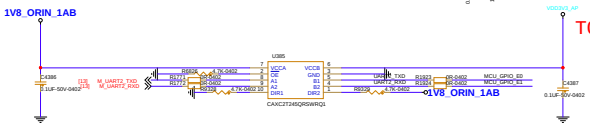


default is 3.3V

3.3V 1A



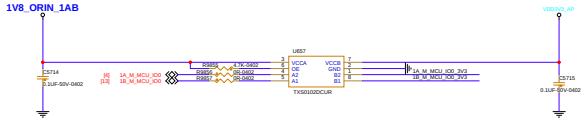


TO ORIN 1B

Table 2. Function Table
(Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
OE	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

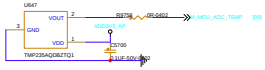


TO S1-MCU UART10

UART4 PPS/NMEA IN

UART4 DEBUG FOR 4232

AD1



M-MCU to 4个ORIN心跳(省掉)

UART4:PPS/NMEA IN
UART5:NMEA/PPS OUT
UART7:DEBUG UART
UART10:SAFETY TO ORIN 2A
UART11:SAFETY TO ORIN 1A
UART9:SAFETY TO ORIN 2B
UART2:AP TO ORIN 1B
UART3 :M-MCU TO S1-MCU UART10
UART6 :M-MCU TO S2-MCU UART10
UART8 :M-MCU TO ORIN-1A DEBUG LOGGER
UART16:MCU TO ORIN 1B DEBUG UART LOGGER
UART15:MCU TO ORIN 2A DEBUG UART LOGGER
UART14:MCU TO ORIN 2B DEBUG UART LOGGER

TO S2-MCU UART10

GPIO_E5	MUX0	GPIO_AP	IO57	Default
	MUX2	USB	OC	
	MUX4	SACI1	TXRXD3	
	MUX5	UART4	RXD	
	MUX6	SEHC2	EMMC_CMD	
GPIO_E6	MUX0	GPIO_AP	IO58	Default
	MUX2	SEHC1	LED_CTRL	
	MUX4	SACI1	TXRXD4	
	MUX5	UART4	CTSN	

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CustomerDoc>			<RevCode>
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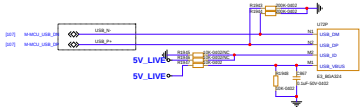

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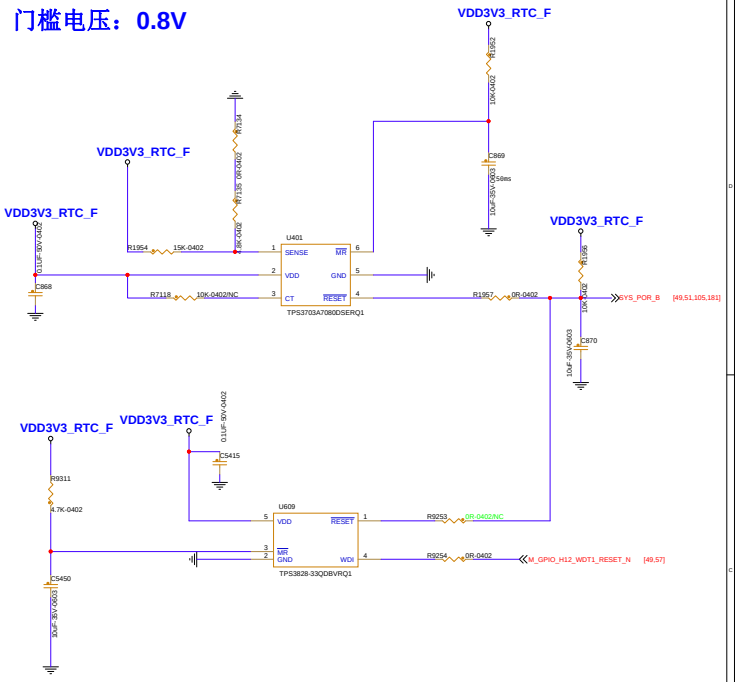
门槛电压：0.8V



监控电压Vit-:2.88V

Td:delay time 200ms

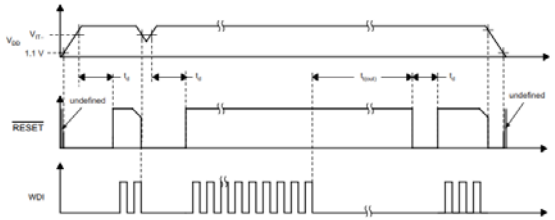


Figure 1. Delay and Time Out Timing Diagram

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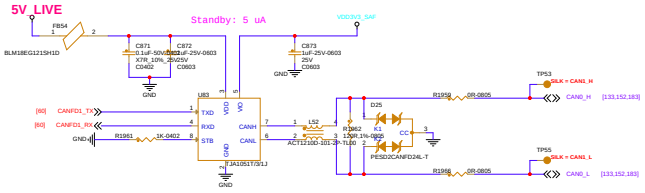
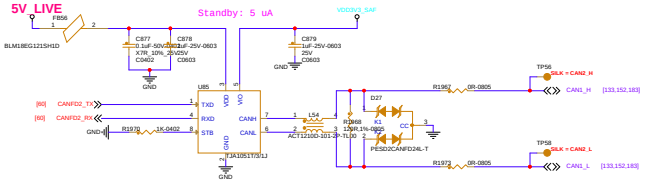
CAN #1



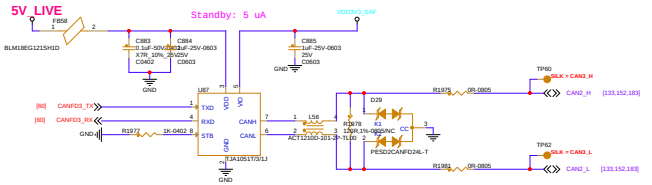
所有CAN总线LAYOUT差分处理

CAN #2

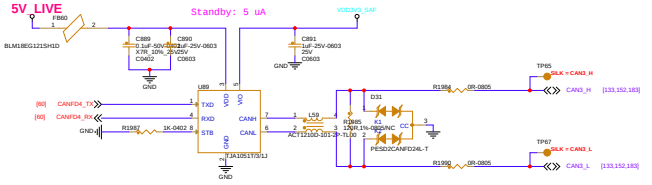


5V:0.5A 3.3V:0.5A

CAN #3



CAN #4



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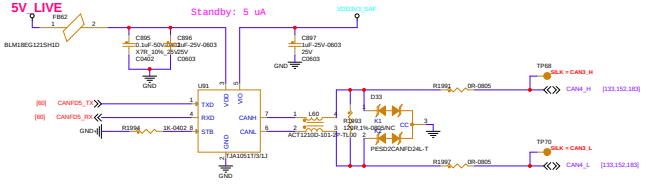
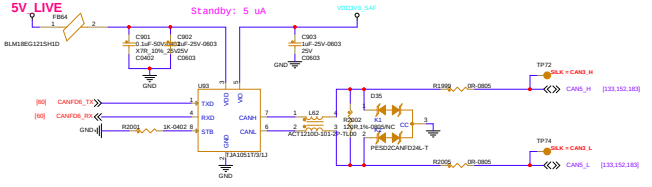


CAN #1-12 SAFETY

CAN #6



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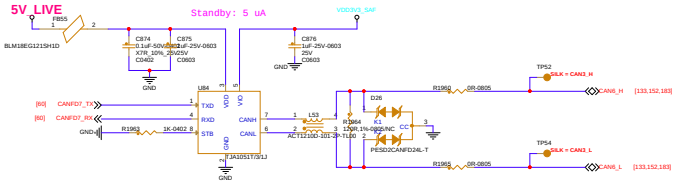
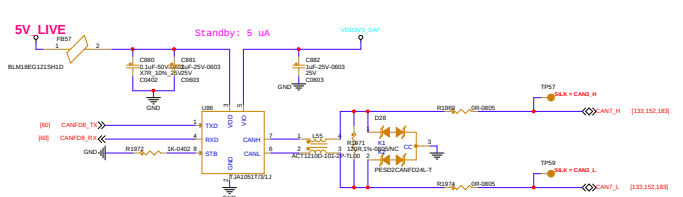
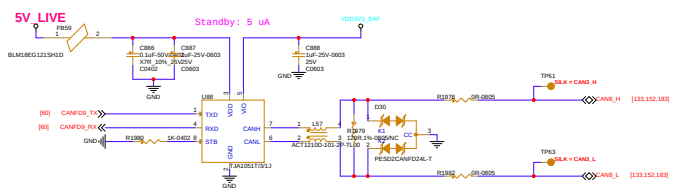


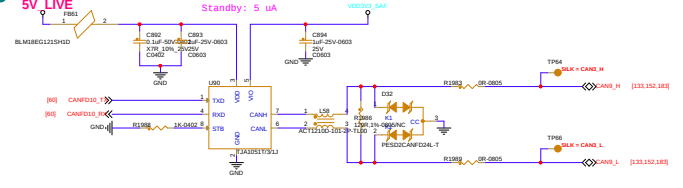
CAN #8



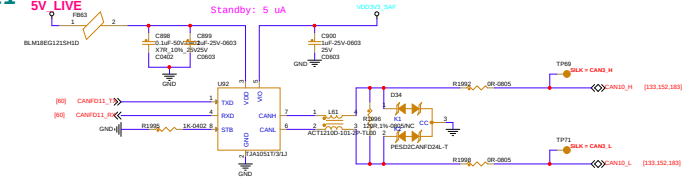
CAN #9



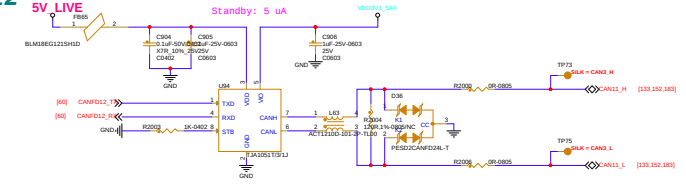
CAN #10



CAN #11



CAN #12



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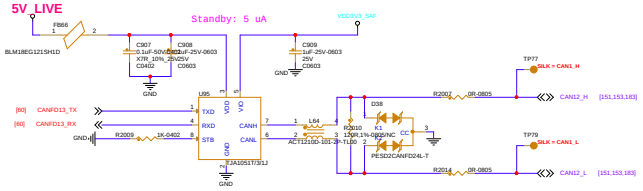

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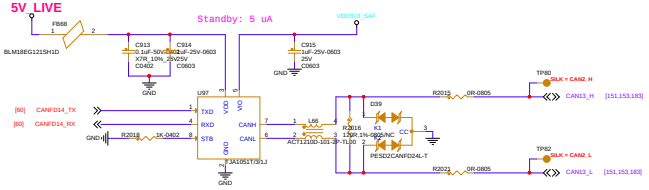

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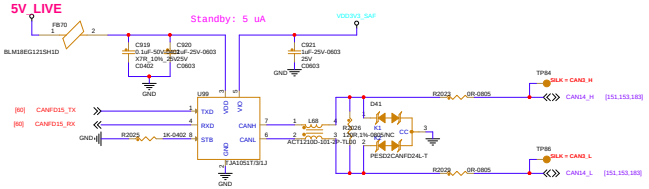

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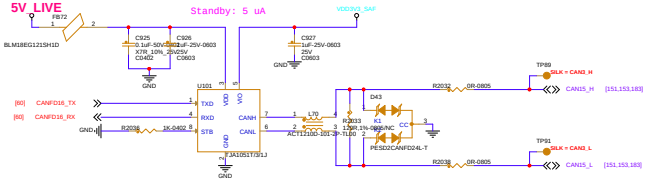

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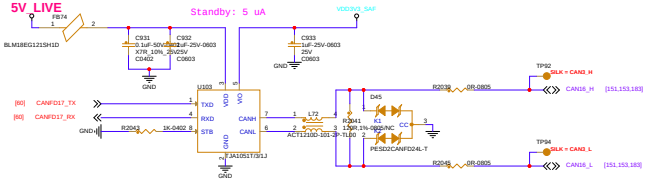

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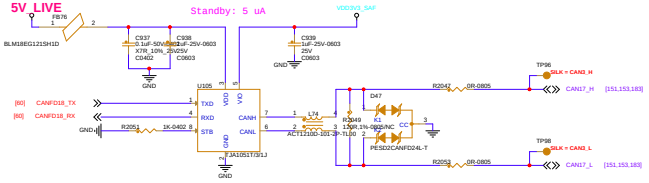

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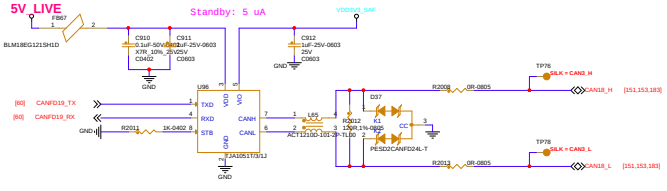
CAN #13-22 SAFETY

CAN #19



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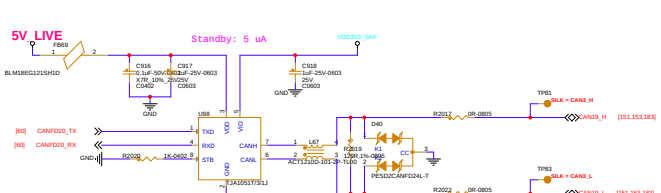

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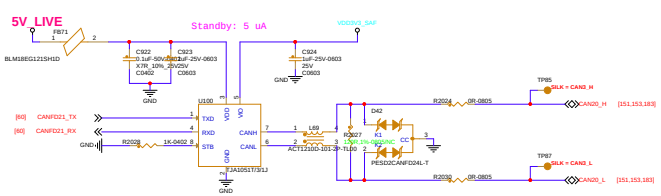

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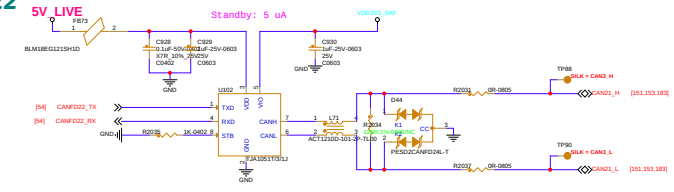

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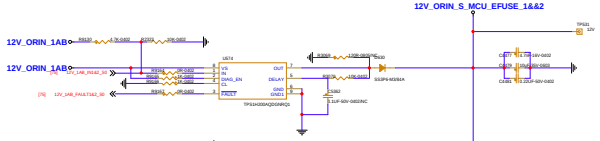
S0-MCU处理

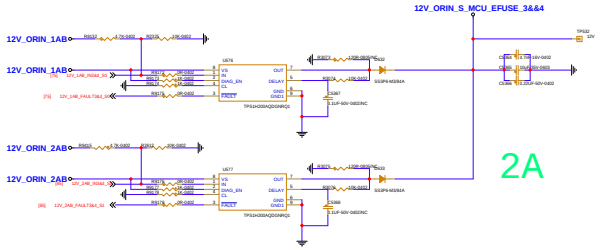
S1-MCU处理



2A

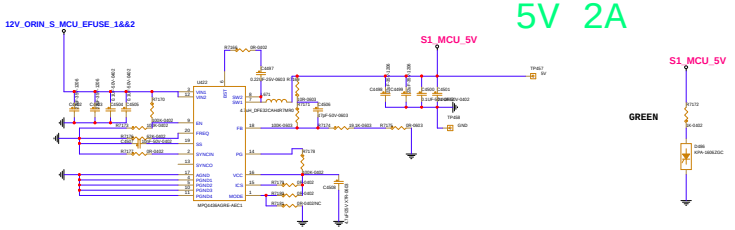
S0-MCU处理

S1-MCU处理

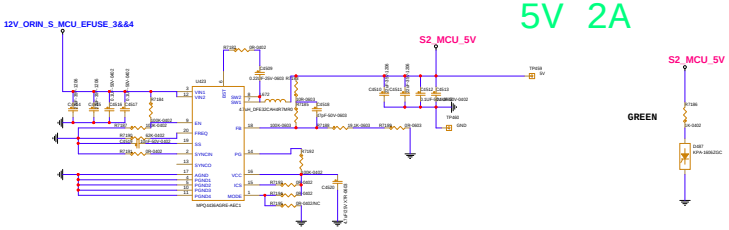


2A

5V 2A



5V 2A



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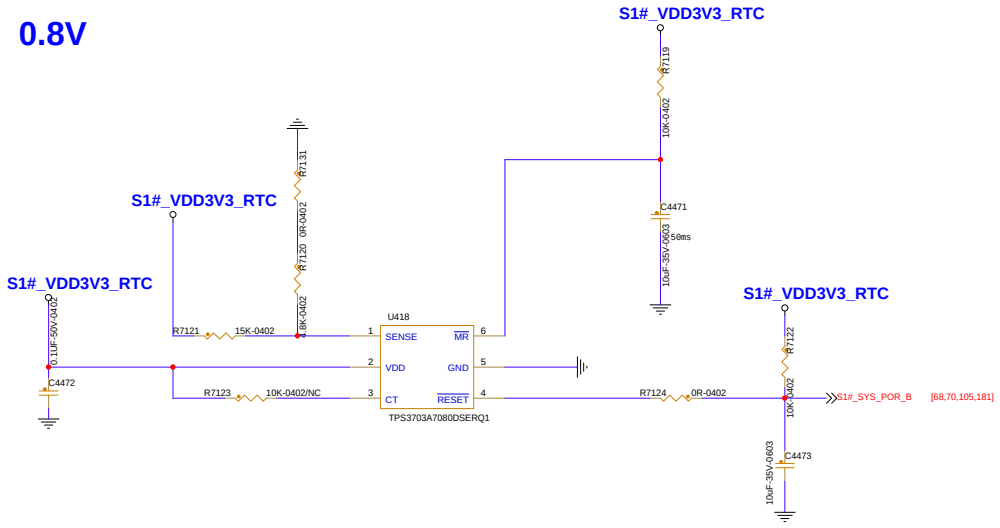
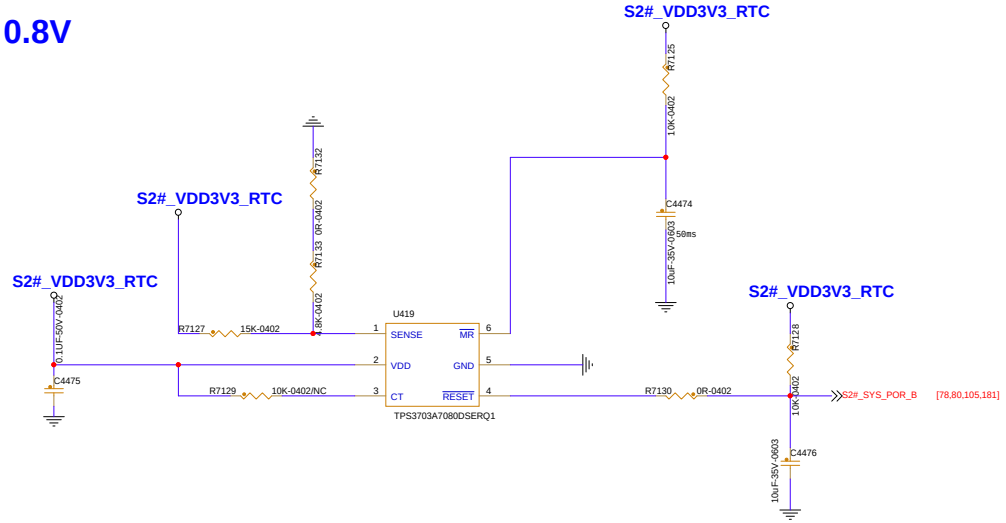


门槛电压：0.8V



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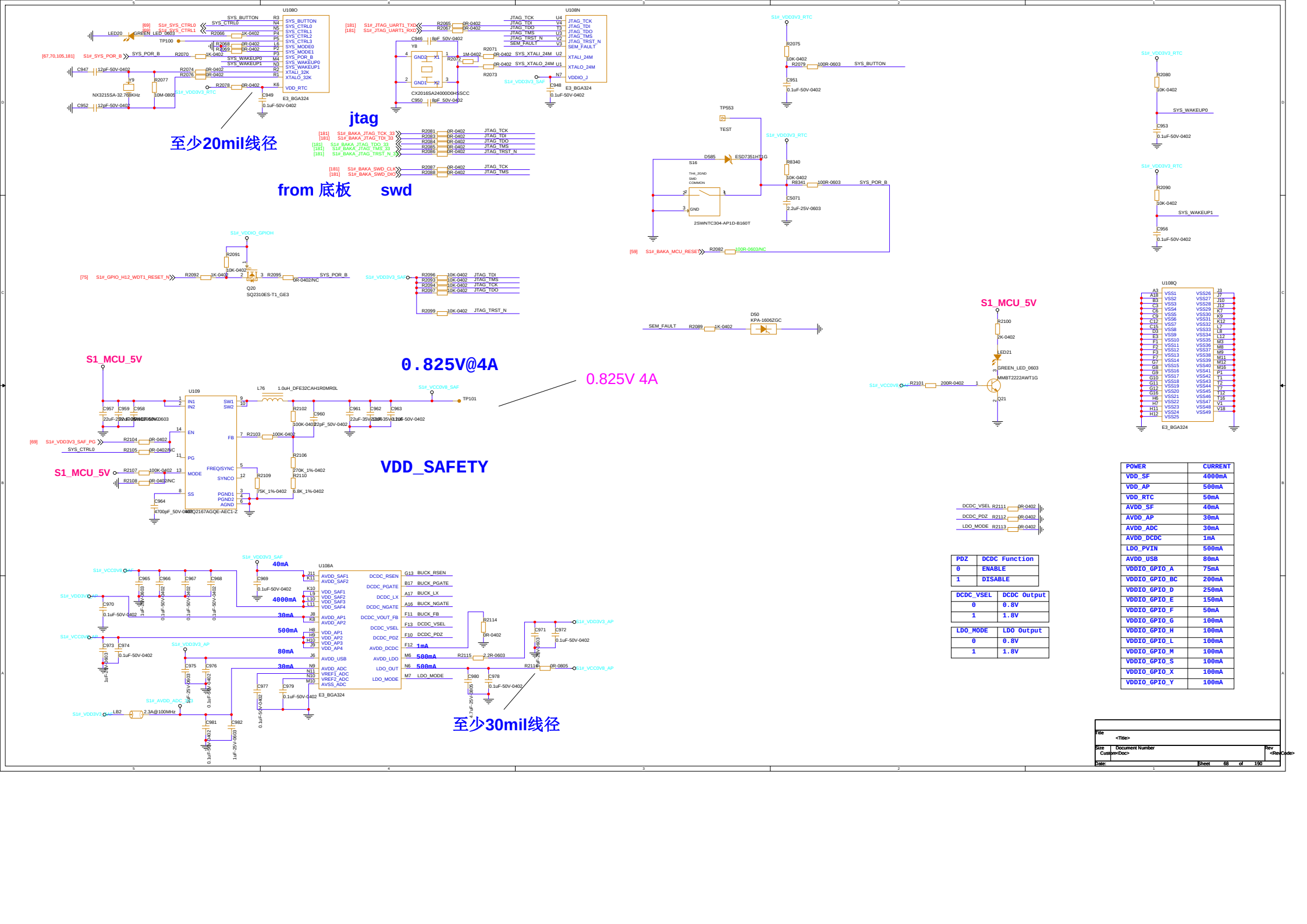

POWER	CURRENT
VDD_SF	4000mA
VDD_AP	500mA
VDD_RTC	50mA
AVDD_SF	40mA
AVDD_AP	30mA
AVDD_ADC	30mA
AVDD_DCDC	1mA
LDO_PVIN	500mA
AVDD_USB	80mA
VDDIO_GPIO_A	75mA
VDDIO_GPIO_BC	200mA
VDDIO_GPIO_D	250mA
VDDIO_GPIO_E	150mA
VDDIO_GPIO_F	50mA
VDDIO_GPIO_G	100mA
VDDIO_GPIO_H	100mA
VDDIO_GPIO_L	100mA
VDDIO_GPIO_M	100mA
VDDIO_GPIO_S	100mA
VDDIO_GPIO_X	100mA
VDDIO_GPIO_Y	100mA

PDZ	DCDC Function
0	ENABLE
1	DISABLE

DCDC_VSEL	DCDC Output
0	0.8V
1	1.8V

LDO_MODE	LDO Output
0	0.8V
1	1.8V

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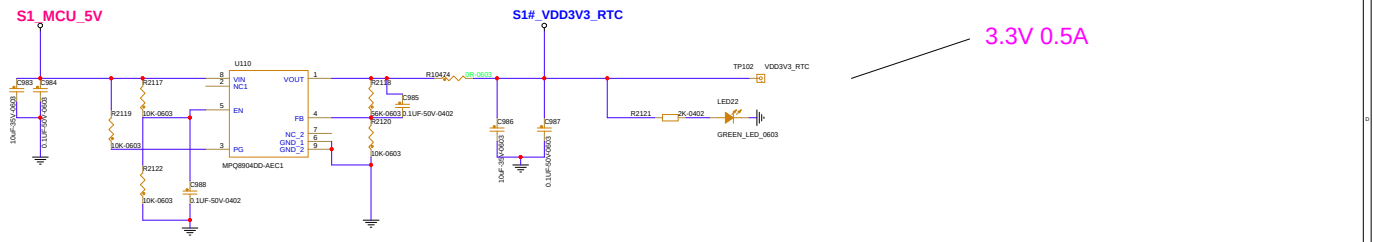
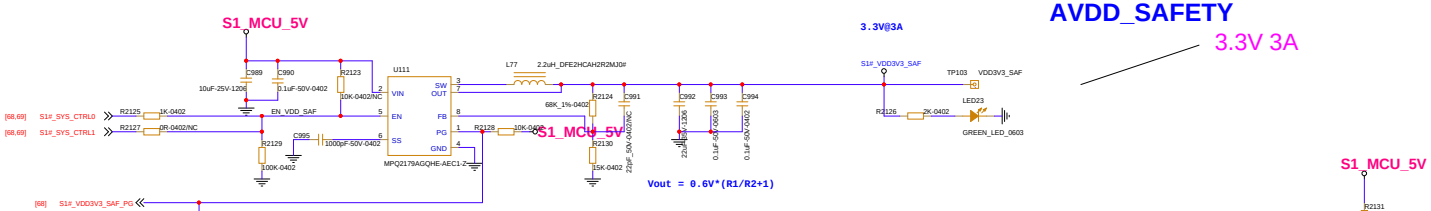
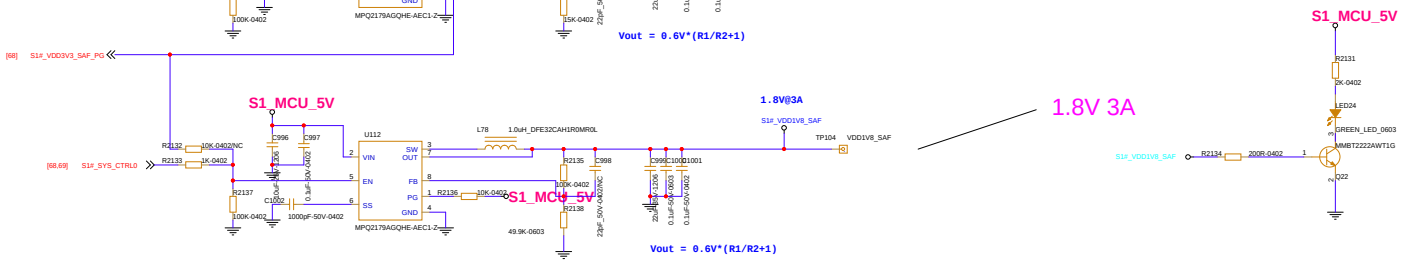
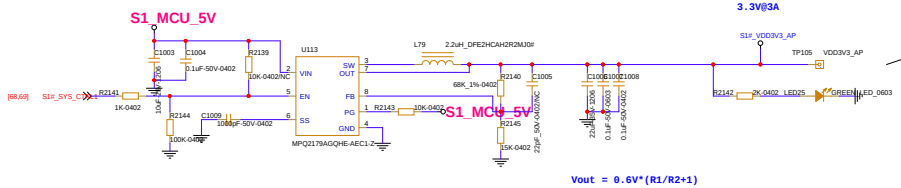
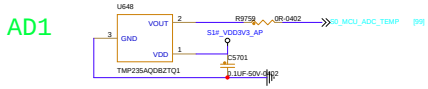


AVDD_SAFETY









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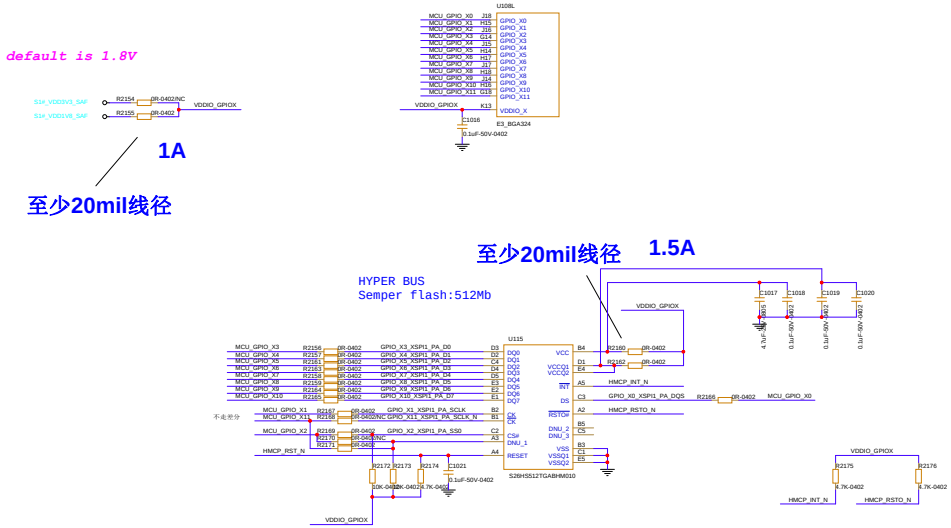
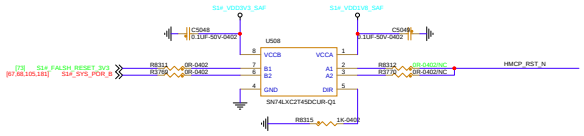


Deault:S76HS512TC0BHB010 1.8V

S76HS512TC0BHB010 1.8V
S76HL512TC0BHB010 3.3V

MT35XU256ABA1G12-0AUT 1.8V

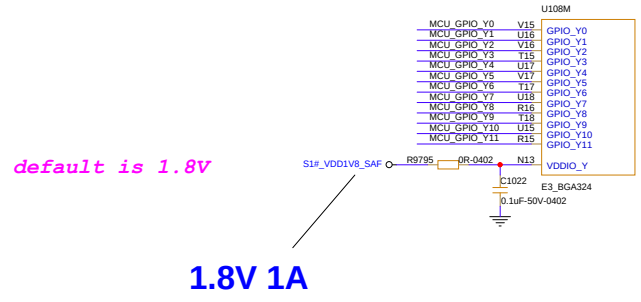


8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。



default is 1.8V

1.8V 1A

UART7 DEBUG FOR 4232

UART7
DEBUG UART

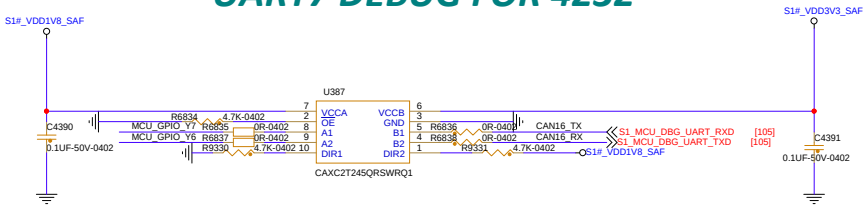
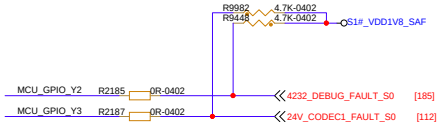
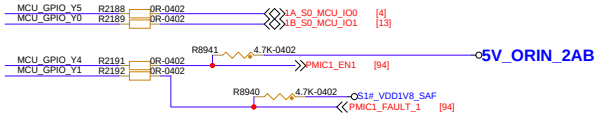


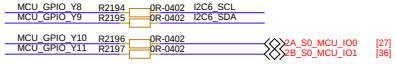
Table 2. Function Table (Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

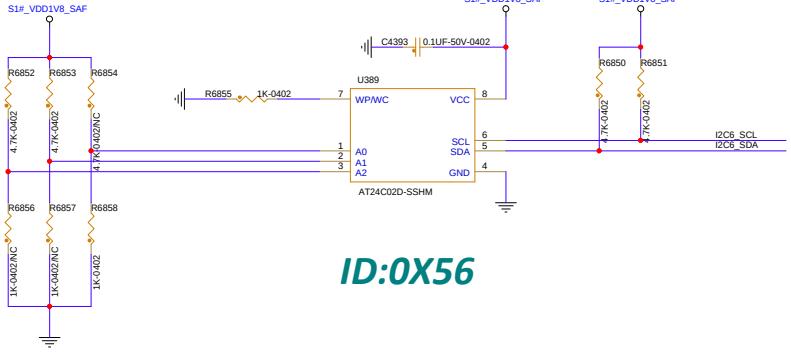
(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.







1.8V 1A



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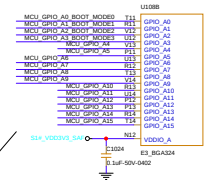
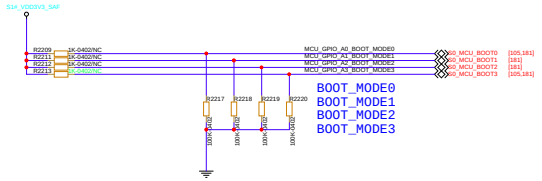


default is 3.3V

3.3V 1A

default mode is FLASH BOOT



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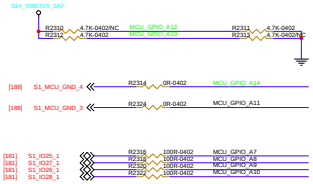

Table 6.1: Boot Mode

Boot Mode	Description	Notes
1110	User JTAG Mode	In this mode,Boot ROM lockout Semidrive confidential information then configure core into ARM mode, disable MPU then enable JTAG. This mode available on Development mode only
0000	XSPI1 NOR/Hyper Flash	-
0001	XSPI1 NAND Flash	-
0010	eMMC1	-
0011	SD1	-
0100	SD2	-
0101	XSPI Slave Port	Boot from XSPI slave interface
1000	USB Boot	-

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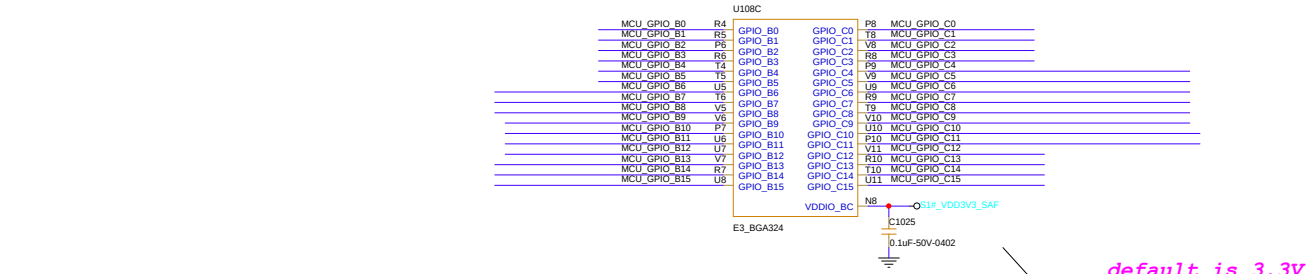
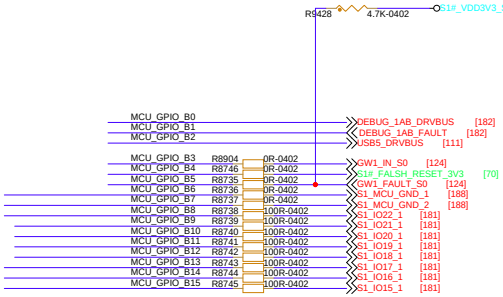
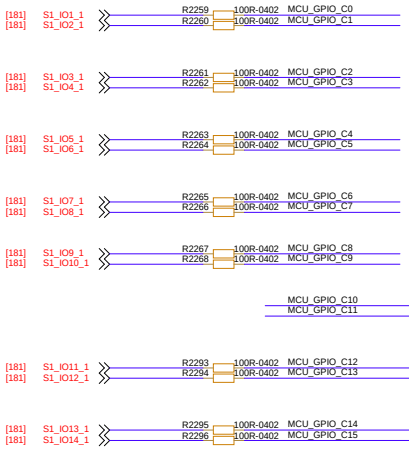
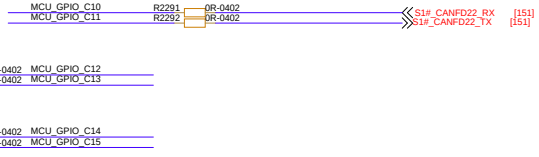


default is 3.3V

3.3V 1A







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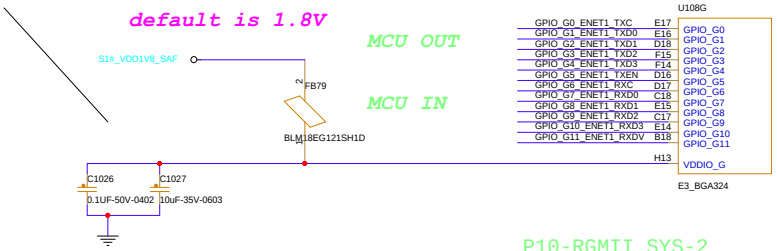
1.8V 1A



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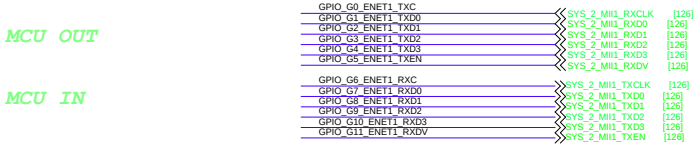
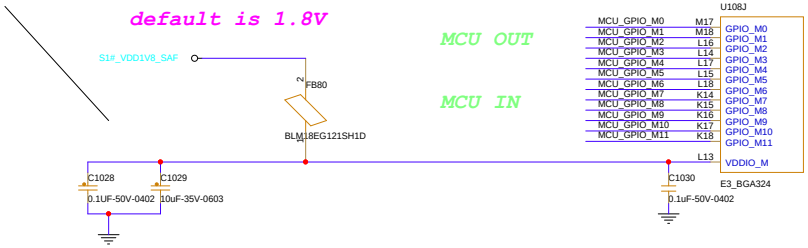


89586 IN

89586 OUT

1.8V 1A



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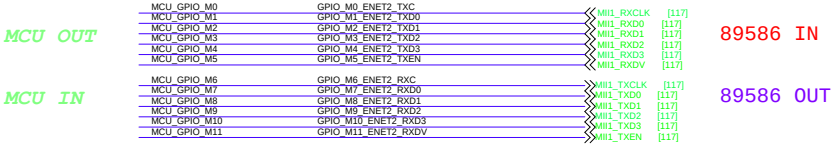

89586 IN

89586 OUT

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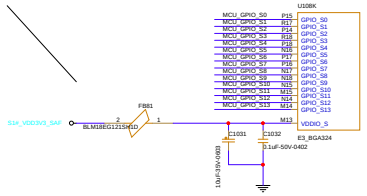
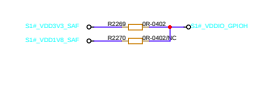
3.3V 1A

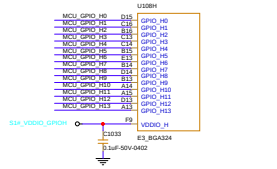
default is 3.3V



3.3V 1A

default is 1.8V



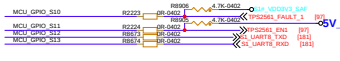


3.3V TTL uart11 txd / uart11 rxd — 485

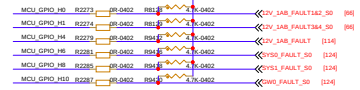
3.3V TTL uart10 txd / uart10 rxd — TO M-MCU

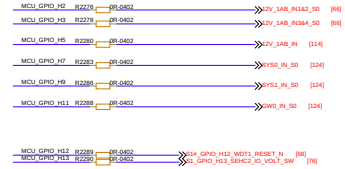
3.3V TTL uart9 txd / uart9 rxd — 485

3.3V TTL uart8 txd / uart8 rxd — TO IO CON



5V_ORIN_1AB





UART4:NMEA/PPS IN
UART7:DEBUG
UART10:TO M-MCU UART3

UART11:485
UART9:485

UART3 :485
UART6 :485
UART2: TO IO CON
UART8: TO IO CON

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Size D	Document Number <Doc>		Rev <RevCode>
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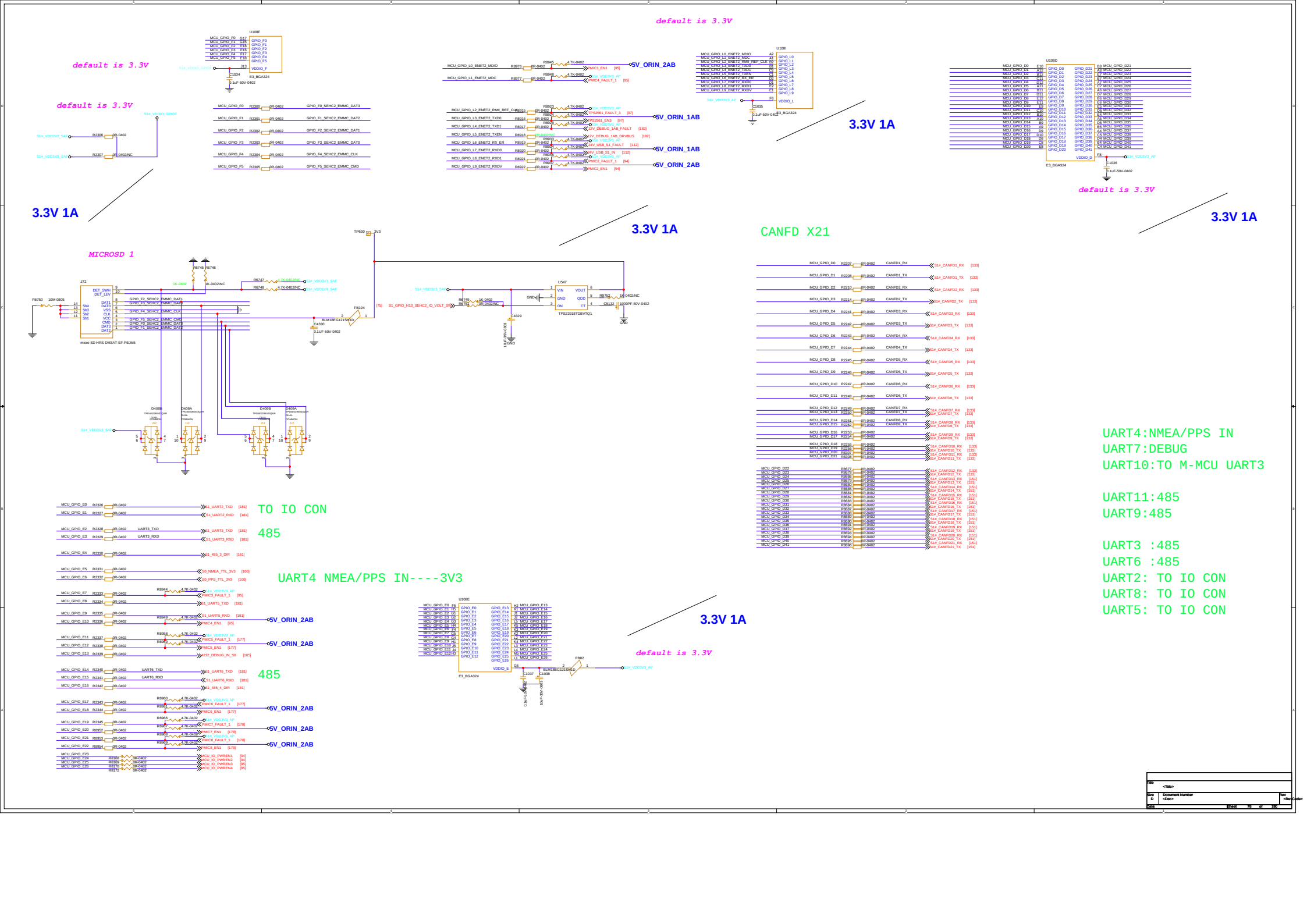
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3.3V 1A
3.3V 1A
3.3V 1A
3.3V 1A
3.3V 1A
MICROSD 1
micro SD HRS DM3AT-SF-PEJM5
CANFD X21
TO IO CON
485
UART4 NMEA/PPS IN----3V3
485
UART4:NMEA/PPS IN
UART7:DEBUG
UART10:TO M-MCU UART3
UART11:485
UART9:485
UART3 :485
UART6 :485
UART2: TO IO CON
UART8: TO IO CON
UART5: TO IO CON
5V_ORIN_2AB
5V_ORIN_1AB
5V_ORIN_1AB
5V_ORIN_2AB
5V_ORIN_2AB
5V_ORIN_2AB
5V_ORIN_2AB
5V_ORIN_2AB
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Document Number
<Doc>
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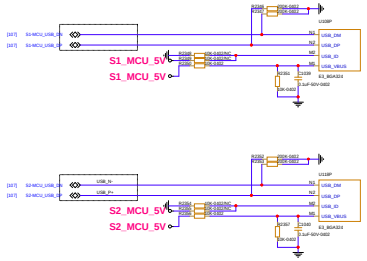
<RevCode>
Date:
Sheet 76 of 190



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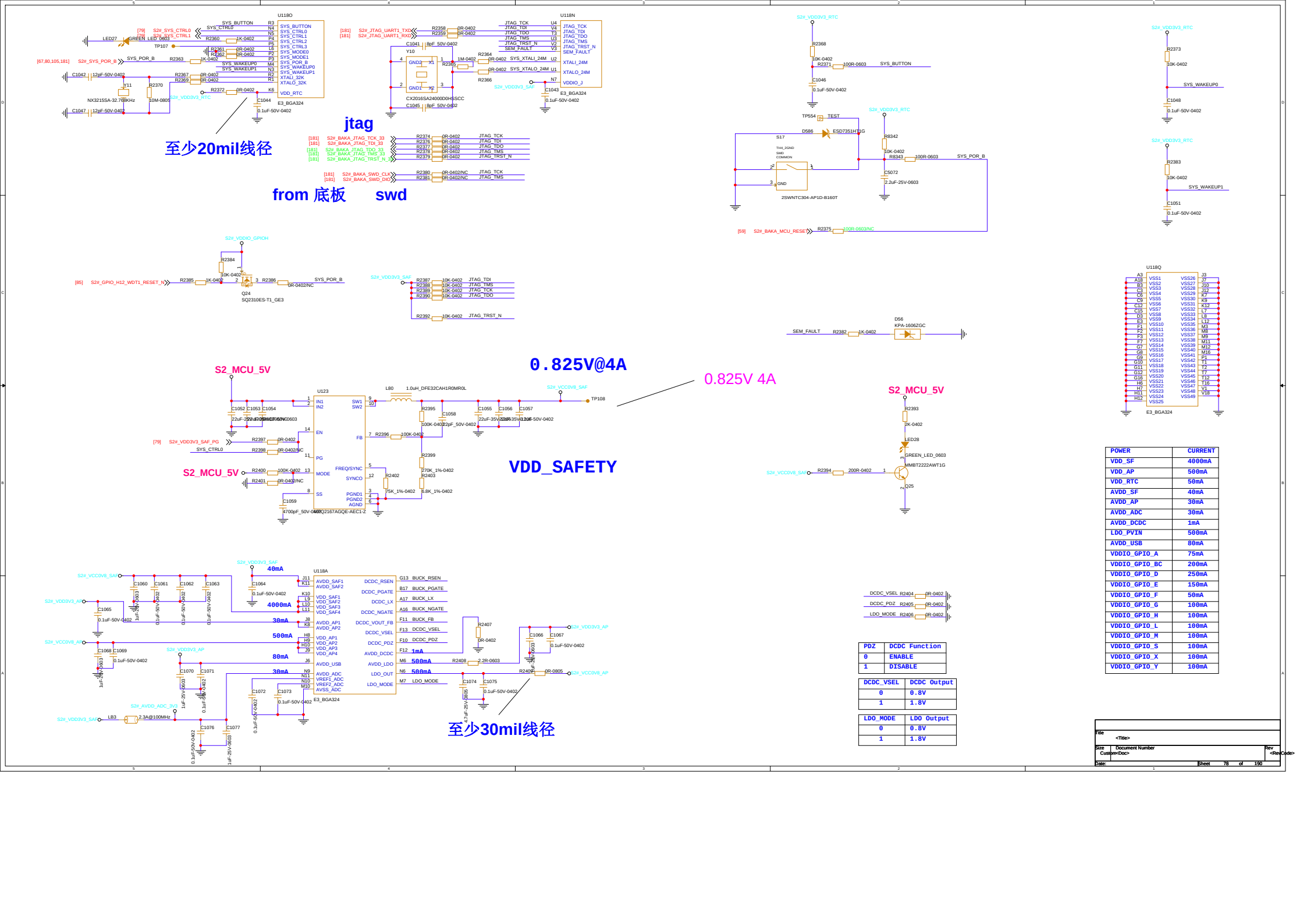

POWER	CURRENT
VDD_SF	4000mA
VDD_AP	500mA
VDD_RTC	50mA
AVDD_SF	40mA
AVDD_AP	30mA
AVDD_ADC	30mA
AVDD_DCDC	1mA
LDO_PVIN	500mA
AVDD_USB	80mA
VDDIO_GPIO_A	75mA
VDDIO_GPIO_BC	200mA
VDDIO_GPIO_D	250mA
VDDIO_GPIO_E	150mA
VDDIO_GPIO_F	50mA
VDDIO_GPIO_G	100mA
VDDIO_GPIO_H	100mA
VDDIO_GPIO_L	100mA
VDDIO_GPIO_M	100mA
VDDIO_GPIO_S	100mA
VDDIO_GPIO_X	100mA
VDDIO_GPIO_Y	100mA

PDZ	DCDC Function
0	ENABLE
1	DISABLE

DCDC_VSEL	DCDC Output
0	0.8V
1	1.8V

LDO_MODE	LDO Output
0	0.8V
1	1.8V

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Rev	<RevCode>
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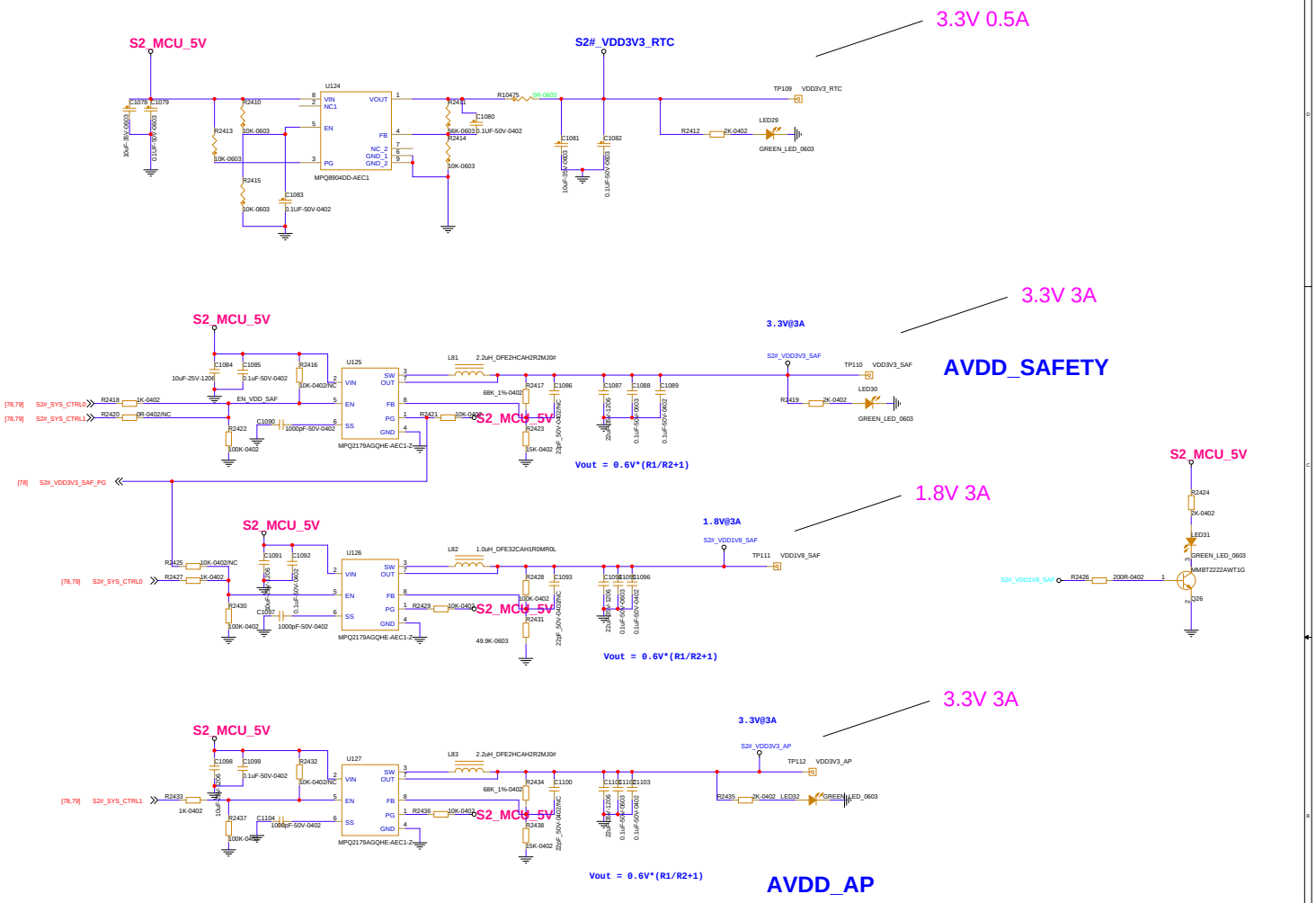

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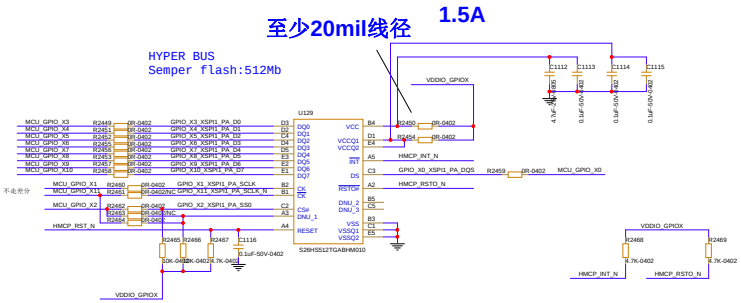
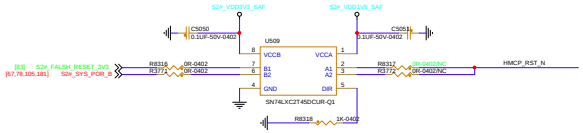


Deault:S76HS512TC0BHB010 1.8V

S76HS512TC0BHB010 1.8V
S76HL512TC0BHB010 3.3V

MT35XU256ABA1G12-0AUT 1.8V



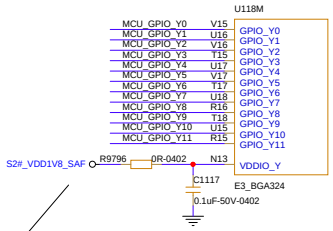
8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

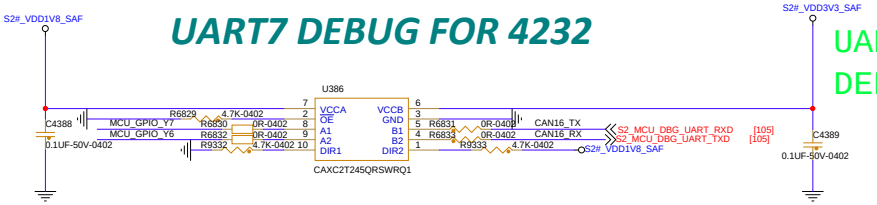
(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

default is 1.8V



1.8V 1A

UART7 DEBUG FOR 4232

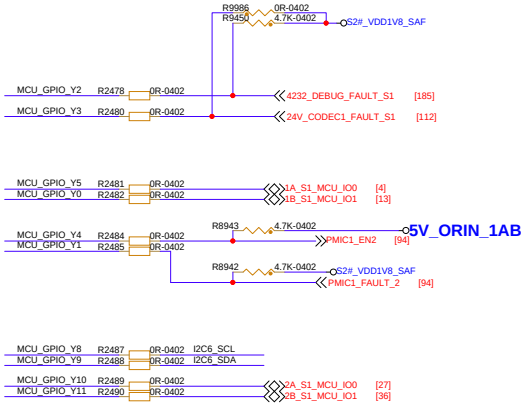


UART7
DEBUG UART

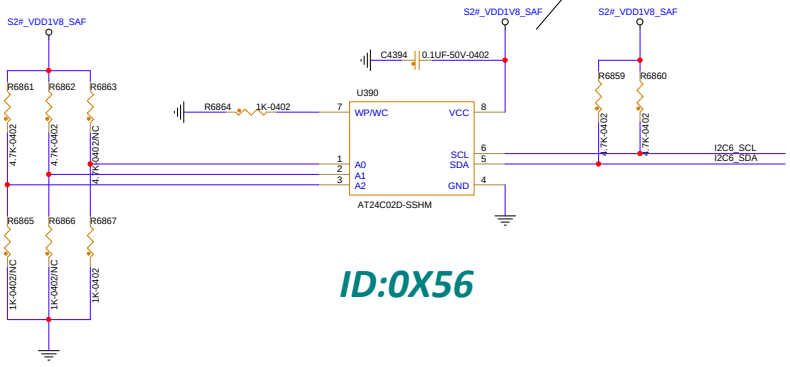
Table 2. Function Table (Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.



1.8V 1A



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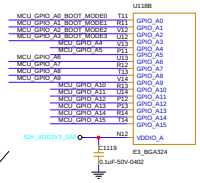


default is 3.3V

3.3V 1A

default mode is FLASH BOOT

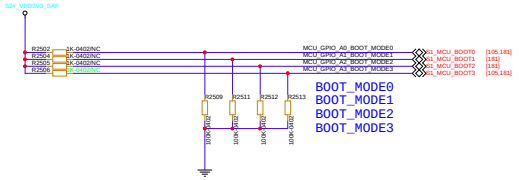
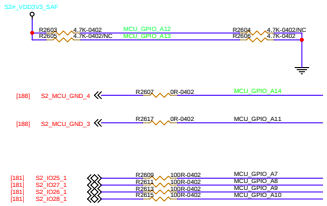


Table 6.1: Boot Mode

Boot Mode	Description	Notes
1110	User JTAG Mode	In this mode,Boot ROM lockout Semidrive confidential information then configure core into ARM mode, disable MPU then enable JTAG. This mode available on Development mode only
0000	XSPI1 NOR/Hyper Flash	-
0001	XSPI1 NAND Flash	-
0010	eMMC1	-
0011	SD1	-
0100	SD2	-
0101	XSPI Slave Port	Boot from XSPI slave interface
1000	USB Boot	-

MCU ID:0X01



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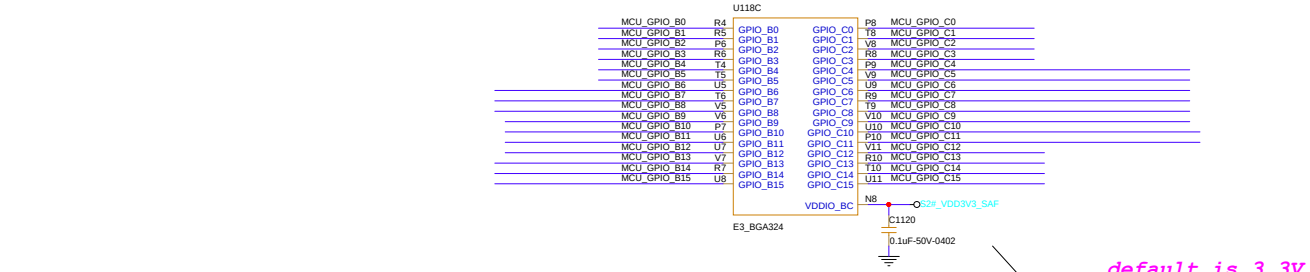
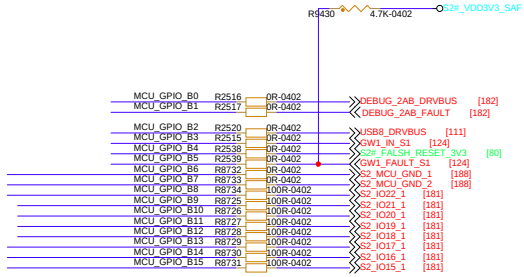
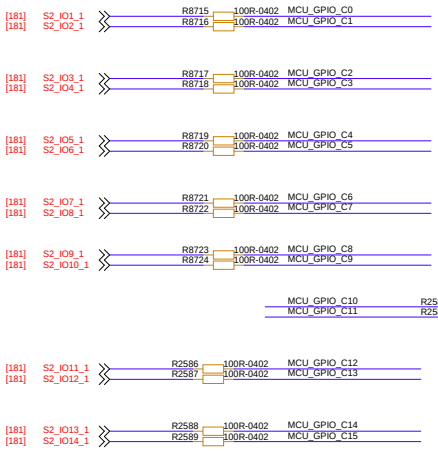
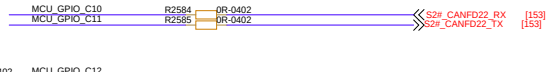


default is 3.3V

3.3V 1A







CANFD 22

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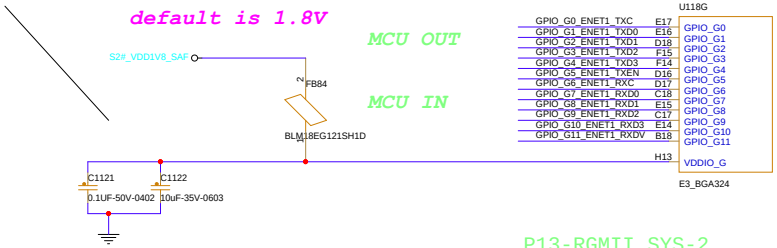
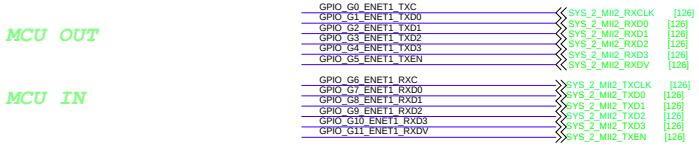
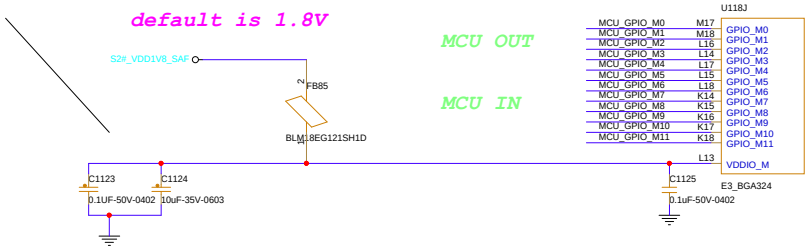
1.8V 1A



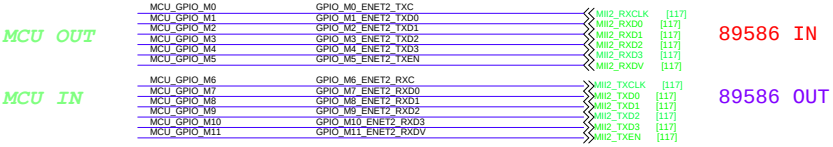
P13-RGMII SYS-2



1.8V 1A



P13-RGMII SYS-1



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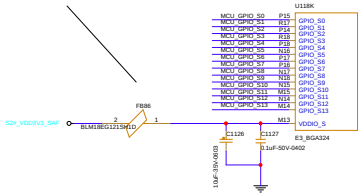
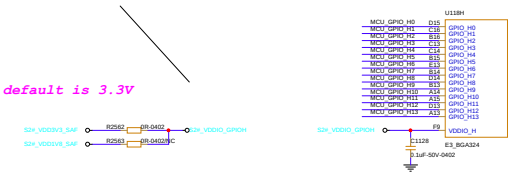
3.3V 1A

default is 3.3V



3.3V 1A

default is 3.3V



3.3V TTL uart11 txd / uart11 rxd

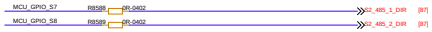
485

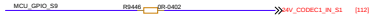
3.3V TTL uart10 txd / uart10 rxd

TO M-MCU

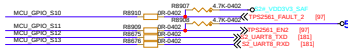
3.3V TTL uart9 txd / uart9 rxd

485

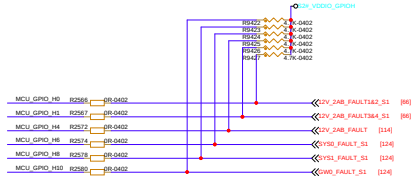


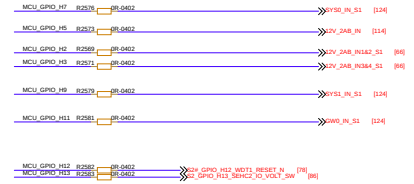


3.3V TTL uart8 txd / uart8 rxd



TO IO CON





UART4:NMEA/PPS IN
UART7:DEBUG
UART10:TO M-MCU UART3

UART11:485
UART9:485

UART3 :485
UART6 :485
UART2: TO IO CON
UART8: TO IO CON

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default is 3.3V

default is 3.3V

挂1个9010AA+1个9000BF

default is 3.3V

3.3V 1A

3.3V 1A

3.3V 1A

3.3V 1A

MICROSD 1

micro SD HRS DM3AT-SF-PEJM5

CANFD X21

TO IO CON

485

UART4 NMEA/PPS IN----3V3

485

default is 3.3V

UART4:NMEA/PPS IN
UART7:DEBUG
UART10:TO M-MCU UART3

UART11:485
UART9:485

UART3 :TO IO CON
UART6 :TO IO CON
UART2: TO IO CON
UART8: TO IO CON
UART5: TO IO CON

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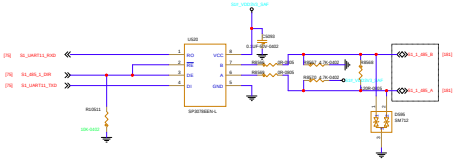
S1/S2 485 x2

3.3V:0.5A

485



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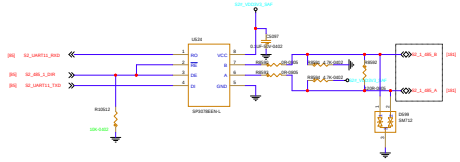
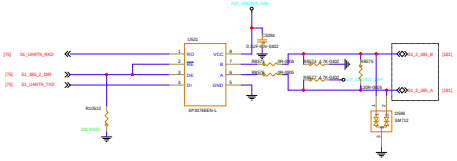


内置IMU485

485



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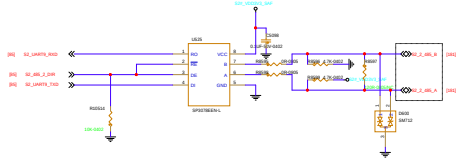
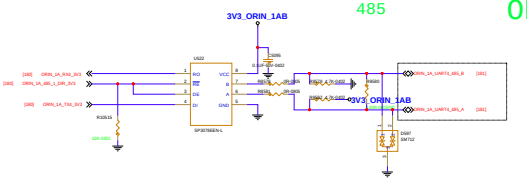


外置IMU485

每个ORIN有2uart 每个MCU有2个uart

ORIN x4 485 x2

485



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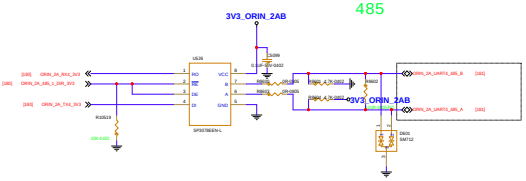

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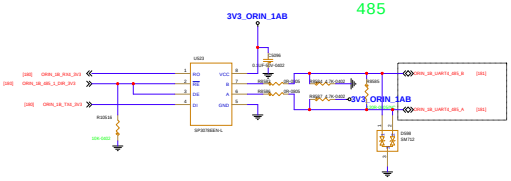

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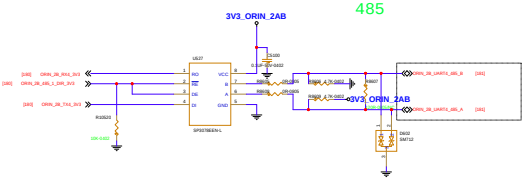

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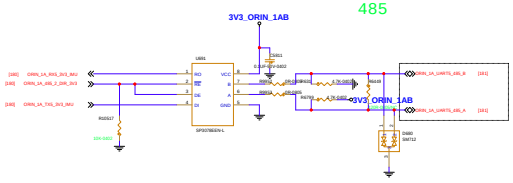

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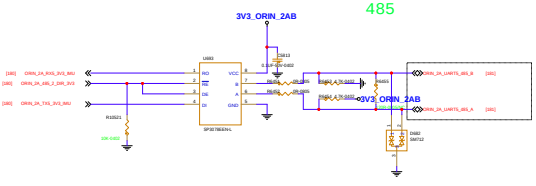

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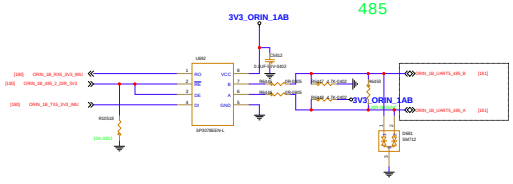

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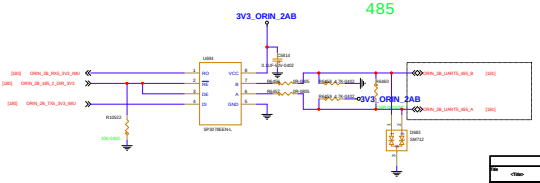
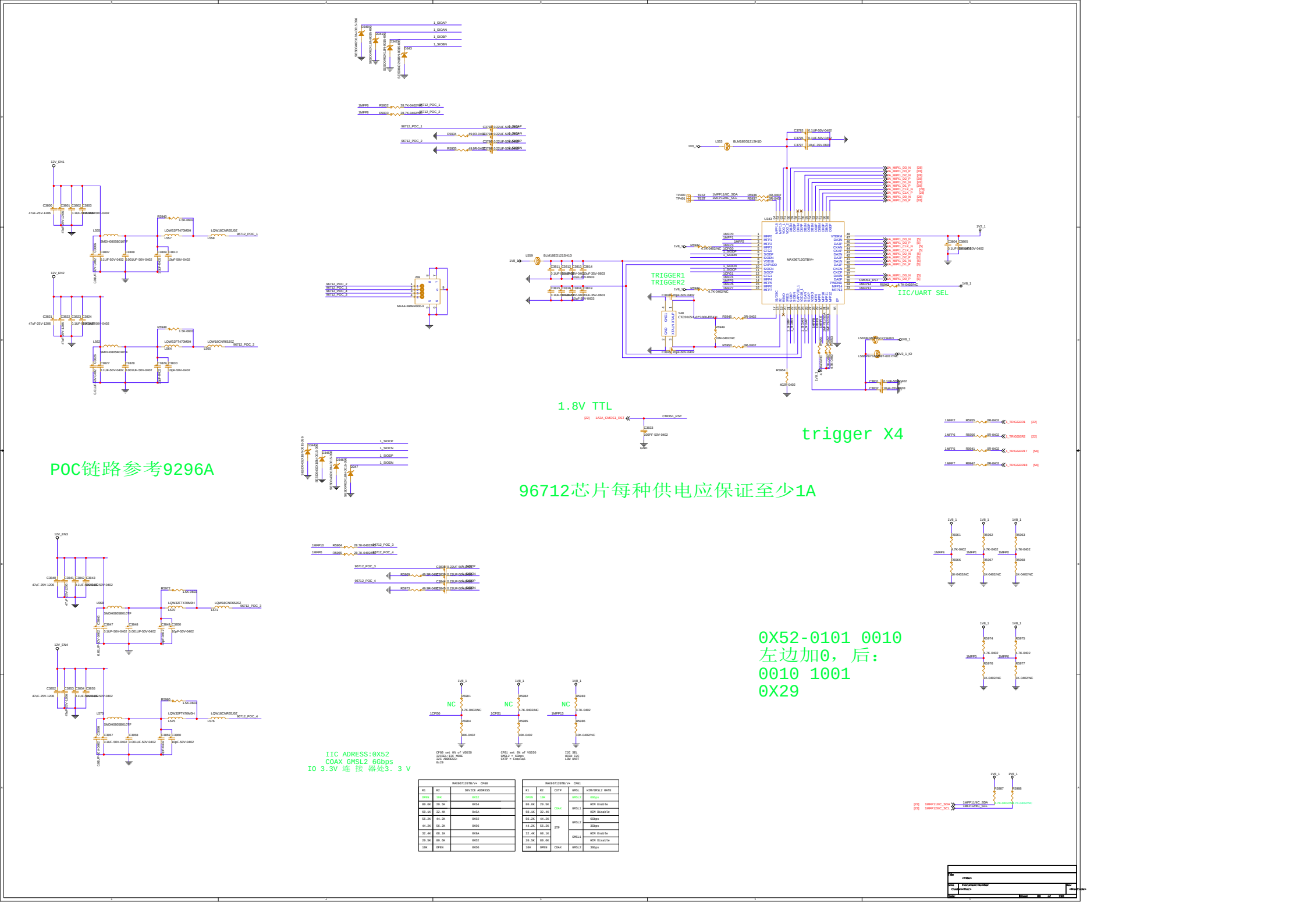
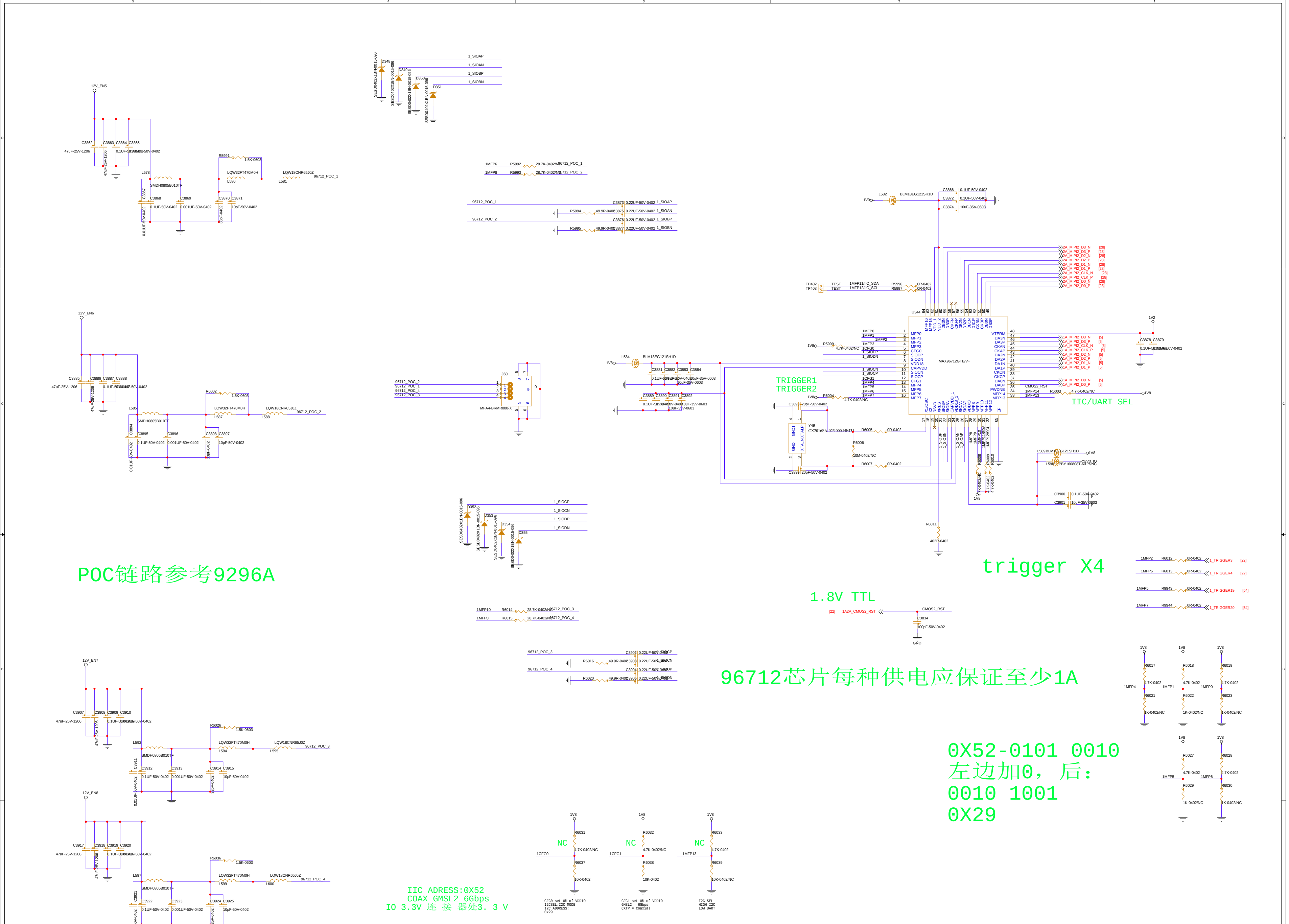



POC链路参考9296A
96712芯片每种供电应保证至少1A
1.8V TTL
trigger X4
TRIGGER1
TRIGGER2
IIC/UART SEL
0X52-0101 0010
左边加0，后：
0010 1001
0X29
IIC ADRESS:0X52
COAX GMSL2 6Gbps
IO 3.3V 连 接 器处3. 3 V
MAX96712GTB/V+
CFG0
CFG1



MAX96712GTB/V+ CFG0		
R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0x5A
56.2K	44.2K	0X92
44.2K	56.2K	0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

MAX96712GTB/V+ CFG1				
R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HIM Enable
68.1K	32.4K			HIM Disable
56.2K	44.2K	STP	GMSL2	6Gbps
44.2K	56.2K			3Gbps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K			HIM Disable
10K	OPEN	COAX	GMSL2	3Gbps

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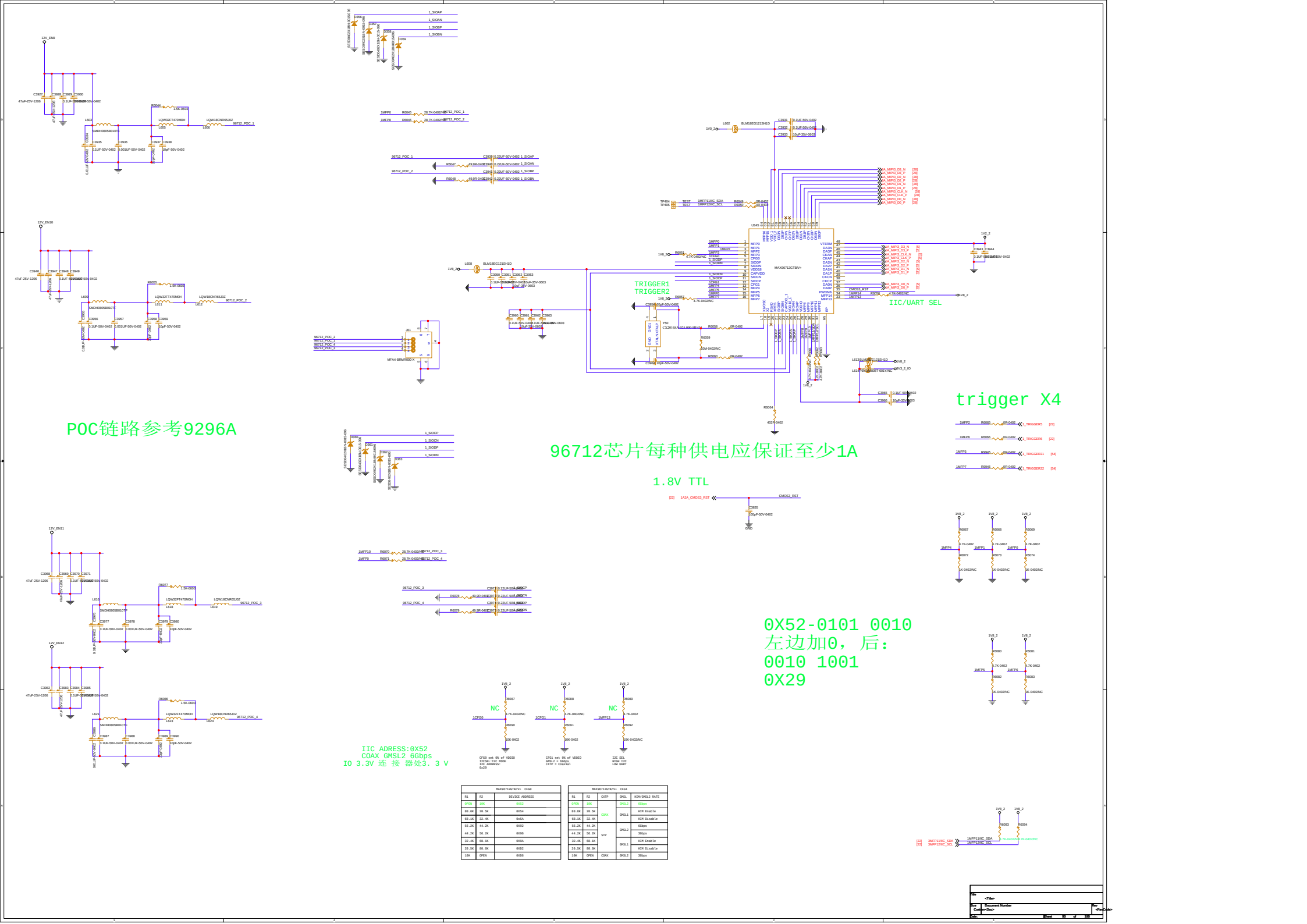
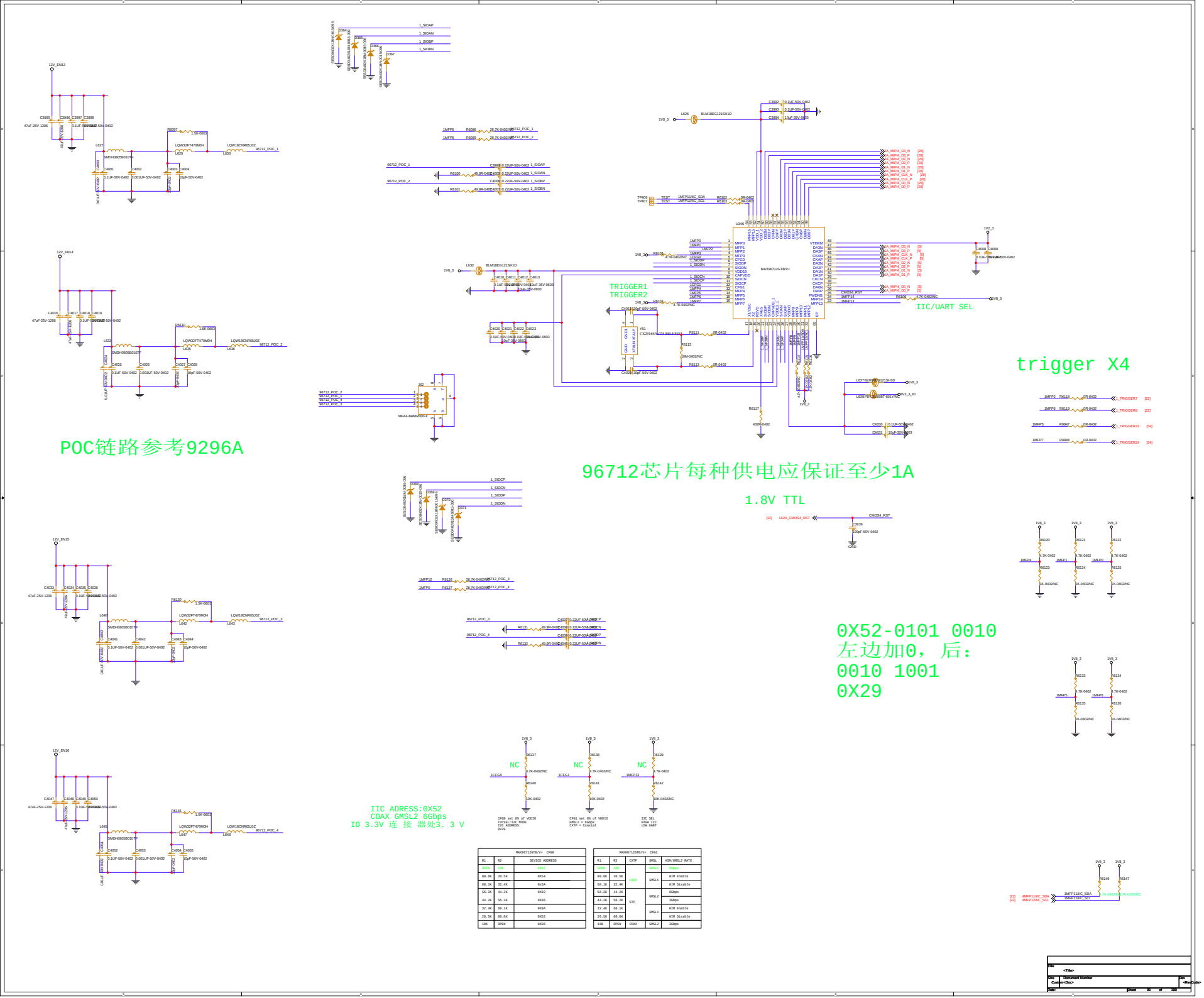
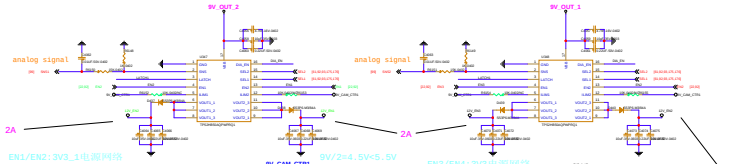
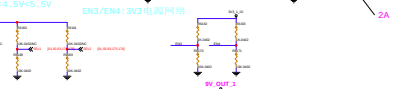


MAX96712GTB/V+ CFG0		
R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0X5A
56.2K 44.2K	44.2K 56.2K	0X92 0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

MAX96712GTB/V+ CFG1				
R1	R2	CXTP	GMSL	HDM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HDM Enable
68.1K	32.4K			HDM Disable
56.2K 44.2K	44.2K 56.2K	STP	GMSL2	6Gbps 3Gbps
32.4K	68.1K		GMSL1	HDM Enable
20.5K	80.6K			HDM Disable
10K	OPEN	COAX	GMSL2	3Gbps

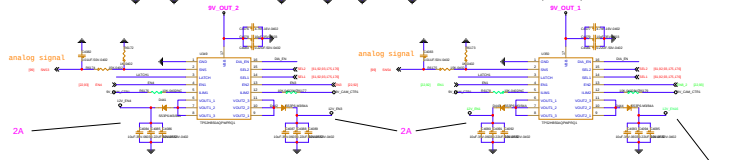

POC链路参考9296A
96712芯片每种供电应保证至少1A
1.8V TTL
trigger X4
0X52-0101 0010
左边加0，后：
0010 1001
0X29
IIC ADRESS:0X52
COAX GMSL2 6Gbps
IO 3.3V 连 接 器处3. 3 V
TRIGGER1
TRIGGER2
IIC/UART SEL



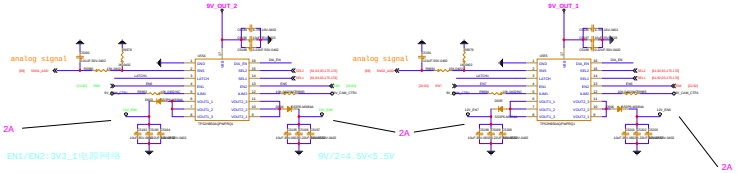


EN3/EN4:3V3电源网络

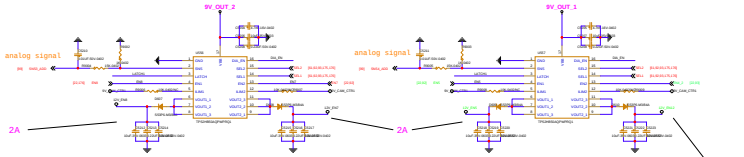
1ST



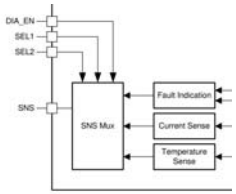
2ND

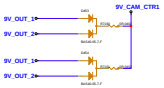


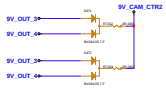
1ST

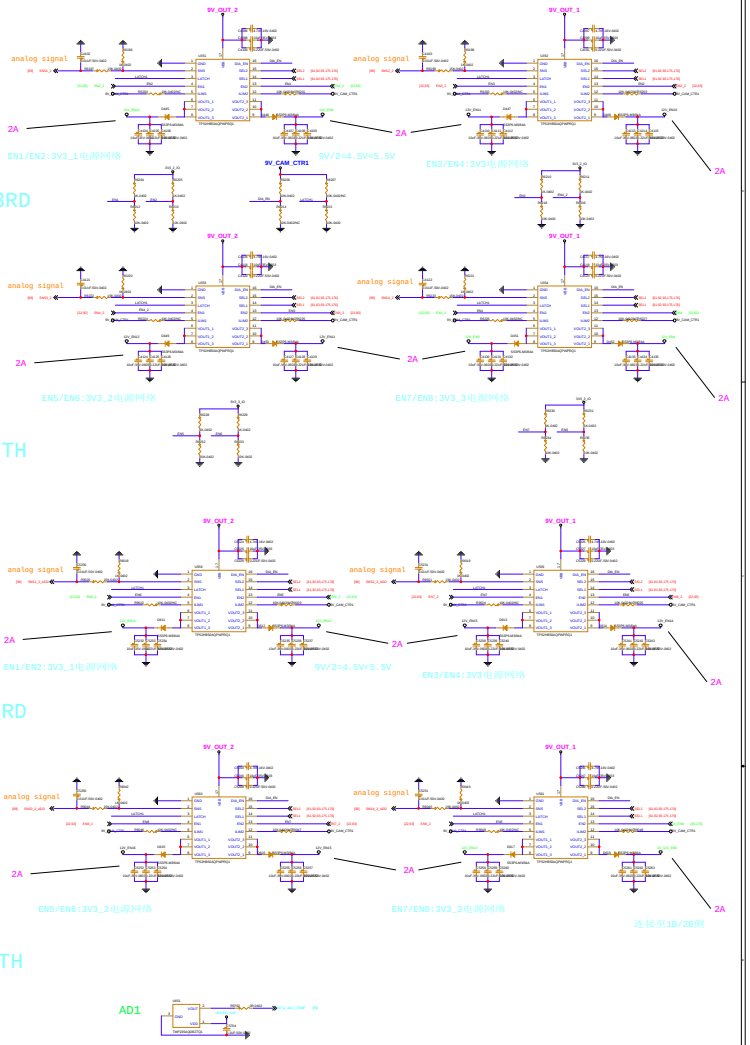


2ND



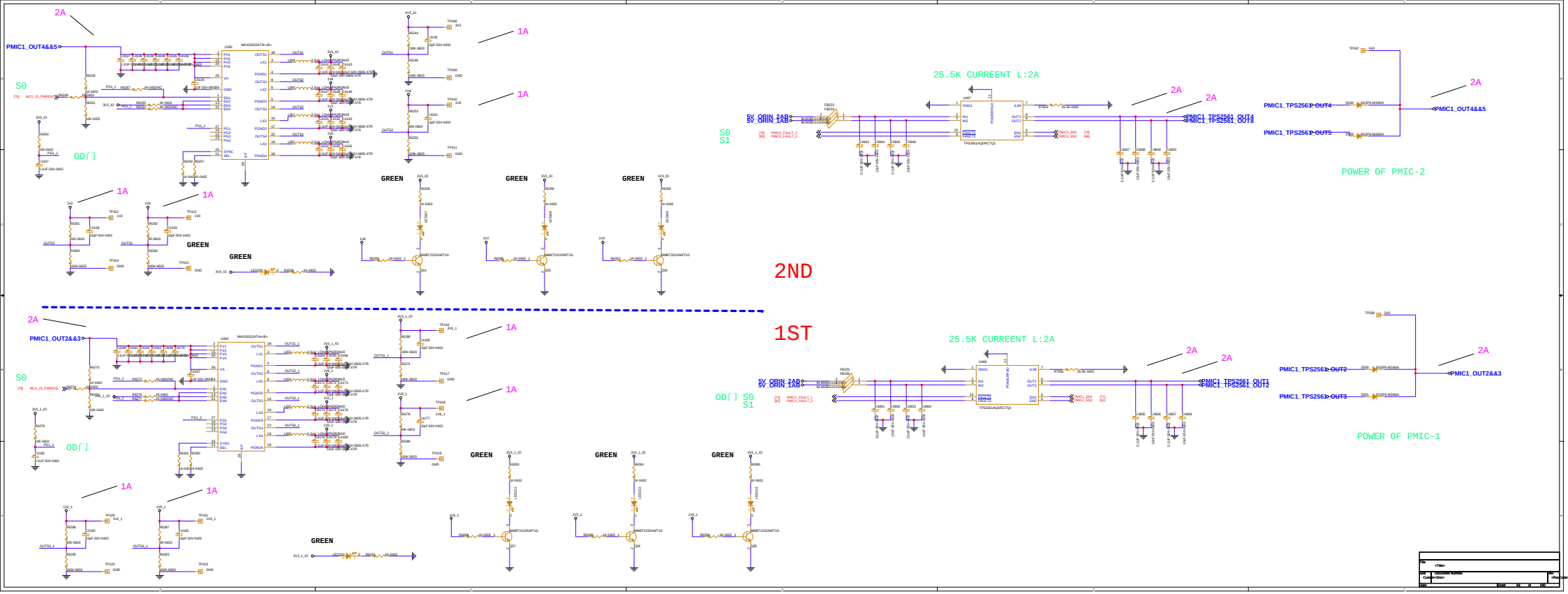


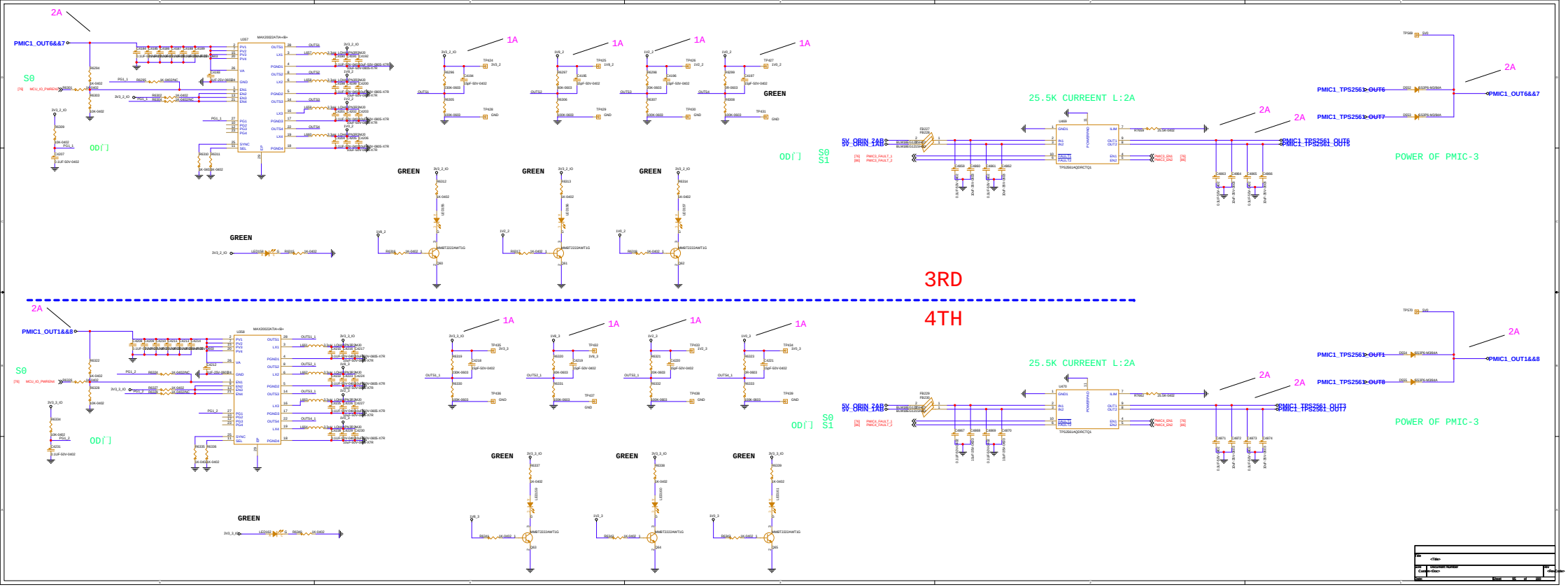



9V_OUT_2
9V_OUT_1
analog signal
2A
EN1/EN2:3V3_1电源网络
9V/2=4.5V<5.5V
EN3/EN4:3V3电源网络
9V_CAM_CTR1
3RD
EN5/EN6:3V3_2电源网络
EN7/EN8:3V3_3电源网络
4TH

9V_OUT_2
9V_OUT_1
analog signal
2A
EN1/EN2:3V3_1电源网络
9V/2=4.5V<5.5V
EN3/EN4:3V3电源网络
3RD
EN5/EN6:3V3_2电源网络
EN7/EN8:3V3_3电源网络
4TH
连接至1B/2B侧

AD1


2ND
1ST
25.5K CURREENT L:2A
POWER OF PMIC-2
POWER OF PMIC-1
PMIC1_OUT4&&5
PMIC1_OUT2&&3
PMIC1_TPS2561_OUT4
PMIC1_TPS2561_OUT5
PMIC1_TPS2561_OUT2
PMIC1_TPS2561_OUT3
PMIC1_TPS2561_OUT1
5V_ORIN_2AB
5V_ORIN_1AB
GREEN
2A
1A
S0
S1
OD
MAX20022ATA+/B+
TPS2561AQDRCTQ1


2A
PMIC1_OUT6&&7
S0
1A
GREEN
OD[`]
25.5K CURREENT L:2A
5V_ORIN_2AB
5V_ORIN_1AB
PMIC1_TPS2561_OUT6
PMIC1_TPS2561_OUT7
PMIC1_OUT6&&7
POWER OF PMIC-3
3RD
4TH
PMIC1_OUT1&&8
PMIC1_TPS2561_OUT1
PMIC1_TPS2561_OUT8
PMIC1_OUT1&&8

Title

PCIE SW CON/2

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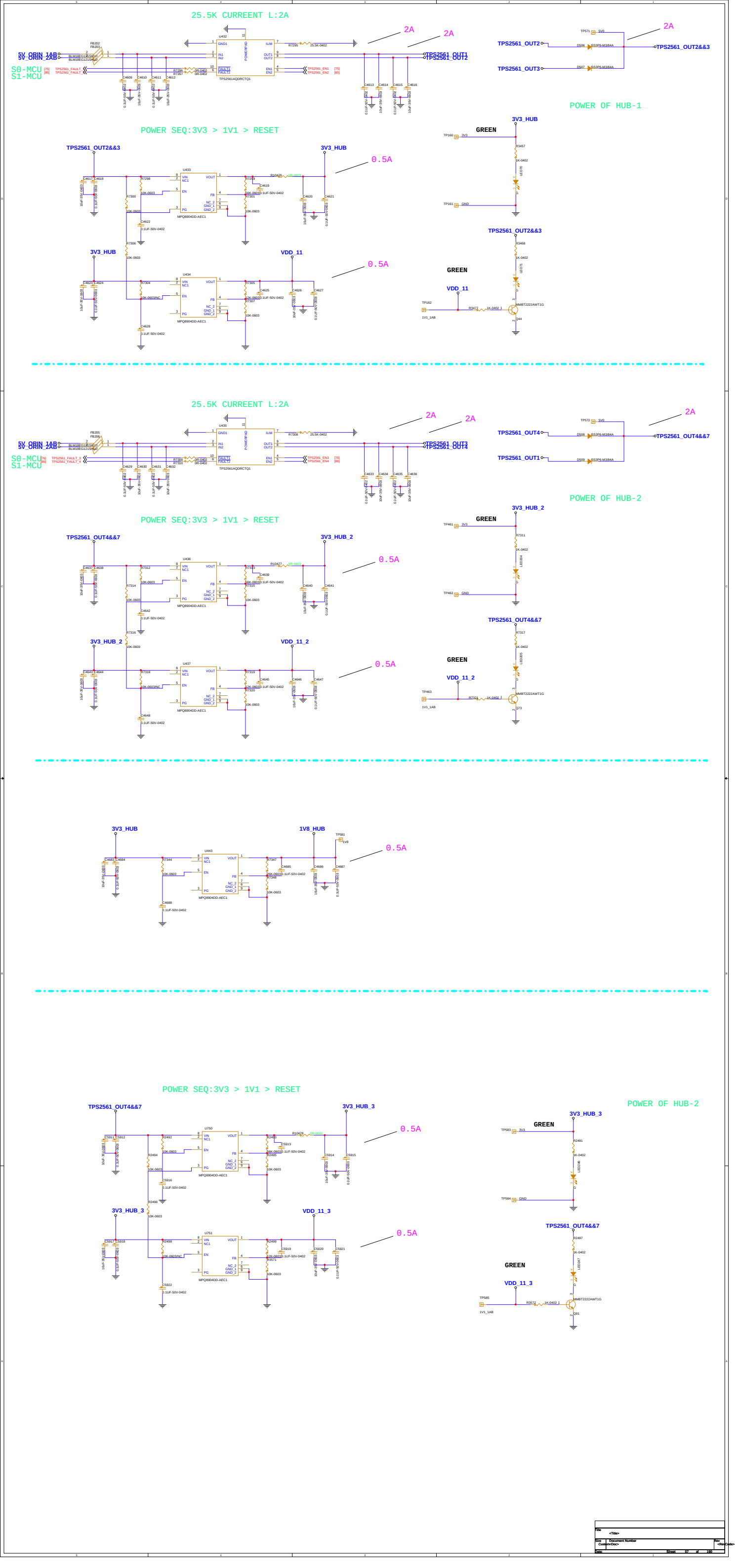

25.5K CURREENT L:2A
2A
2A
2A
TPS2561_OUT2
TPS2561_OUT3
TPS2561_OUT2&&3
S0-MCU
S1-MCU
POWER OF HUB-1
POWER SEQ:3V3 > 1V1 > RESET
TPS2561_OUT2&&3
3V3_HUB
0.5A
GREEN
3V3_HUB
VDD_11
0.5A
TPS2561_OUT2&&3
GREEN
VDD_11
25.5K CURREENT L:2A
2A
2A
2A
TPS2561_OUT4
TPS2561_OUT1
TPS2561_OUT4&&7
S0-MCU
S1-MCU
POWER OF HUB-2
POWER SEQ:3V3 > 1V1 > RESET
TPS2561_OUT4&&7
3V3_HUB_2
0.5A
GREEN
3V3_HUB_2
VDD_11_2
0.5A
TPS2561_OUT4&&7
GREEN
VDD_11_2
3V3_HUB
1V8_HUB
0.5A
POWER SEQ:3V3 > 1V1 > RESET
POWER OF HUB-2
TPS2561_OUT4&&7
3V3_HUB_3
0.5A
GREEN
3V3_HUB_3
GREEN
3V3_HUB_3
VDD_11_3
0.5A
TPS2561_OUT4&&7
GREEN
VDD_11_3

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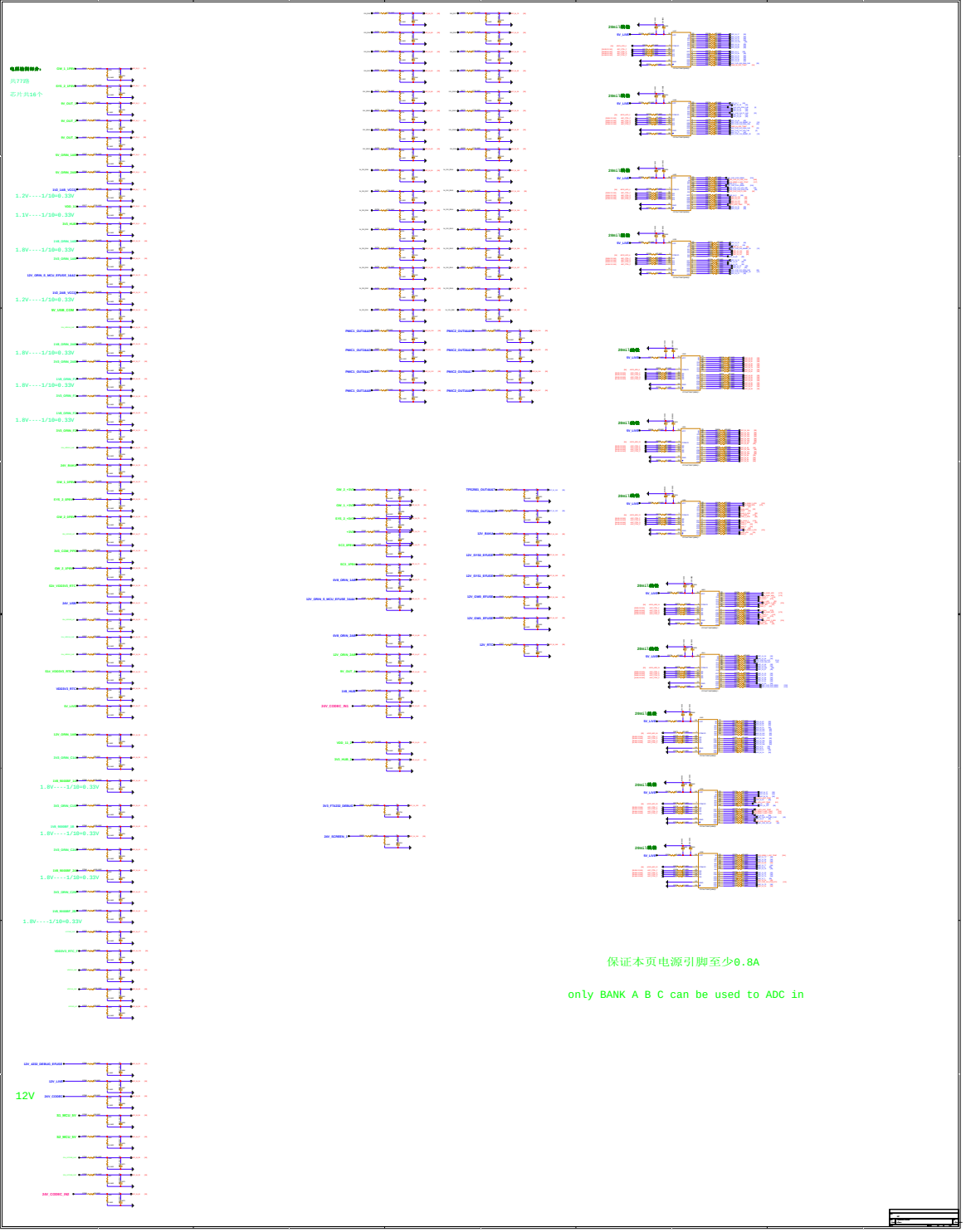
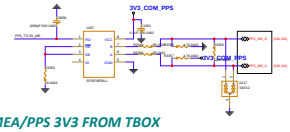
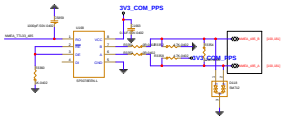
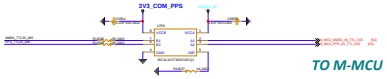

电源检测特点：
共77路
芯片共16个
1.2V----1/10=0.33V
1.1V----1/10=0.33V
1.8V----1/10=0.33V
1.2V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
1.8V----1/10=0.33V
12V
保证本页电源引脚至少0.8A
only BANK A B C can be used to ADC in





NMEA/PPS 3V3 FROM TBOX

M_MCU_PPS/NMEA_TTL_3V3

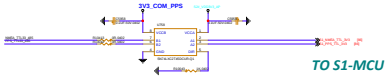


TO M-MCU

S0_MCU_PPS_TTL_3V3

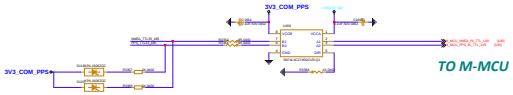
TO S0-MCU

S1_MCU_PPS_TTL_3V3



TO S1-MCU

M_MCU_PPS_TTL_1V8应接到PWM PIN



TO M-MCU

8.4 器件功能模式

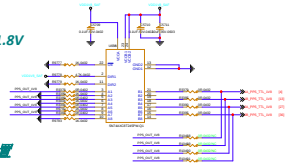
表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（已反）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（已反）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持与有效逻辑电平。

保证本页电源引脚至少0.8A

PPS 1.8V TO 1.8V



U654 U655靠近U529放置

默认形态是直通给到3个MCU和4个ORIN+IO CON

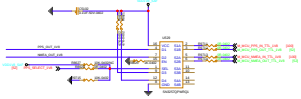
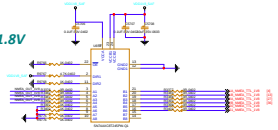


Figure 8-1. SN3257-Q1 Functional Block Diagram

NMEA 1.8V TO 1.8V

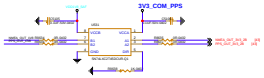


8.1 Function Table(1)

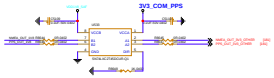
CONTROL INPUTS			Signal Direction	
OE	DIR1	DIR2	Bits 1-4	Bits 5-8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	B to A
L	L	H	B to A	A to B
L	H	L	A to B	B to A
L	H	H	A to B	A to B

(1) Input circuits of the data I/Os are always active and must be driven to a valid high level.

TO ORIN 2B USB



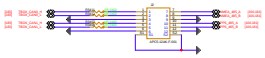
TO子板 for IMU



深台纬翔 12PIN

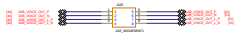
定位信息

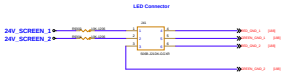
TBOX CAN0-AD0
TBOX CAN1-AD1



红绿灯+codec 深台纬翔 24PIN

散热铜皮

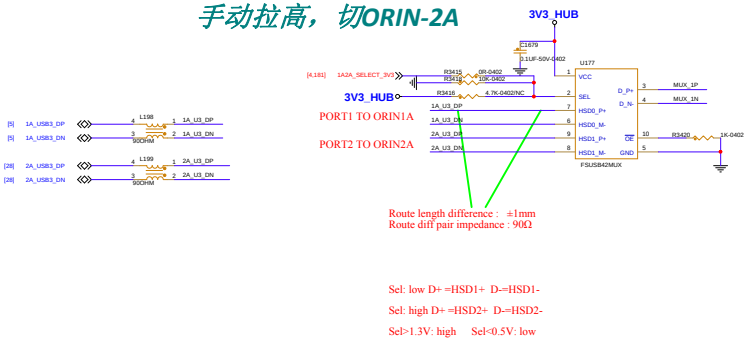




MUX-1

DEFAULT IS ORIN1A

手动拉高，切ORIN-2A

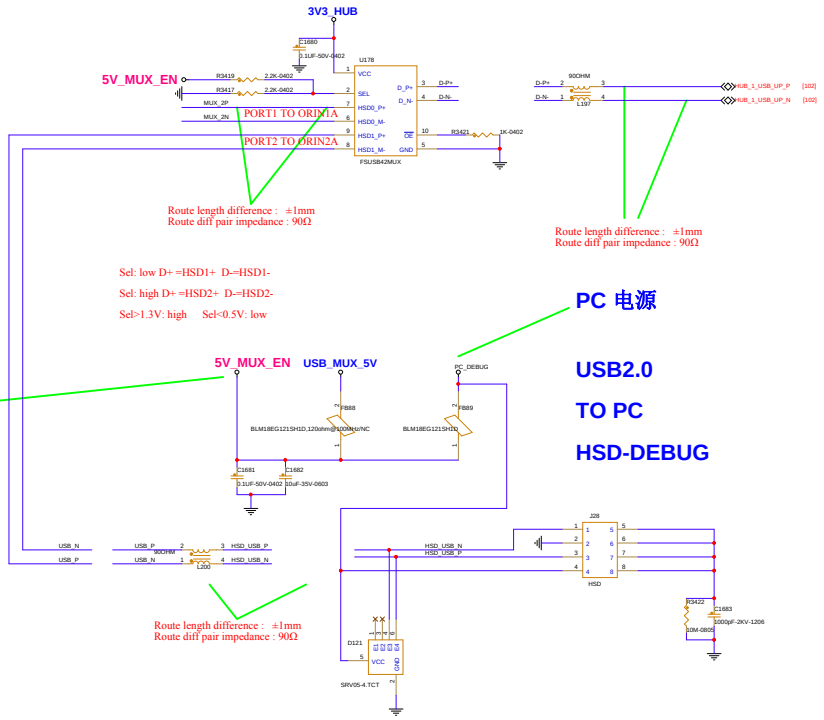


MCU BOOTMODE 拉高信号

默认该电压为0V，接上USB线缆后为5V

USB烧录后拔线重启，即从flash启动

MUX-2



磁珠两侧至少1A通流

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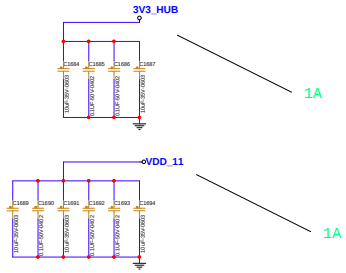
HUB-1



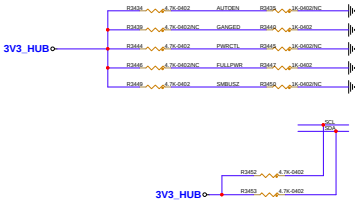
第一级HUB：上行通道

HUB-2-USB-UP

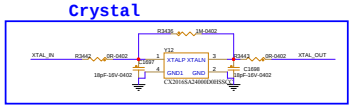
4232-4 IO子板

PDU USB-1

PDU USB-2(原来)
HUB-3上行口(现在)

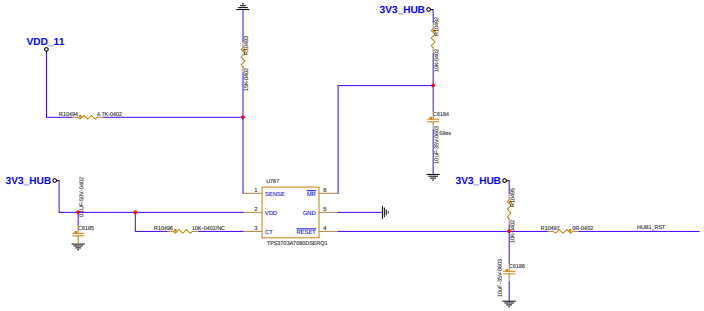


Crystal



Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

门槛电压：0.8V　　delay time is 10ms



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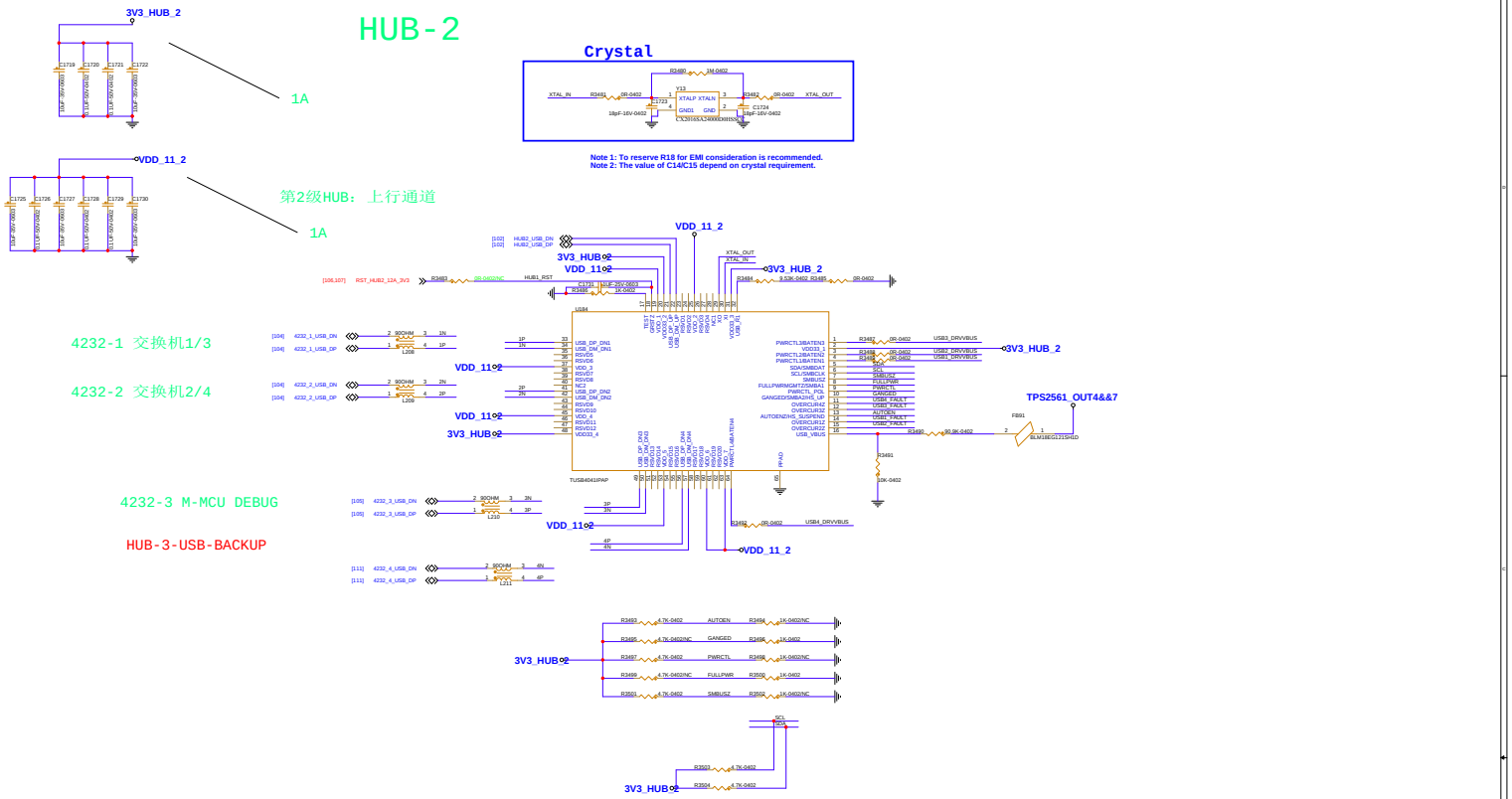
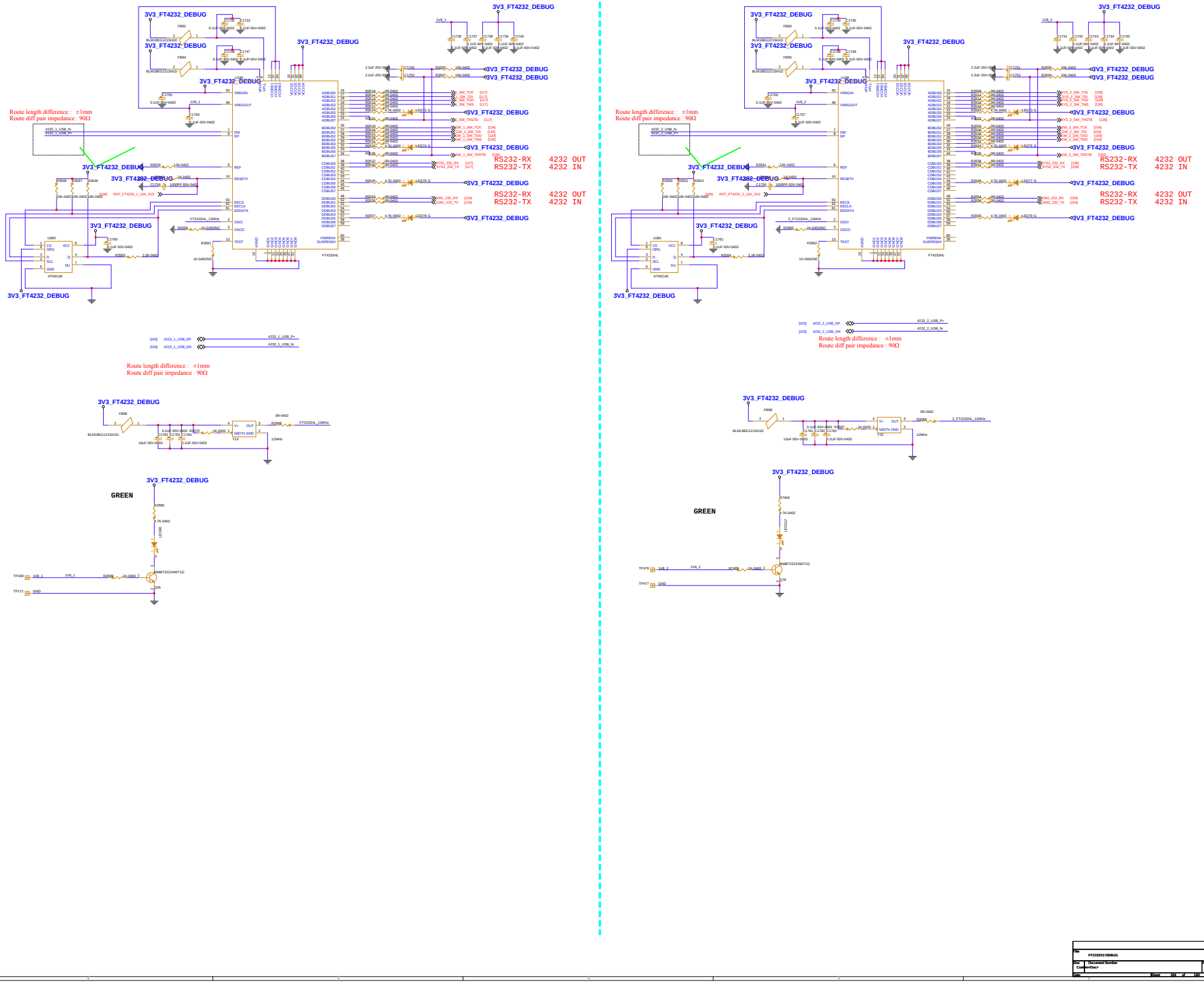
Date:		Sheet 102 of 106	

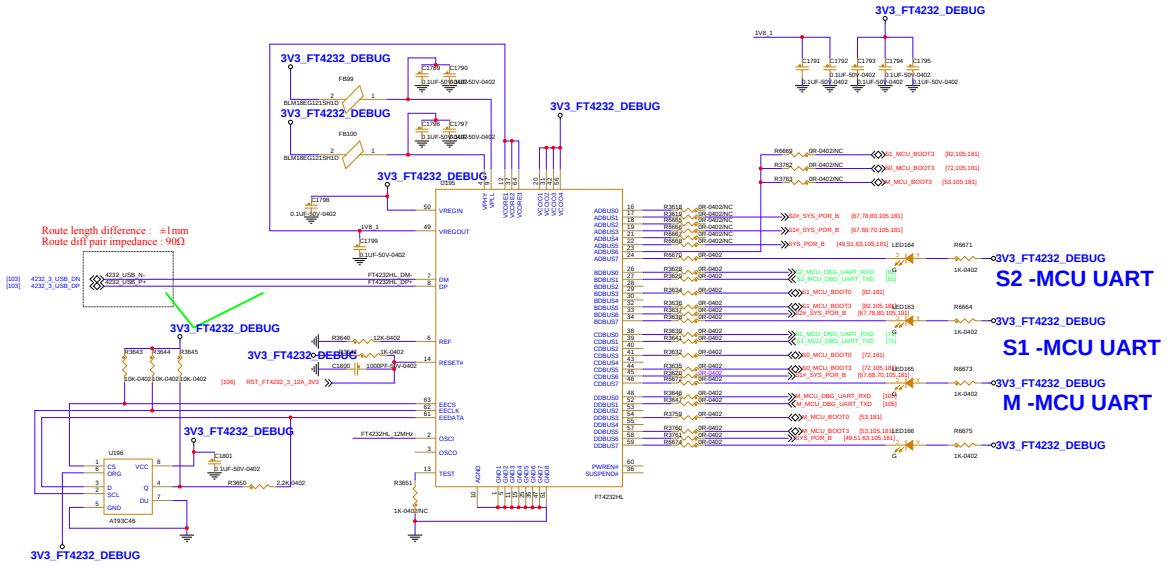
HUB-2



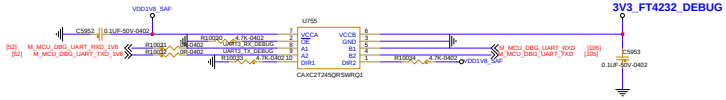
门槛电压：0.8V　　delay time is 10ms

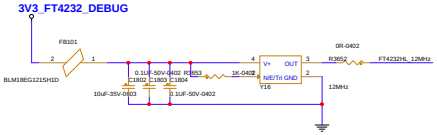
File	USB2.0_1A&2A1-DEBUG		
Size	Document Number		Rev
Custom<Doc>			<RevCode>
Date:		Sheet 103 of 180	

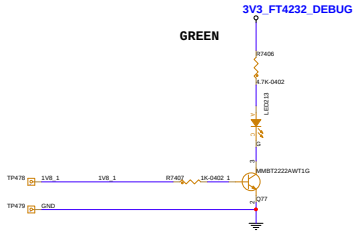

3V3_FT4232_DEBUG
Route length difference : ±1mm
Route diff pair impedance : 90Ω
4232_1_USB_N
4232_1_USB_P+
RST_FT4232_1_12A_3V3
FT2232HL_12MHz
RS232-RX
RS232-TX
4232 OUT
4232 IN
GREEN
4232_2_USB_DP
4232_2_USB_DN
4232_2_USB_P+
4232_2_USB_N-
2_FT2232HL_12MHz



M-MCU DEBUG UART







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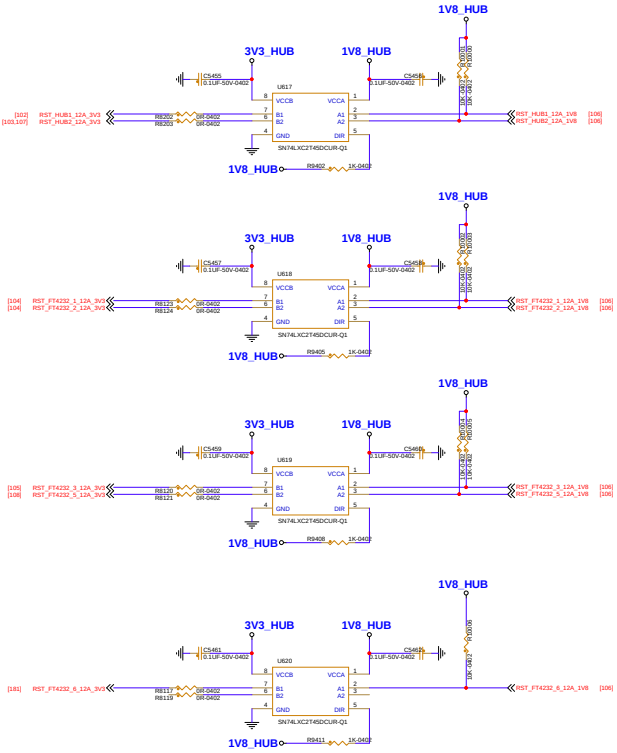


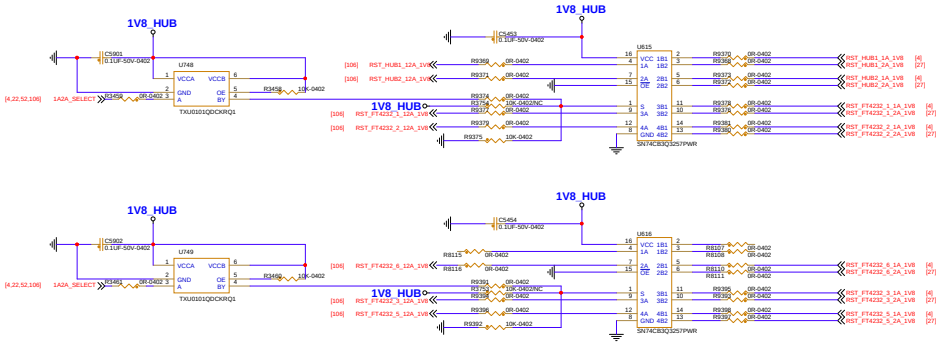
8.4 器件功能模式

表 8-1. 功能表

控制输入(1)	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) 数据 I/O 的输入电路始终处于激活状态，并应保持为有效逻辑电平。

手动拉高，切ORIN-2A



DEFAULT MODE IS A=B2（ORIN-1A）

Table 1. Function Table

INPUTS		INPUT/OUTPUT	FUNCTION
$\overline{OE}$	S	A	
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

Title	NC		
Size D	Document Number <Doc>		Rev <RevCode>
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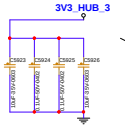
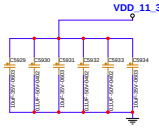
HUB-2



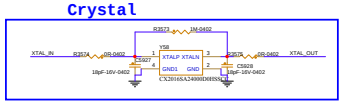
1A



第2级HUB：上行通道

1A

Crystal

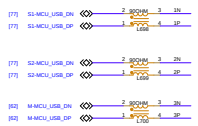


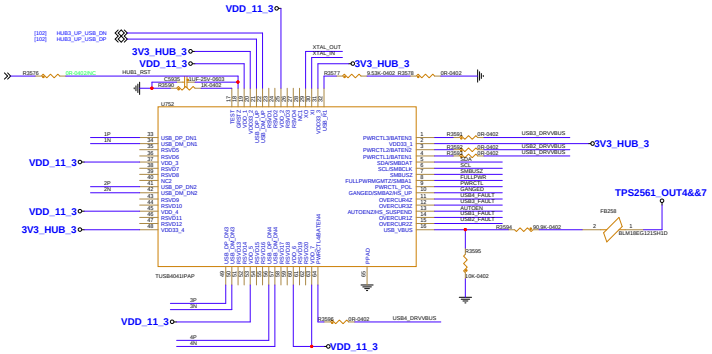
Note 1: To reserve R18 for EMI consideration is recommended.
Note 2: The value of C14/C15 depend on crystal requirement.

S1-MCU USB烧录

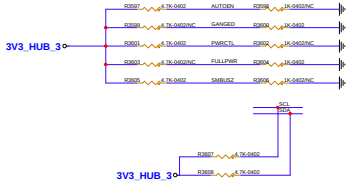
S2-MCU USB烧录

M-MCU USB烧录

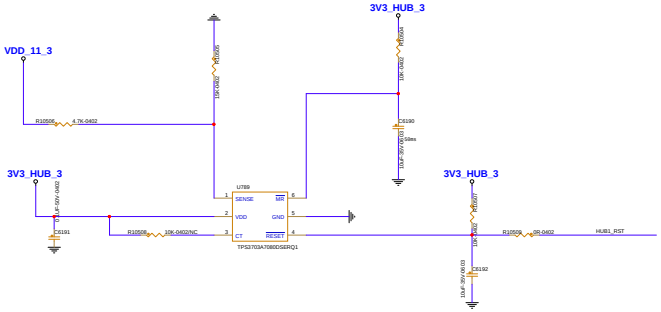




PDU USB-2(现在)



门槛电压：0.8V　　delay time is 10ms



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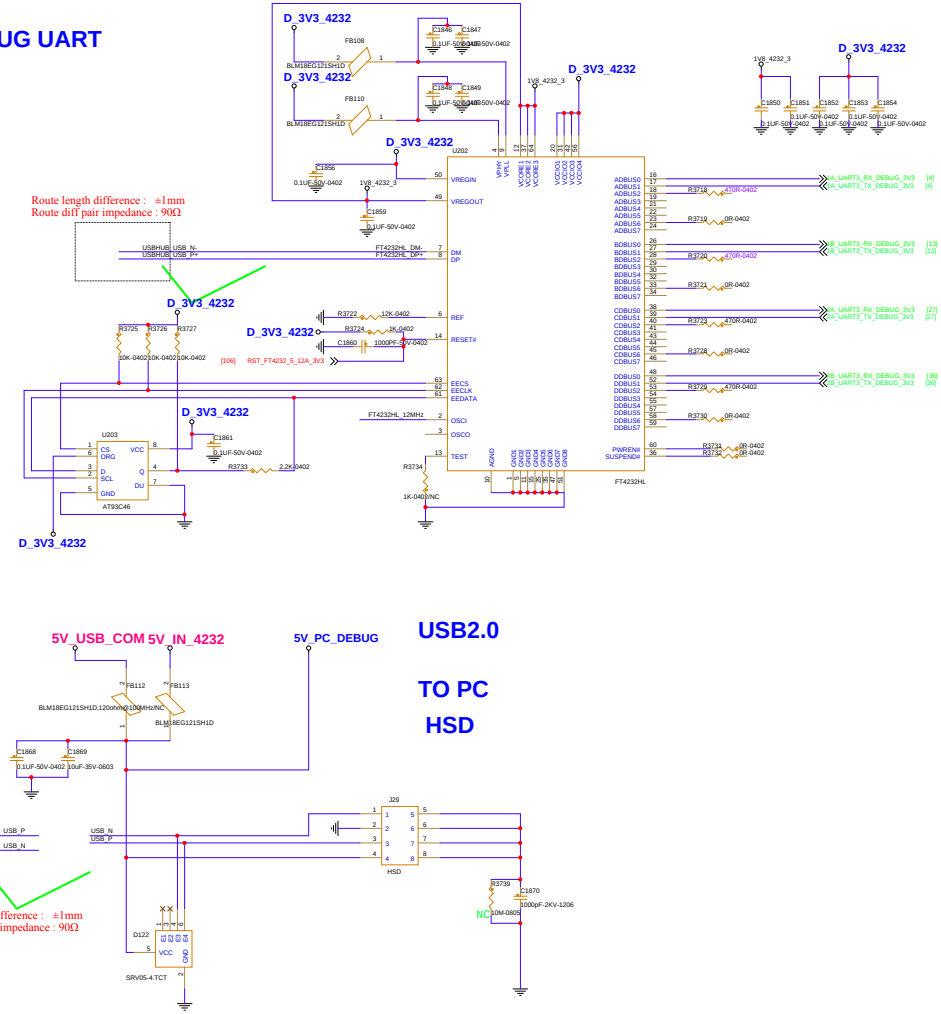
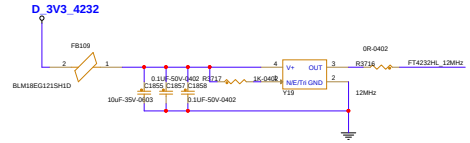
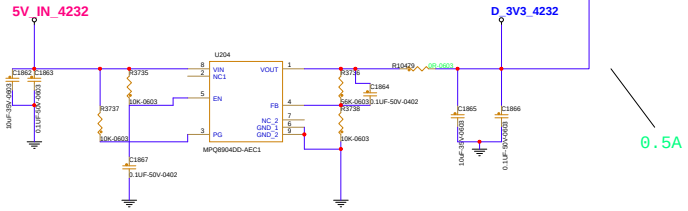
4 ORIN DEBUG UART







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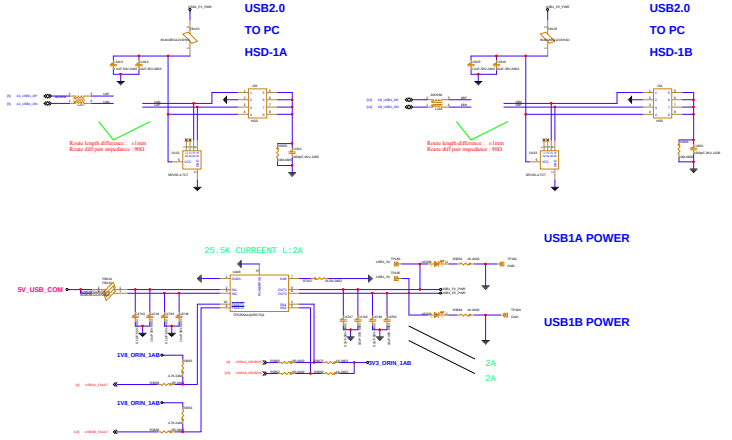
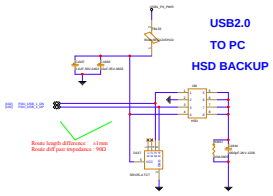
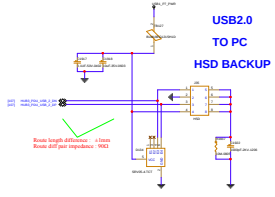
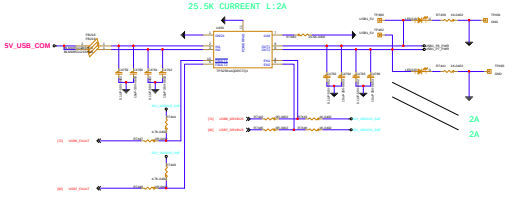


USB1A POWER

USB1B POWER



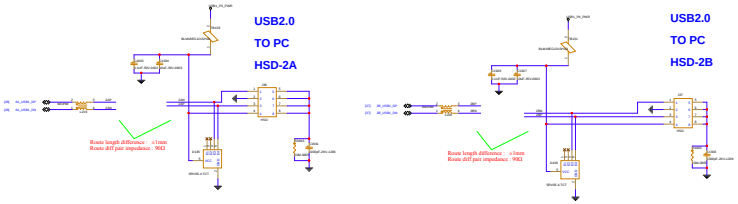


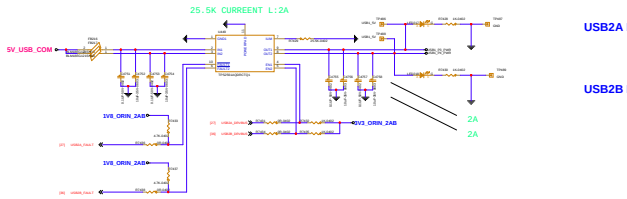


S0
S1

HSD BACKUP POWER-PDU

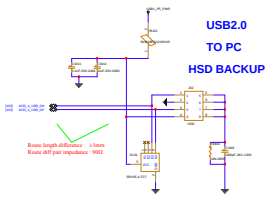
HSD BACKUP POWER-PDU

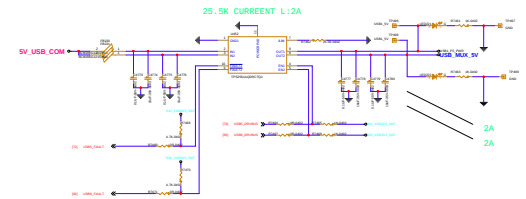




USB2A POWER

USB2B POWER





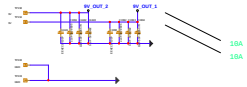
S0
S1

HSD BACKUP POWER

This part power is used to ORIN 1A/1B.

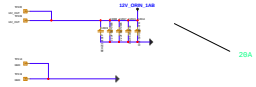
POWER IN 9V TO MIPI

9V MODULE



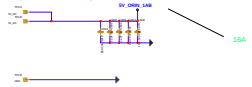
POWER IN 12V

12V MODULE

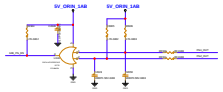


POWER IN 5V

5V MODULE



default mode is OR.



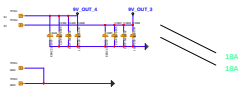
Power sequence: 12V>>12V_PG(VIN_PWR_BAD_N)

12V_PG(3V3/1V8_EN)->3V3_PG(MODULE_POWER_ON)

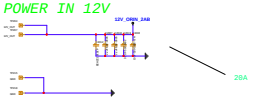
Mirror

This part power is used to ORIN 2A/2B.

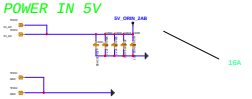
POWER IN 9V TO MIPI



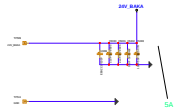
POWER IN 12V

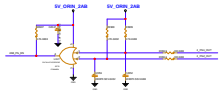


POWER IN 5V



POWER IN 24V_BAKA

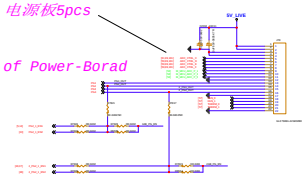




default mode is OR.

电源板5pcs

Signal of Power-Borad



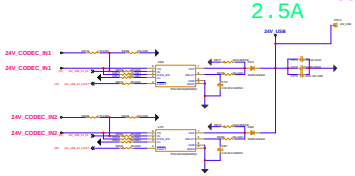
VIN_PWR_BAD_N

3V3/1V8 EN

TO M-MCU

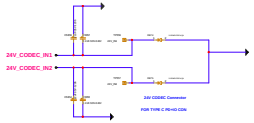
USB POWER

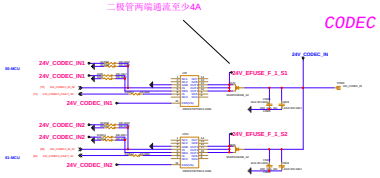
2.5A

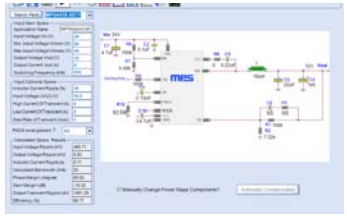


二极管两端通流至少4A

CODEC POWER

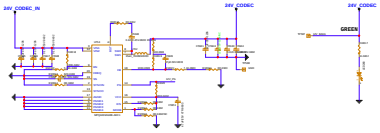






12V 4A

12V



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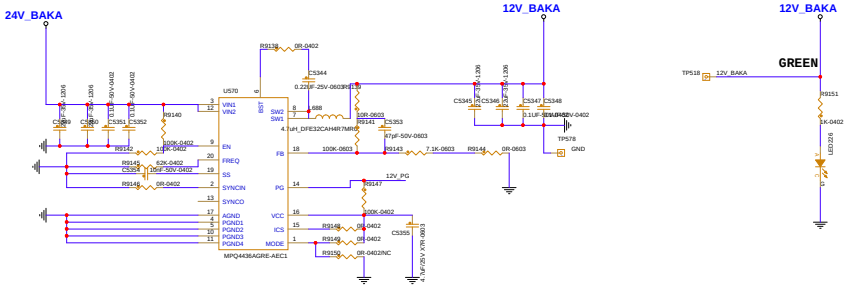
12V 3合1

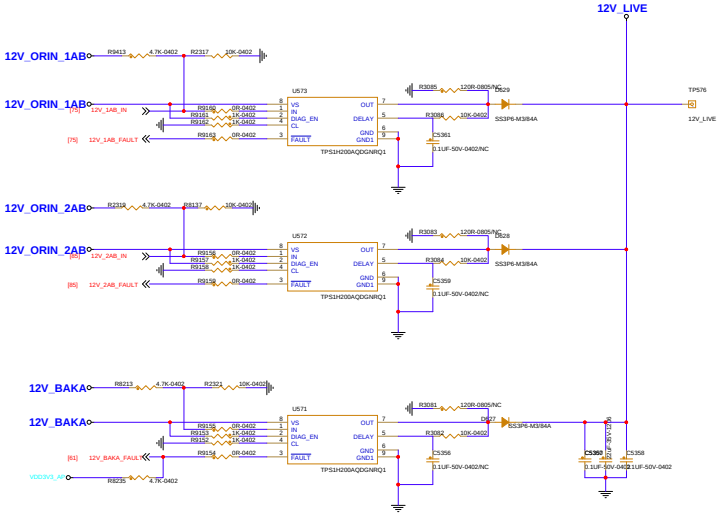
12V 1A



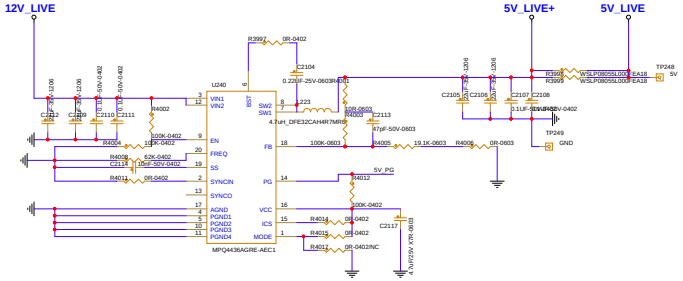
S0-MCU处理

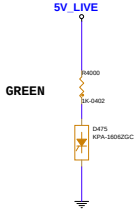
S1-MCU处理

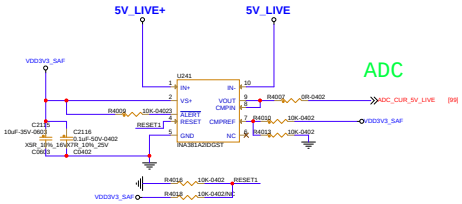
M-MCU不处理



5V 2A







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Size: D	Document Number: <Doc>	Rev: <RevCode>
Date:	Sheet 114 of 190	

5V_COM_PPS&&NMEA

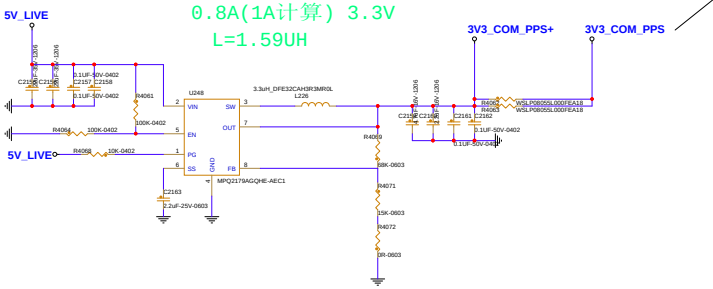
1A

F=2.4MHZ

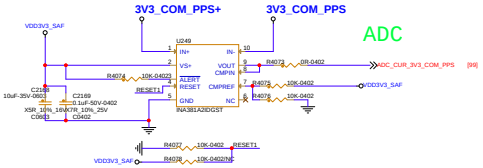
FCCM MODE

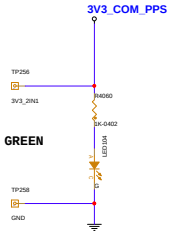
0.8A(1A计算) 3.3V

L=1.59UH



L=1.5uH 0.003V Cout=5.9uF





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Size	Document Number	Rev
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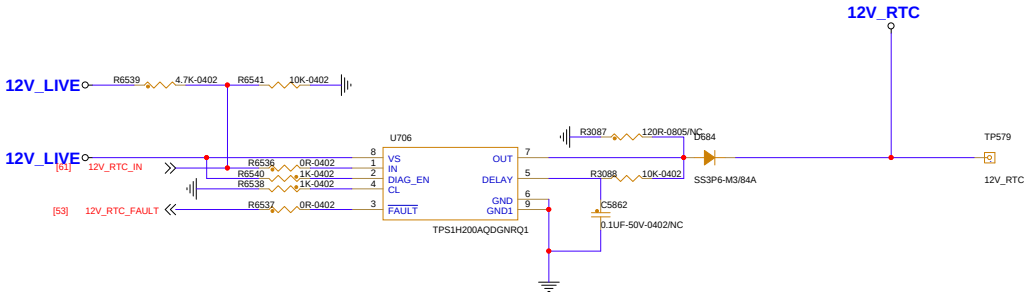

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Size C	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 116 of 190	

Table 1: BCM89586M Port Mapping

Interface Name	Total Number of Interfaces	Port Number Mapping Options
1000BASE-T1/100BASE-T1/BroadR-Reach	4	Port 0, 1, 2, 3
100BASE-T1/BroadR-Reach	6	Port 4, 5, 6, 9, 10, 11
1-Gb/s SGMII	4	Port 4, 5, 6, 9
1000BASE-T/100Base-TX	1	Port 11
XFI/5G/2.5G/1G SerDes	6	Port 8, 12, 13, 14, 15,16
RGMII/MII/RvMII/RMII	4	Port 8, 10, 11, 12, 13, 14, 15, 16
PCIe Gen4	2	Port 8, 15, 16
Internal 1-Gb/s interface to an Arm subsystem	1	Port 7

SYS-1

DISABLE auto-negotion

MASTER MODE

DISABLE ISOLATE MODE

enable global reset from safety monitor

EN FRAME FORWARD

LANE1 TO IPC

FORCE DOWNLOAD MODE

RGMII 1000

RGMII 1000

RGMII 1000

RGMII 1000

TC10 MODE:00

1000BASE-T1

Default is Crystal, 00

Crystal

AD1

P4 IO CON 89586 IN
P5 IO CON 89586 OUT
P6 ORIN 1B 89586 IN
P9 ORIN 1A 89586 OUT
89586 IN
89586 OUT
P14-XFI0 89586 IN
89586 OUT
P15-XFI1
P16-XFI2
P8-XFI3 (NC)
P12-XFI4
P13-XFIS/SGMII

12-16、8: XFI

P10-RGMII S-MCU-1 -RGMII2
89586 IN
89586 OUT
MII1:P10 OR P12 RGMII,P10

P13-RGMII S-MCU-2 -RGMII2
89586 IN
89586 OUT
MII2:P11 OR P13 RGMII,P13

P8-RGMII M-MCU-RGMII2
89586 IN
89586 OUT
P8 OR P15 RGMII

P14 OR P16 RGMII

PCIE/NC
PCIE1:P8
PCIE0:P16

P0-P3 1000-T1

P4
P5
P6
P9
P10
P11

P11

1000TX

DEBUG C OR F?

RS232-RX

RS232-TX

M IS PC

SMI SLAVE
SMI MASTER TO PHY

SMI MASTER TO PHY

SMI MASTER TO PHY

GPIO4-7 IS PWM

ID CODE:0X01

GPIO5:ID0

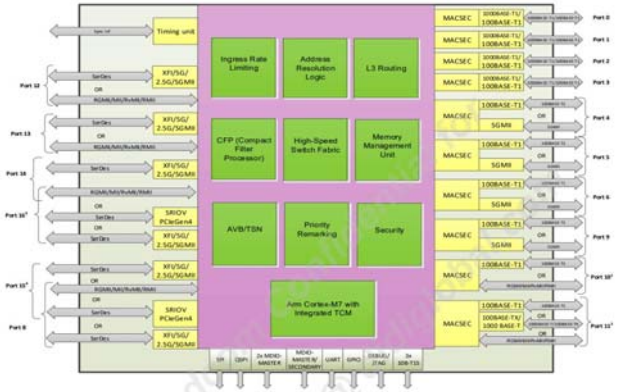
GPIO3:ID1

SW状态指示LED0 指示心跳

状态指示LED1 预留

SPI Flash

Note: Place R169 a 0-ohm resistor to ground at SPI_SIO1 pin if flash-less mode is used. Remove this 0ohm resistor when the flash is attached.

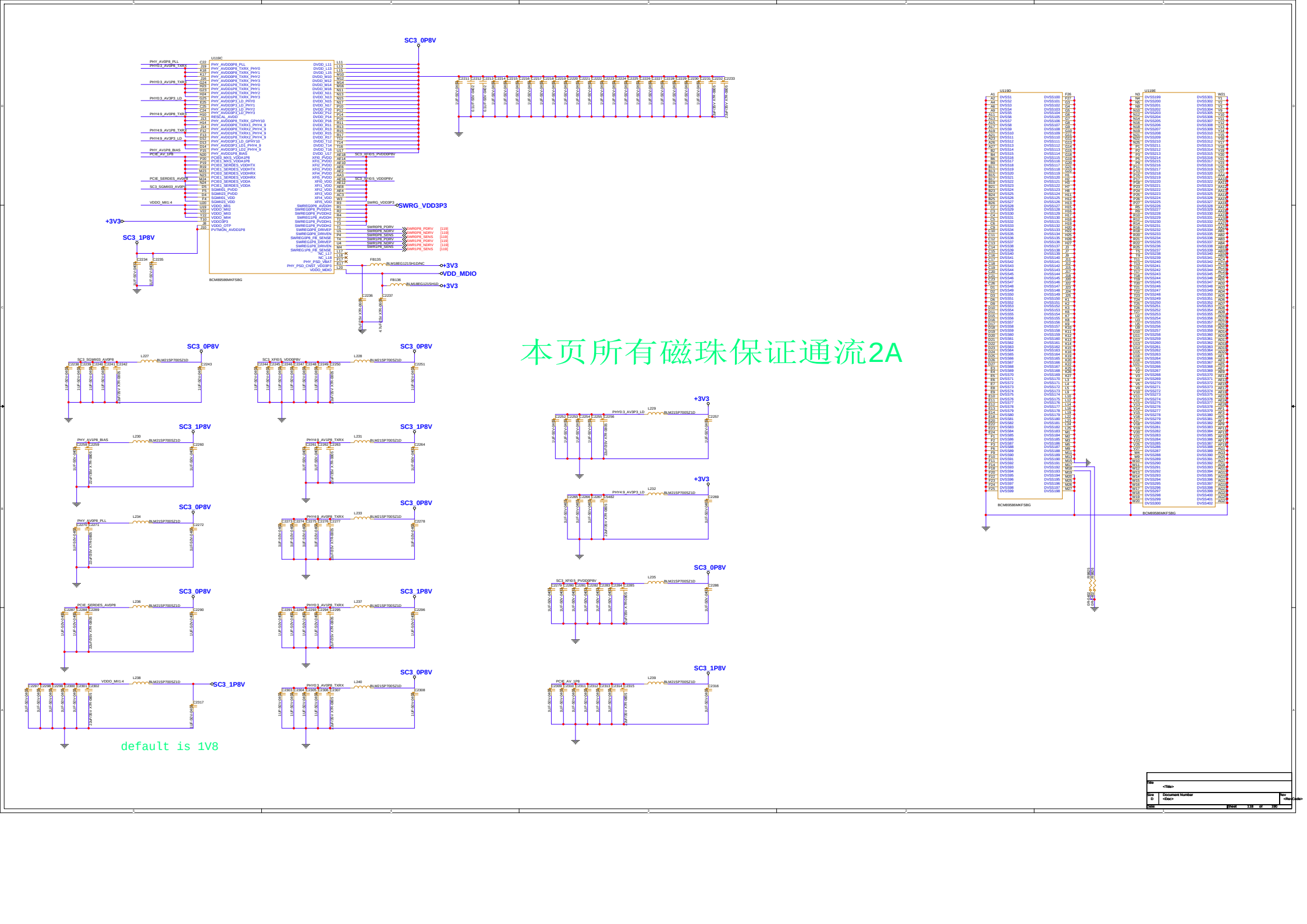


1: Port 10 RGMII/MII/RvMII/RMII interface is available only if Port 12 RGMII/MII/RvMII/RMII interface is not used.

2: Port 11 RGMII/MII/RvMII/RMII interface is available only if Port 13 RGMII/MII/RvMII/RMII interface is not used.

3: Port 16 RGMII/MII/RvMII/RMII interface is available only if Port 14 RGMII/MII/RvMII/RMII interface is not used.

4: Port 15 RGMII/MII/RvMII/RMII interface is available only if Port 8 RGMII/MII/RvMII/RMII interface is not used. Port 15 PCIe interface is available only if Port 8 PCIe interface is not used.


SC3_0P8V
U119C
PHY_AVDDP8_PLL
PHY0/3_AVDP8_TXRX
PHY0/3_AVIP8_TXRX
PHY0/3_AVIP3_LD
PHY4/9_AVDP8_TXRX
PHY4/9_AVIP8_TXRX
PHY4/9_AVIP3_LD
PHY_AVIP8_BIAS
PCIE_AV_1P8
PCIE_SERDES_AVDP8
SC3_SGMII03_AVDP8
VDDO_MII1:4
BCM89586MKFSBG
SWRG_VDD3P3
+3V3
SC3_1P8V
VDD_MDIO
SC3_XFI0:5_PVDDOP8V
SC3_XFI0:5_VDDOP8V
FB135
FB136
BLM18EG121SH1D/NC
BLM18EG121SH1D
本页所有磁珠保证通流2A
default is 1V8
U119D
U119E
BCM89586MKFSBG
Title
<Title>
Size
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Document Number
<Doc>
Rev
<RevCode>
Date:
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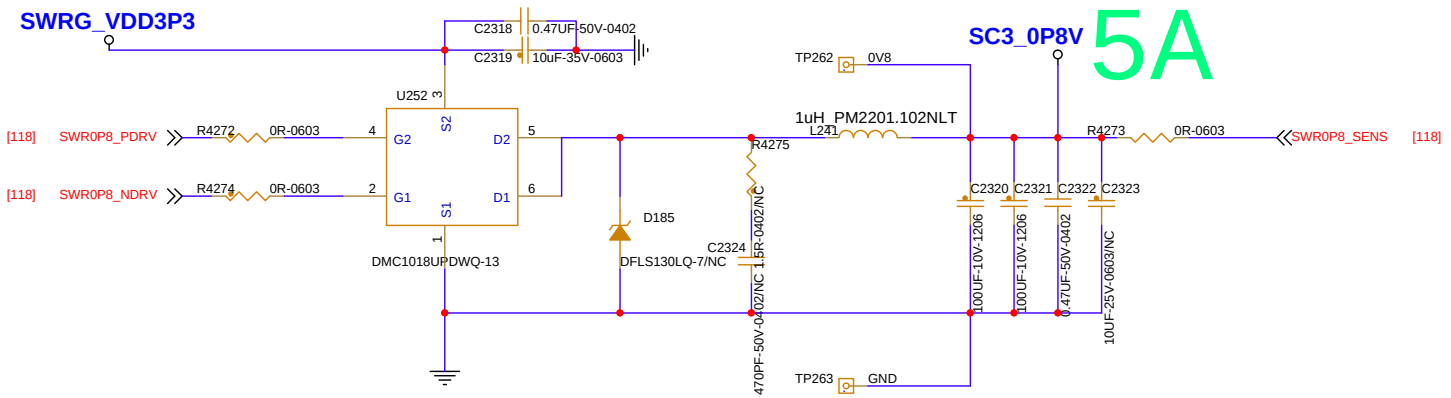

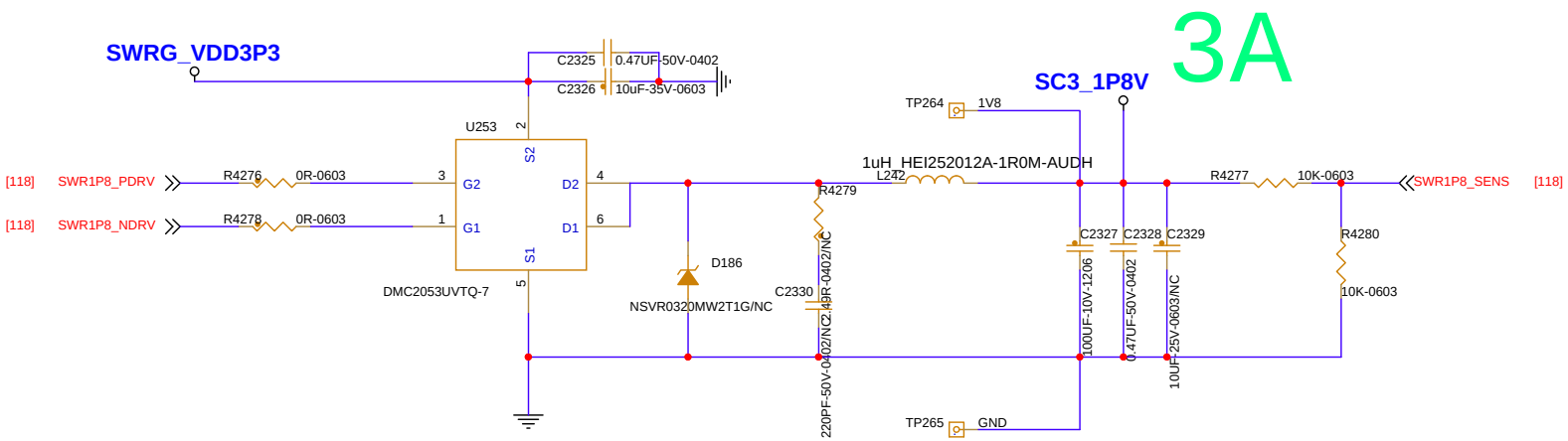

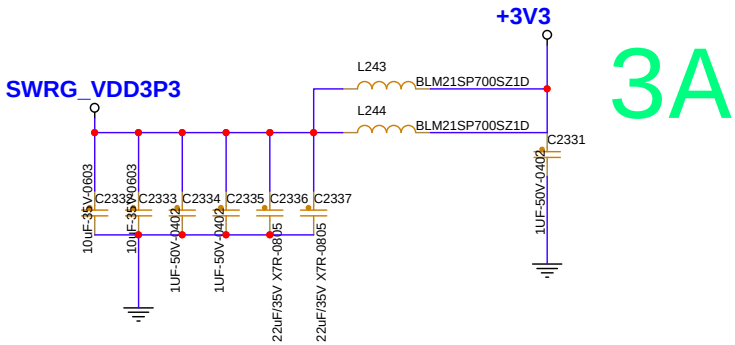

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Size B	Document Number <Doc>	Rev <RevCode>
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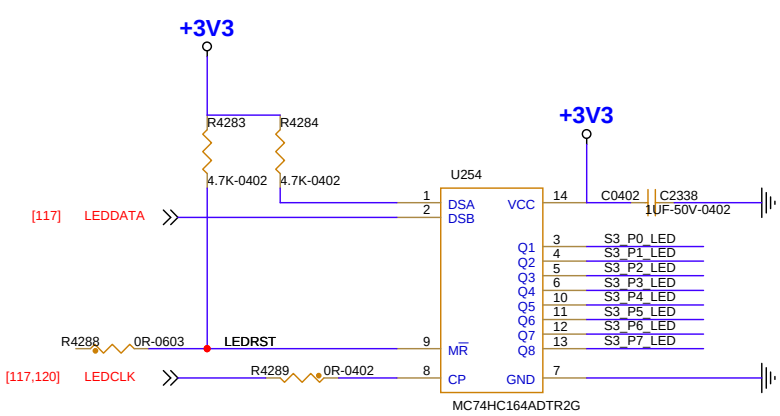

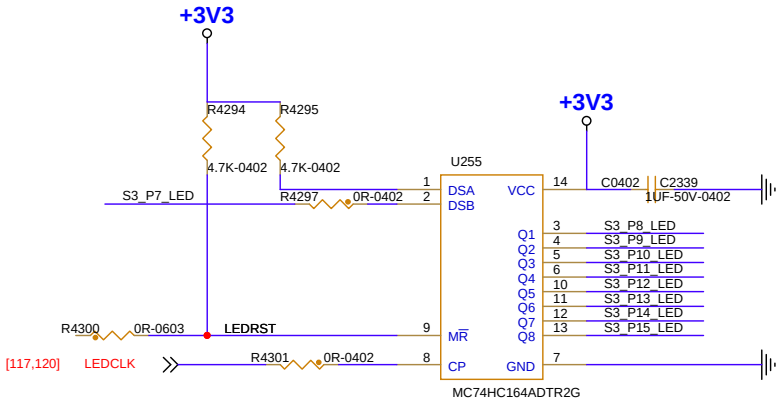

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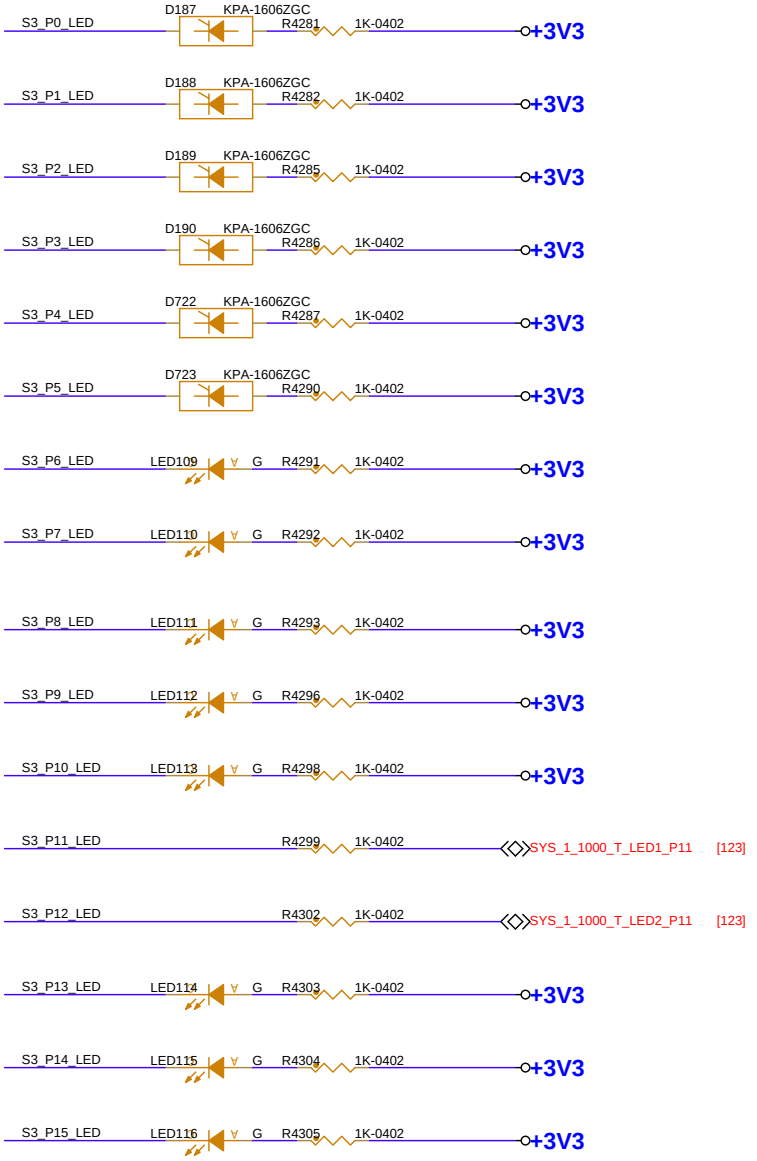

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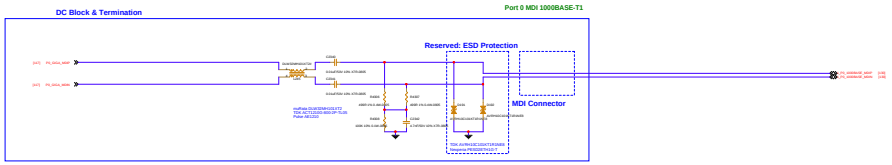
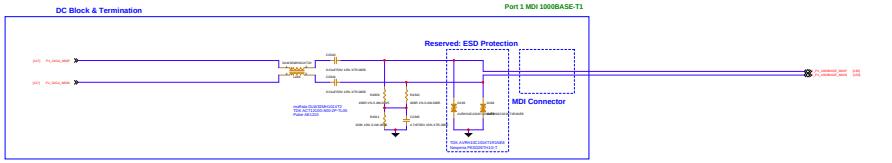
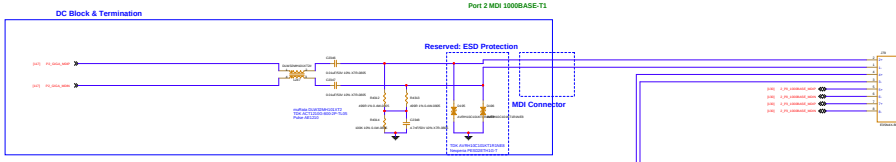
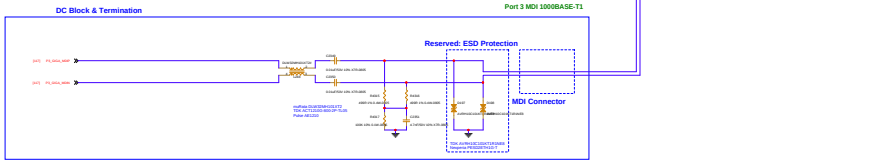








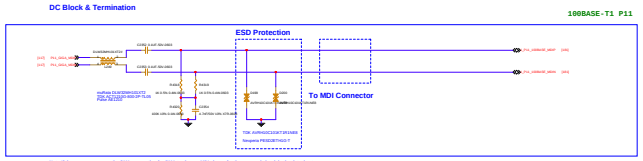
内显千兆T1-P2
内显千兆T1-P3
内显千兆T1-P0
内显千兆T1-P3

SWITCH-1

1	2

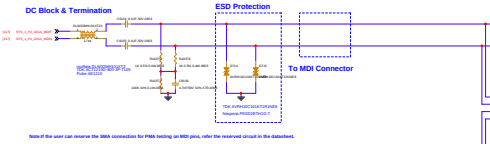
SWITCH-2

4	3



Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

100BASE-T1 P4 5 6 9



Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

100BASE-T1 P4

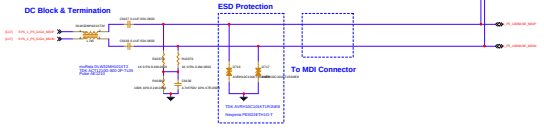
SWITCH-1

1	2

SWITCH-2

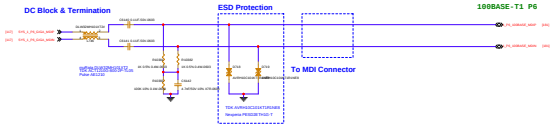
4	3

内显百兆T1-P4
内显百兆T1-P5
内显百兆T1-P4
内显百兆T1-P5

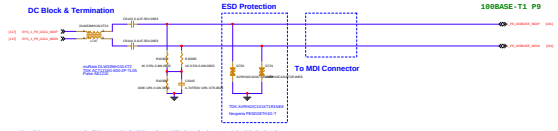


Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

100BASE-T1 P5



Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

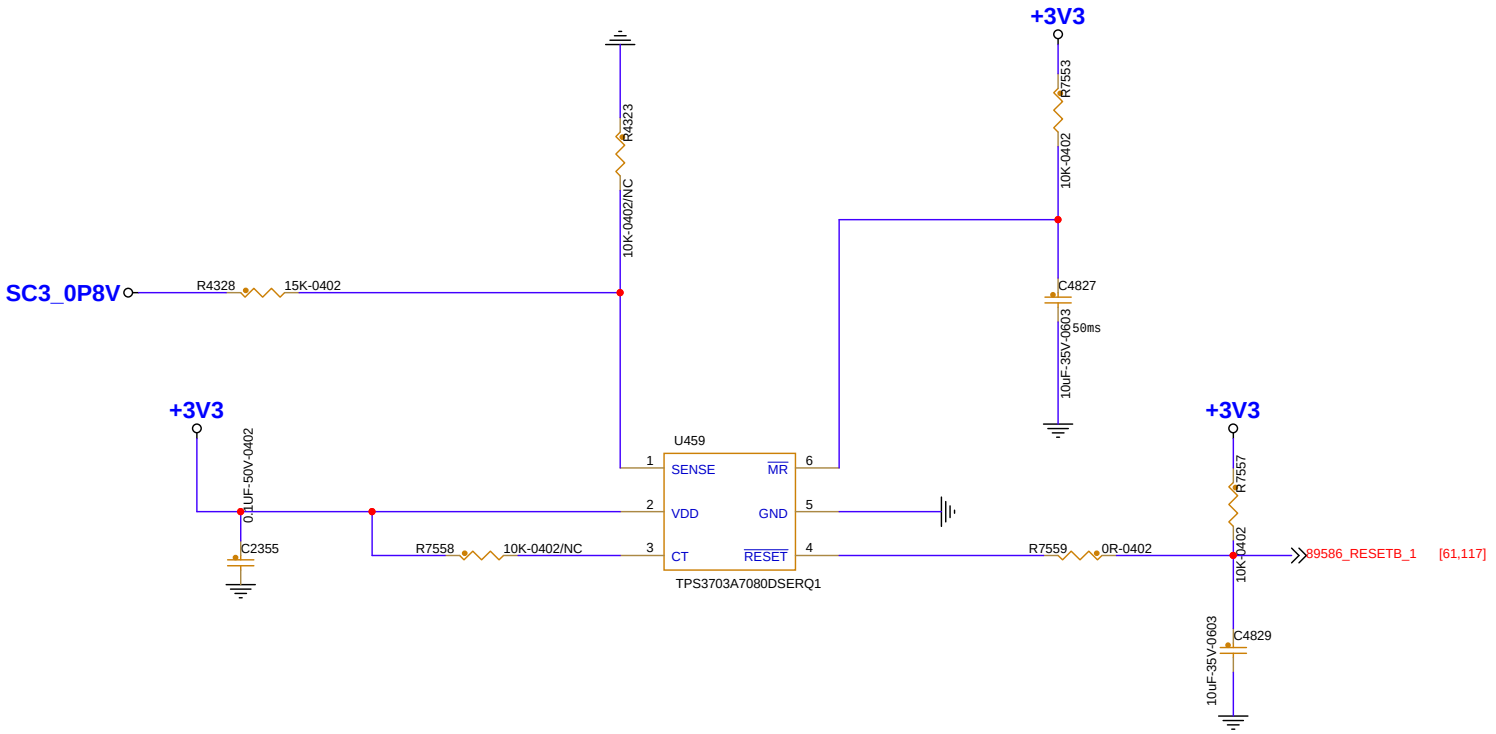


Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

门槛电压：0.8V

delay time is 10ms

89586M



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Size B	Document Number <Doc>	Rev <RevCode>
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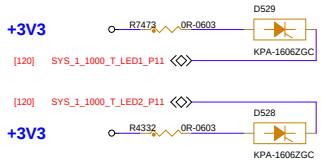

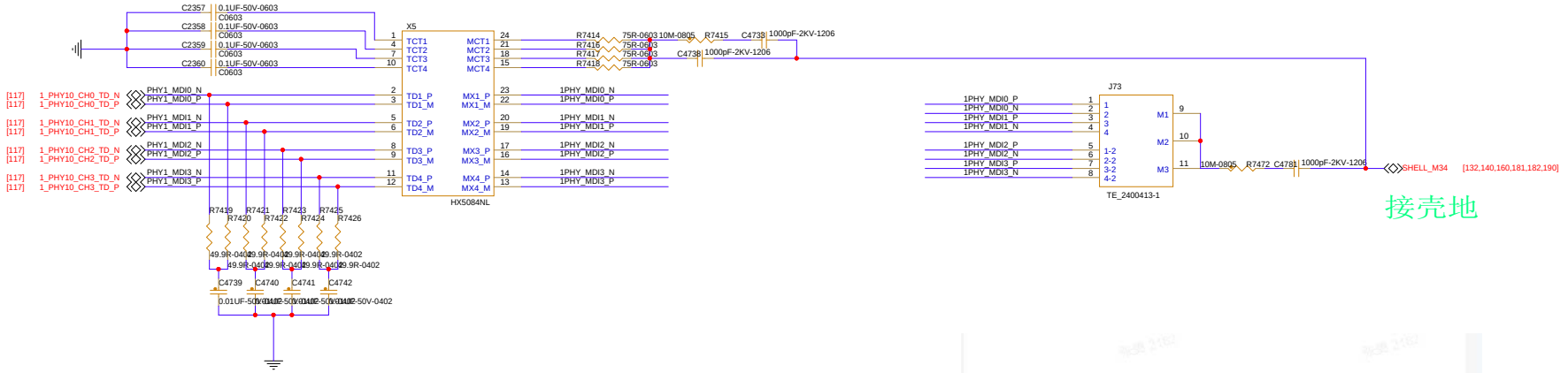

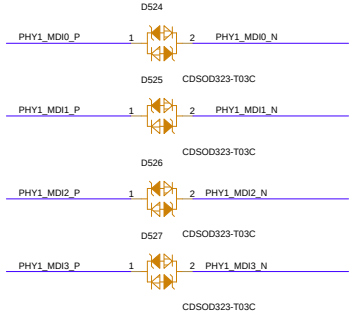

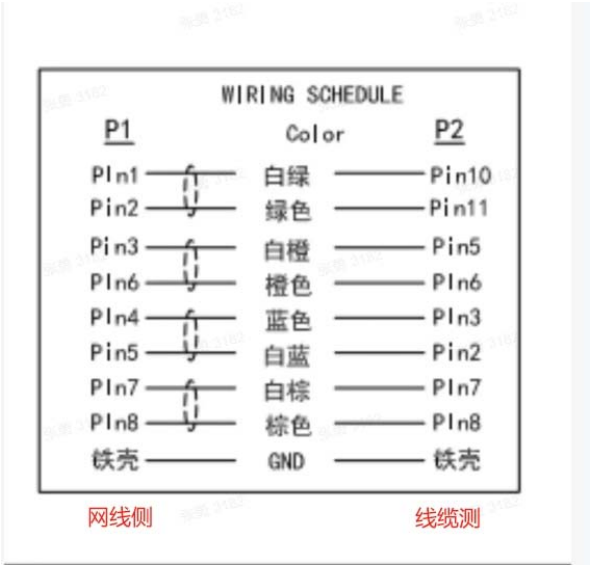

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Size C	Document Number <Doc>		Rev <RevCode>
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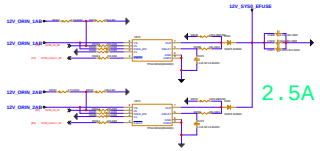
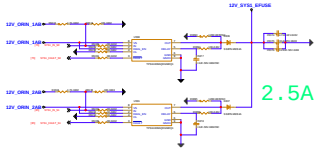
S0-MCU处理

S1-MCU处理



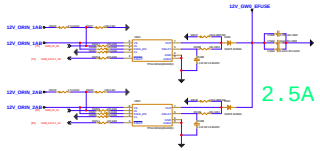
2.5A



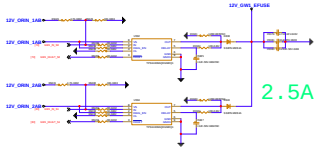
2.5A

S0-MCU处理

S1-MCU处理

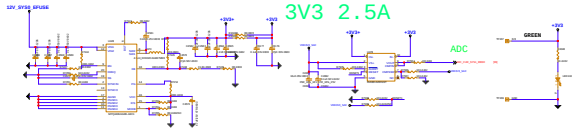


2.5A

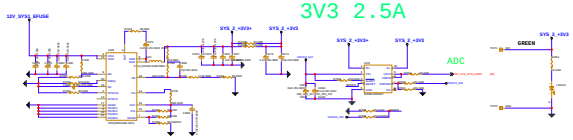


2.5A

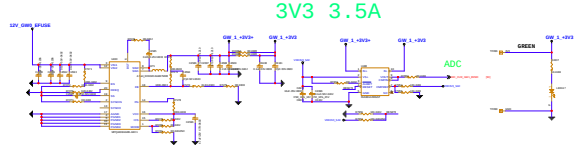
POWER OF SYS-SW-1



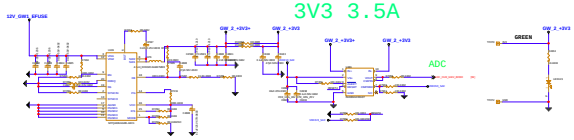
POWER OF SYS-SW-2



POWER OF GW-SW-1



POWER OF GW-SW-2



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Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Sheet 125 of 190

Table 1: BCM89586M Port Mapping

Interface Name	Total Number of Interfaces	Port Number Mapping Options
1000BASE-T1/100BASE-T1/BroadR-Reach	4	Port 0, 1, 2, 3
100BASE-T1/BroadR-Reach	6	Port 4, 5, 6, 9, 10, 11
1-Gb/s SGMII	4	Port 4, 5, 6, 9
1000BASE-T/100Base-TX	1	Port 11
XFI/5G/2.5G/1G SerDes	6	Port 8, 12, 13, 14, 15,16
RGMII/MII/RvMII/RMII	4	Port 8, 10, 11, 12, 13, 14, 15, 16
PCIe Gen4	2	Port 8, 15, 16
Internal 1-Gb/s interface to an Arm subsystem	1	Port 7

SYS-2

P4 5 6 7 TO IO CON

P4 IO CON 89586 IN
P5 IO CON 89586 OUT
P6 ORIN 2B 89586 IN
P9 ORIN 2A 89586 OUT
89586 IN
89586 OUT
89586 IN
89586 OUT

P14-XFI0
P15-XFI1
P16-XFI2
12-16、8: XFI
P8-XFI3 (NC)
P12-XFI4
P13-XFI5/SGMII

P10-RGMII
P13-RGMII
P8-RGMII

PCIE/NC
PCIE1:P8
PCIE0:P16

P11

P0-P3 1000-T1

P4
P5
P6
P9
P10
P11

1000TX

DEBUG C OR F?

M IS PC

MII1:P10 OR P12 RGMII,P10
MII2:P11 OR P13 RGMII,P13

P8 OR P15 RGMII

P14 OR P16 RGMII

DISABLE auto-negotion
MASTER MODE
DISABLE ISOLATE MODE
enable global reset from safety monitor
EN FRAME FORWARD
LANE1 TO IPC
FORCE DOWNLOAD MODE
RGMII 1000
RGMII 1000
RGMII 1000
RGMII 1000
TC10 MODE:00
1000BASE-T1

Default is Crystal, 00

Crystal

AD1

RS232-RX
RS232-TX

SMI MASTER TO PHY
SMI MASTER TO PHY

SMI SLAVE
SMI MASTER TO PHY

GPIO4-7 IS PWM

ID CODE:0X03

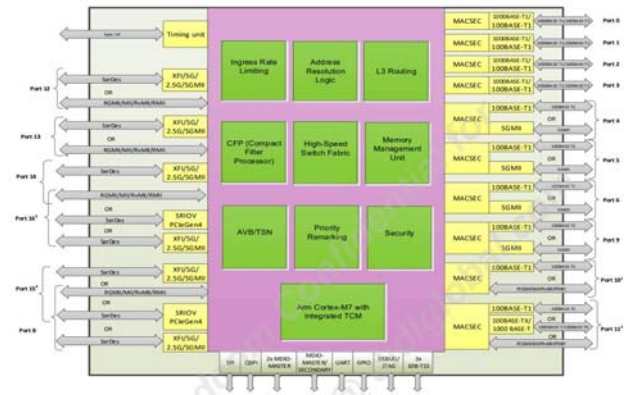
GPIO5:ID0
GPIO3:ID1

SW状态指示LED0 指示心跳

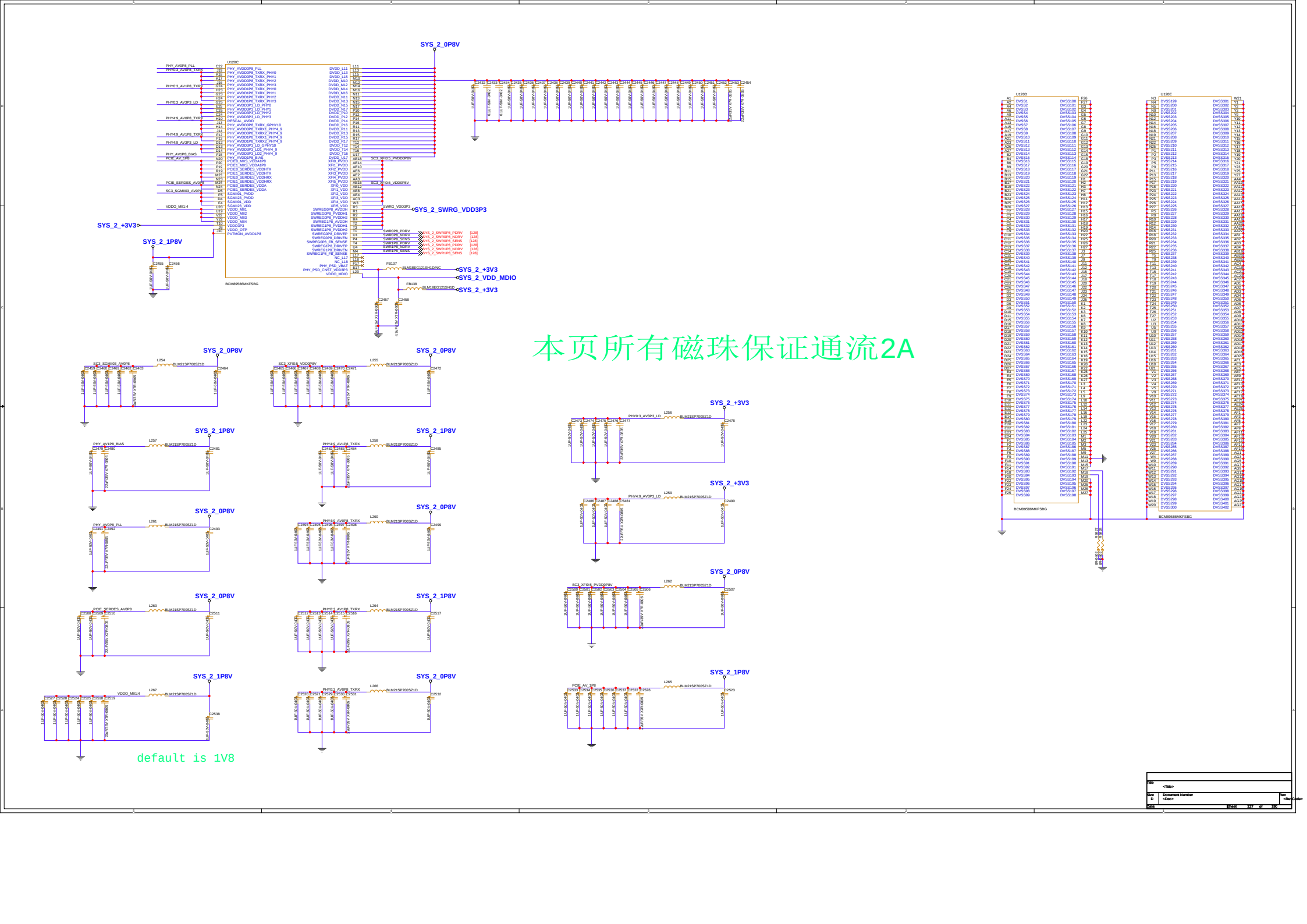
IIC SCL
IIC SDA

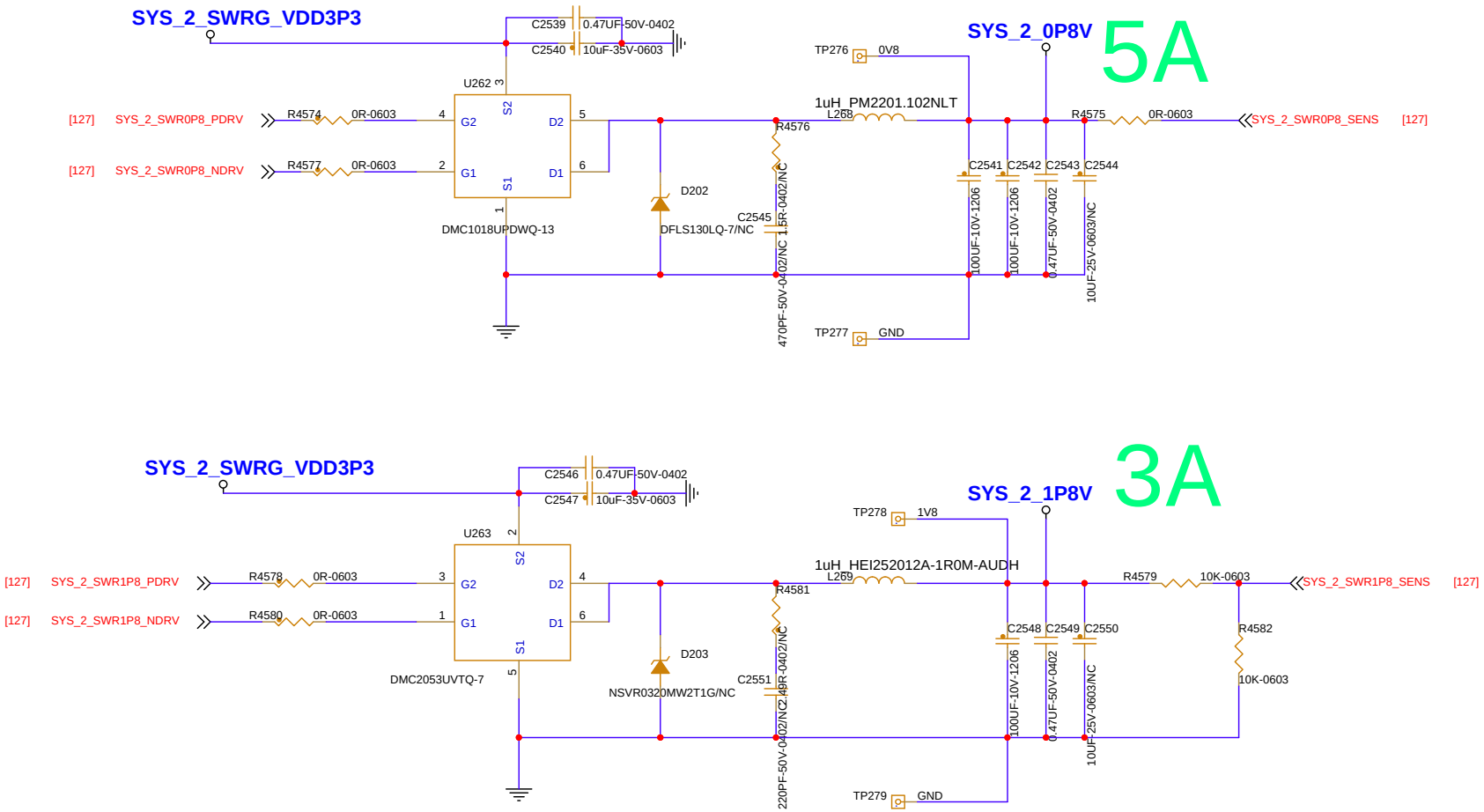
SPI Flash

Note: Place R169 a 0-ohm resistor to ground at SPI_SIO1 pin if flash-less mode is used. Remove this 0ohm resistor when the flash is attached.



1: Port 10 RGMII/MII/RvMII/RMII interface is available only if Port 12 RGMII/MII/RvMII/RMII interface is not used.
2: Port 11 RGMII/MII/RvMII/RMII interface is available only if Port 13 RGMII/MII/RvMII/RMII interface is not used.
3: Port 16 RGMII/MII/RvMII/RMII interface is available only if Port 14 RGMII/MII/RvMII/RMII interface is not used.
4: Port 15 RGMII/MII/RvMII/RMII interface is available only if Port 8 RGMII/MII/RvMII/RMII interface is not used. Port 15 PCIe interface is available only if Port 8 PCIe interface is not used.


SYS_2_0P8V
SYS_2_+3V3
SYS_2_1P8V
SYS_2_SWRG_VDD3P3
SYS_2_VDD_MDIO
本页所有磁珠保证通流2A
default is 1V8
U120C
U120D
U120E
BCM89586MKFSBG



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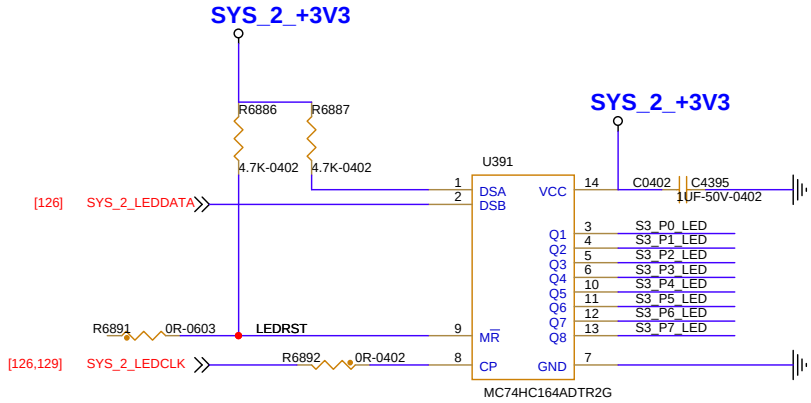
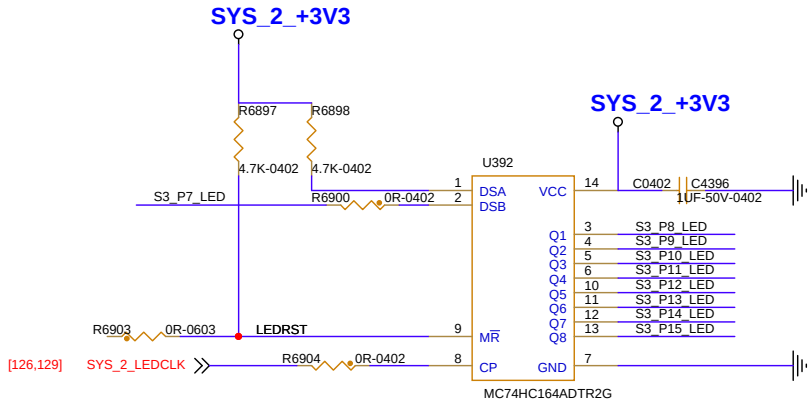
Size B	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 128 of 190	





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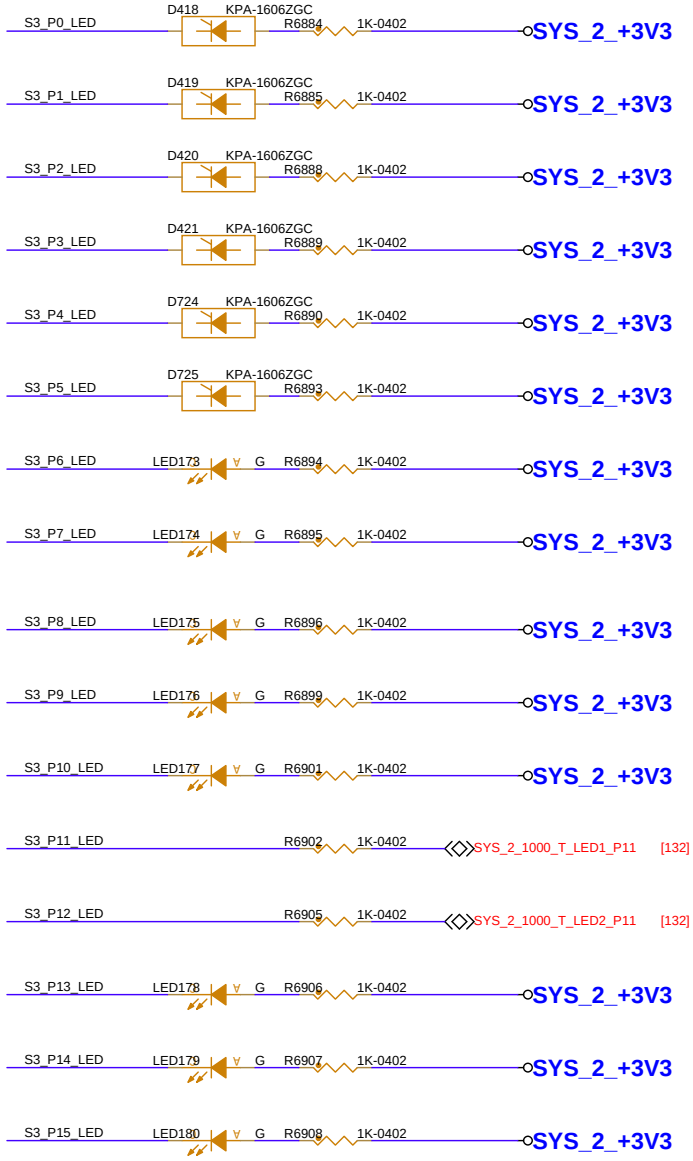

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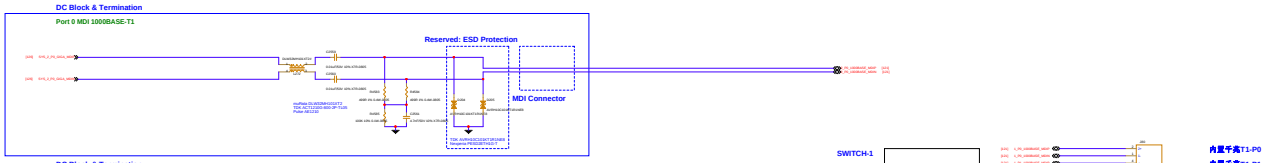
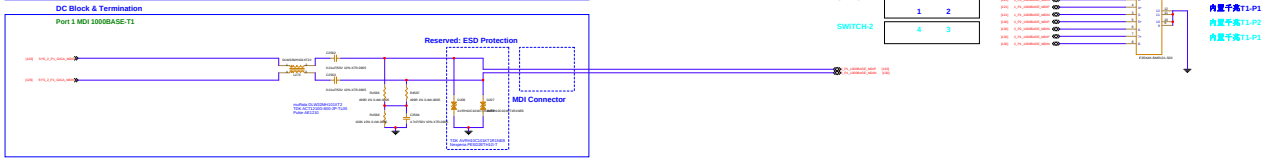
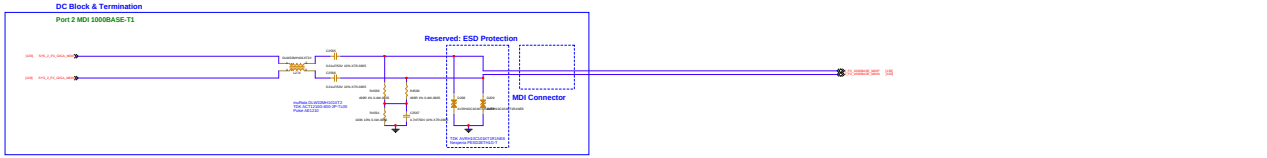
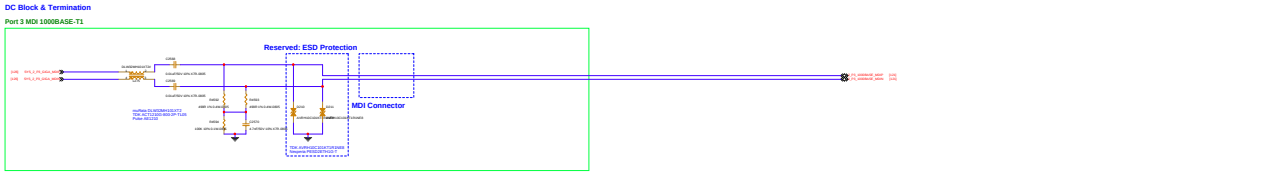
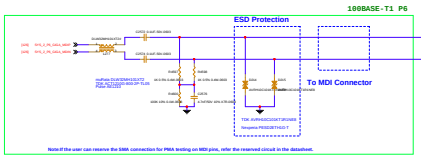

DC Block & Termination
Port 0 MDI 1000BASE-T1
Reserved: ESD Protection
MDI Connector

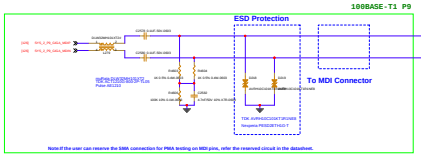

DC Block & Termination
Port 1 MDI 1000BASE-T1
Reserved: ESD Protection
MDI Connector

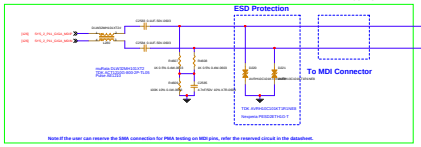

DC Block & Termination
Port 2 MDI 1000BASE-T1
Reserved: ESD Protection
MDI Connector

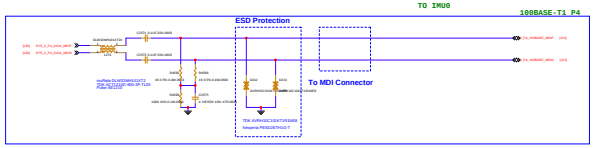

DC Block & Termination
Port 3 MDI 1000BASE-T1
Reserved: ESD Protection
MDI Connector
DC Block & Termination

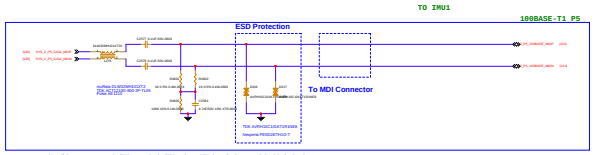
SWITCH-1
SWITCH-2
向里千兆T1-P0
向里千兆T1-P1
向里千兆T1-P2
向里千兆T1-P1


100BASE-T1 P6
ESD Protection
To MDI Connector
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.


100BASE-T1 P9
ESD Protection
To MDI Connector
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

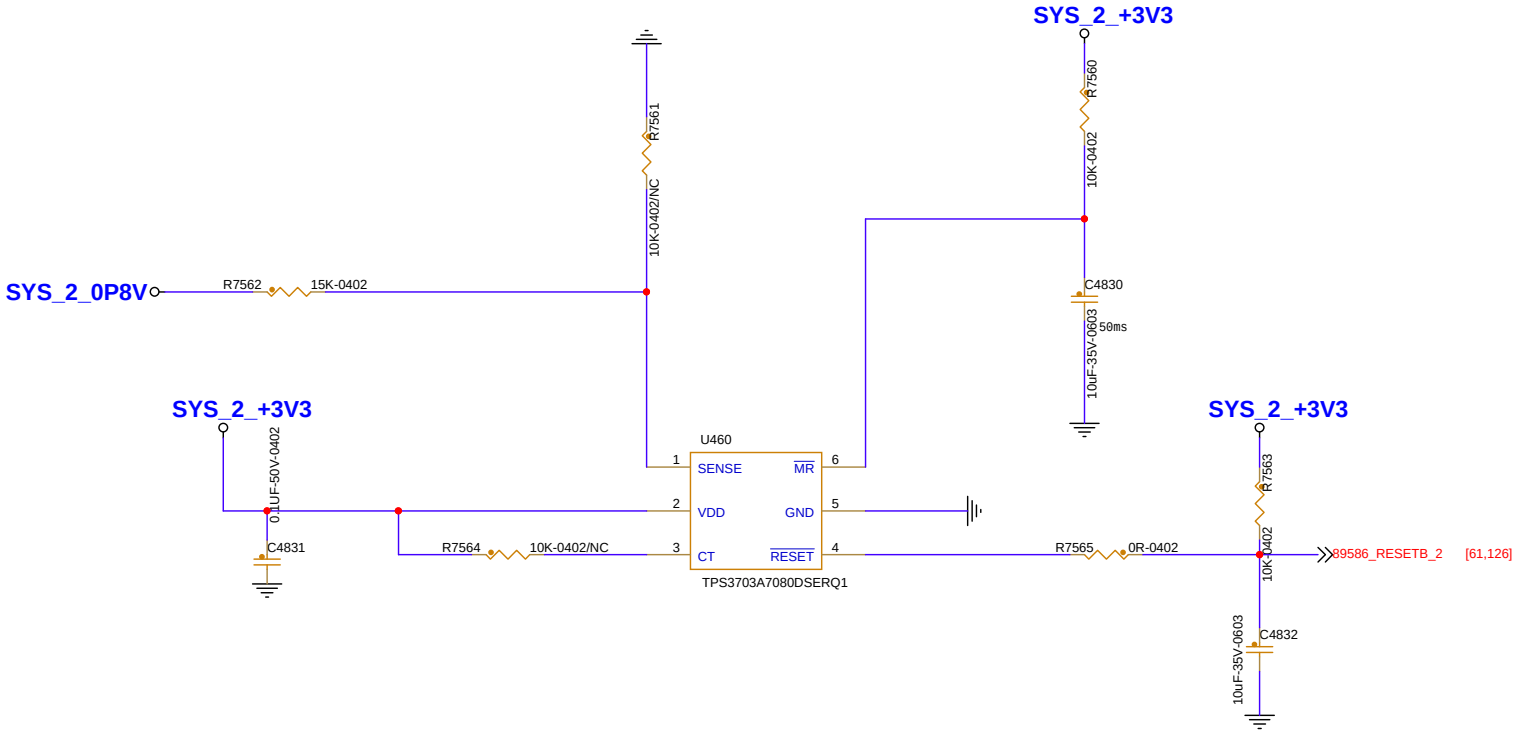

100BASE-T1 P11
ESD Protection
To MDI Connector
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.


TO IMU0
100BASE-T1 P4
ESD Protection
To MDI Connector
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.


TO IMU1
100BASE-T1 P5
ESD Protection
To MDI Connector
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

delay time is 10ms

89586M



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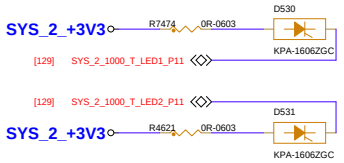

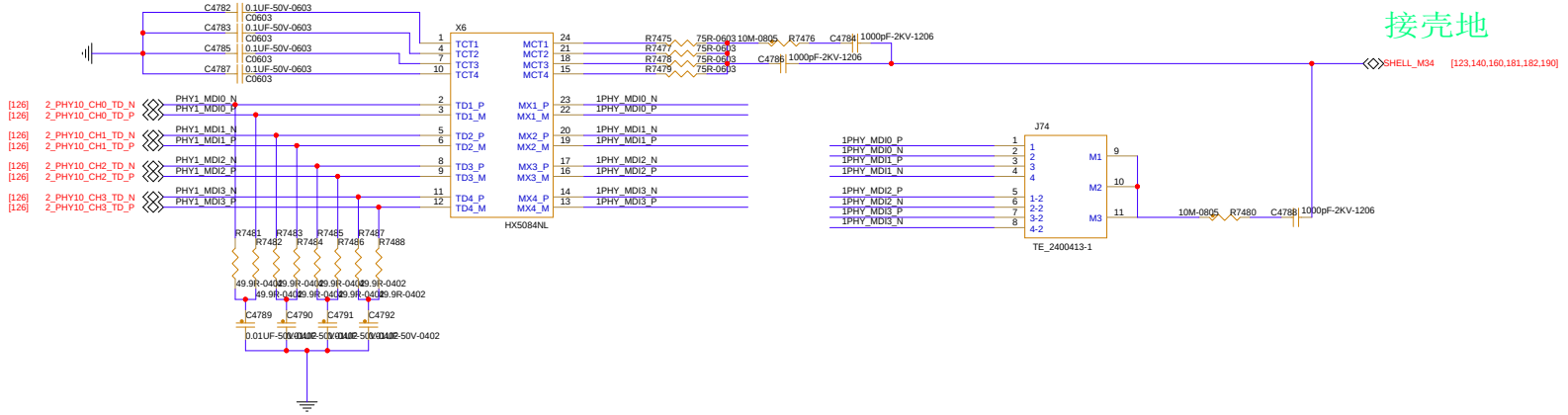

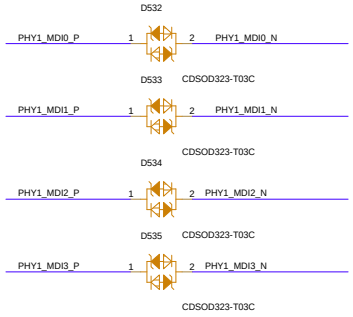

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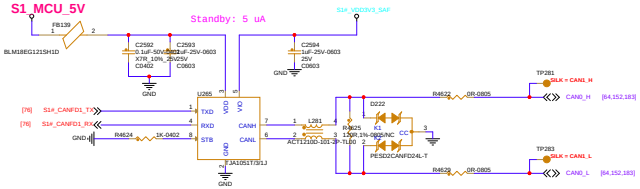
CAN #1



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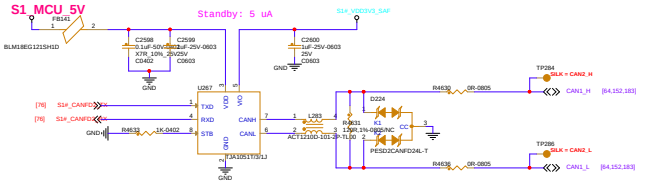
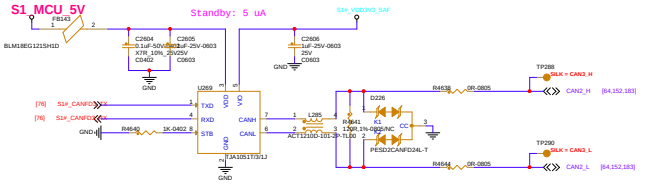


CAN #3



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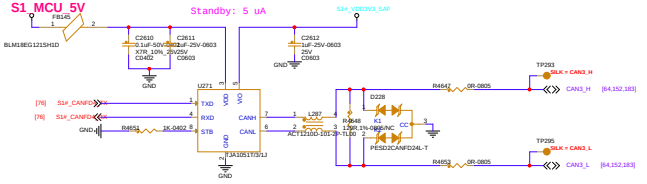

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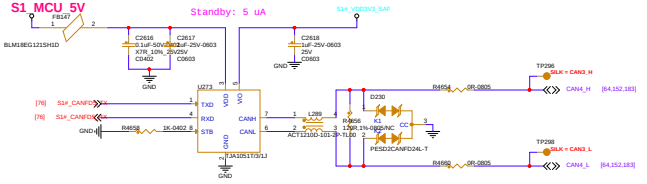
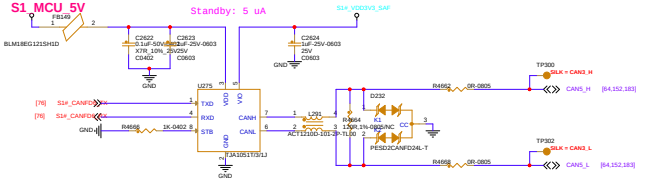


CAN #6

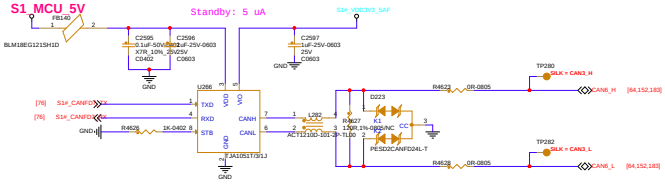


所有CAN总线LAYOUT差分处理

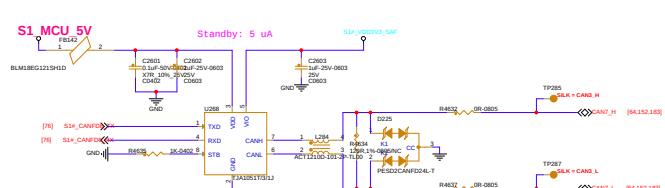
5V:0.5A 3.3V:0.5A

CAN #1-12 SAFETY

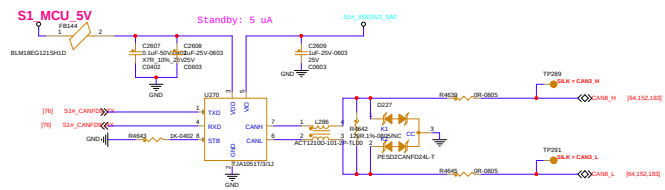
CAN #7



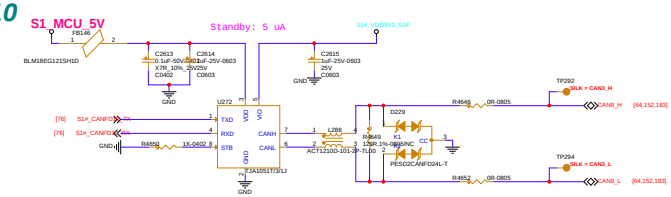
CAN #8



CAN #9



CAN #10



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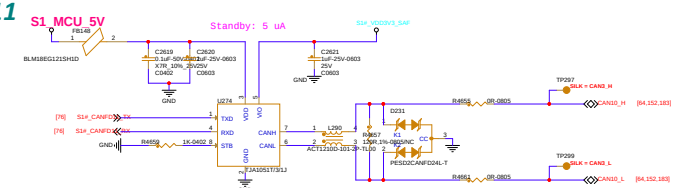

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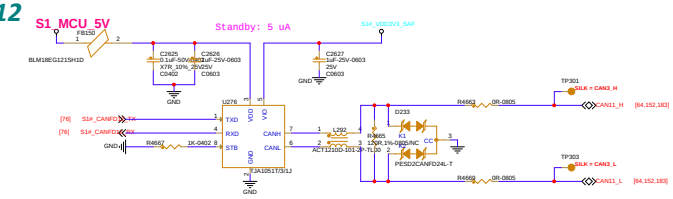

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Size: D	Document Number: <Doc>		Rev: <RevCode>
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Interface Name	Total Number of Interfaces	Port Number Mapping Options
1000BASE-T1/100BASE-T1/BroadR-Reach	4	Port 0, 1, 2, 3
100BASE-T1/BroadR-Reach	6	Port 4, 5, 6, 9, 10, 11
1-Gb/s SGMII	4	Port 4, 5, 6, 9
1000BASE-T/100Base-TX	1	Port 11
XFI/5G/2.5G/1G SerDes	6	Port 8, 12, 13, 14, 15,16
RGMII/MII/RvMII/RMII	4	Port 8, 10, 11, 12, 13, 14, 15, 16
PCIe Gen4	2	Port 8, 15, 16
Internal 1-Gb/s interface to an Arm subsystem	1	Port 7

GATEWAY-1

DISABLE auto-negotion
MASTER MODE
DISABLE ISOLATE MODE
enable global reset from safety monitor
EN FRAME FORWARD
LANE1 TO IPC
FORCE DOWNLOAD MODE
RGMII 1000
RGMII 1000
RGMII 1000
RGMII 1000
NORMAL 2 MODE:TC10 DIS
1000BASE-T1

Default is Crystal, 00

Crystal

P4 ORIN 2B 89586 IN / 89586 OUT
P5 ORIN 2A 89586 IN / 89586 OUT
P6 ORIN 1B 89586 IN / 89586 OUT
P9 ORIN 1A 89586 IN / 89586 OUT
P14-XFI0 89586 OUT
P15-XFI1
P16-XFI2
12-16、8: XFI P8-XFI3 (SGMII)
P12-XFI4
P13-XFI/SGMII

89586 IN
89586 OUT
P13-RGMII
89586 IN
89586 OUT
P8-RGMII
89586 IN
89586 OUT

MII1:P10 OR P12 RGMII
MII2:P11 OR P13 RGMII,P13
MII3:P8 OR P15 RGMII,P8

PCIE/NC
PCIE1:P8
PCIE0:P16

P14 OR P16 RGMII

P0-P3 1000-T1
P11
P4 P5 P6 P9 P10 P11

AD1

RS232-RX
RS232-TX

1000TX

DEBUG C OR F?

M IS PC

MDC/MDIO IS 3V3

P8 P13 3.3V---CHANGED

SMI MASTER TO PHY

P5 P6 P9 P4 3.3V

SMI MASTER TO PHY

SMI SLAVE
SMI MASTER TO PHY

GPIO4-7 IS PWM

ID CODE:0X01

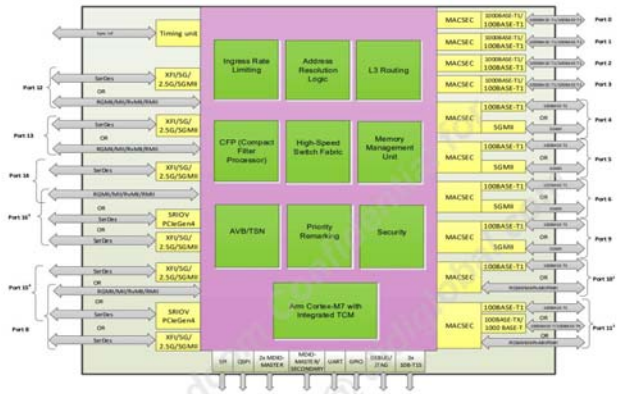
GPIO5:ID0
GPIO3:ID1

SW状态指示LED0 指示心跳

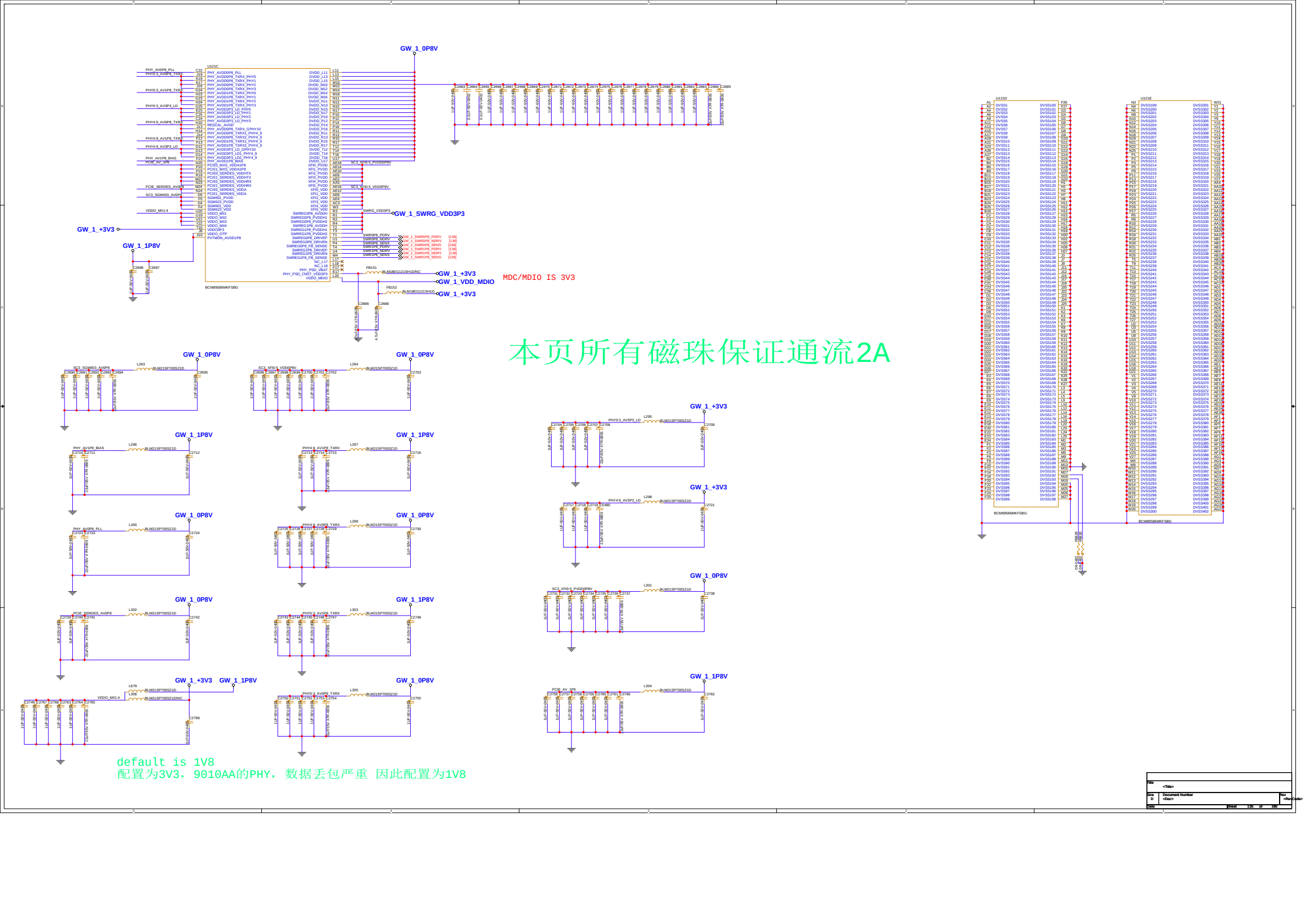
GPIO3:IIC SCL
GPIO5:IIC SDA

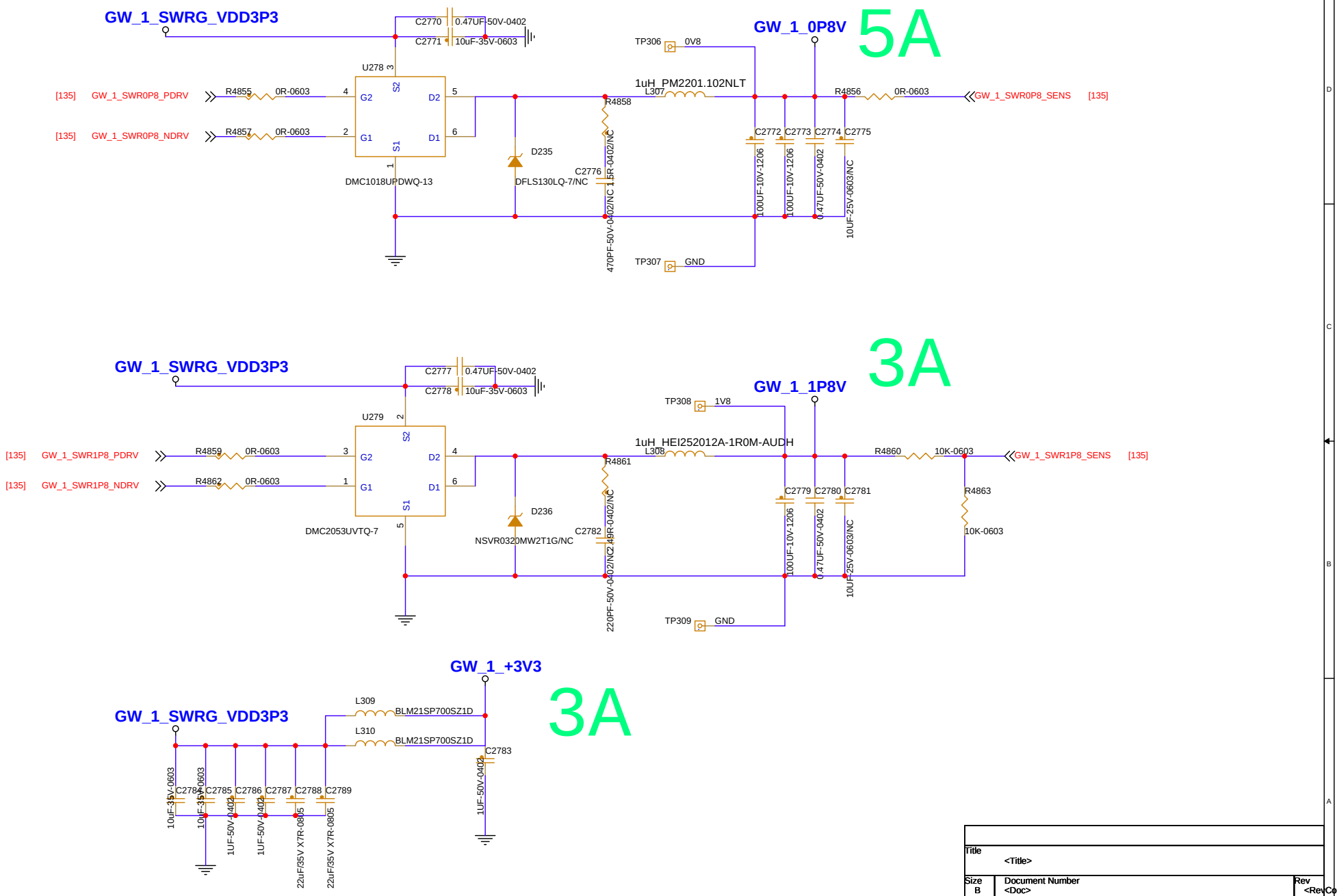
SPI Flash

Note: Place R169 a 0-ohm resistor to ground at SPI_SIO1 pin if flash-less mode is used. Remove this 0ohm resistor when the flash is attached.



1: Port 10 RGMII/MII/RvMII/RMII interface is available only if Port 12 RGMII/MII/RvMII/RMII interface is not used.
2: Port 11 RGMII/MII/RvMII/RMII interface is available only if Port 13 RGMII/MII/RvMII/RMII interface is not used.
3: Port 16 RGMII/MII/RvMII/RMII interface is available only if Port 14 RGMII/MII/RvMII/RMII interface is not used.
4: Port 15 RGMII/MII/RvMII/RMII interface is available only if Port 8 RGMII/MII/RvMII/RMII interface is not used. Port 15 PCIe interface is available only if Port 8 PCIe interface is not used.


GW_1_0P8V
GW_1_+3V3
GW_1_1P8V
GW_1_SWRG_VDD3P3
GW_1_VDD_MDIO
MDC/MDIO IS 3V3
本页所有磁珠保证通流2A
default is 1V8
配置为3V3，9010AA的PHY，数据丢包严重 因此配置为1V8



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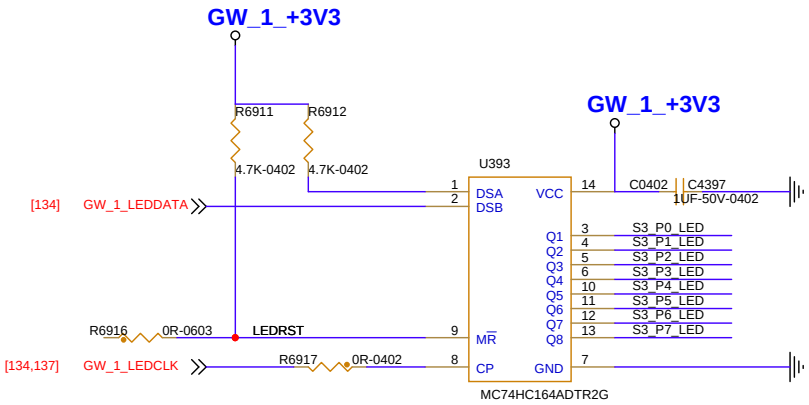

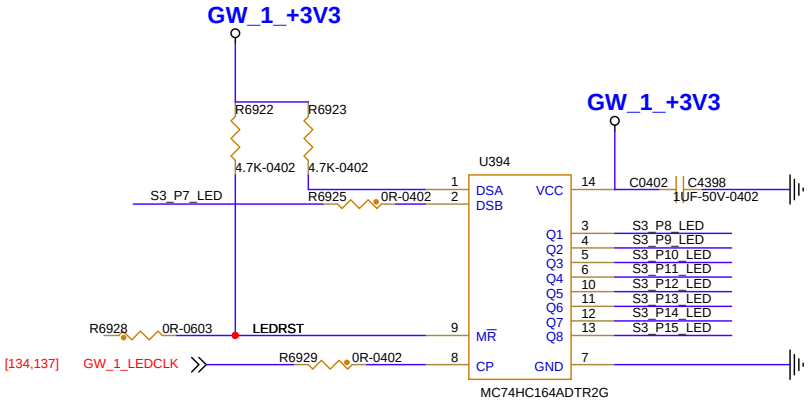

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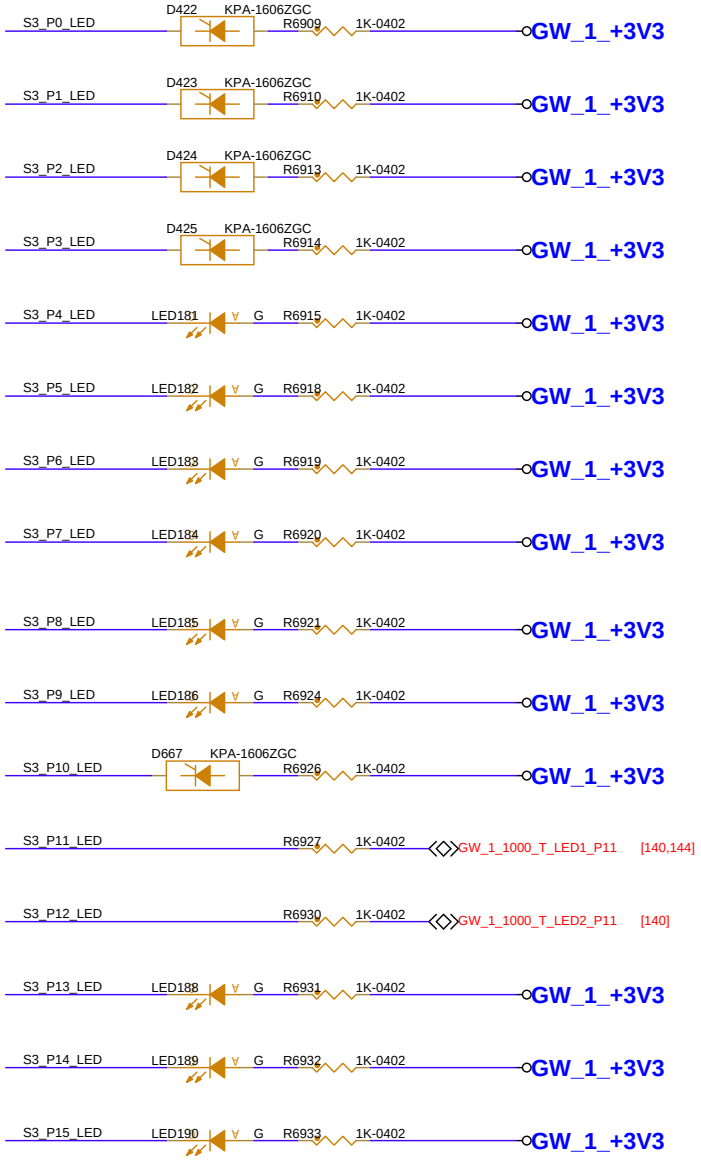

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Size B	Document Number <Doc>	Rev <RevCode>
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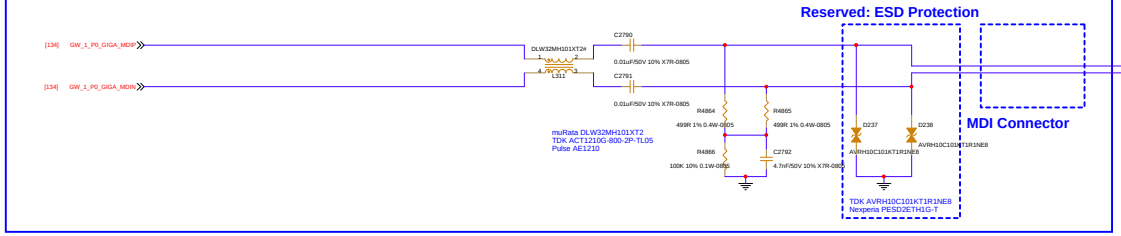
DC Block & Termination

Port 0 MDI 1000BASE-T1



SWITCH-1 1 2

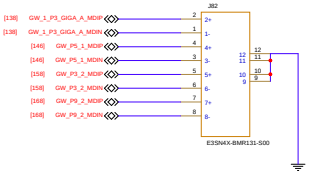
SWITCH-2 4 3

内置千兆T1-P3

SGMII-P5

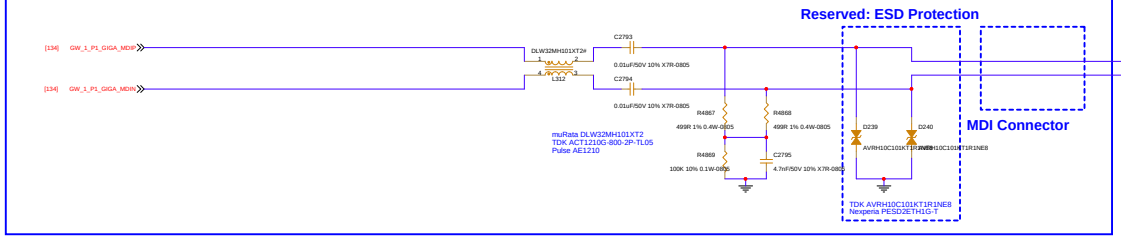
内置千兆T1-P3

SGMII-P9



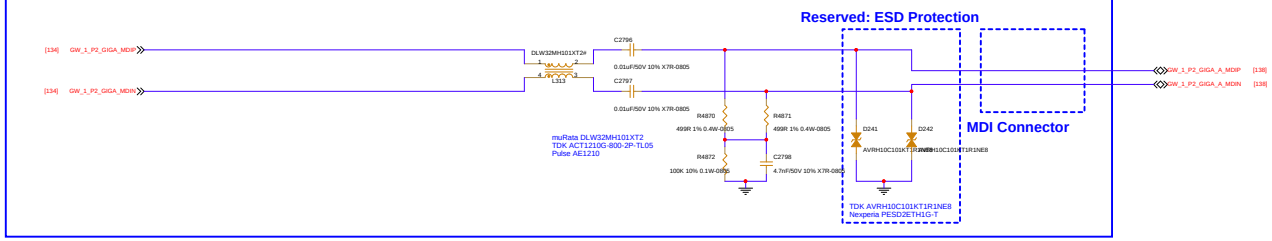
DC Block & Termination

Port 1 MDI 1000BASE-T1



DC Block & Termination

Port 2 MDI 1000BASE-T1



SWITCH-1 1 2

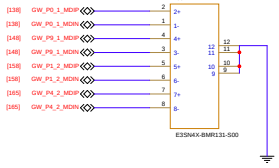
SWITCH-2 4 3

内置千兆T1-P0

SGMII-P9

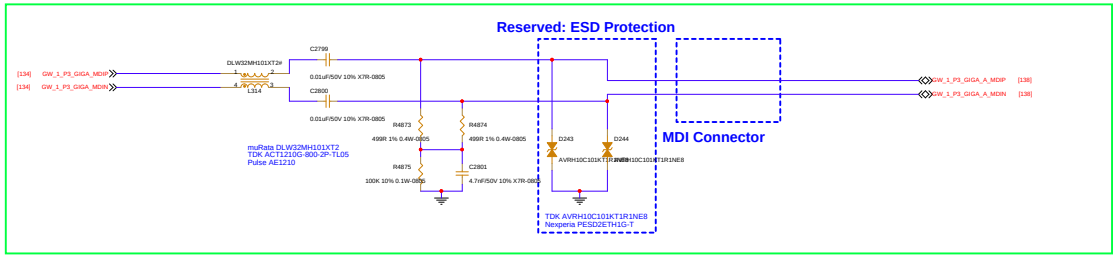
内置千兆T1-P1

SGMII-P4



DC Block & Termination

Port 3 MDI 1000BASE-T1



SWITCH-1 1 2

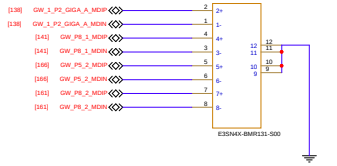
SWITCH-2 4 3

内置千兆T1-P2

RGMII-P8

SGMII-P5

RGMII-P8



DC Block & Termination

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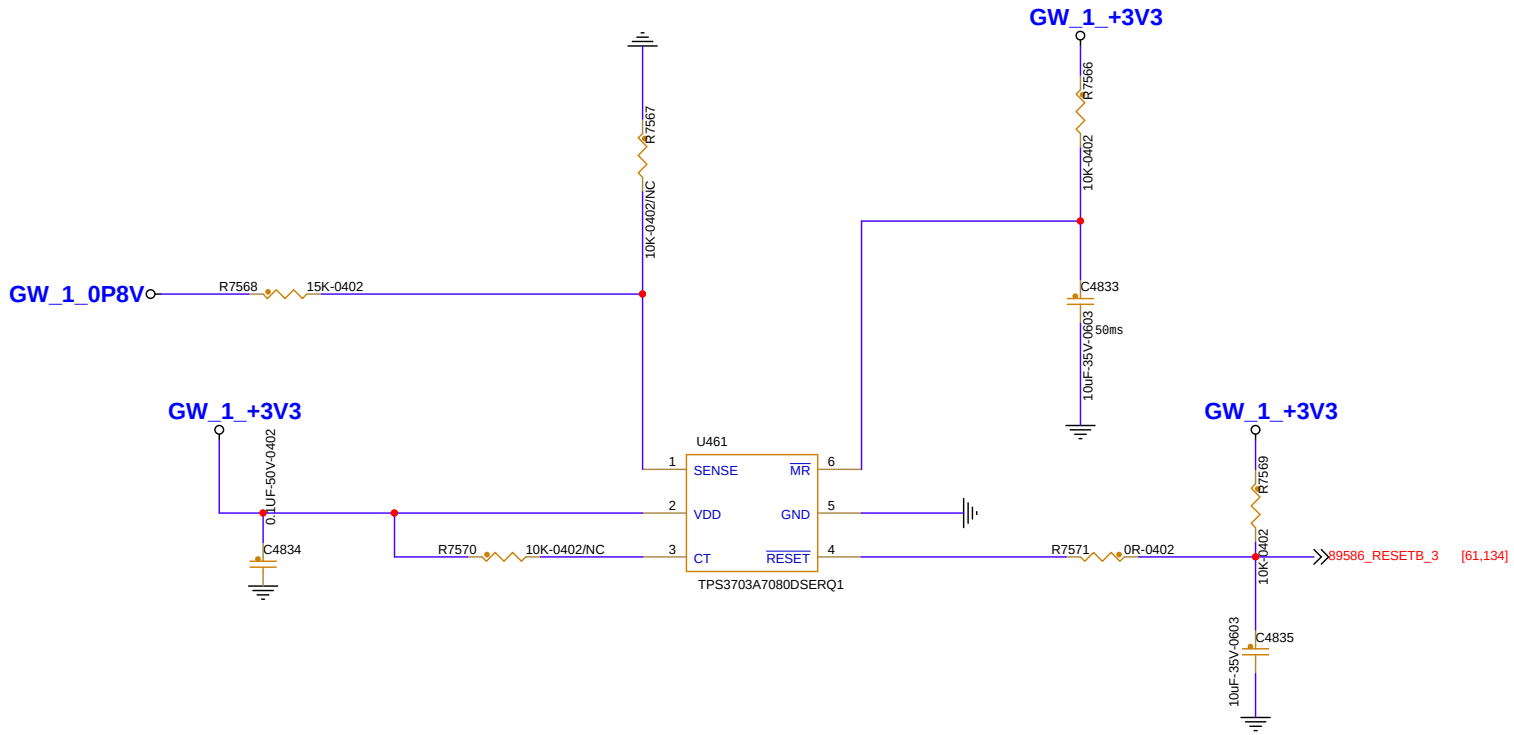
Size D	Document Number <Doc>		Rev <RevCode>
Date:		Sheet 138 of 190	

delay time is 10ms

89586M



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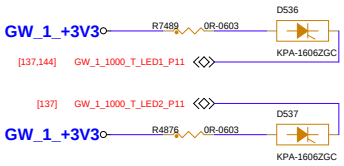
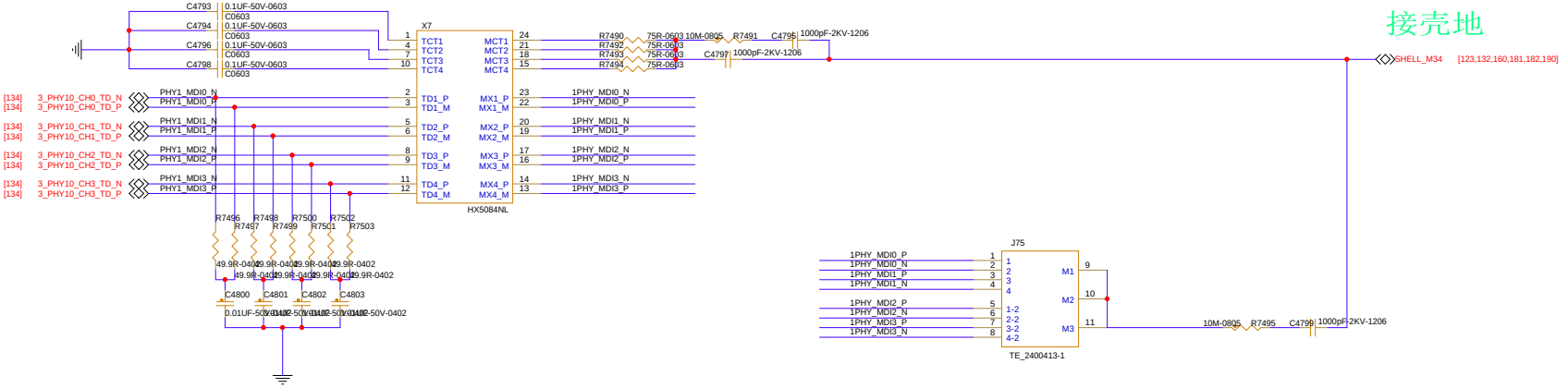
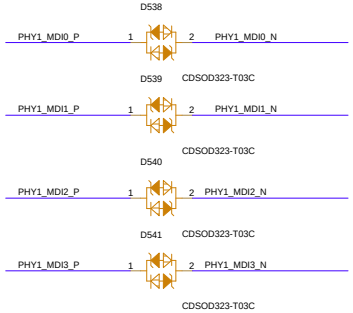
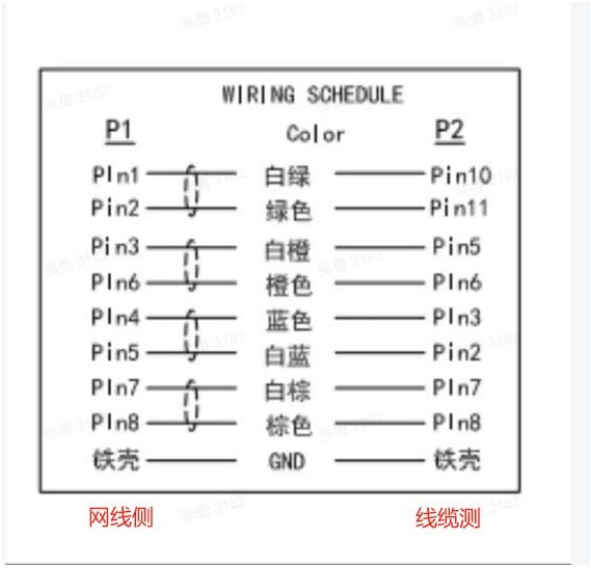
Date:	Sheet 139 of 190	









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Rev	<RevCode>
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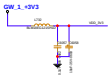


1.8V TTL

ADDR:0X00

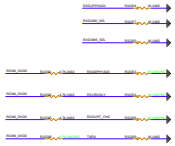
CLK SEL: CRYSTAL

AN_EN: DISABLE ANTO

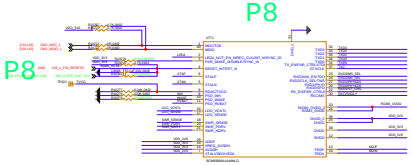
SPD: 1000-T1

MS SEL:MASTER

PAR_CTRL:01 DISABLE



P8



P8-RGMII

RGMII

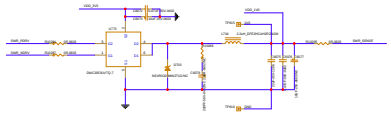
PHY OUT

89586 IN

PHY IN

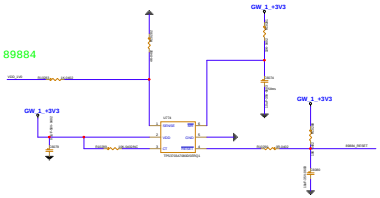
89586 OUT

Link/Act LED



delay time is 10ms

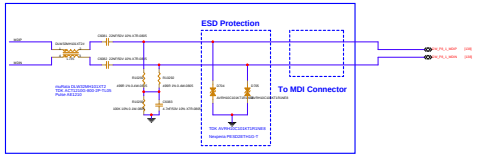
89884



DC Block & Termination

ESD Protection

To MDI Connector



Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

2.6.2 PHY Address

The BCM89884 allows a unique PHY address for the Management Interface. The address is set through the logic value of PHYA0, latched during reset. PHYA0 is shared with the RXD1. The BCM89884 checks each MII management read or write command and performs the operation only if the address in the command matches the latched PHY address stored in the device.

Table 9: PHY Address Settings

PHYA0	PHY Address
0	0x0
1	0x1

Figure 5 shows a typical layout for the Management interface. To set a PHY Address signal to 0, leave the signal floating. No external pull-down resistor is required since the PHYA0 address signal has internal pull-down resistors. To set the PHYA0 address signal to 1, install a 4.7-kΩ pull-up resistor (R_{PU}) to OVDD.

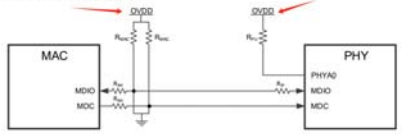
The MDIO signal typically require a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}), and series termination resistor near the PHY (R_{SP}) to match the trace impedance of the line. (Contact the MAC vendor for requirements.) For 50Ω traces, stuff R_{SP} with a 33Ω resistor.

The MDC signal typically requires a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}) to match the trace impedance of the line (contact the MAC vendor for requirements).

) and MDC Interfaces

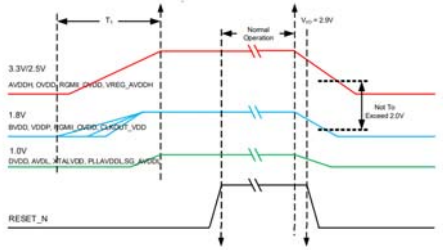
MDC interfaces can support either 2.5V or 3.3V operation depending on the voltage on the OVDD. The MDC le at rates up to 25 MHz. By default, the BCM89884 supports preamble suppression. This still requires a ones for the first MDIO transaction. To disable preamble suppression set DEVAD = 0x1, Address = 0xA000, and DEVAD = 0x1.

Figure 5: Management Interface Layout



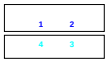
When a MAC is driving more than one PHY, a star topology, shown in Figure 6, can be used for clock distribution. In this approach, the stub lengths should be kept equal to obtain the best results.

Figure 10: Power-Up and Power-Down Sequence



SWITCH-1

SWITCH-2



SGMII-P6

RGMII-P13

内置千兆T1-P0

RGMII-P13

P8

ADRESS:0

1000BASE-T1 MASTER

RGMII MODE

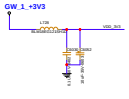
PHY管理 MDCMDIO 原生

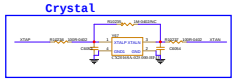
本页所有磁珠保证通流1A

RGMII 1.8V BANK

MDCMDIO 3.3V BANK

P8 13





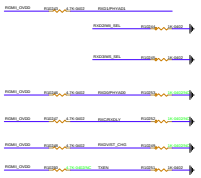
1.8V TTL
ADDR:0X01
CLK SEL: CRYSTAL

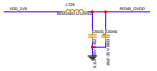
AN_EN: DISABLE ANTO

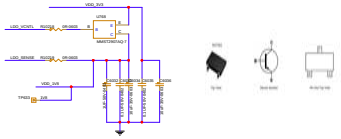
SPD: 1000-T1

MS SEL:MASTER

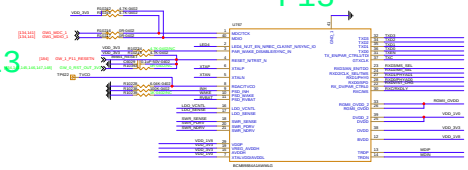
PAR_CTRL:01 DISABLE







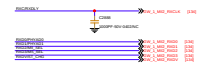
P13



P13

P13-RGMII

RGMII



PHY OUT

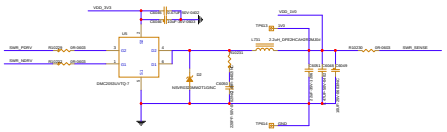
89586 IN

PHY IN

89586 OUT

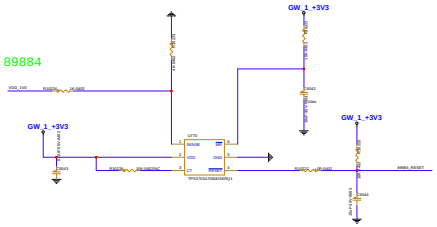
Note 1: Reserve R26-R31/C23 for driving and EMI consideration.
Note 2: Recommend to reserve R32-R37/C24 close to another chip.

Link/Act LED

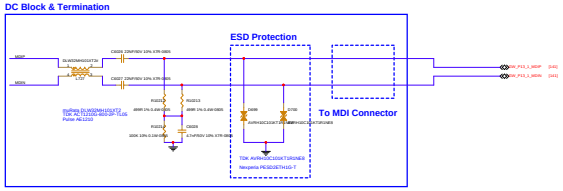


delay time is 10ms

89884



DC Block & Termination



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2.6.2 PHY Address

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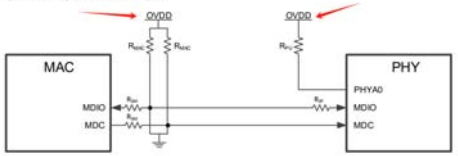
Figure 5: Management Interface Layout



When a MAC is driving more than one PHY, a star topology, shown in Figure 6, can be used for clock distribution. In this approach, the stub lengths should be kept equal to obtain the best results.

2.6.1 MDIO and MDC Interfaces

The MDIO and MDC interfaces can support either 2.5V or 3.3V operation depending on the voltage on the OVDD. The MDC clock can operate at rates up to 25 MHz. By default, the BCM89884 supports preamble suppression. This still requires a preamble of 32 ones for the first MDIO transaction. To disable preamble suppression set DEVAD = 0x1, Address = 0xA000, and bit[0] = 0x0.

Figure 10: Power-Up and Power-Down Sequence

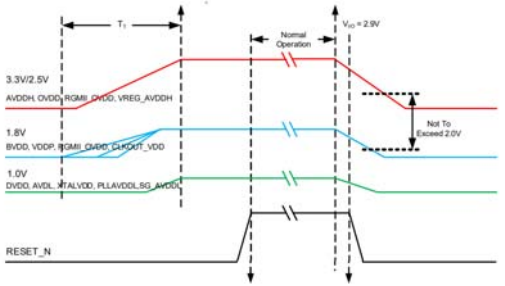
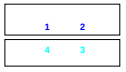


Table 2: MDI Hardware Configuration Settings

MDI Configuration	AN_EN	SPD	MS
Force 100BASE-T1 Secondary	0	0	0
Force 100BASE-T1 Master	0	0	1
Force 1000BASE-T1 Secondary	0	1	0
Force 1000BASE-T1 Master	0	1	1

SWITCH-1

SWITCH-2



内置千兆T1-P1

SGMII-P4

内置千兆T1-P2

SGMII-P6

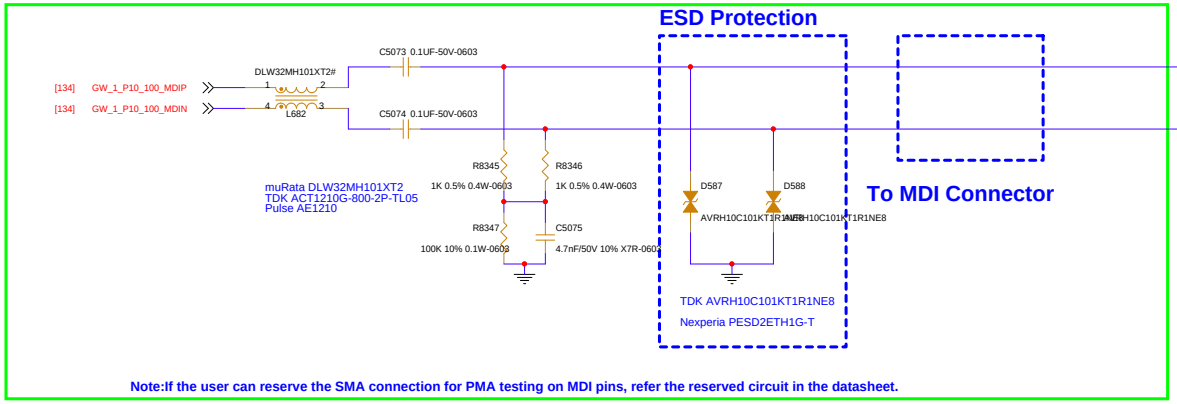
P13
ADRESS:1
1000BASE-T1 MASTER
RGMII MODE

PHY管理　MDC/MDIO原生

本页所有磁珠保证通流1A

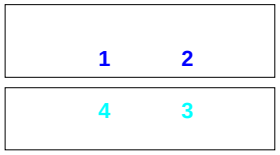
RGMII 1.8V BANK
MDCMDIO 3.3V BANK
P8 13

100BASE-T1 P10



SWITCH-1

SWITCH-2

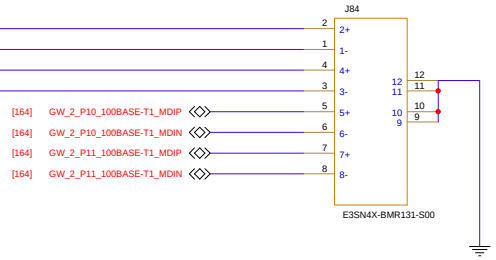


P10

P11

P10

P11



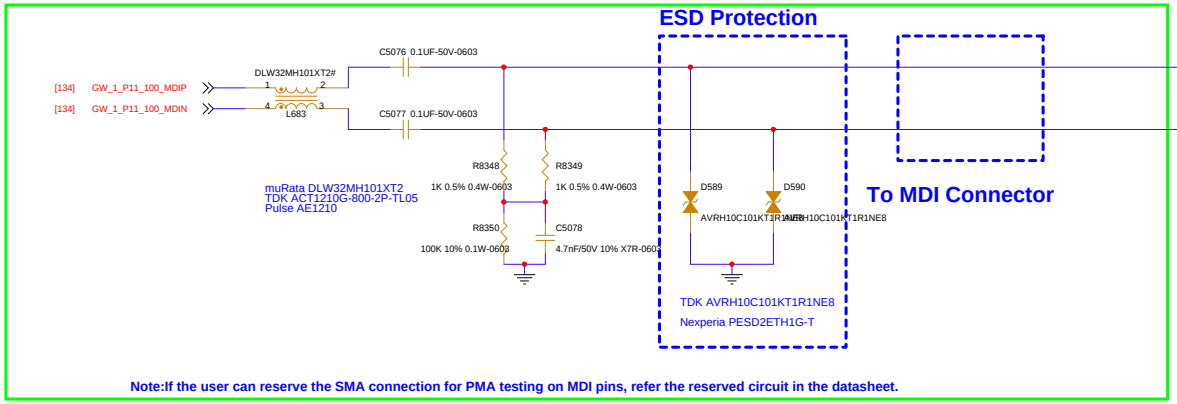
内置百兆T1-P10

内置百兆T1-P11

内置百兆T1-P10

内置百兆T1-P11

100BASE-T1 P11



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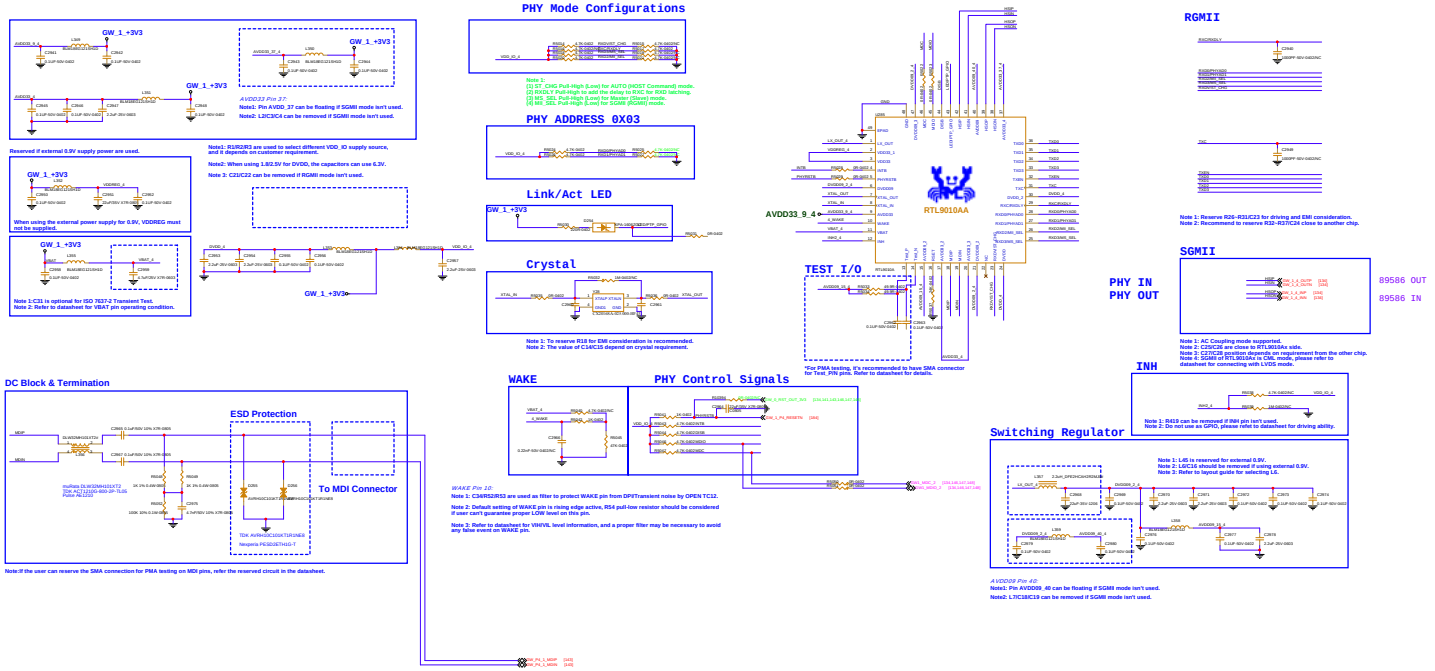


本页所有磁珠保证通流1A

ADRESS:3

1000BASE-T1 MASTER

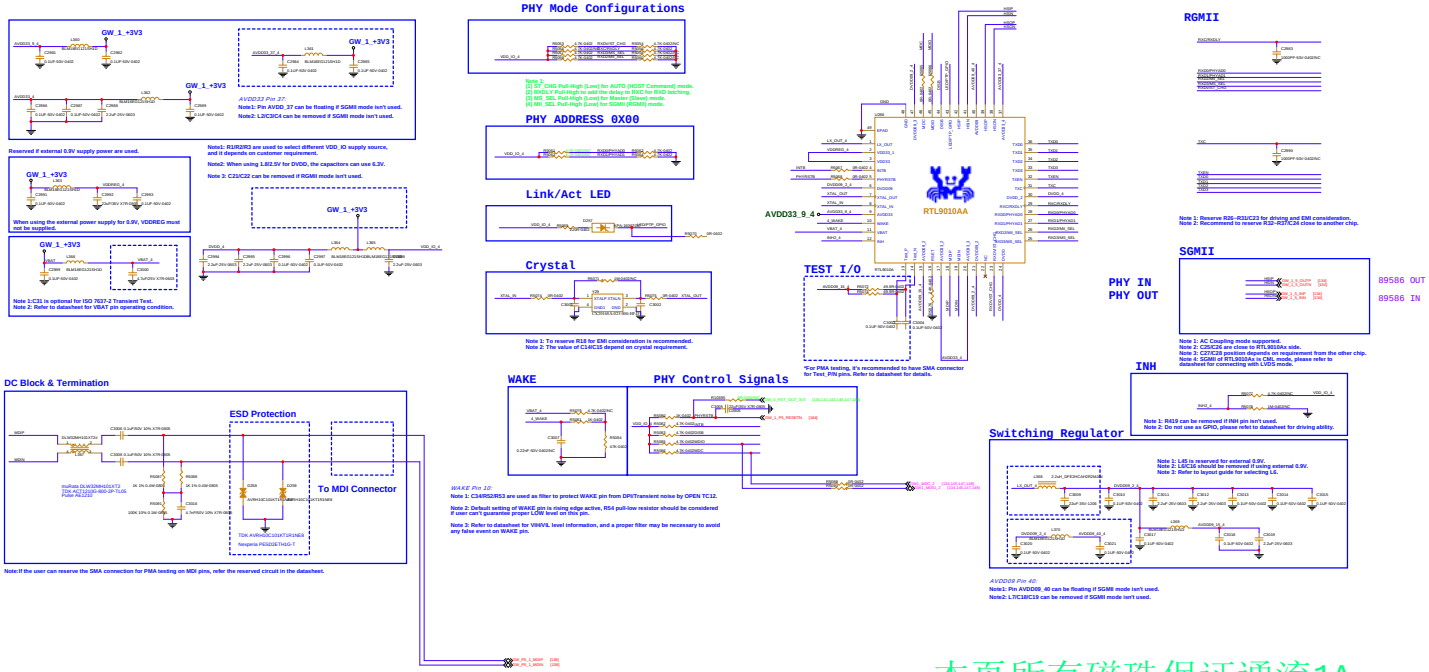
SGMII MODE

PHY管理　IO模拟

P4　3.3V IO

3.3V BANK

P5 6 9 4



本页所有磁珠保证通流1A

ADRESS:0

1000BASE-T1 MASTER

SGMII MODE

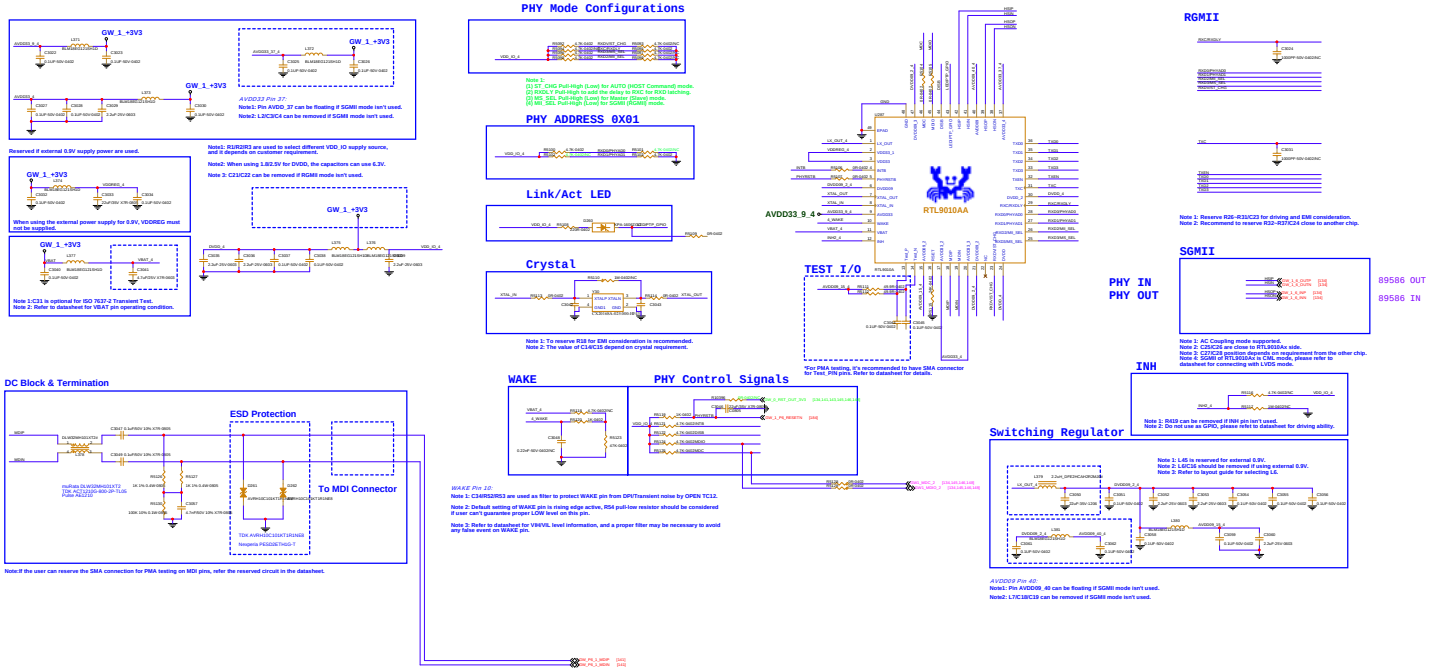
P5

3.3V IO

3.3V BANK

P5 6 9 4

PHY管理 MDC/MDIO原生



ADRESS:1

1000BASE-T1 MASTER

SGMII MODE

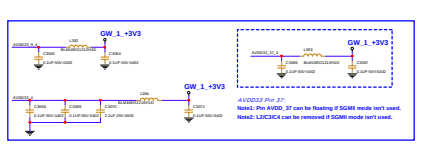
P6

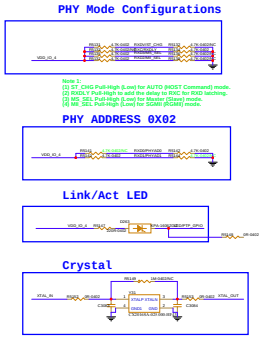
3.3V IO

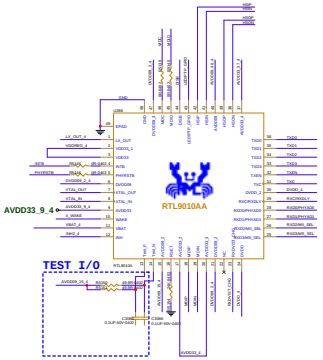
3.3V BANK

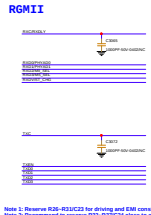
P5 6 9 4

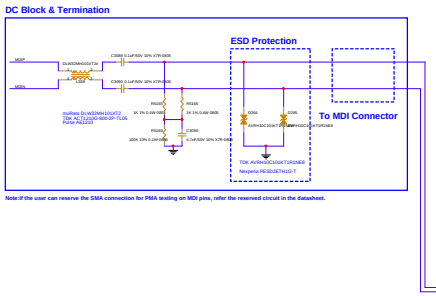
PHY管理 MDC/MDIO原生

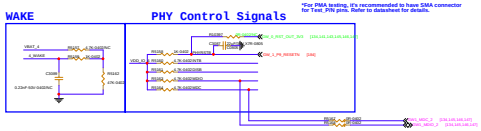


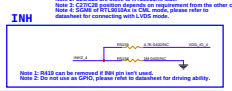


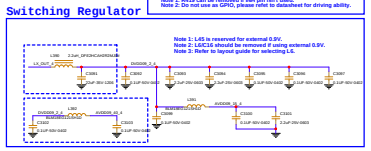












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ADRESS:2

1000BASE-T1 MASTER　　P9　　3.3V IO　　3.3V BANK

SGMII MODE　　P5 6 9 4

PHY管理　MDC/MDIO原生

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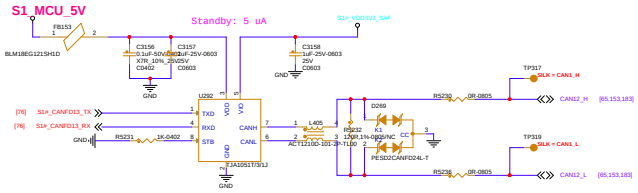
Size C	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 150 of 190	

CAN #13



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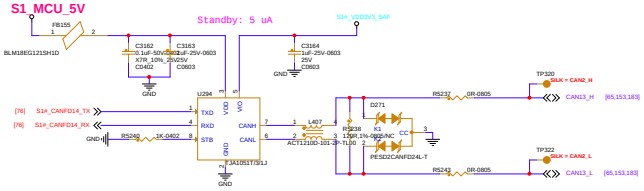

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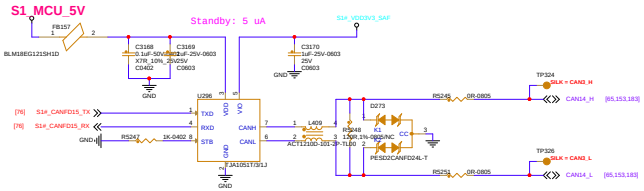

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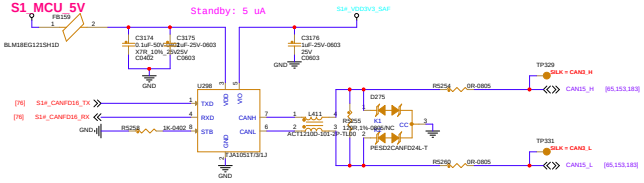

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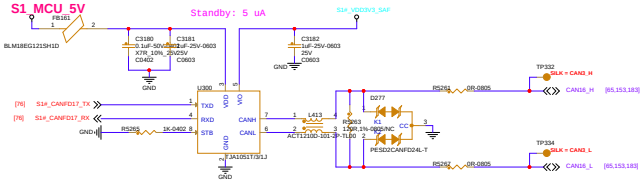

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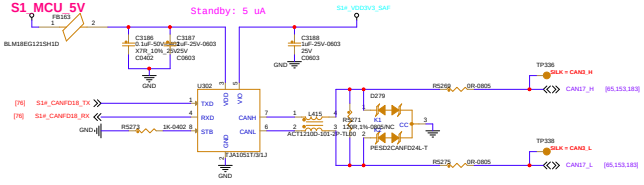

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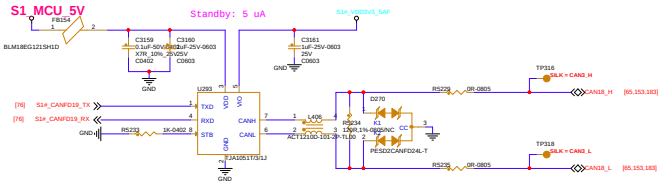
CAN #13-22 SAFETY

CAN #19



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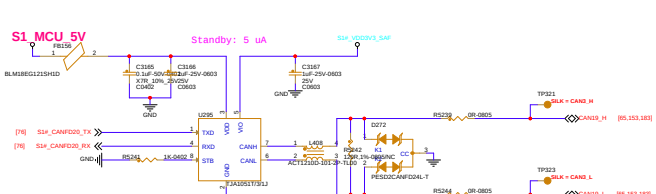

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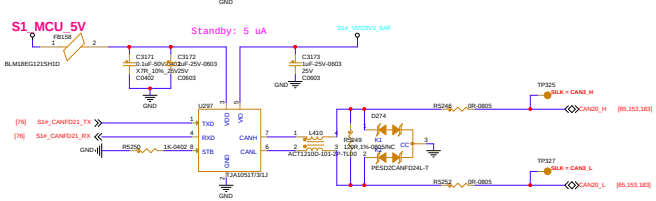

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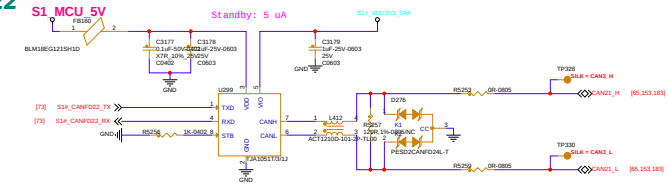

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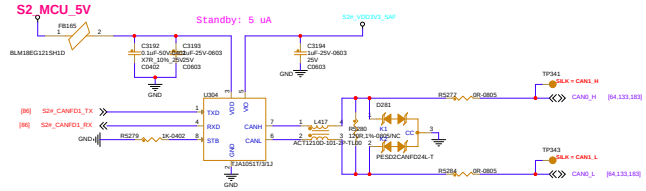

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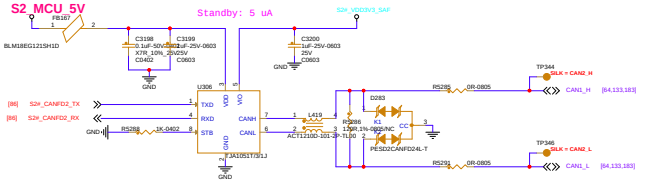

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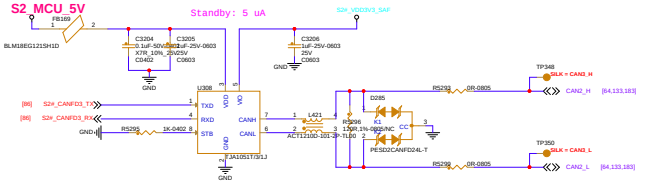

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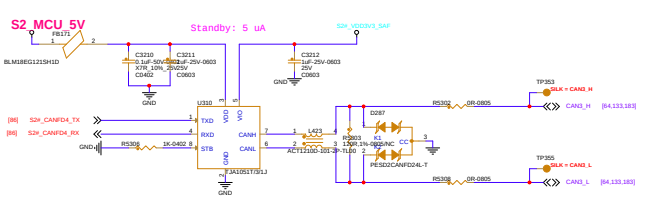

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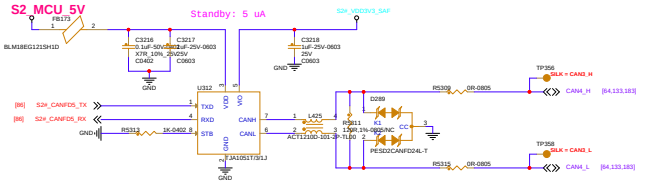

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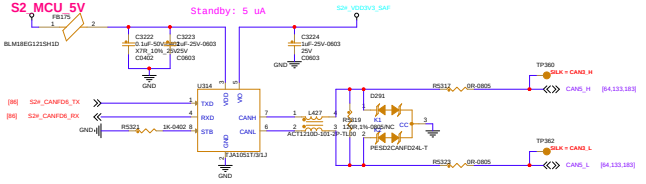

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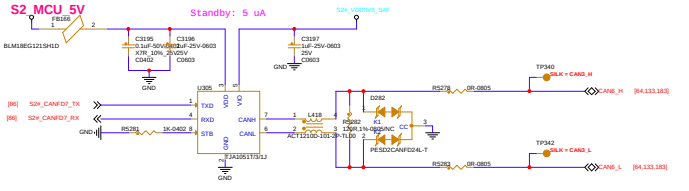
CAN #1-12 SAFETY

CAN #7



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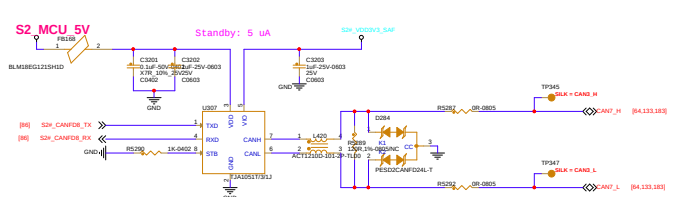

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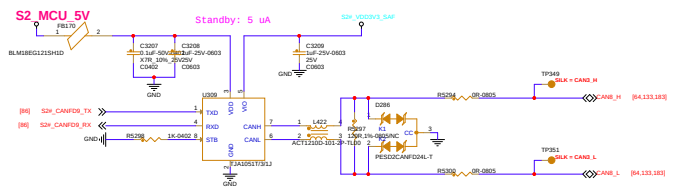

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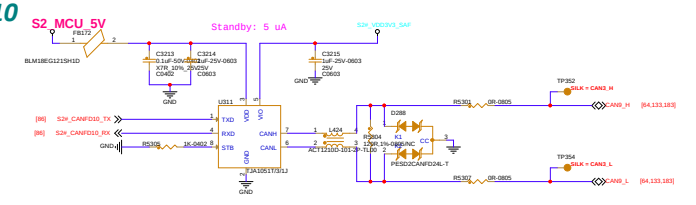

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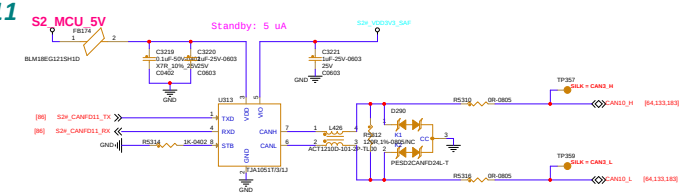

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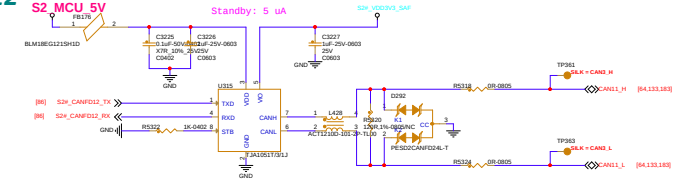

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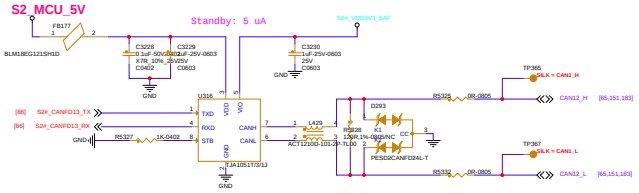

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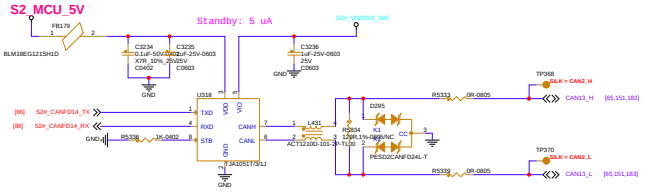

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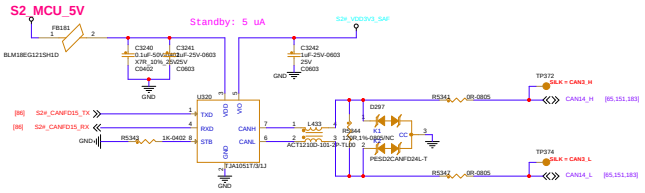

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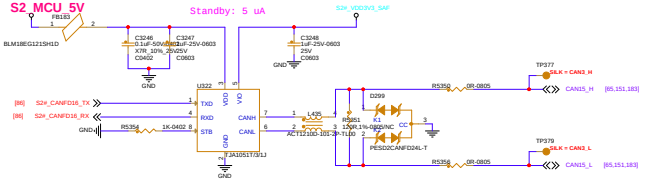

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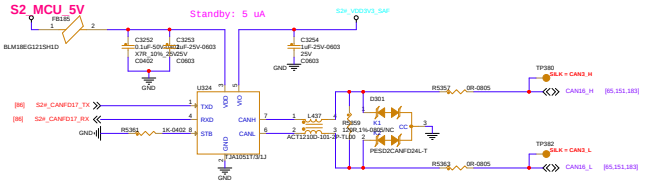

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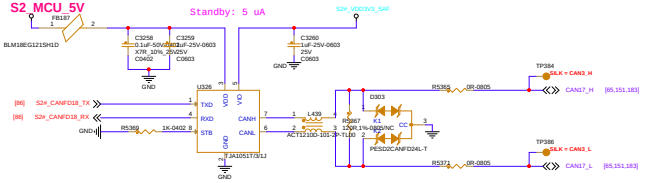

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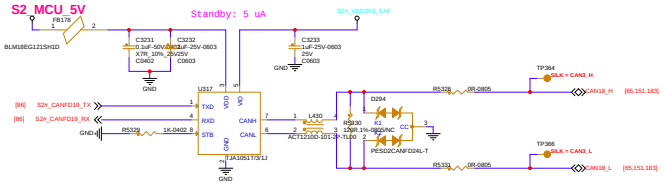

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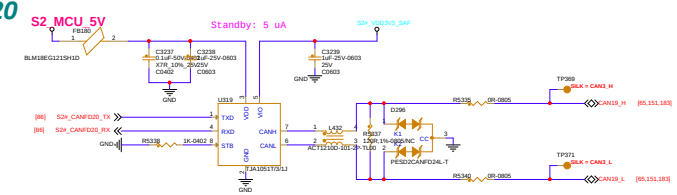

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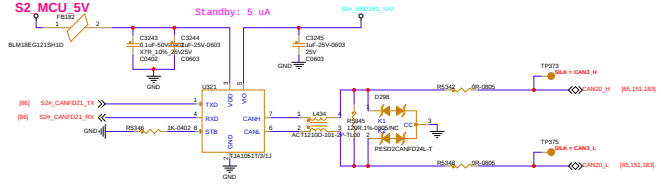

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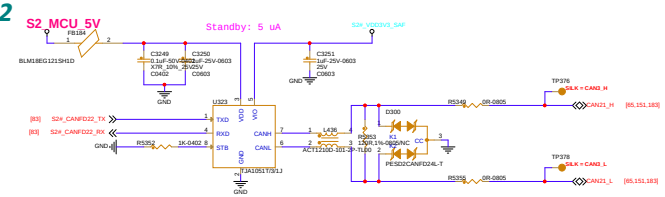

所有CAN总线LAYOUT差分处理

5V:0.5A 3.3V:0.5A

CAN #13-22 SAFETY

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Interface Name	Total Number of Interfaces	Port Number Mapping Options
1000BASE-T1/100BASE-T1/BroadR-Reach	4	Port 0, 1, 2, 3
100BASE-T1/BroadR-Reach	6	Port 4, 5, 6, 9, 10, 11
1-Gb/s SGMII	4	Port 4, 5, 6, 9
1000BASE-T/100Base-TX	1	Port 11
XFI/5G/2.5G/1G SerDes	6	Port 8, 12, 13, 14, 15,16
RGMII/MII/RvMII/RMII	4	Port 8, 10, 11 12, 13, 14, 15, 16
PCIe Gen4	2	Port 8, 15, 16
Internal 1-Gb/s interface to an Arm subsystem	1	Port 7

GATEWAY-2

DISABLE auto-negotion
MASTER MODE
DISABLE ISOLATE MODE
enable global reset from safety monitor
EN FRAME FORWARD
LANE1 TO IPC
FORCE DOWNLOAD MODE
RGMII 1000
RGMII 1000
RGMII 1000
RGMII 1000
NORMAL 2 MODE:TC10 DIS
1000BASE-T1

Default is Crystal：00

Crystal

AD1

P4 ORIN 2B 89586 IN
P5 ORIN 2A 89586 OUT
P6 ORIN 1B 89586 IN
P9 ORIN 1A 89586 OUT
89586 IN
89586 OUT
P14-XFI0
P15-XFI1
P16-XFI2
12-16. 8: XFI
P8-XFI3 (SGMII)
P12-XFI4
P13-XFI/SGMII

P10-RGMII
89586 IN
89586 OUT
P11-RGMII
89586 IN
89586 OUT

MII1:P10 OR P12 RGMII,P10
MII2:P11 OR P13 RGMII,P13

P8-RGMII
89586 IN
89586 OUT

MII3:P8 OR P15 RGMII,P8

P14 OR P16 RGMII

PCIE/NC
PCIE1:P8
PCIE0:P16

P0-P3 1000-T1

P11

P4
P5
P6
P9
P10
P11

1000TX

DEBUG C OR F?

M IS PC

RS232-RX
RS232-TX

MDC/MDIO IS 3V3

P8 P13 3.3V---CHANGED

SMI MASTER TO PHY

P5 P6 P9 P4 3.3V

SMI MASTER TO PHY

SMI SLAVE
SMI MASTER TO PHY

GPIO4-7 IS PWM

ID CODE:0X03

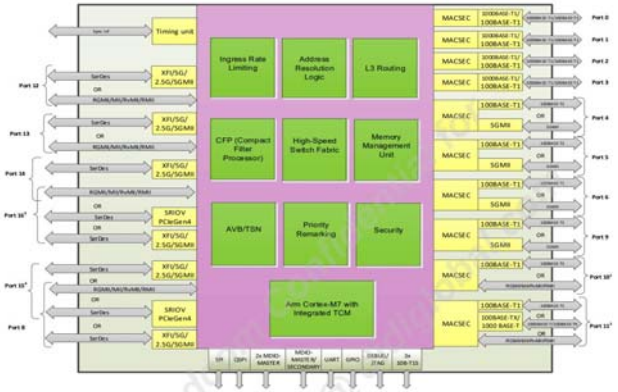
GPIO5:ID0
GPIO3:ID1

SW状态指示LED0 指示心跳

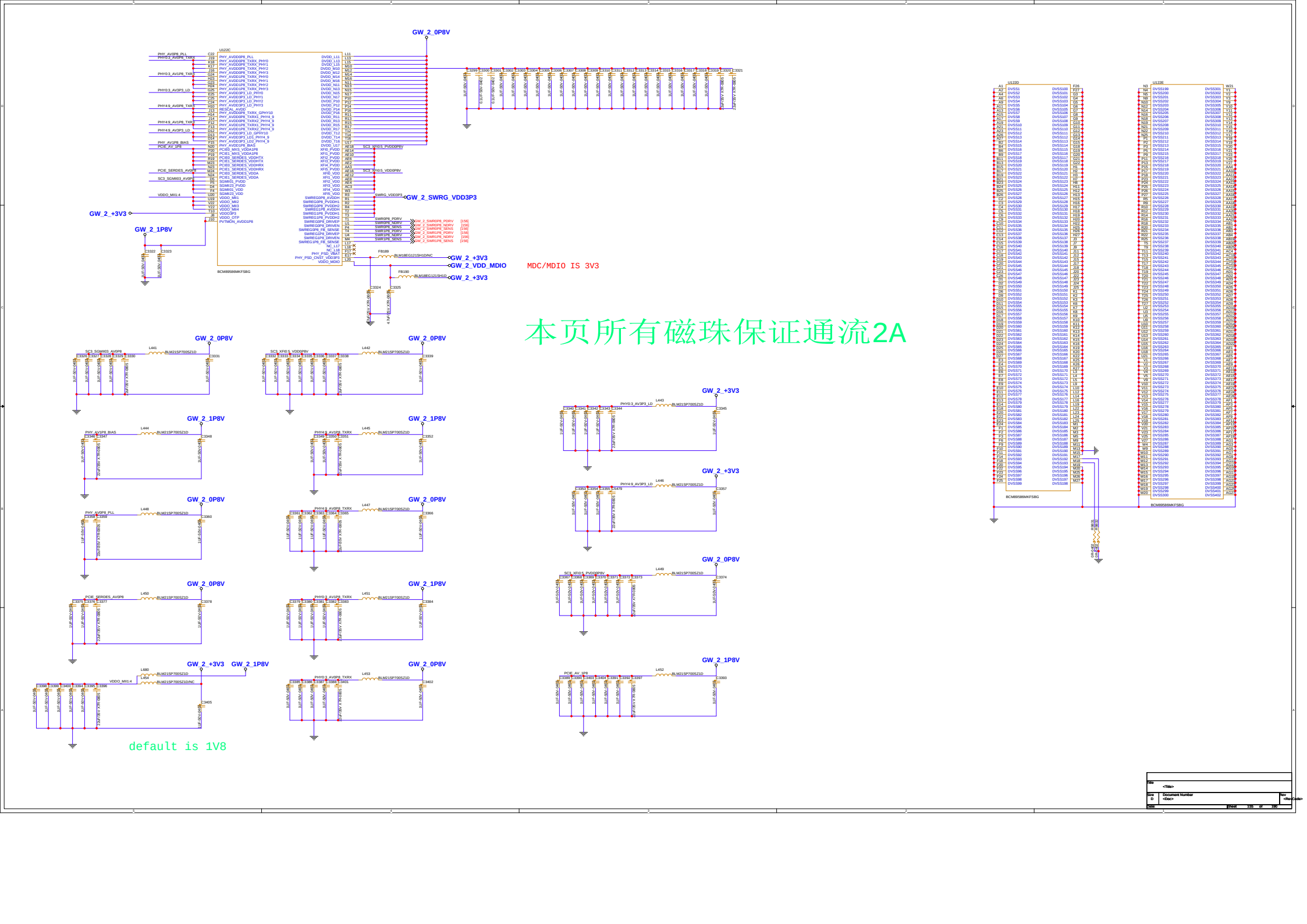
GPIO3:IIC SCL
GPIO5:IIC SDA

SPI Flash

Note: Place R169 a 0-ohm resistor to ground at SPI_SIO1 pin if flash-less mode is used. Remove this 0ohm resistor when the flash is attached.



1: Port 10 RGMII/MII/RvMII/RMII interface is available only if Port 12 RGMII/MII/RvMII/RMII interface is not used.
2: Port 11 RGMII/MII/RvMII/RMII interface is available only if Port 13 RGMII/MII/RvMII/RMII interface is not used.
3: Port 16 RGMII/MII/RvMII/RMII interface is available only if Port 14 RGMII/MII/RvMII/RMII interface is not used.
4: Port 15 RGMII/MII/RvMII/RMII interface is available only if Port 8 RGMII/MII/RvMII/RMII interface is not used. Port 15 PCIe interface is available only if Port 8 PCIe interface is not used.


GW_2_0P8V
GW_2_+3V3
GW_2_1P8V
GW_2_SWRG_VDD3P3
GW_2_VDD_MDIO
MDC/MDIO IS 3V3
本页所有磁珠保证通流2A
default is 1V8
U122C
BCM89586MKFSBG
U122D
U122E
BCM89586MKFSBG
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<Title>
Size
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Document Number
<Doc>
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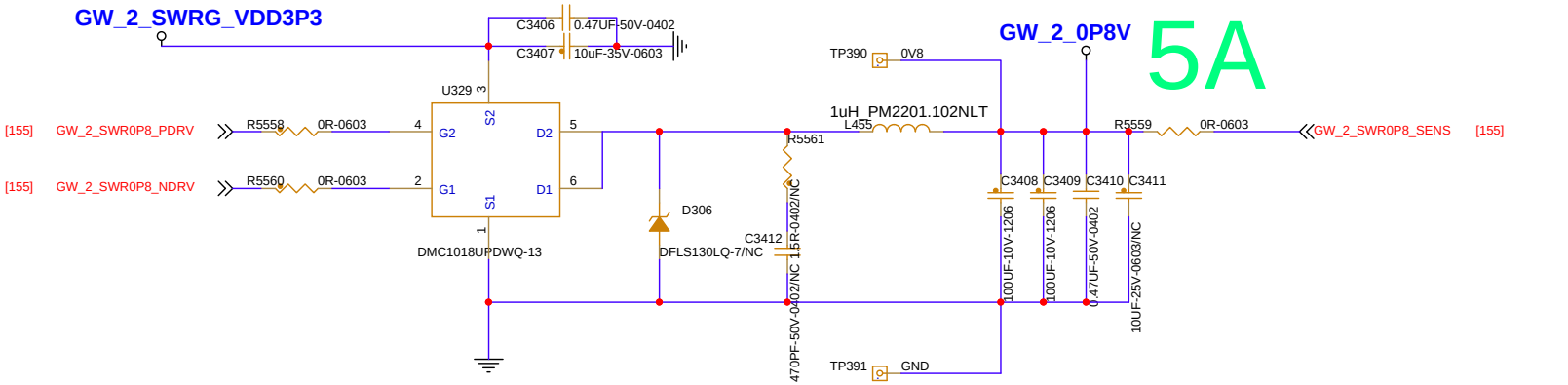

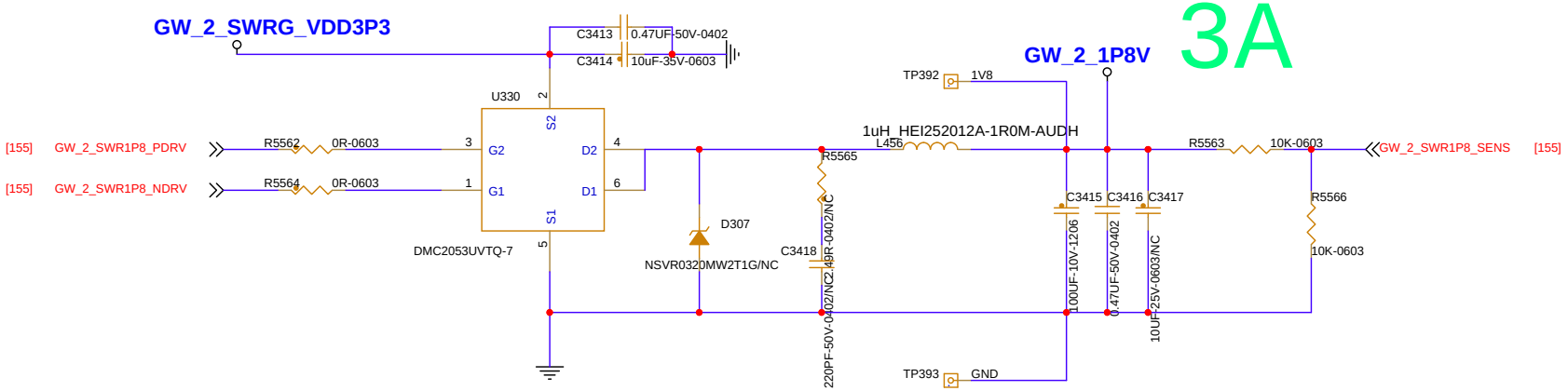

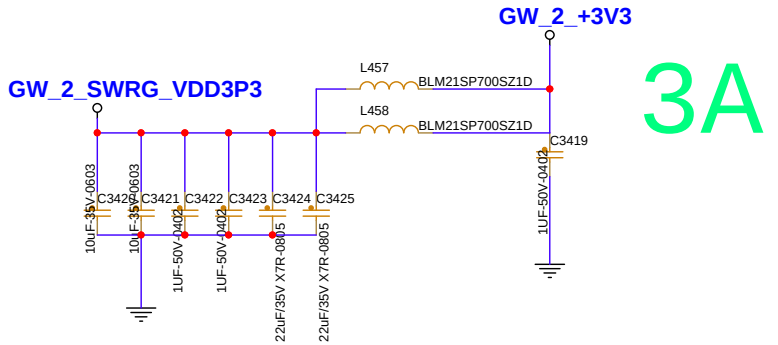

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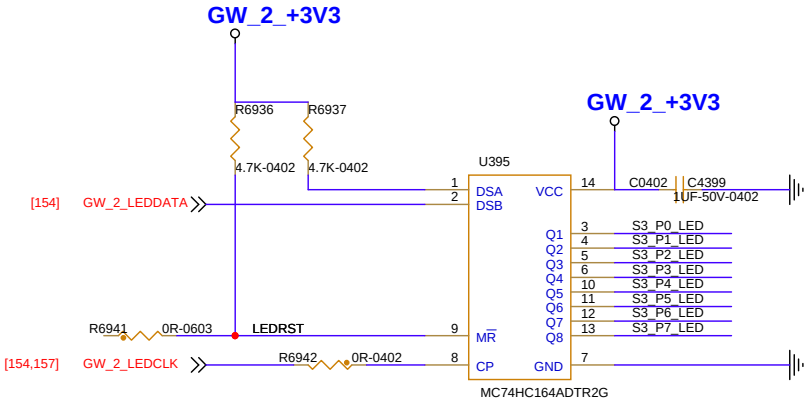

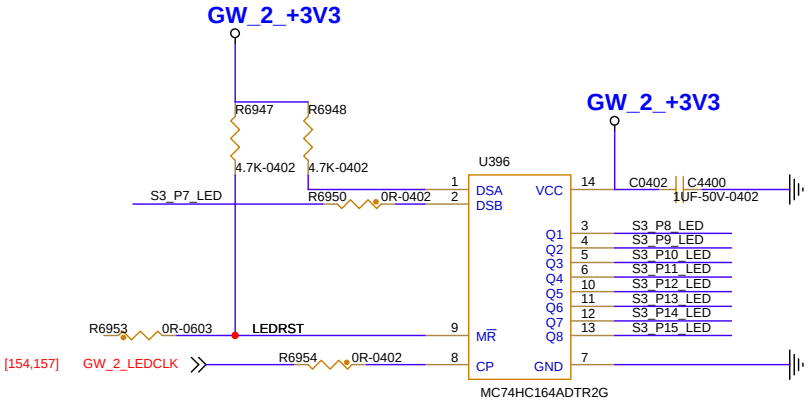

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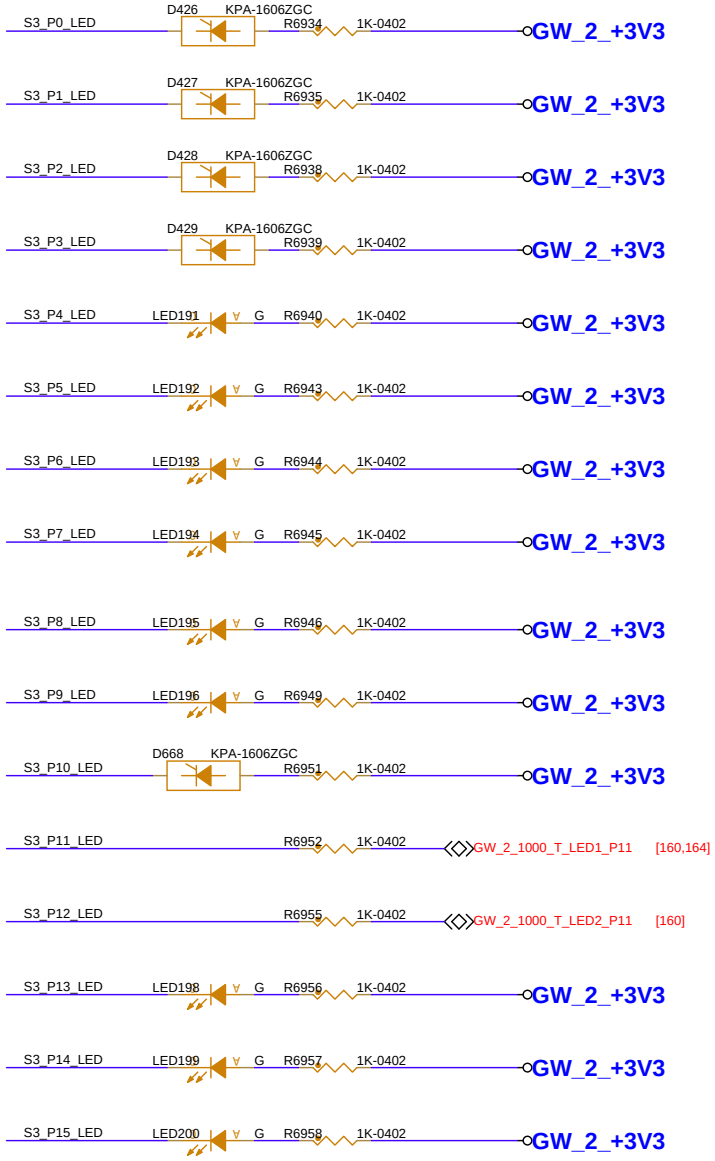

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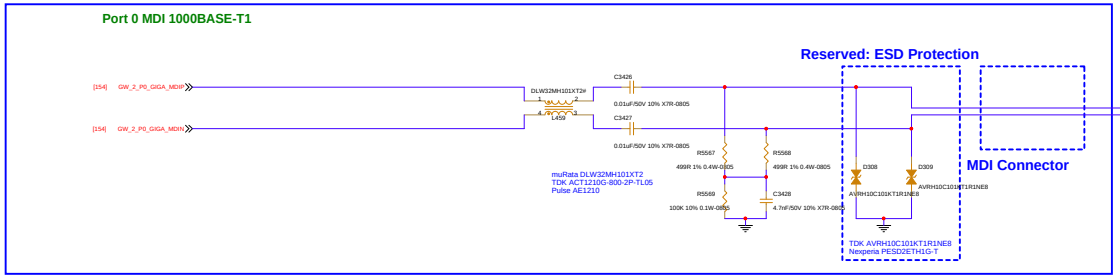
Size B	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 157 of 190	

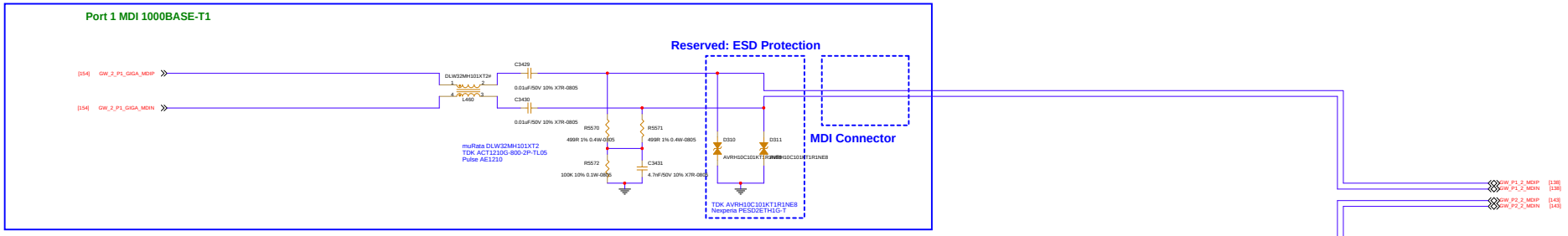
DC Block & Termination

Port 0 MDI 1000BASE-T1



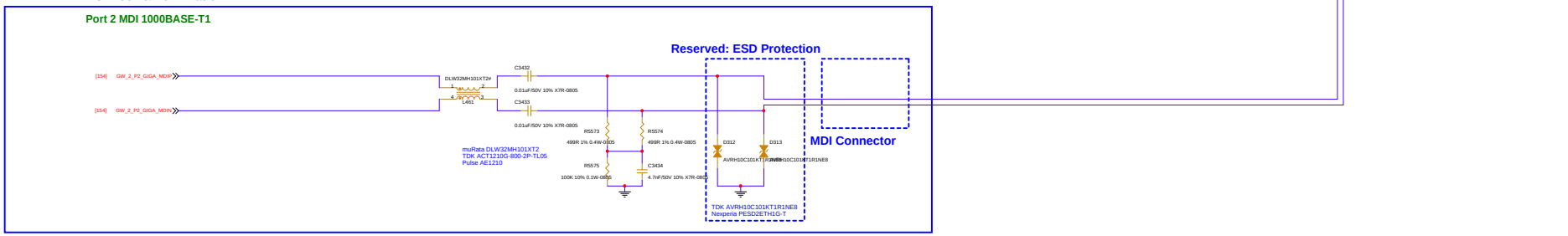
DC Block & Termination

Port 1 MDI 1000BASE-T1



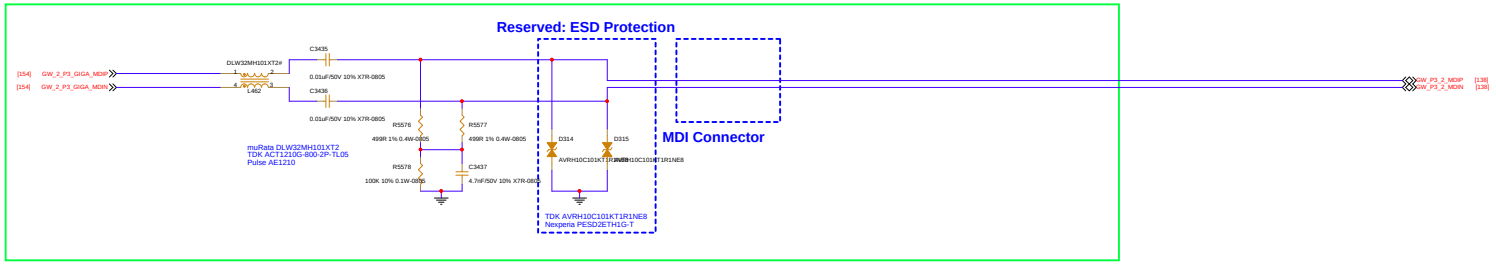
DC Block & Termination

Port 2 MDI 1000BASE-T1



DC Block & Termination

Port 3 MDI 1000BASE-T1

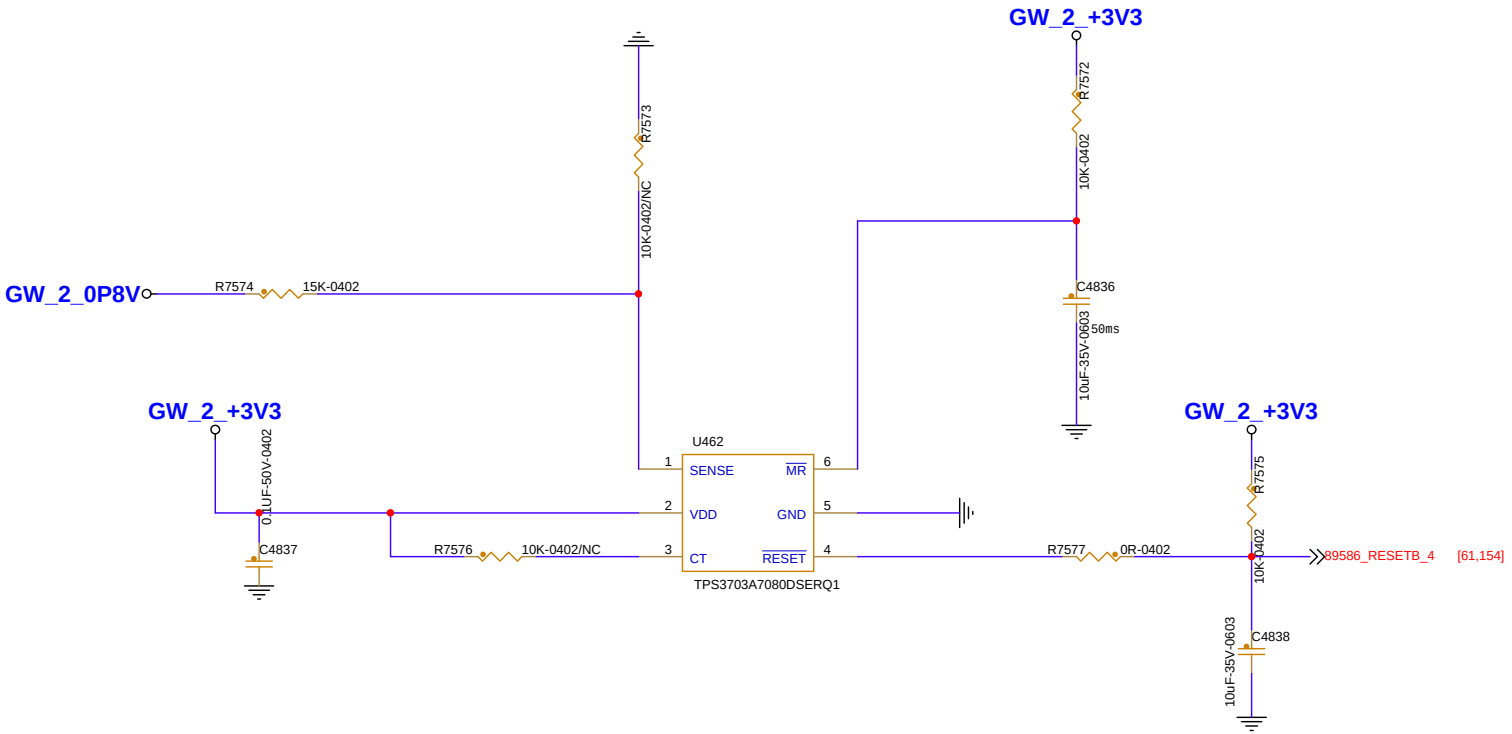


DC Block & Termination

Title	<Title>		
Size: D	Document Number: <Doc>		Rev: <RevCode>
Date:		Sheet 158 of 190	

delay time is 10ms

89586M



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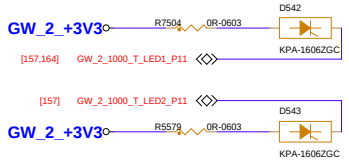
Size B	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 159 of 190	



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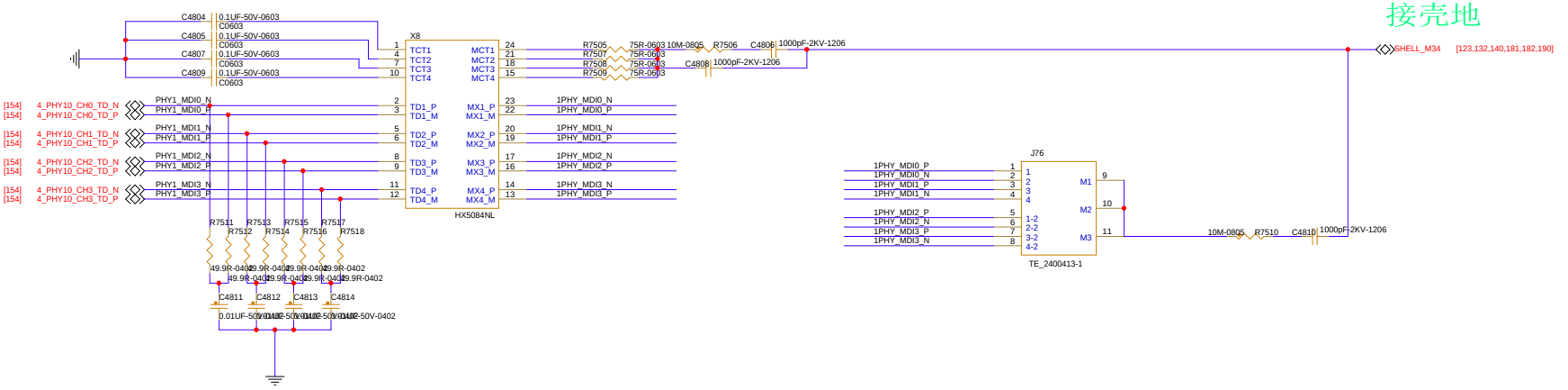

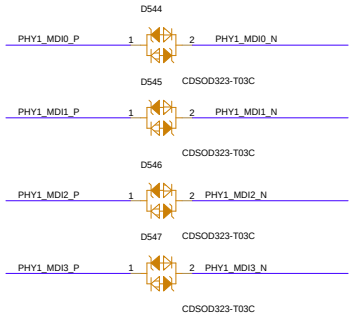

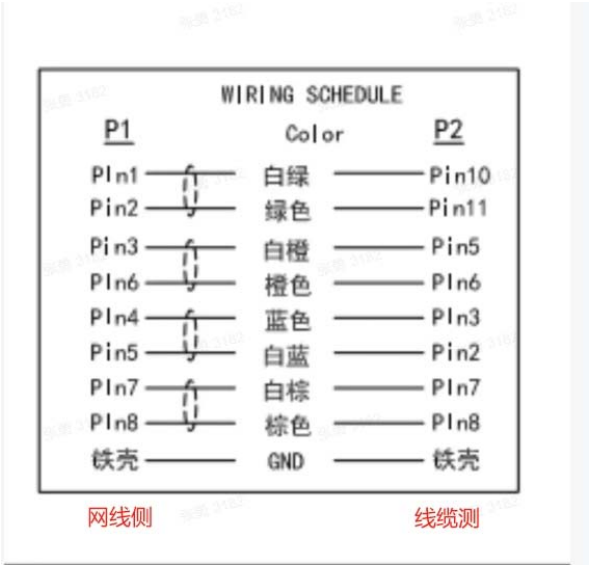

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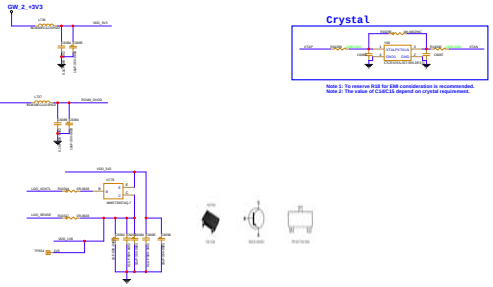
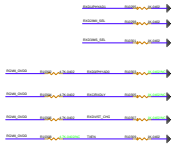
Size C	Document Number <Doc>		Rev <RevCode>
Date:		Sheet 160 of 190	



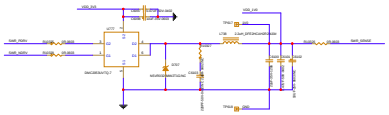
1.8V TTL
ADDR:0X00
CLK SEL: CRYSTAL
AN_EN: DISABLE ANTO
SPD: 1000-T1
MS SEL:MASTER
PAR_CTRL:01 DISABLE



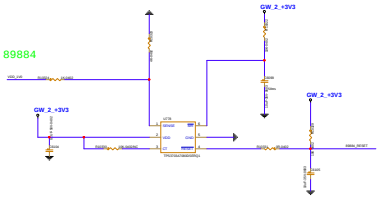
P8-RGMII
RGMII

P8

Link/Act LED



delay time is 10ms



2.6.2 PHY Address

The BCM89884 allows a unique PHY address for the Management Interface. The address is set through the logic value of PHYA0, latched during reset. PHYA0 is shared with the RXD1. The BCM89884 checks each MII management read or write command and performs the operation only if the address in the command matches the latched PHY address stored in the device.

Table 9: PHY Address Settings

PHYA0	PHY Address
0	0x0
1	0x1

Figure 5 shows a typical layout for the Management interface. To set a PHY Address signal to 0, leave the signal floating. No external pull-down resistor is required since the PHYA0 address signal has internal pull-down resistors. To set the PHYA0 address signal to 1, install a 4.7-kΩ pull-up resistor (R_{PU}) to OVDD.

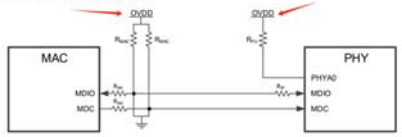
The MDIO signal typically require a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}), and series termination resistor near the PHY (R_{SP}) to match the trace impedance of the line. (Contact the MAC vendor for requirements.) For 50Ω traces, stuff R_{SP} with a 33Ω resistor.

The MDC signal typically requires a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}) to match the trace impedance of the line (contact the MAC vendor for requirements).

) and MDC Interfaces

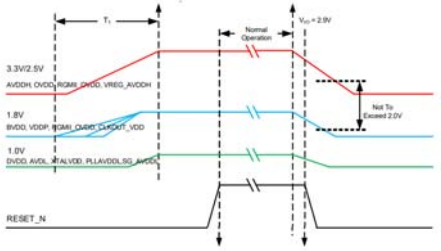
ADC interfaces can support either 2.5V or 3.3V operation depending on the voltage on the OVDD. The MDC le at rates up to 25 MHz. By default, the BCM89884 supports preamble suppression. This still requires a ones for the first MDIO transaction. To disable preamble suppression set DEVAD = 0x1, Address = 0xA000, and DEVAD = 0x0.

Figure 5: Management Interface Layout

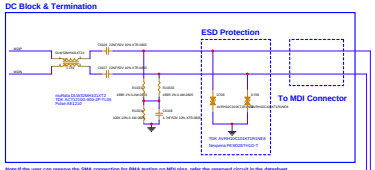


When a MAC is driving more than one PHY, a star topology, shown in Figure 6, can be used for clock distribution. In this approach, the stub lengths should be kept equal to obtain the best results.

Figure 10: Power-Up and Power-Down Sequence



DC Block & Termination



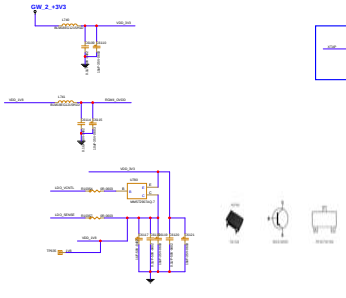
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

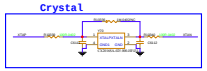
RGMII

P8
ADRESS:0
1000BASE-T1 MASTER
RGMII MODE
PHY管理 MDCMDIO 原生

本页所有磁珠保证通流1A

RGMII 1.8V BANK
MDCMDIO 3.3V BANK
P8 13





1.8V TTL
ADDR:0X01
CLK SEL: CRYSTAL

AN_EN: DISABLE ANTO

SPD: 1000-T1

MS SEL:MASTER

PAR_CTRL:01 DISABLE

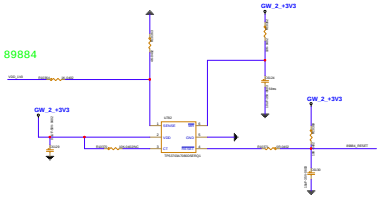
P13

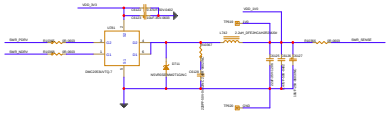
P13-RGMII

RGMII

Note 1: Reserve R26-R31/C23 for driving and EMI consideration.
Note 2: Recommend to reserve R32-R37/C24 close to another chip.

delay time is 10ms





2.6.2 PHY Address

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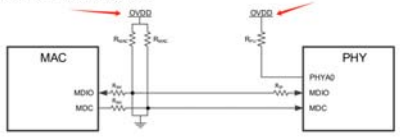
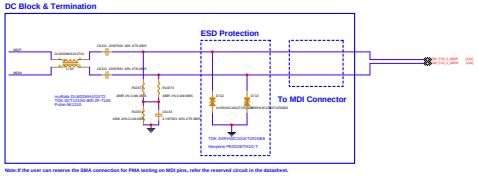
The MDIO signal typically require a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}), and series termination resistor near the PHY (R_{SP}) to match the trace impedance of the line. (Contact the MAC vendor for requirements.) For 50Ω traces, stuff R_{SP} with a 33Ω resistor.

The MDC signal typically requires a 1.5-kΩ pull-up resistor (R_{MAC}) near the MAC, a series termination resistor near the MAC (R_{SM}) to match the trace impedance of the line (contact the MAC vendor for requirements).

Figure 5: Management Interface Layout



When a MAC is driving more than one PHY, a star topology, shown in Figure 6, can be used for clock distribution. In this approach, the stub lengths should be kept equal to obtain the best results.



Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

2.6.1 MDIO and MDC Interfaces

The MDIO and MDC interfaces can support either 2.5V or 3.3V operation depending on the voltage on the OVDD. The MDC clock can operate at rates up to 25 MHz. By default, the BCM89884 supports preamble suppression. This still requires a preamble of 32 ones for the first MDIO transaction. To disable preamble suppression set DEVAD = 0x1, Address = 0xA000, and bit[0] = 0x0.

Figure 10: Power-Up and Power-Down Sequence

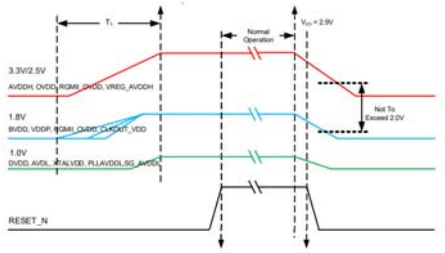


Table 2: MDI Hardware Configuration Settings

MDI Configuration	AN_EN	SPD	MS
Force 100BASE-T1 Secondary	0	0	0
Force 100BASE-T1 Master	0	0	1
Force 1000BASE-T1 Secondary	0	1	0
Force 1000BASE-T1 Master	0	1	1

P13
ADRESS:1
1000BASE-T1 MASTER
RGMII MODE

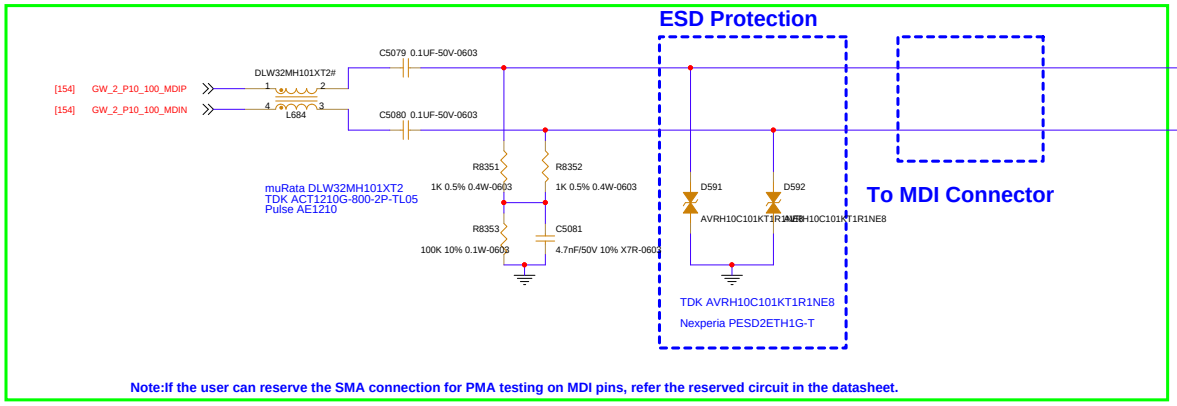
PHY管理　MDC/MDIO原生

本页所有磁珠保证通流1A

RGMII 1.8V BANK
MDCMDIO 3.3V BANK
P8 13

100BASE-T1 P10

ESD Protection



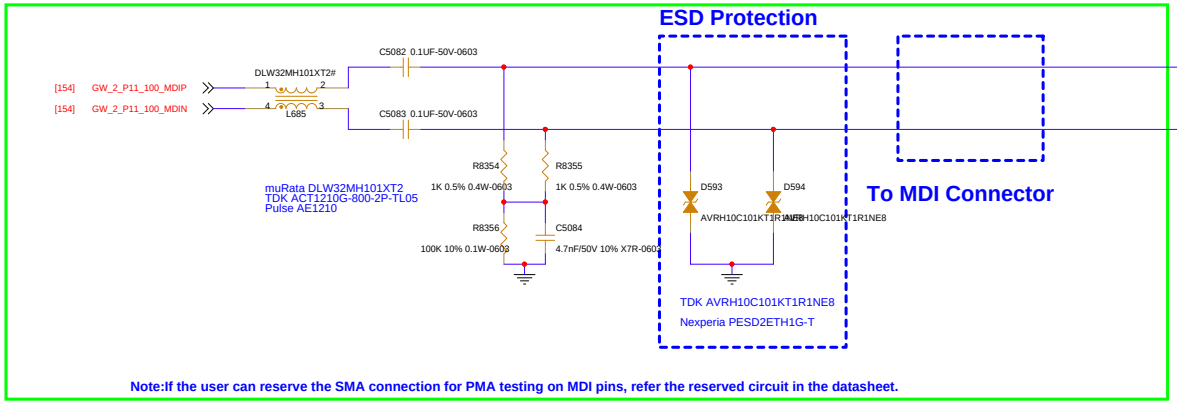
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

GW_2_P10_100BASE-T1_MDIP [144]
GW_2_P10_100BASE-T1_MDIN [144]
GW_2_P11_100BASE-T1_MDIP [144]
GW_2_P11_100BASE-T1_MDIN [144]

GW_2_+3V3
R9988 0R-0402
D679
KPA-1606ZGC
[157,160] GW_2_1000_T_LED1_P11

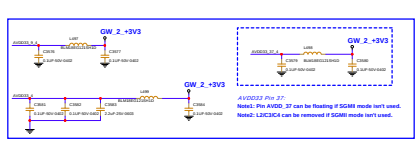
100BASE-T1 P11

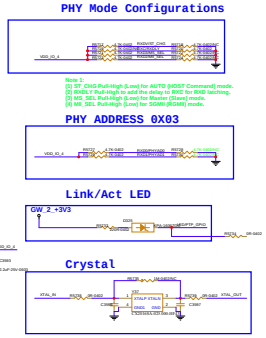
ESD Protection

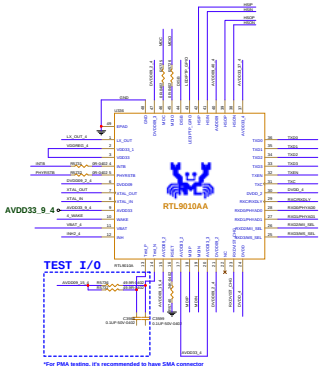


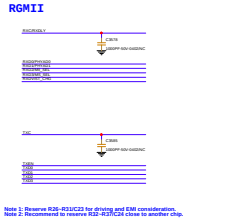
Note:If the user can reserve the SMA connection for PMA testing on MDI pins, refer the reserved circuit in the datasheet.

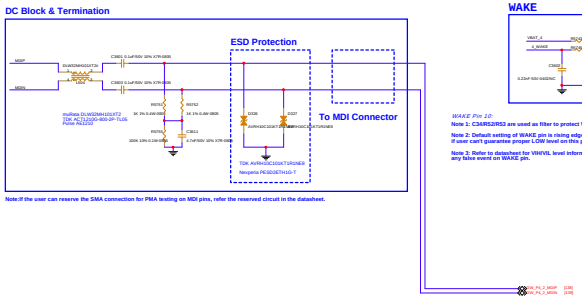
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 164 of 190	

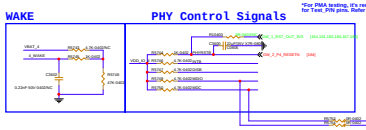












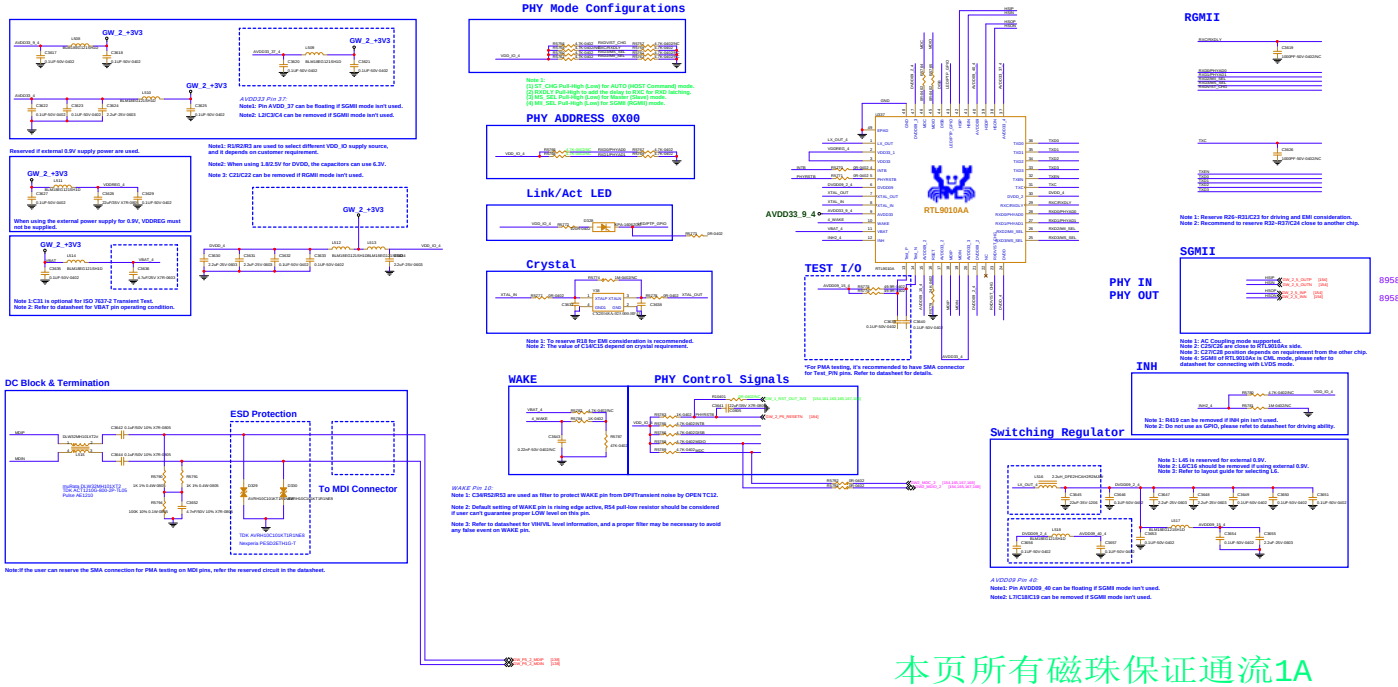
本页所有磁珠保证通流1A

ADRESS:3
1000BASE-T1 MASTER
SGMII MODE

P4 3.3V IO

3.3V BANK
P5 6 9 4

PHY管理 IO模拟



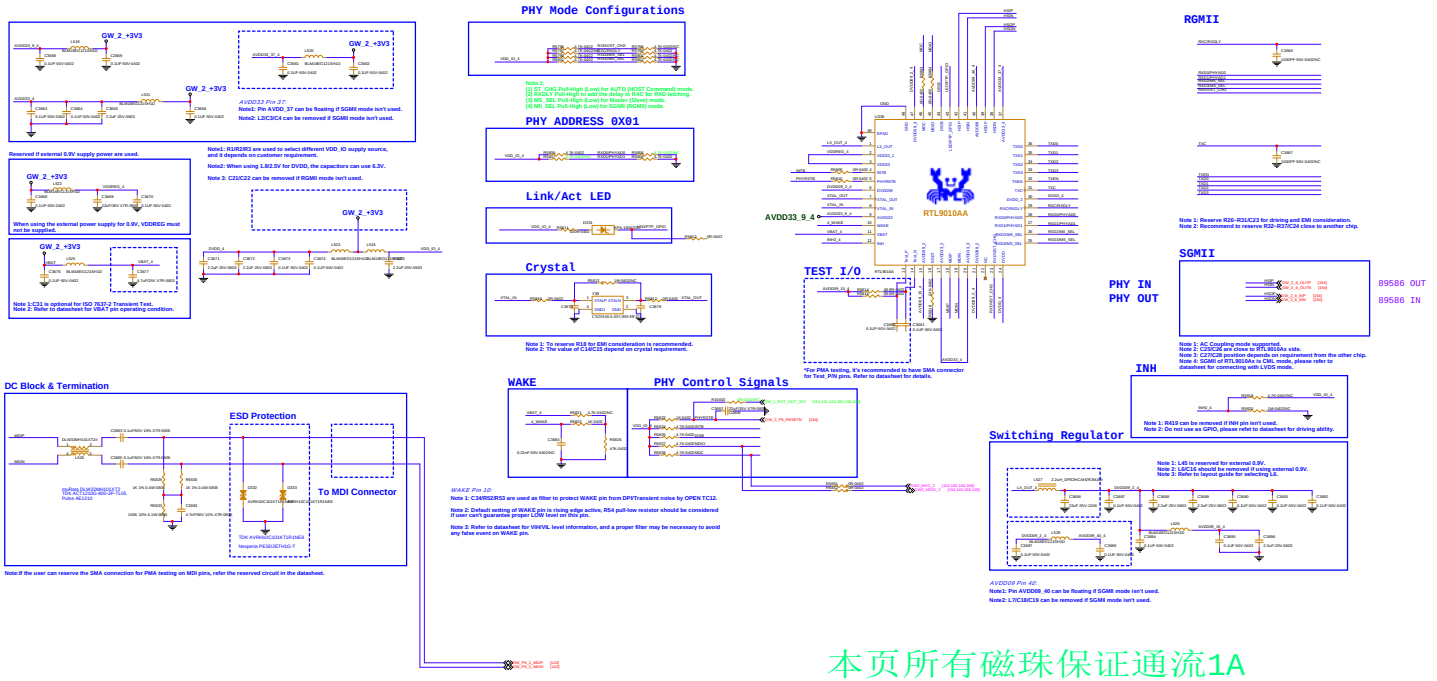
本页所有磁珠保证通流1A

ADRESS:0

1000BASE-T1 MASTER　　P5　　3V3 IO　　3.3V BANK

SGMII MODE　　P5 6 9 4

PHY管理　　MDC/MDIO原生



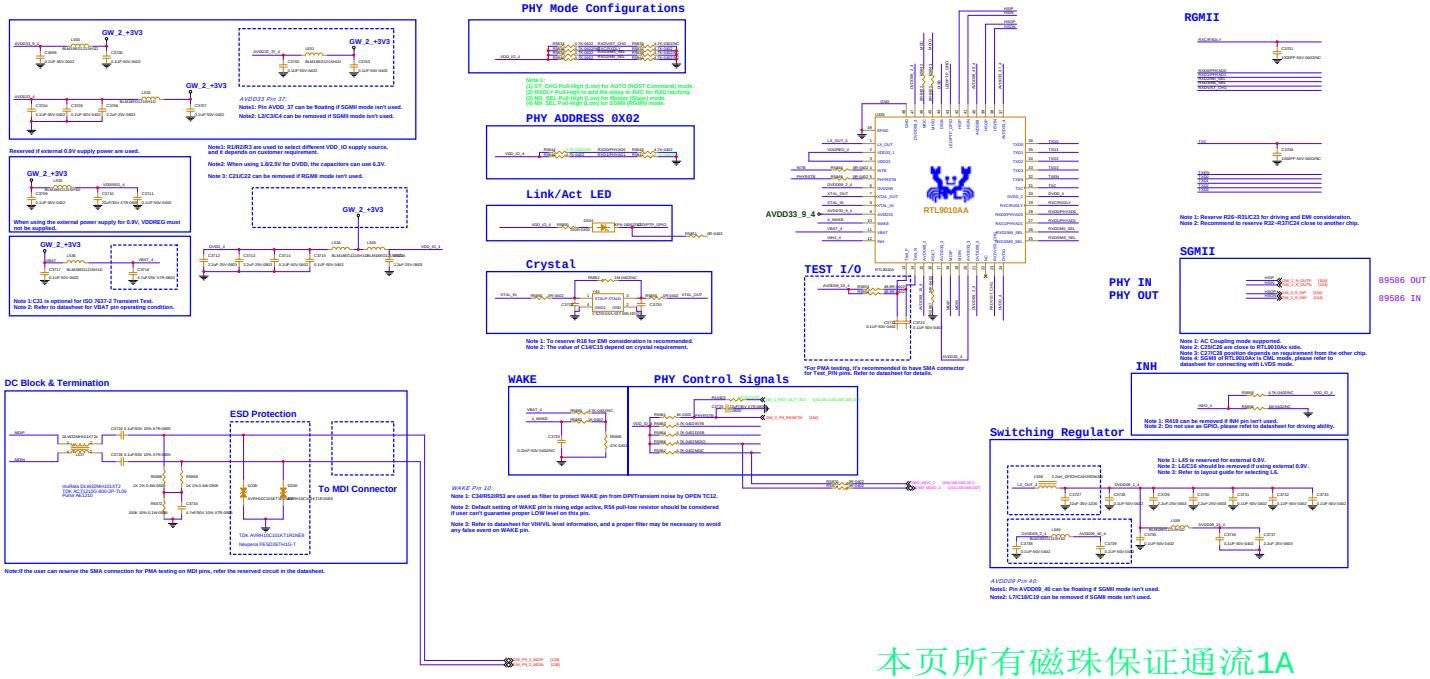
本页所有磁珠保证通流1A

ADRESS:1

1000BASE-T1 MASTER P6 3V3 IO 3.3V BANK P5 6 9 4

SGMII MODE

PHY管理 MDC/MDIO原生



本页所有磁珠保证通流1A

ADRESS:2

1000BASE-T1 MASTER

SGMII MODE

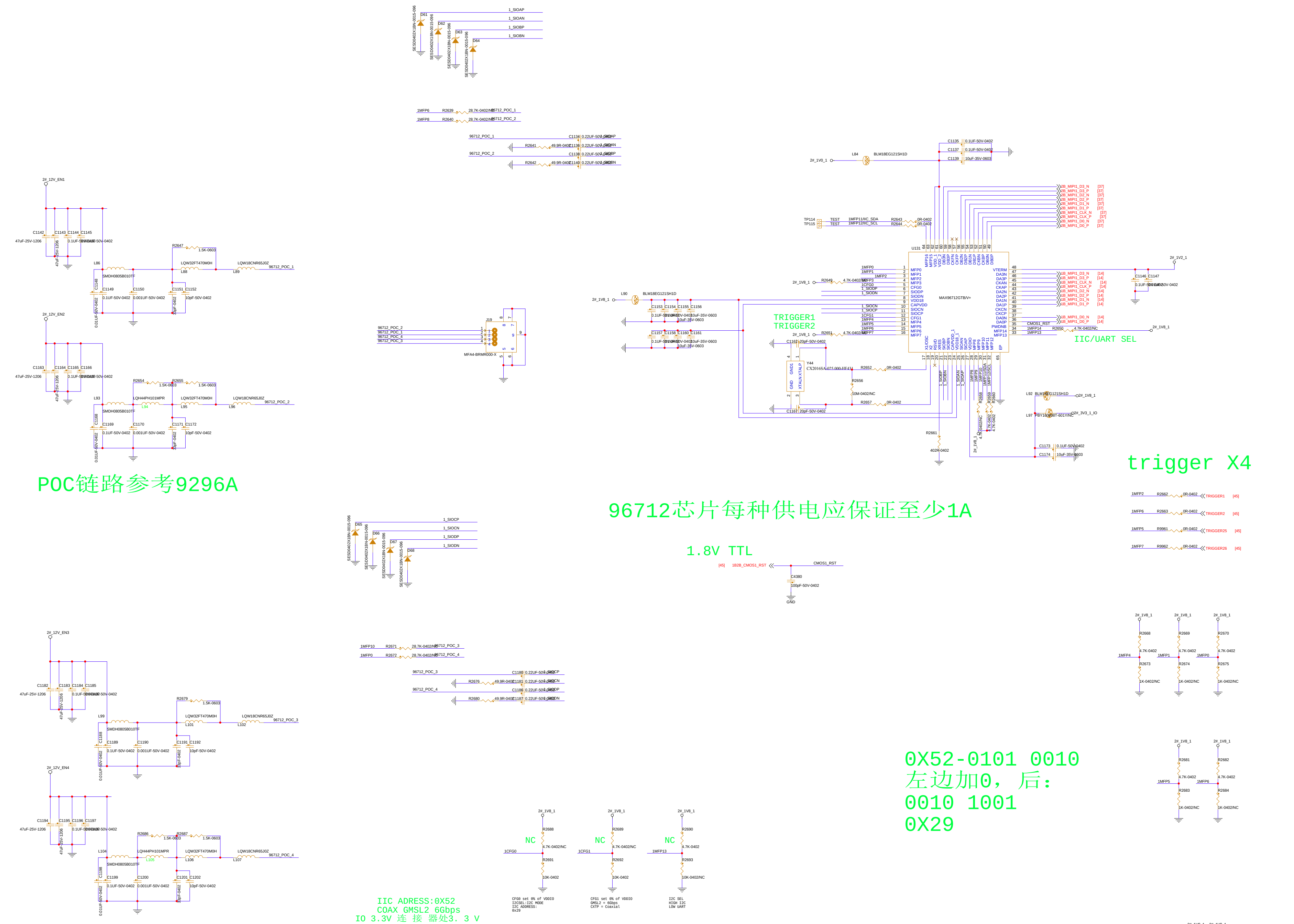
P9 3V3 IO

3.3V BANK

P5 6 9 4

PHY管理 MDC/MDIO原生

Title	<Title>
Size C	Document Number <Doc>
Rev	<RevCode>
Date:	Sheet 170 of 190



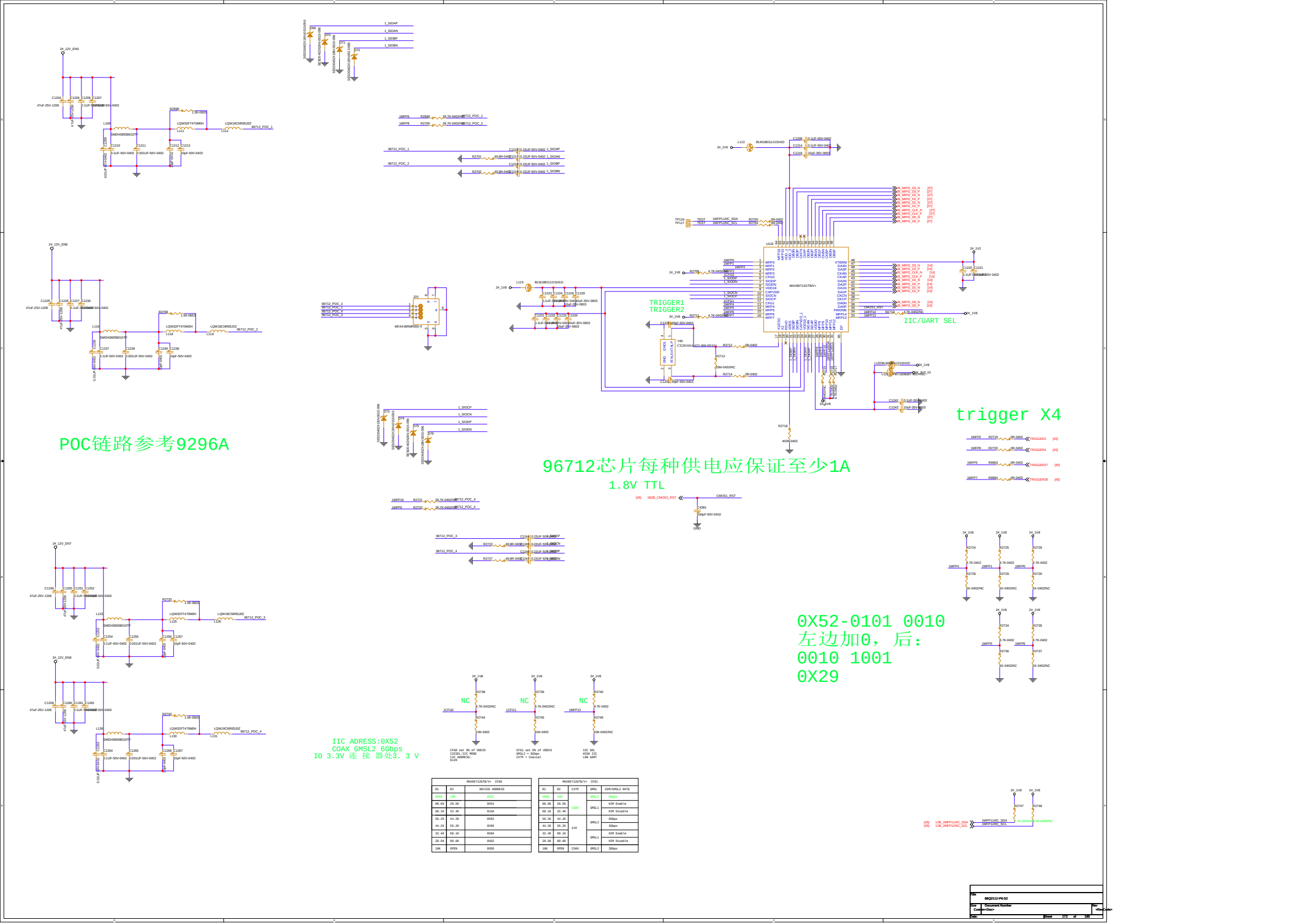
MAX96712GTB/V+ CFG0

R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0x5A
56.2K	44.2K	0X92
44.2K	56.2K	0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

MAX96712GTB/V+ CFG1

R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HIM Enable
68.1K	32.4K			HIM Disable
56.2K	44.2K	STP	GMSL2	6Gbps
44.2K	56.2K			3Gbps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K			HIM Disable
10K	OPEN	COAX	GMSL2	3Gbps

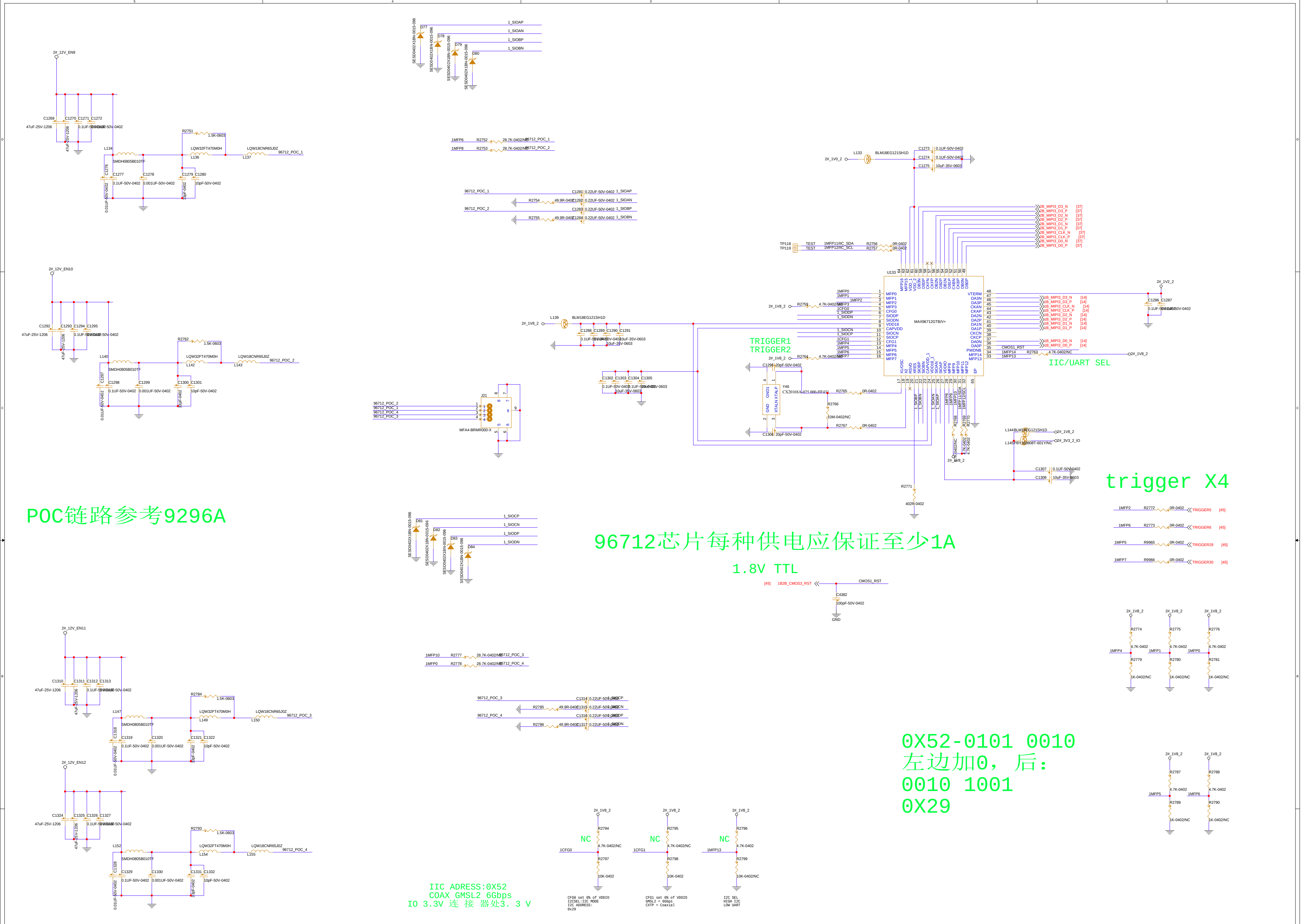
Title 88Q2112-P5-S1		
Size Custom	Document Number <Doc>	Rev <RevCode>
Date:	Sheet 171 of 190	



MAX96712GTB/V+ CFG0		
R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0x5A
56.2K	44.2K	0X92
44.2K	56.2K	0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

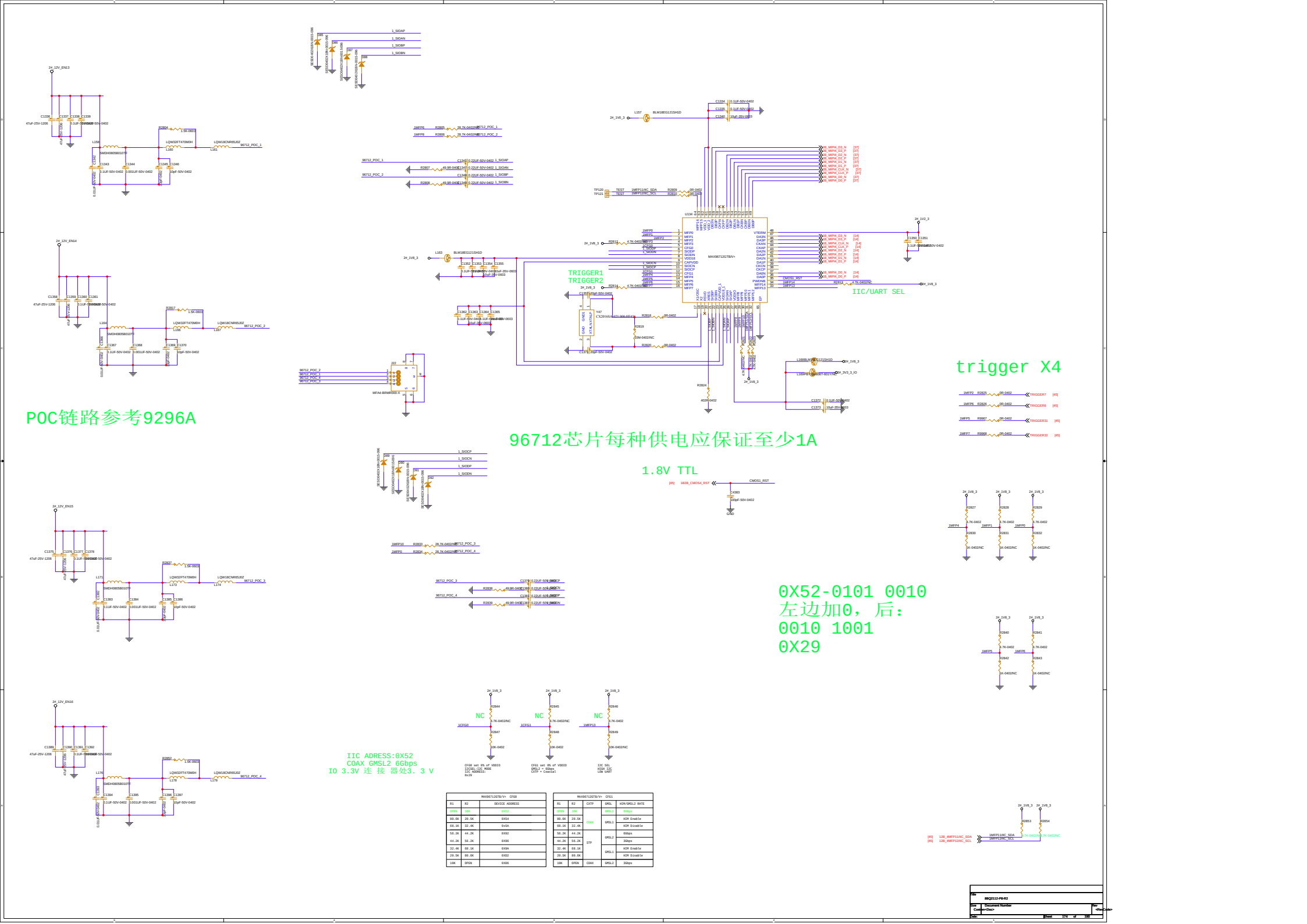
MAX96712GTB/V+ CFG1				
R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HIM Enable
68.1K	32.4K			HIM Disable
56.2K	44.2K	STP	GMSL2	6Gbps
44.2K	56.2K			3Gbps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K			HIM Disable
10K	OPEN	COAX	GMSL3	3Gbps

File	88Q2112-P6-S2		
Size	Document Number		Rev
Custom	<Doc>		<RevCode>
Date:		Sheet 172 of 180	



MAX96712GTB/V+ CFG0		
R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0x5A
56.2K	44.2K	0X92
44.2K	56.2K	0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

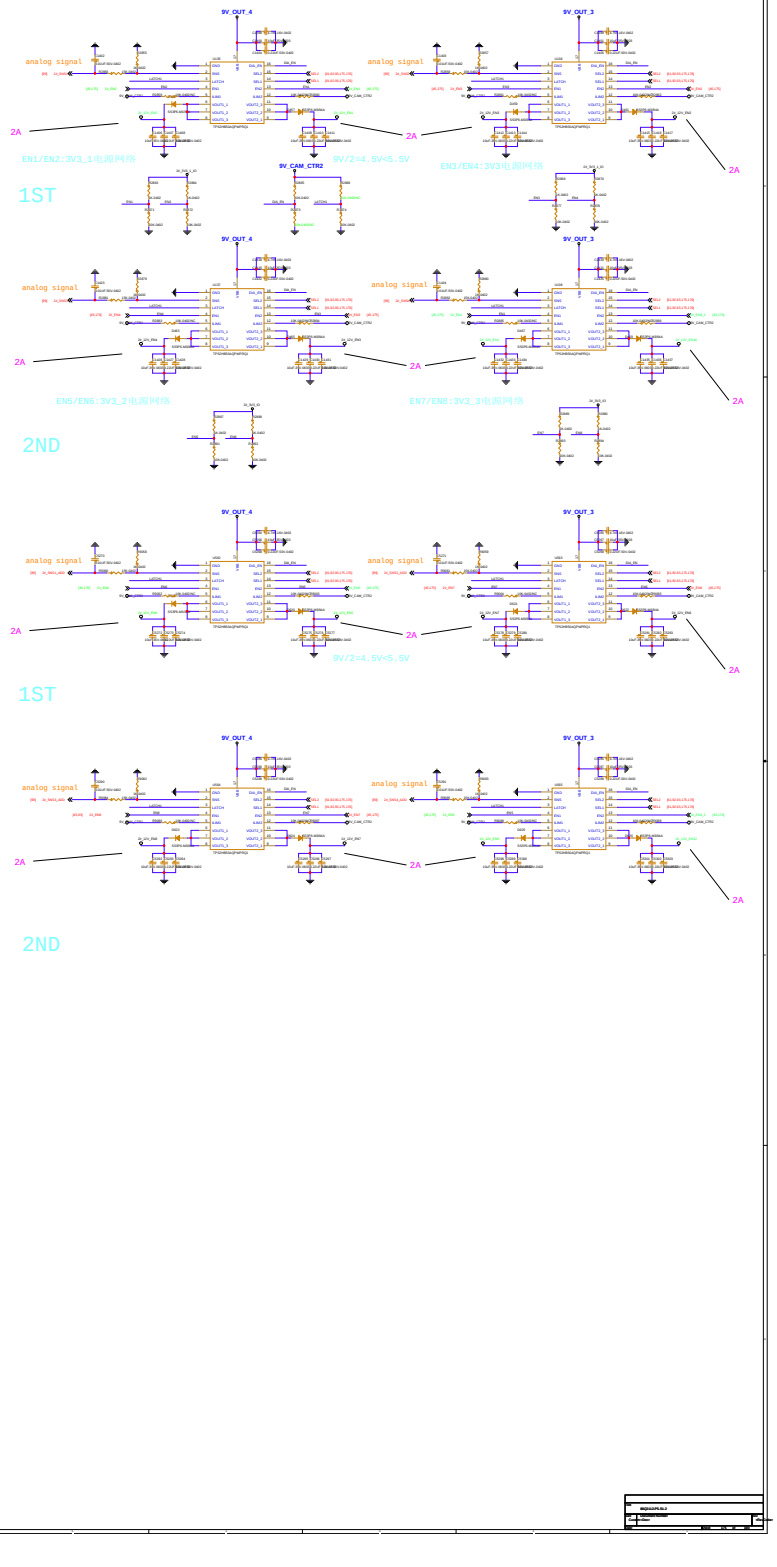
MAX96712GTB/V+ CFG1				
R1	R2	CXTP	GMSL	HIM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HIM Enable
68.1K	32.4K			HIM Disable
56.2K	44.2K	STP	GMSL2	6Gbps
44.2K	56.2K			3Gbps
32.4K	68.1K		GMSL1	HIM Enable
20.5K	80.6K			HIM Disable
10K	OPEN	COAX	GMSL2	3Gbps

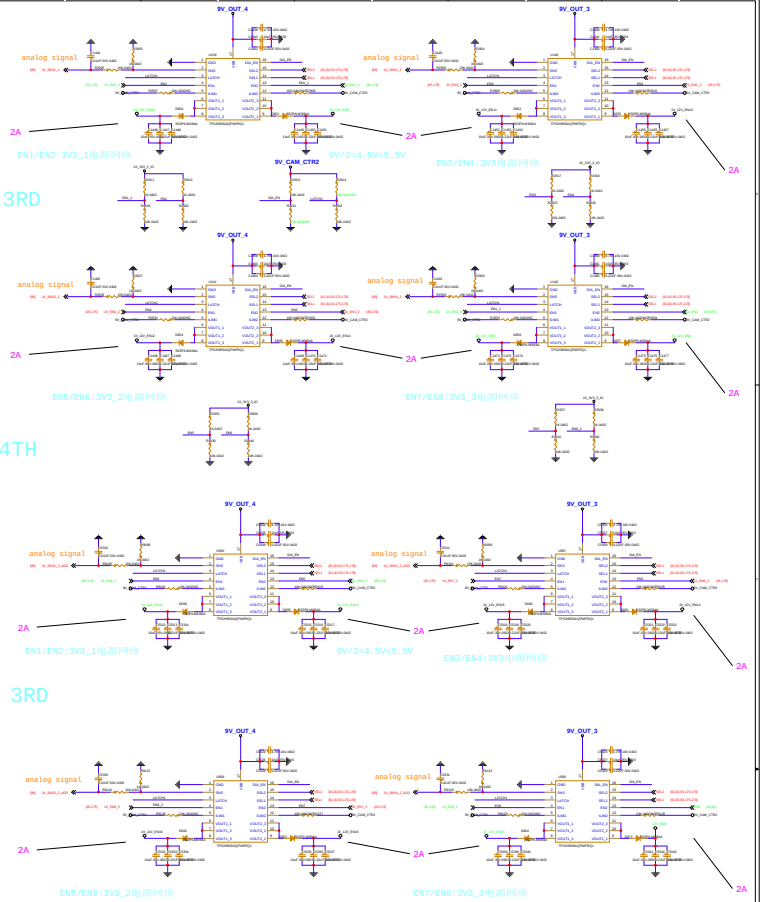


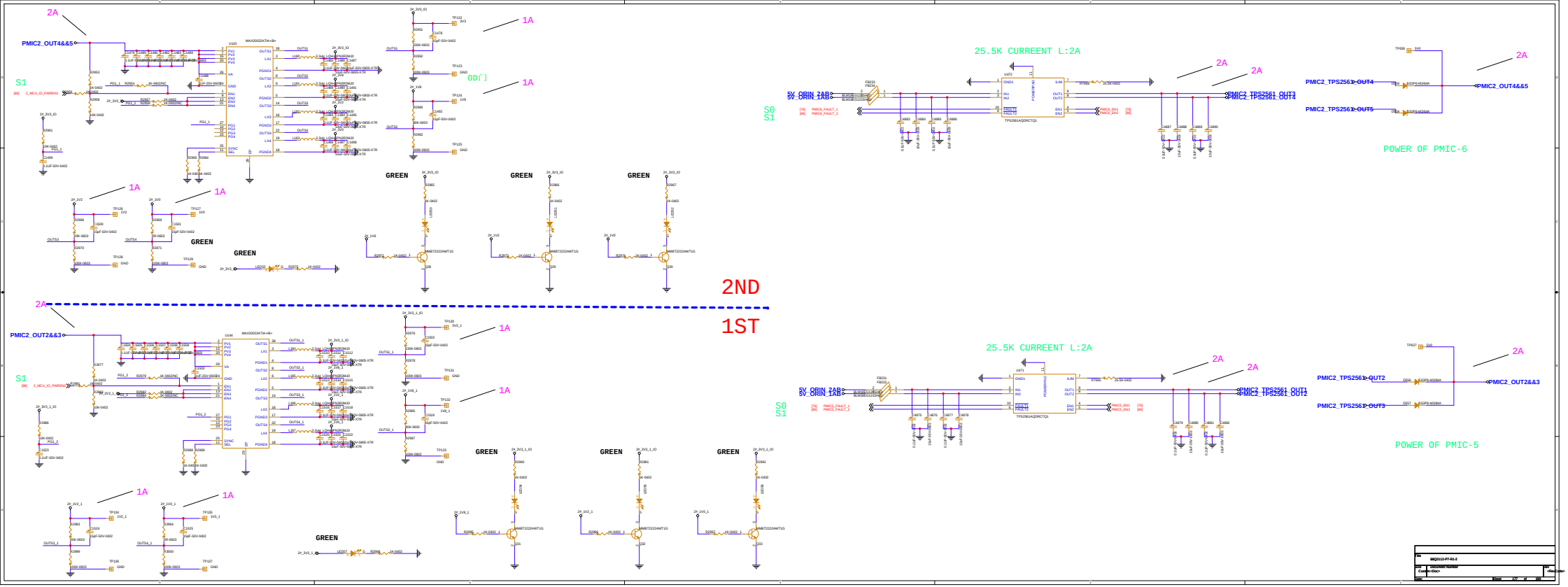
MAX96712GTB/V+ CFG0		
R1	R2	DEVICE ADDRESS
OPEN	10K	0X52
80.6K	20.5K	0X54
68.1K	32.4K	0X5A
56.2K	44.2K	0X92
44.2K	56.2K	0X96
32.4K	68.1K	0X9A
20.5K	80.6K	0XD2
10K	OPEN	0XD6

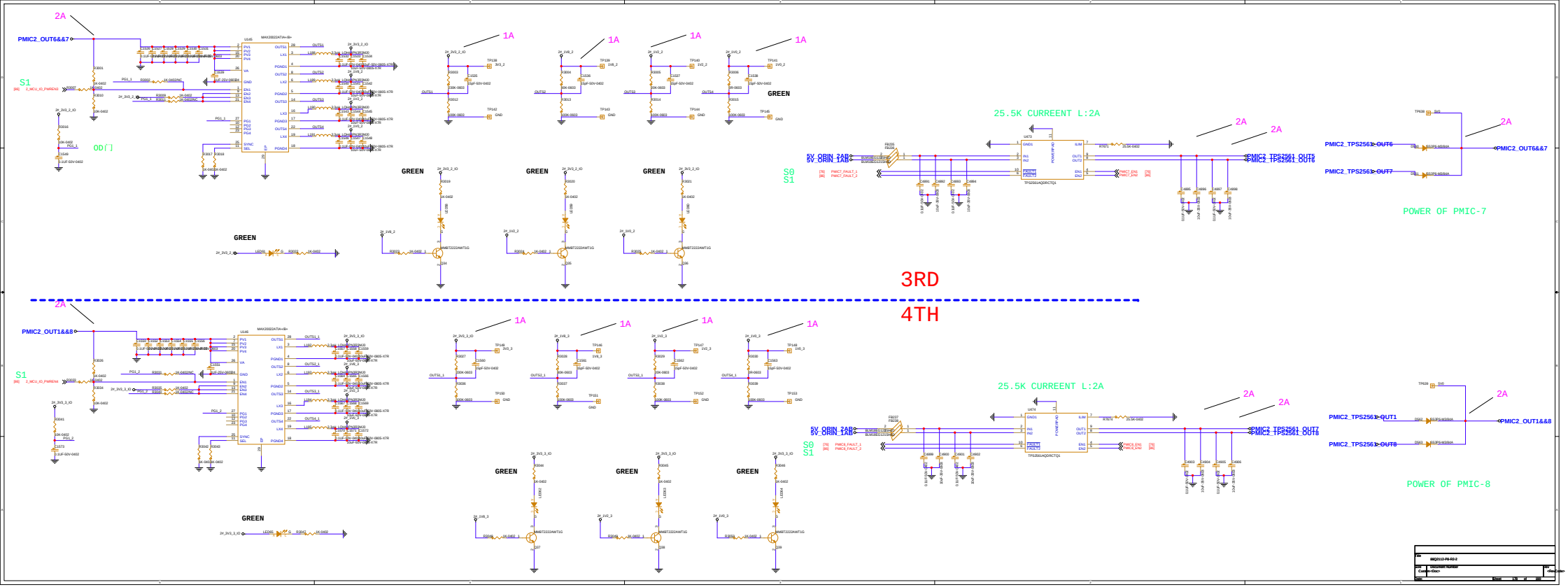
MAX96712GTB/V+ CFG1				
R1	R2	CXTP	GMSL	HDM/GMSL2 RATE
OPEN	10K	COAX	GMSL2	6Gbps
80.6K	20.5K		GMSL1	HDM Enable
68.1K	32.4K			HDM Disable
56.2K	44.2K	STP	GMSL2	6Gbps
44.2K	56.2K			3Gbps
32.4K	68.1K		GMSL1	HDM Enable
20.5K	80.6K			HDM Disable
10K	OPEN	COAX	GMSL2	3Gbps

File:	88Q2112-P9-R2		
Size:	Document Number: Custom<Doc>		Rev: <Rev Code>
Date:		Sheet 174 of 180	


9V_OUT_4
9V_OUT_3
analog signal
2A
EN1/EN2:3V3_1电源网络
9V/2=4.5V<5.5V
EN3/EN4:3V3电源网络
1ST
9V_CAM_CTR2
EN5/EN6:3V3_2电源网络
EN7/EN8:3V3_3电源网络
2ND


9V_OUT_4
9V_OUT_3
analog signal
2A
EN1/EN2:3V3_1电源网络
9V/2=4.5V<5.5V
EN3/EN4:3V3电源网络
3RD
9V_CAM_CTR2
EN5/EN6:3V3_2电源网络
EN7/EN8:3V3_3电源网络
4TH


2A
PMIC2_OUT4&&5
S1
1A
GREEN
2ND
1ST
2A
PMIC2_OUT2&&3
S1
1A
GREEN
25.5K CURREENT L:2A
5V_ORIN_2AB
5V_ORIN_1AB
S0
S1
PMIC2_TPS2561_OUT3
PMIC2_TPS2561_OUT4
PMIC2_TPS2561_OUT4
PMIC2_TPS2561_OUT5
PMIC2_OUT4&&5
POWER OF PMIC-6
PMIC2_TPS2561_OUT1
PMIC2_TPS2561_OUT2
PMIC2_TPS2561_OUT2
PMIC2_TPS2561_OUT3
PMIC2_OUT2&&3
POWER OF PMIC-5


2A
PMIC2_OUT6&&7
S1
1A
GREEN
25.5K CURREENT L:2A
5V_ORIN_2AB
5V_ORIN_1AB
PMIC2_TPS2561_OUT5
PMIC2_TPS2561_OUT6
PMIC2_TPS2561_OUT7
PMIC2_OUT6&&7
POWER OF PMIC-7
3RD
4TH
PMIC2_OUT1&&8
PMIC2_TPS2561_OUT1
PMIC2_TPS2561_OUT8
PMIC2_OUT1&&8
POWER OF PMIC-8

Title	<Title>
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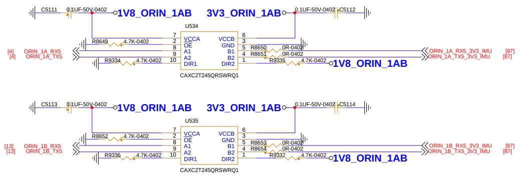
Rev	<RevCode>
Date:	Sheet 179 of 190

外置IMU给到4个ORIN+S1/S2-MCU

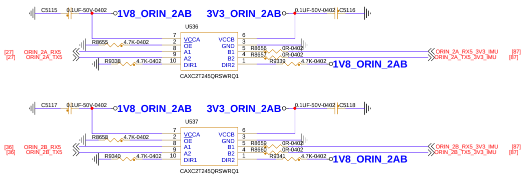
IMU TO ORIN x4+S1/S2-MCU　接到IO CON

H: A TO B
L: B TO A

IMU TO ORIN 1A/B
ORIN OUT

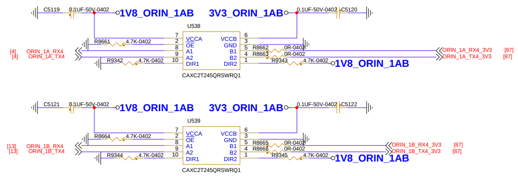


IMU TO ORIN 2A/B



H: A TO B
L: B TO A

ORIN 1A/B UART4 TO IO CON



ORIN 2A/B UART4 TO IO CON

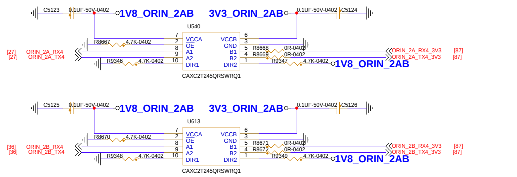


Table 2. Function Table (Each Transceiver)[(1)(2)]

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

Table 2. Function Table (Each Transceiver)[(1)(2)]

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

8.4 器件功能模式

表 8-1. 功能表

控制输入[(1)]	端口状态		操作
DIR	A 端口	B 端口	
L	输出（启用）	输入（高阻态）	B 数据到 A 总线
H	输入（高阻态）	输出（启用）	A 数据到 B 总线

(1) [illegible]

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Size Custom	Document Number <Doc>	Rev <RevCode>
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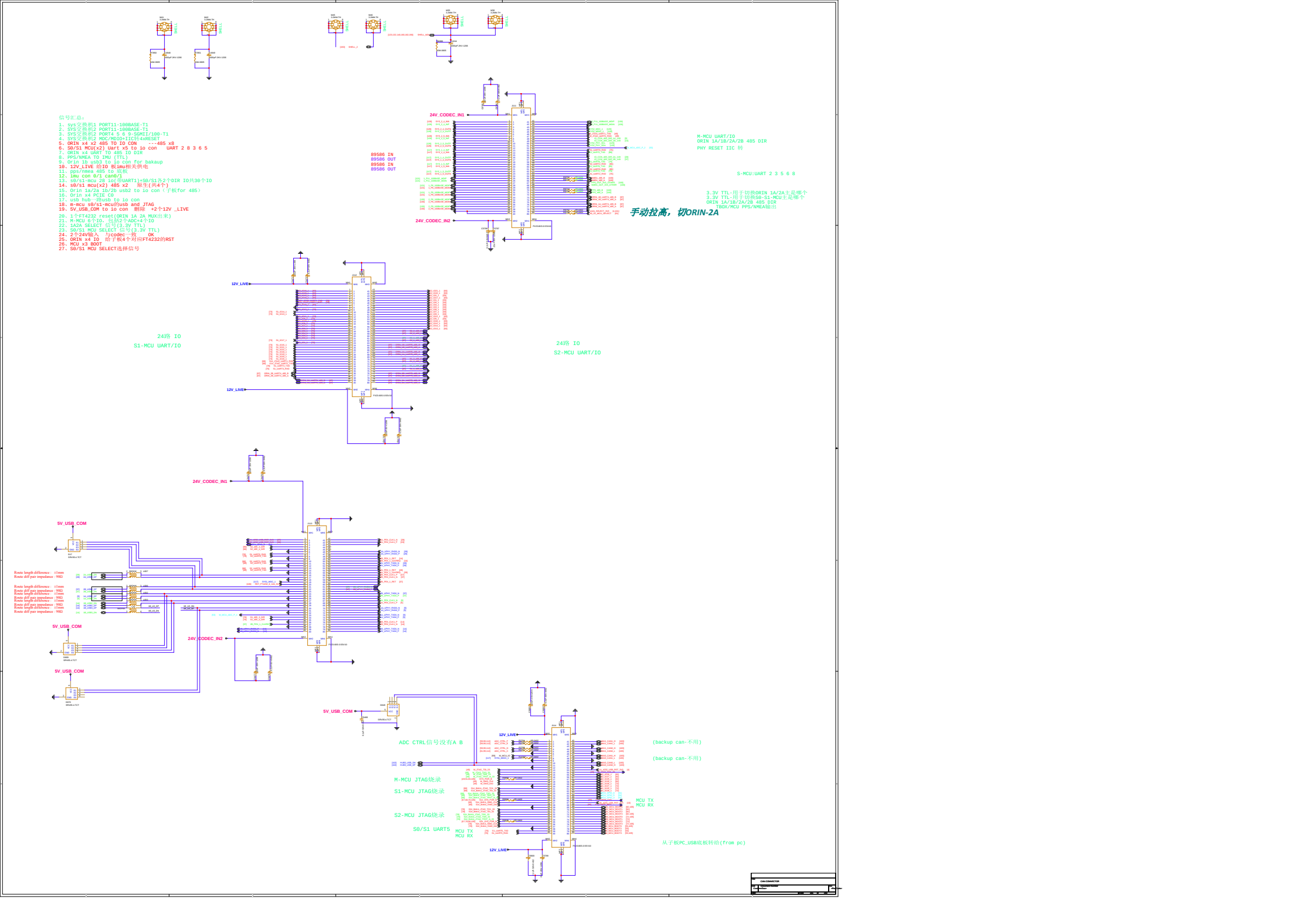
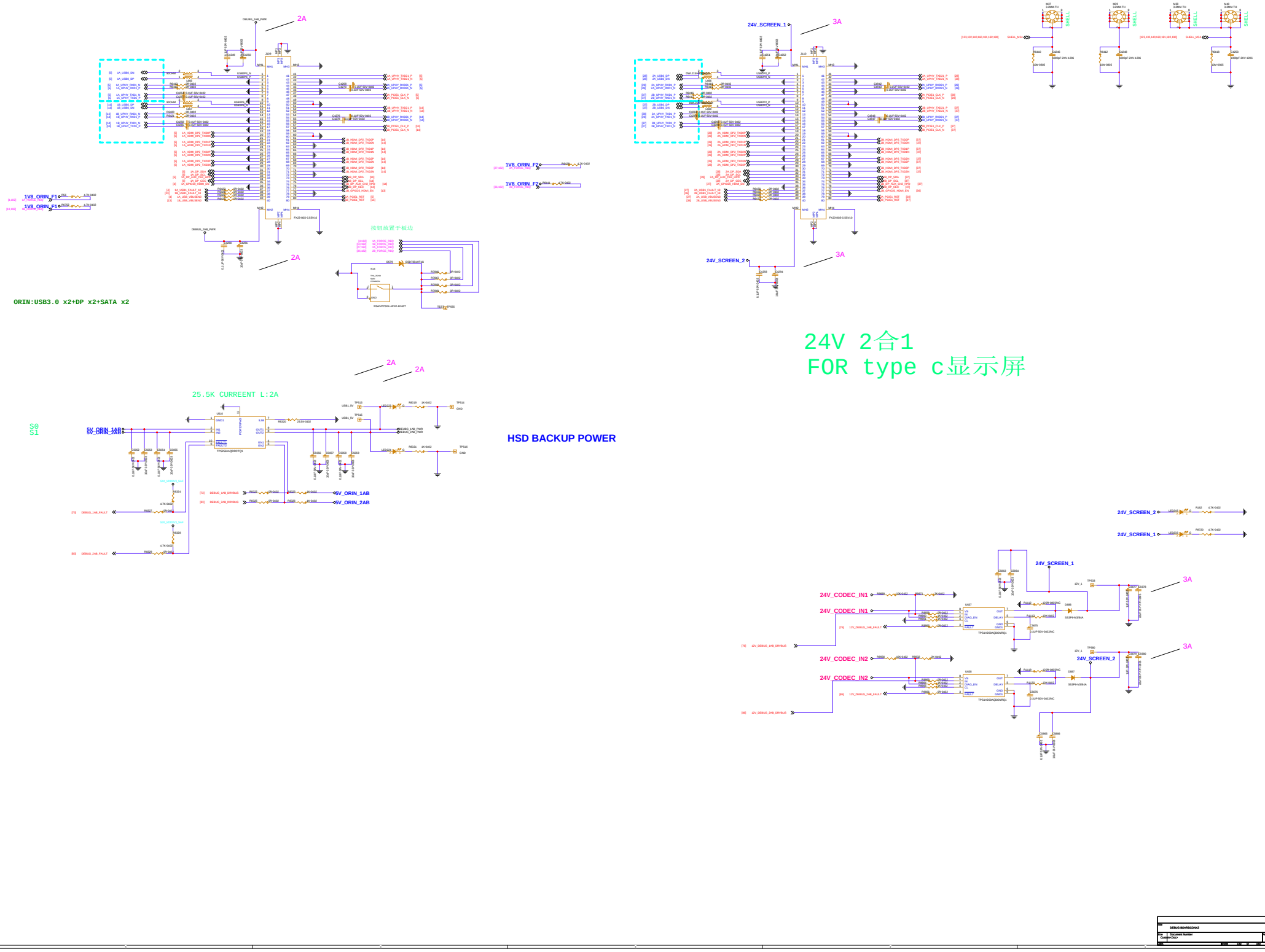
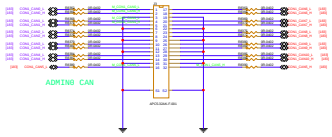

信号汇总：
1、sys交换机1 PORT11-100BASE-T1
2、SYS交换机2 PORT11-100BASE-T1
3、SYS交换机2 PORT4 5 6 9-SGMII/100-T1
4、SYS交换机2 MDC/MDIO+TI三转4xRESET
5、ORIN x4 x2 485 TO IO CON ---485 x8
6、S0/S1 MCU(x2) Uart x5 to io con UART 2 8 3 6 5
7、ORIN x4 UART TO 485 IO DIR
8、PPS/NMEA TO IMU (TTL)
9、Orin 1b usb3 to io con for bakaup
10、12V_LIVE 给IO 板imu相关供电
11、pps/nmea 485 to 底板
12、imu con 0/1 canb/1
13、s0/s1-mcu 2B io引出UART1+S0/S1各2个DIR IO共30个IO
14、s0/s1 mcu(x2) 485 x2 预生(共4个)
15、Orin 1a/2a 1b/2b usb2 to io con（子板for 485）
16、Orin x4 PCIE C0
17、usb hub一拖usb to io con
18、m-mcu s0/s1-mcu的usb and JTAG
19、5V_USB_COM to io con 删除 +2个12V _LIVE
20、1个FT4232 reset(ORIN 1A 2A MUX出来)
21、M-MCU 6个IO，包括2个ADC+4个IO
22、1A2A SELECT 信号(3.5V TTL)
23、S0/S1 MCU SELECT 信号(3.3V TTL)
24、2个24V输入 与codec一致 OK
25、ORIN x4 IO 给子板4个对应FT4232的RST
26、MCU x3 BOOT
27、S0/S1 MCU SELECT选择信号
89586 IN
89586 OUT
89586 IN
89586 OUT
24V_CODEC_IN1
24V_CODEC_IN2
M-MCU UART/IO
ORIN 1A/1B/2A/2B 485 DIR
PHY RESET IIC 转
S-MCU:UART 2 3 5 6 8
3.3V TTL-用于切换ORIN 1A/2A主是哪个
3.3V TTL-用于切换S0-S1-MCU主是哪个
ORIN 1A/1B/2A/2B 485 DIR
TBOX/MCU PPS/NMEA输出
手动拉高，切ORIN-2A
12V_LIVE
24路 IO
S1-MCU UART/IO
24路 IO
S2-MCU UART/IO
5V_USB_COM
ADC CTRL信号没有A B
M-MCU JTAG烧录
S1-MCU JTAG烧录
S2-MCU JTAG烧录
S0/S1 UARTS
MCU TX
MCU RX
(backup can-不用)
(backup can-不用)
从子板PC_USB底板转给(from pc)
CAN CONNECTOR


ORIN:USB3.0 x2+DP x2+SATA x2
24V_SCREEN_1
24V_SCREEN_2
3A
2A
按钮放置于板边
25.5K CURREENT L:2A
HSD BACKUP POWER
24V 2合1
FOR type c显示屏
24V_CODEC_IN1
24V_CODEC_IN2
5V_ORIN_1AB
5V_ORIN_2AB

全部命名：0-5

ORIN X4=8 CANS
IMU X2 =4 CANS
TBOX CAN=2 CANS
MONITOR1-MCU=22 CANS
SYS1-MCU=22 CANS
SYS2-MCU=22 CANS
3个MCU的22路CAN底板在合并

共36路CAN ， 每个连接器18路CAN
CON OUT端共2个连接器
每个连接器定义11路CAN



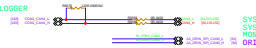
ADMIN0 CAN

CON1

V-CAN:接线控底盘CAN+CAN LOGGER

SYS-MCU1-CAN2
SYS-MCU2-CAN2
MONITOR-MCU1-CAN2 FOR CANLOGGER
ORIN-1A SPI CAN0 FOR CAN LOGGER

R-CAN:原车前向408RADAR以及前向smartcamera+CAN LOGGER

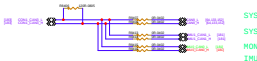


SYS-MCU1-CAN4
SYS-MCU2-CAN4
MONITOR-MCU1-CAN4 FOR CANLOGGER
ORIN-2A SPI CAN0

转速CAN:MCU和导远之间链接的轮速can
MCU将轮速信息通过这路can发给导远
24年量产版本，无此路can定义

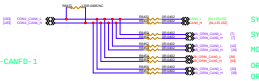
SYS-MCU1-CAN6
SYS-MCU2-CAN6
MONITOR-MCU1-CAN6 FOR CANLOGGER

I CAN:导远的imu数据，通过这路can传给s-mcu，再由s-mcu传给orin
外置的imu数据接入，第0路，此功能为冗余



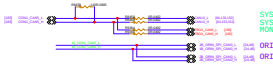
SYS-MCU1-CAN8
SYS-MCU2-CAN8
MONITOR-MCU1-CAN8 FOR CANLOGGER
CANFD-0是有效的
IMU2-CAN0
IMU1-CAN0

M CAN:ORIN(IPC)和S-MCU通信，此功能带冗余
CAN LOGGER
120R电阻放置在ORIN-1A M-MCU侧
导远INS数据CAN
VCAN底盘数据从SYS-MCU CANFD-2接收，再用CANFD-1转给ORIN-CANFD-1

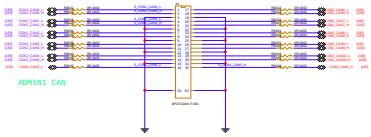


SYS-MCU1-CAN0
SYS-MCU2-CAN0
MONITOR-MCU1-CAN0 FOR CANLOGGER
ORIN-1A CAN0
ORIN-1B CAN0
ORIN-2B CAN0
ORIN-2A CAN0

ADMIN0 CAN
无人驾驶域的管理CAN0

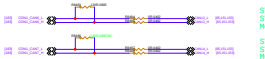


SYS-MCU1-CAN10
SYS-MCU2-CAN10 TBOX-CAN0
MONITOR-MCU1-CAN10 FOR CANLOGGER
ORIN-1B SPI CAN0
ORIN-2B SPI CAN0



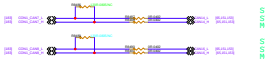
ADMIN1 CAN

FIRCAN CAN
整车解锁和看车控制



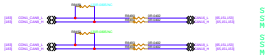
SYS-MCU1-CAN12
SYS-MCU2-CAN12
MONITOR-MCU1-CAN12 FOR CANLOGGER

NC



SYS-MCU1-CAN14
SYS-MCU2-CAN14
MONITOR-MCU1-CAN14 FOR CANLOGGER

QCAN-0

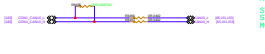


SYS-MCU1-CAN16
SYS-MCU2-CAN16
MONITOR-MCU1-CAN16 FOR CANLOGGER

NC

SYS-MCU1-CAN18
SYS-MCU2-CAN18
MONITOR-MCU1-CAN18 FOR CANLOGGER

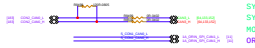
NC



SYS-MCU1-CAN20
SYS-MCU2-CAN20
MONITOR-MCU1-CAN20 FOR CANLOGGER

CON2

V-CAN:接线控底盘CAN+CAN LOGGER



SYS-MCU1-CAN3
SYS-MCU2-CAN3
MONITOR-MCU1-CAN3 FOR CANLOGGER
ORIN-1A SPI CAN1 FOR CAN LOGGER

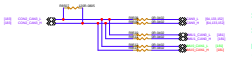
NC

SYS-MCU1-CAN5
SYS-MCU2-CAN5
MONITOR-MCU1-CAN5 FOR CANLOGGER
ORIN-2A SPI CAN1

NC

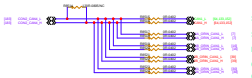
SYS-MCU1-CAN7
SYS-MCU2-CAN7
MONITOR-MCU1-CAN7 FOR CANLOGGER

I CAN:导远的imu数据，通过这路can传给s-mcu，再由s-mcu传给orin
外置的imu数据接入，第0路，此功能为冗余



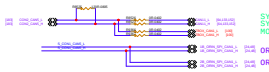
SYS-MCU1-CAN9
SYS-MCU2-CAN9
MONITOR-MCU1-CAN9 FOR CANLOGGER
IMU2-CAN1
IMU1-CAN1
CANFD-0是有效的

M CAN:ORIN(IPC)和S-MCU通信，此功能带冗余
CAN LOGGER
120R电阻放置在ORIN-1A M-MCU侧



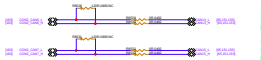
SYS-MCU1-CAN1
SYS-MCU2-CAN1
MONITOR-MCU1-CAN1 FOR CANLOGGER
ORIN-1A CAN1
ORIN-1B CAN1
ORIN-2B CAN1
ORIN-2A CAN1

ADMIN1 CAN
无人驾驶域的管理CAN1，带冗余



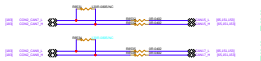
SYS-MCU1-CAN11 TBOX-CAN1
SYS-MCU2-CAN11
MONITOR-MCU1-CAN11 FOR CANLOGGER
ORIN-1B SPI CAN1
ORIN-2B SPI CAN1

OBD CAN1



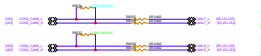
SYS-MCU1-CAN13
SYS-MCU2-CAN13
MONITOR-MCU1-CAN13 FOR CANLOGGER

OBD CAN2



SYS-MCU1-CAN15
SYS-MCU2-CAN15
MONITOR-MCU1-CAN15 FOR CANLOGGER

NC

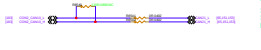


SYS-MCU1-CAN17
SYS-MCU2-CAN17
MONITOR-MCU1-CAN17 FOR CANLOGGER

NC

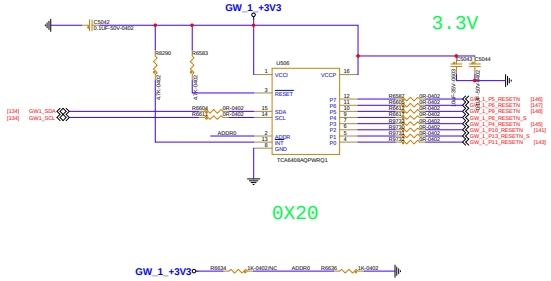
SYS-MCU1-CAN19
SYS-MCU2-CAN19
MONITOR-MCU1-CAN19 FOR CANLOGGER

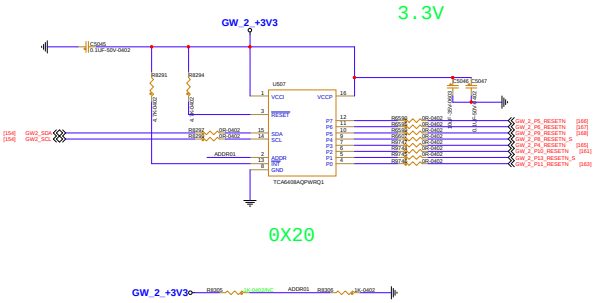
NC



SYS-MCU1-CAN21
SYS-MCU2-CAN21
MONITOR-MCU1-CAN21 FOR CANLOGGER

本页芯片供电引脚应至少1A





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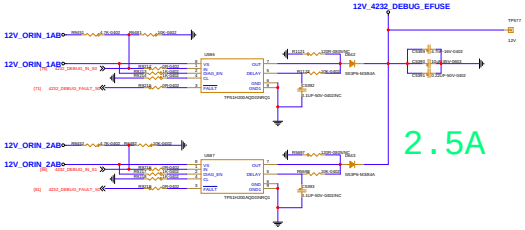
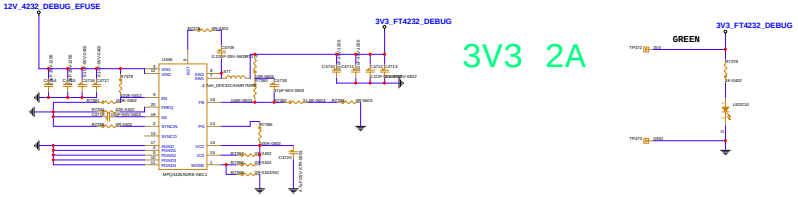
S0-MCU处理

S1-MCU处理

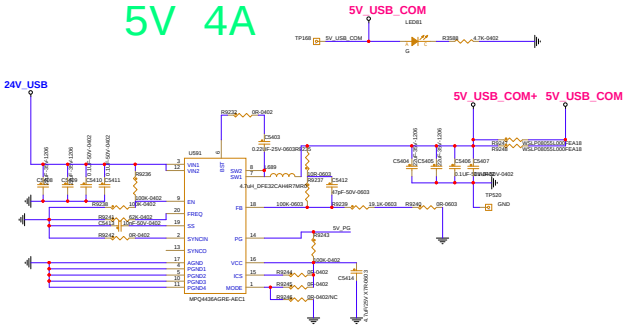


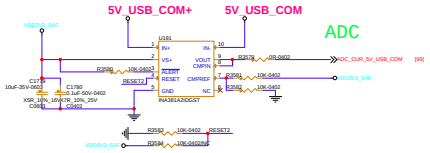
2.5A



3V3 2A

5V 4A





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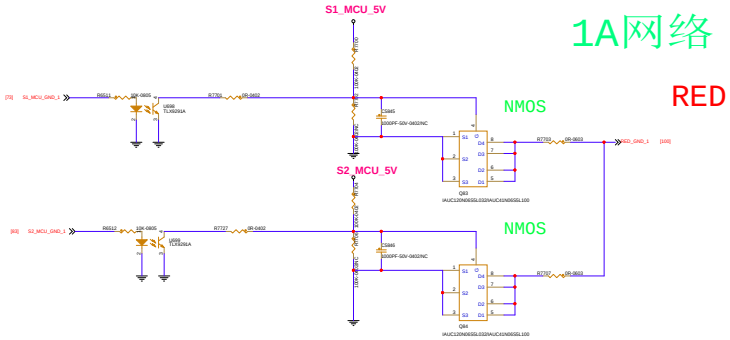
Vds最大60V

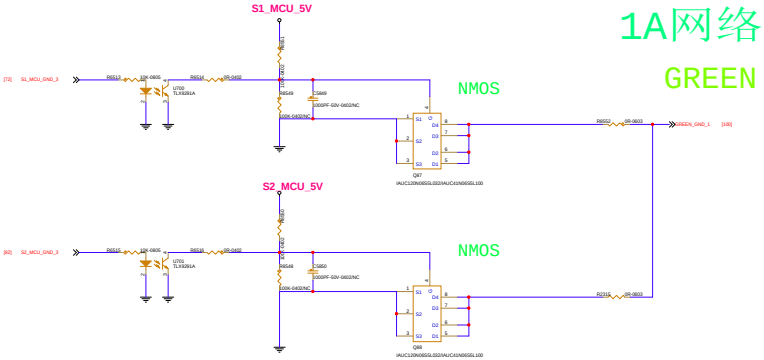
N MOS when Vgs>2.5V,Rds=0.05ohm,Id=40A

IO为1，Vgs不为1，24V灯不亮
IO为0，Vgs=5V，S D导通 24V灯亮



1A网络

RED



1A网络

GREEN

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

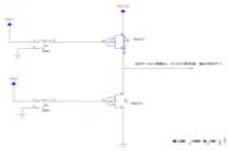
LOGIC DIAGRAM (POSITIVE LOGIC)

推挽输出高电平

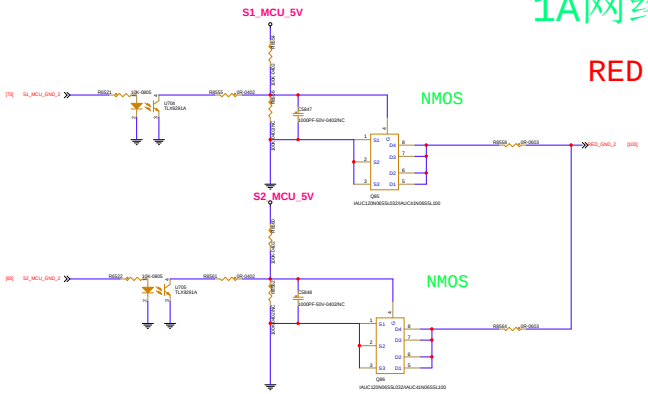
在推挽输出模式下，P-MOS管和N-MOS管同时工作，通过对两个MOS管的导通控制，实现控制输出高低电平，如图所示：

推挽输出低电平

在推挽输出模式下，GPIO口是可以直接输出高低电平的，不需要额外的上来或下拉辅助电路，如图所示：

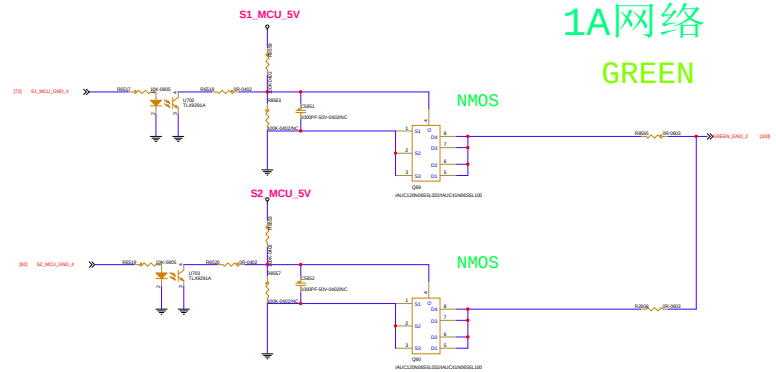


N MOS when Vgs>2.5V,Rds=0.05ohm,Id=3.6A



1A网络

RED



1A网络

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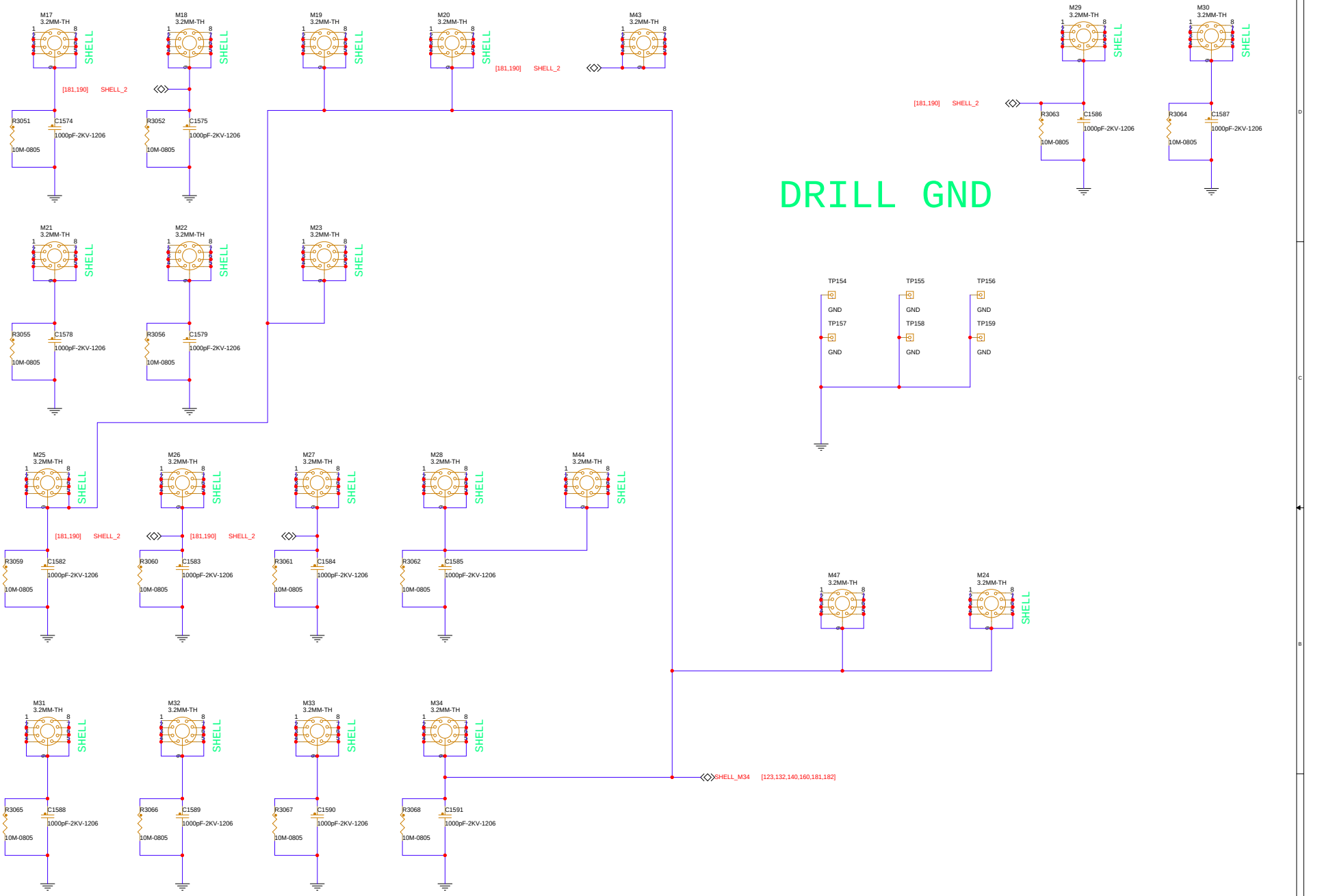

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