CO224 Computer Architecture - 2020 Department of Computer Engineering

Preparation for Lab 6

In preparation for Lab 6, where you will add a memory hierarchy to your processor, please make the below mentioned minor changes related to timing in your existing CPU design. These changes will not affect the functionality of the CPU in any way other than timing.

- 1. Change the clock period to #8 time units
- 2. Change the writing latency in the Register File to #1 time unit
- 3. Add a #1 time unit latency to the Two's Complement unit

With these changes, the datapath timing for our current instructions should be as follows:

add:

DC He Jaka	In atom ation 1	formaria Dand	Danista	n Daad		т.	
PC Update	Instruction Memory Read		Register Read		ALU		
#1	#2		#2		#2		
	PC+4 Adder		Decode				
	#1		#1				
Register		-					
Register Write							
#1							

sub:

PC II. 1.1.	T112 3	f D 1	D tal	. n 1	-2- C	ATTT
PC Update	Instruction N	Memory Read	Register	r Kead	2's Comp	ALU
#1	#2		#2		#1	#2
	PC+4 Adder		Decode			
	#1		#1			
Register Write		_				
Write						
#1						

and/or/mov:

PC Update	Instruction Memory Read		Register Read		ALU		
#1	#2		#2		#1		
	PC+4 Adder		Decode				
	#1		#1				
Register			-				
Register Write							
#1							

loadi:

PC Update	Instruction M	Iemory Read		ALU	
#1	#2			#1	
	PC+4 Adder		Decode		
	#1		#1		
Register					
Register Write					
#1					

j:

PC Update	Update Instruction Memory Read		Decode	
#1	#2		#1	
	PC+4 Adder		Branch/Jump	Target Adder
	#1		#:	2

beq:

			•			
PC Update	Instruction Memory Read		Register Read		2's Comp	ALU
#1	#2		#2		#1	#2
	PC+4 Adder		Branch/Jump Target Adder			
	#1		#2			
			Decode			
			#1			