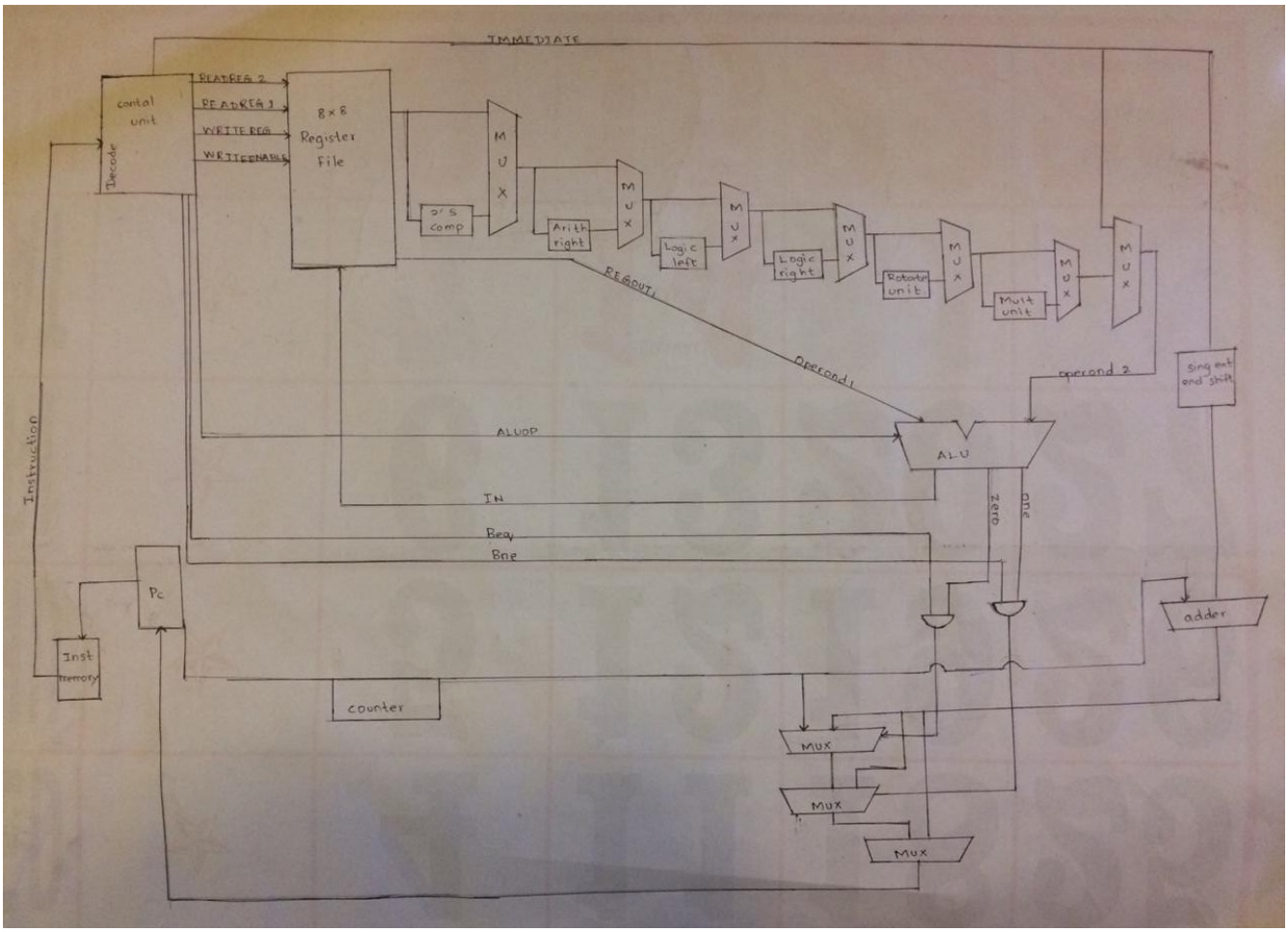
This is data path of my cpu module .



Here I add new five module for Part 5 – Extended ISA those are

- Multiplication module
- Arithmetic right shift module
- Logical right shift module
- Logical left shift module
- Rotate module

* Multiplication module have 8 adding operation and concatenation inside the module but it all operations happened when only the mult instruction come so I put the delay as 2 time unit because if I give long time delay then its take more then one clock cycle .

* Other modules are doing only concatenation so this operation is taking less amount of time and this all operations are happened when only that function working that's why I put the delay as 1 time unit.

*Branch not equal instruction done same as branch equal instruction so there only adder taking 2 time unit .

* All module function are selecting by mux and out put send to ALU then alu updating register file