CO224 Computer Architecture - 2020
Department of Computer Engineering

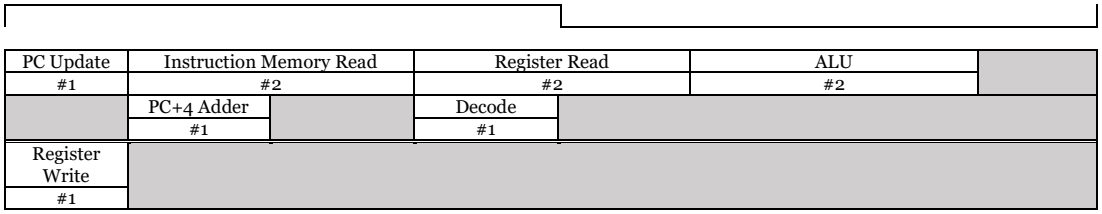
Preparation for Lab 6

In preparation for Lab 6, where you will add a memory hierarchy to your processor, please make the below mentioned minor changes related to timing in your existing CPU design. These changes will not affect the functionality of the CPU in any way other than timing.

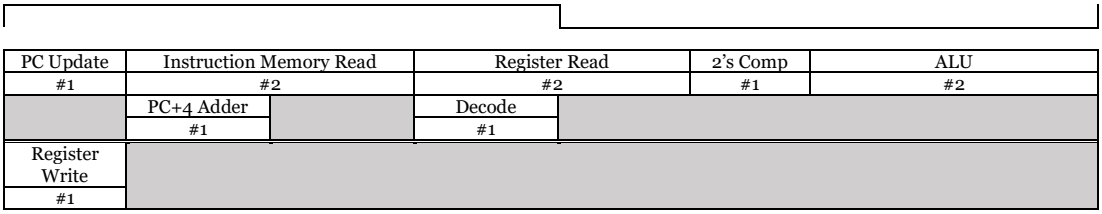
1. Change the clock period to #8 time units
2. Change the writing latency in the Register File to #1 time unit
3. Add a #1 time unit latency to the Two's Complement unit

With these changes, the datapath timing for our current instructions should be as follows:

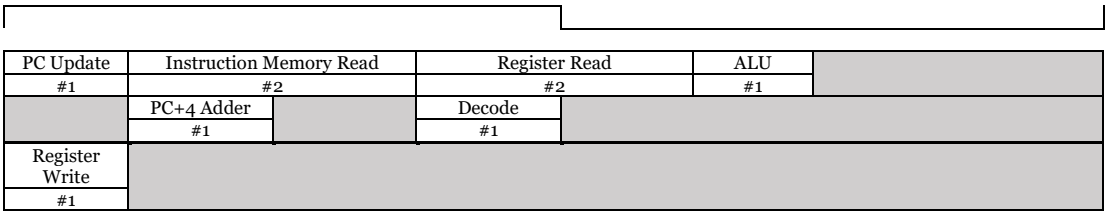
add:



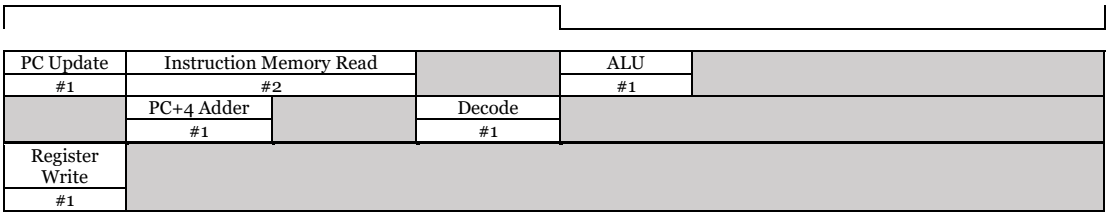
sub:



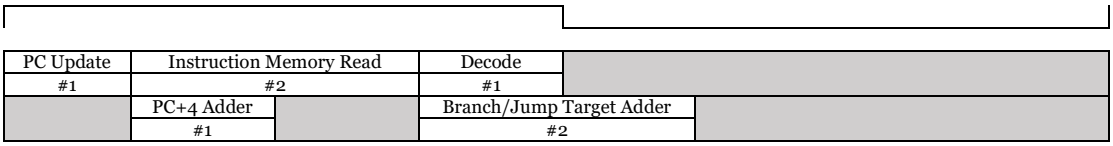
and/or/mov:



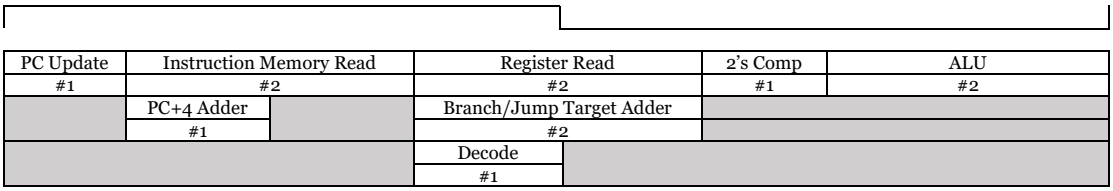
loadi:


PC Update
#1
Instruction Memory Read
#2
ALU
#1
PC+4 Adder
#1
Decode
#1
Register Write
#1

j:


PC Update
#1
Instruction Memory Read
#2
Decode
#1
PC+4 Adder
#1
Branch/Jump Target Adder
#2

beq:


PC Update
#1
Instruction Memory Read
#2
Register Read
#2
2's Comp
#1
ALU
#2
PC+4 Adder
#1
Branch/Jump Target Adder
#2
Decode
#1