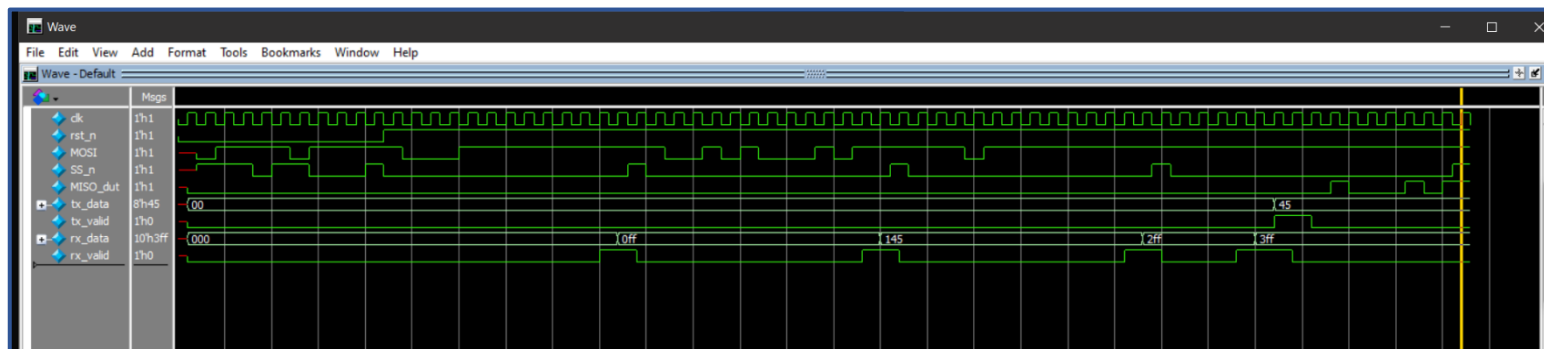


Project_2

SPI Slave with Single Port RAM

- QuestaSim Waveform:



- QuestaLint:

The image shows the QuestaLint interface with the source code of the `SPI_slave_top_module` and the Lint Summary table.

```
1 module SPI_slave_top_module(
2     input MOSI,
3     input SS_n,
4     input clk,
5     input rst_n,
6     output MISO
7 );
8
9 wire [9:0] rx_data;
10 wire [7:0] tx_data;
11 wire rx_valid, tx_valid;
12 // SPI_slave module
13 spi_slave_if SPI_Slave(
14     .MOSI(MOSI),
15     .SS_n(SS_n),
16     .clk(clk),
17     .rst_n(rst_n),
18     .tx_data(tx_data),
19     .tx_valid(tx_valid),
20     .MISO(MISO),
21     .rx_data(rx_data),
22     .rx_valid(rx_valid)
23 );
24 // MEMORY module
25 spi_sync_ram RAM(
26     .tx_data(tx_data),
27     .rx_data(rx_data)
28 );
```

Lint Summary

Name	Count
Open(uninspected, pendi...	2
Warning	1
Info	1

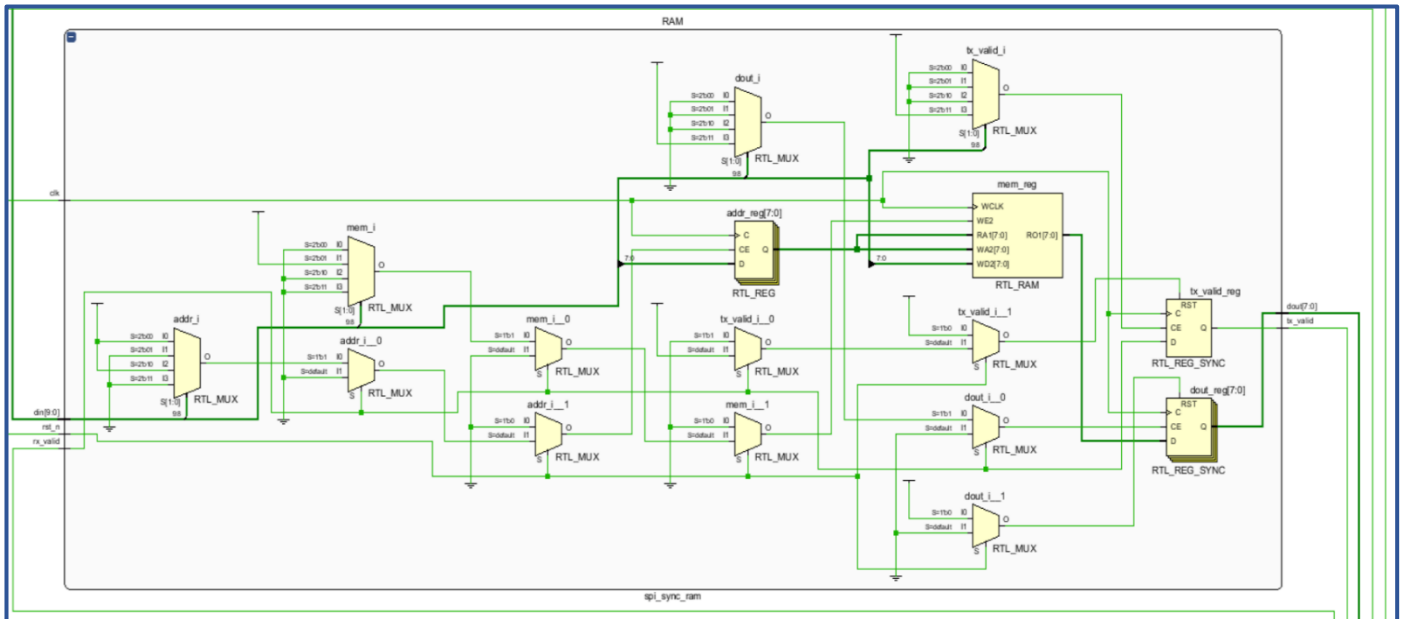
Lint Checks

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	STARC Reference
Warning	2	if_stmt_shares_arithmeti...		If statement has three or more operations sharing the...	spi_slave_if	Rtl Design Style	open	unassign...	2.10.5.3
Warning	2	always_signal_assign_large		Always block has more signal assignments than the s...	spi_slave_if	Rtl Design Style	open	unassign...	2.6.1.3

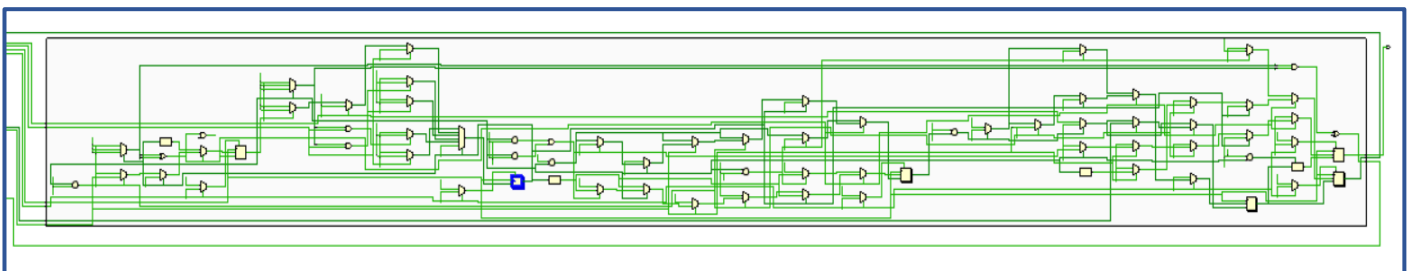
- **Gray Code:**

- **Elaboration:**

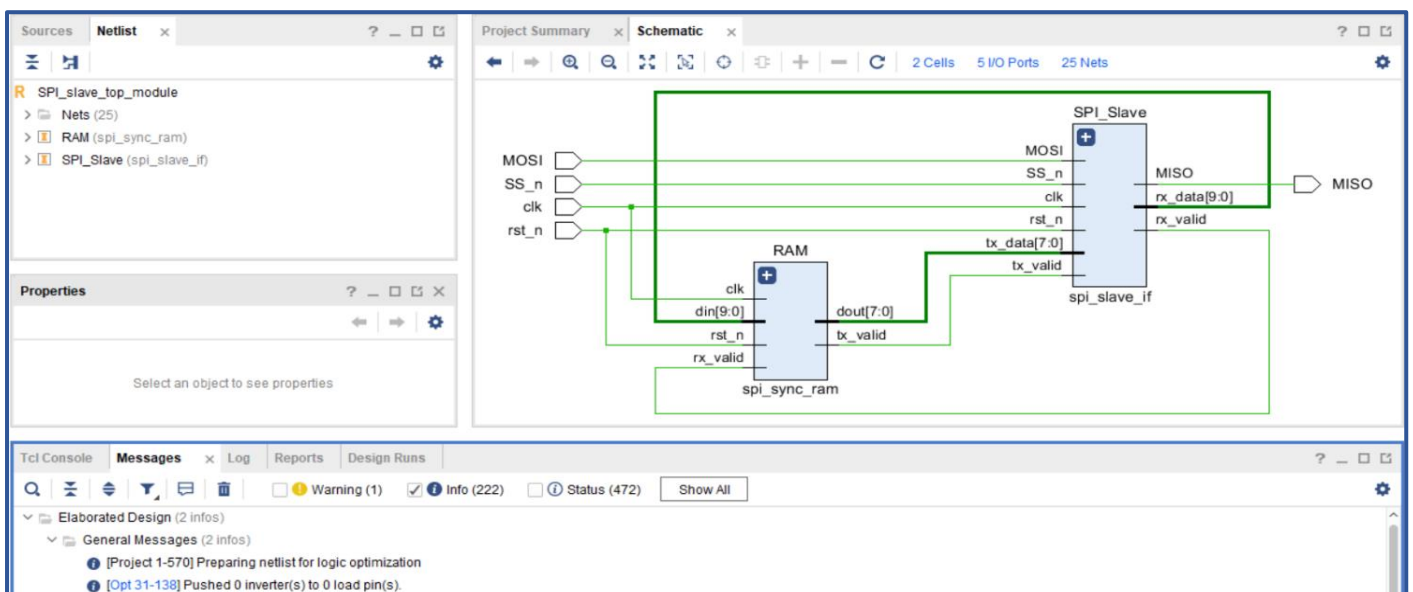
- 1) Ram



- 2) SPI_slave



- 3) Wrapper



○ Synthesis:

Sources | **Netlist** | ? | □ | ✕

- SPL_slave_top_module
 - Nets (33)
 - Leaf Cells (6)
 - RAM (spi_sync_ram)
 - SPL_Slave (spi_slave_if)

Properties | ? | □ | ✕

Select an object to see properties

Schematic | ? | □ | ✕

102 Cells | 5 I/O Ports | 166 Nets

Tcl Console | **Messages** | Log | Reports | Design Runs | Debug | ? | □ | ✕

Warning (1) | Info (156) | Status (311) | Show All

Synthesis (34 Infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- [Synth 8-6157] synthesizing module 'SPL_slave_top_module' [Wrapper.v:1] (2 more like this)
- [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPL_slave.v:19]
- [Synth 8-6155] done synthesizing module 'spi_slave_if' (1#1) [SPL_slave.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35t1cp236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Digital_Design_codes/Project_2/Constraints_basys3_SPL.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/SPL_slave_top_module_proplmpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Schematic | **synth_1_synth_synthesis_report_0 - synth_1** | □ | ✕

D:/Digital_Design_codes/Project_2/project_2/project_2.runs/synth_1/SPL_slave_top_module.vds

Read-only

92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

93 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

94 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

95

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	111	001
READ_DATA	001	100
READ_ADD	011	011
WRITE	010	010

104 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave_if'

105

106 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:46 ; elapsed = 00:00:53 . Memory (MB): peak = 759.723 ; gain

107

108

Tcl Console | **Messages** | Log | Reports | Design Runs | **Timing** | Debug | ? | □ | ✕

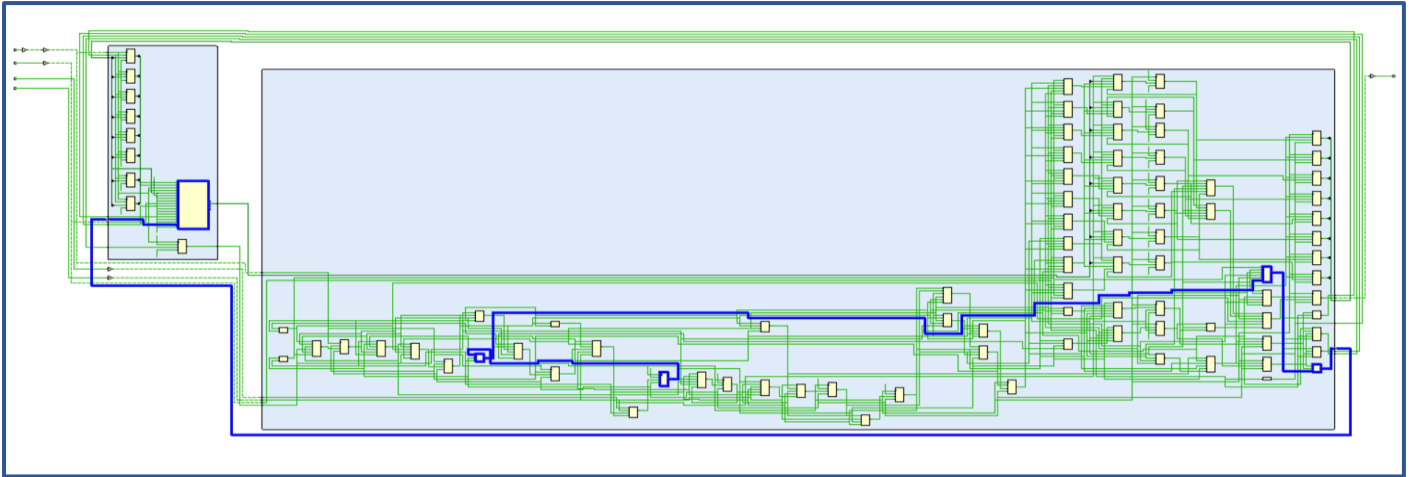
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.755 ns	Worst Hold Slack (WHS): 0.156 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 88	Total Number of Endpoints: 88	Total Number of Endpoints: 41

All user specified timing constraints are met.

Timing Summary - timing_1

Critical Path:



Implementation:

Sources Netlist x ? _ □ □

- SPI_slave_top_module
 - Nets (86)
 - Leaf Cells (6)
 - dbg_hub (dbg_hub)
 - RAM (spi_sync_ram)
 - SPI_Slave (spi_slave_if)
 - u_ila_0 (u_ila_0)

Properties ? _ □ □ x

Select an object to see properties

Project Summary x Device x ? _ □ □

Tcl Console Messages x Log Reports Design Runs Power DRC Methodology Timing ? _ □ □

No Unisim elements were transformed.

Implementation (1 warning, 105 infos, 237 status messages)

- Design Initialization (7 infos, 7 status messages)
 - Command: link_design -top SPI_slave_top_module -part xc7a35t1cp236-1L (6 more like this)
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35t1cp236-1L
 - [Project 1-570] Preparing netlist for logic optimization

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x ? _ □ □

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.187 ns	Worst Hold Slack (WHS): 0.049 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4188	Total Number of Endpoints: 4172	Total Number of Endpoints: 2366

All user specified timing constraints are met.

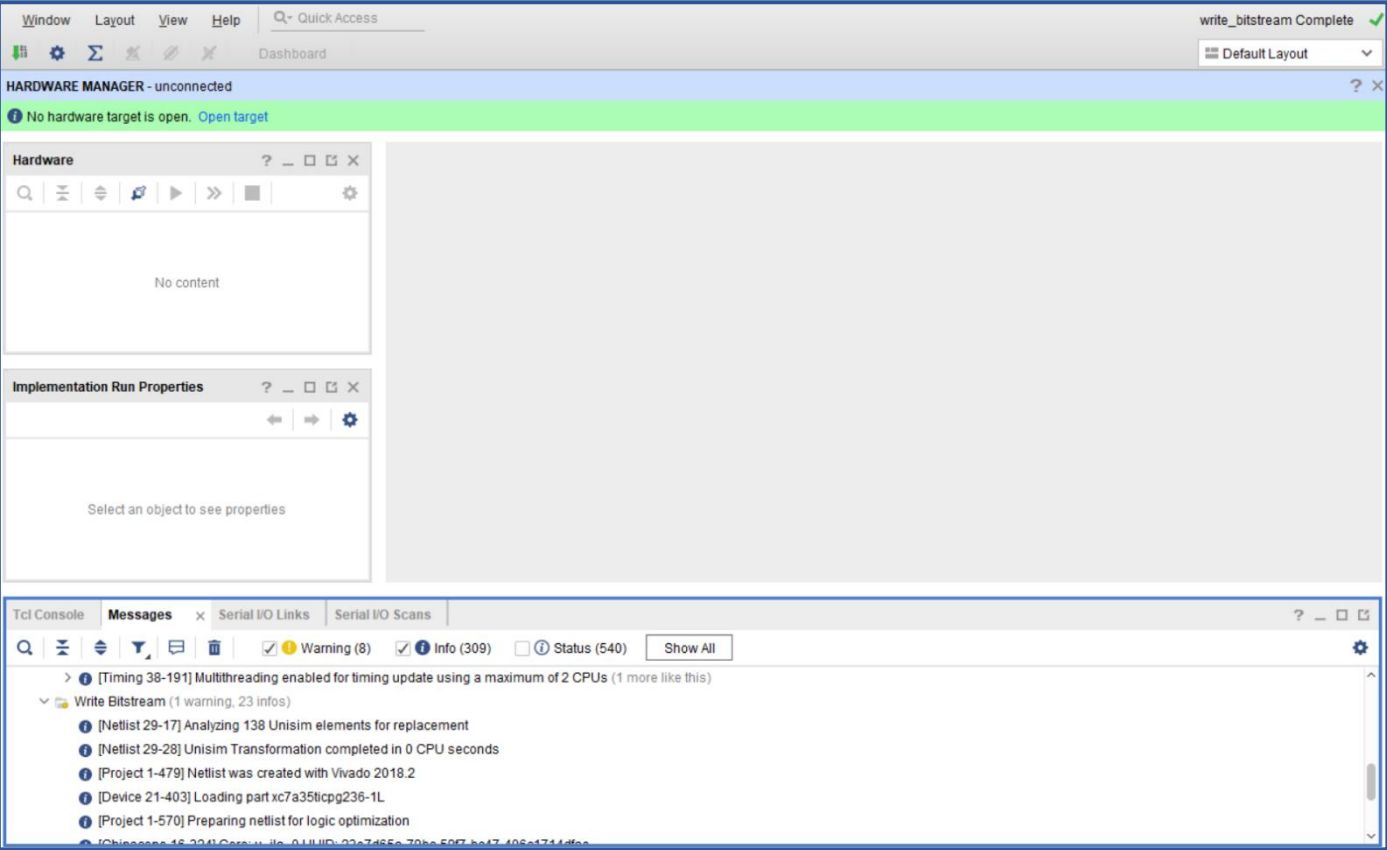
Tcl Console Messages Log Reports Design Runs Power DRC Methodology Utilization x Timing ? _ □ □

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFG (3)
SPI_slave_top_module	1366	2145	13	667	1240	126	819	1.5	5	
dbg_hub (dbg_hub)	476	727	0	232	452	24	310	0	0	
RAM (spi_sync_ram)	0	9	0	2	0	0	0	0.5	0	
CDI Slave (spi_slave_if)	50	20	0	21	50	0	16	0	0	

utilization_1

Generated Bitstream:



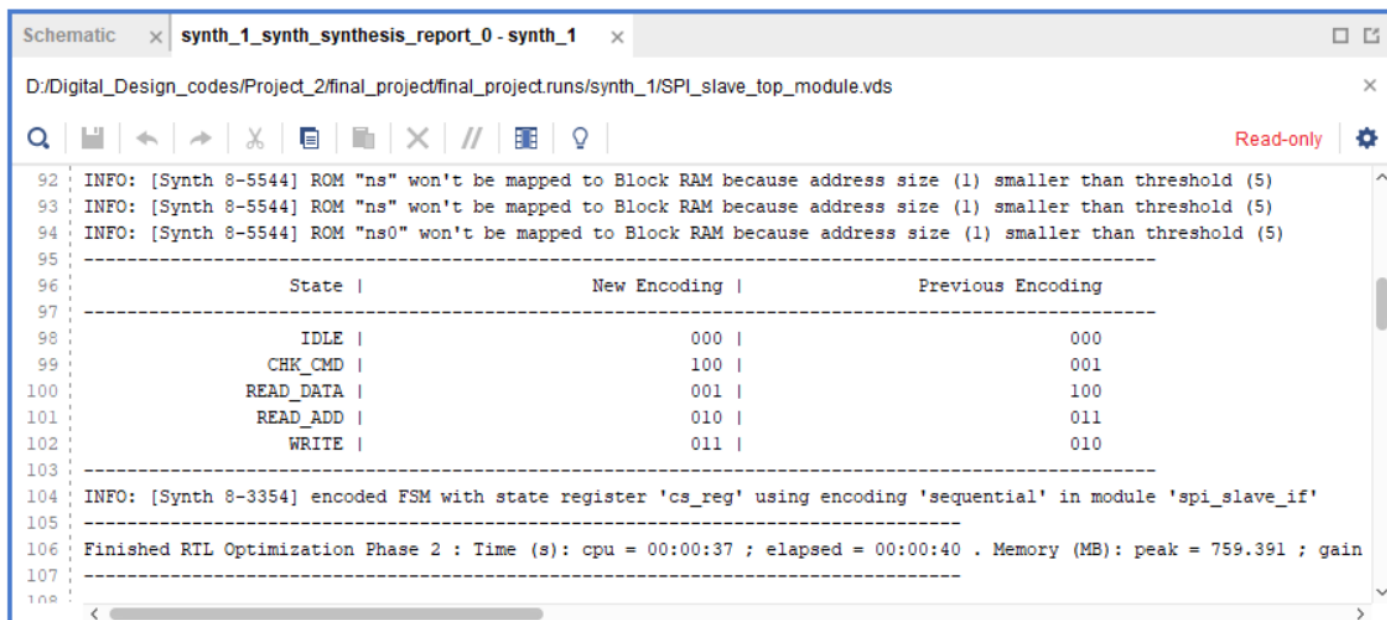
- **Binary Code:**

- **Elaboration:**

The screenshot shows the Vivado IDE during the Elaboration stage. The Sources window on the left lists the Netlist components: counter_reg[1] (RTL_REG_SYNC__BREG_1), counter_reg[2] (RTL_REG_SYNC__BREG_1), counter_reg[3] (RTL_REG_SYNC__BREG_1), cs_j (RTL_MUX), cs_j_0 (RTL_MUX39), cs_reg[0] (RTL_REG_SYNC__BREG_2), cs_reg[1] (RTL_REG_SYNC__BREG_2), and cs_reg[2] (RTL_REG_SYNC__BREG_2). The Cell Properties window shows the details for cs_reg[2], including its Name (SPI_Slave/cs_reg[2]) and Parent (SPI_Slave). The Schematic window displays a complex logic diagram with 130 Cells, 5 I/O Ports, and 347 Nets. The Messages window shows various status and warning messages, including: [Synth 8-6157] synthesizing module 'SPI_slave_top_module' [Wrapper.v:1] (2 more like this), [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [SPI_slave.v:19], [Synth 8-6155] done synthesizing module 'spi_slave_if' (1#1) [SPI_slave.v:1] (2 more like this), [Project 1-570] Preparing netlist for logic optimization, and [Processing XDC Constraints (6 more like this)].

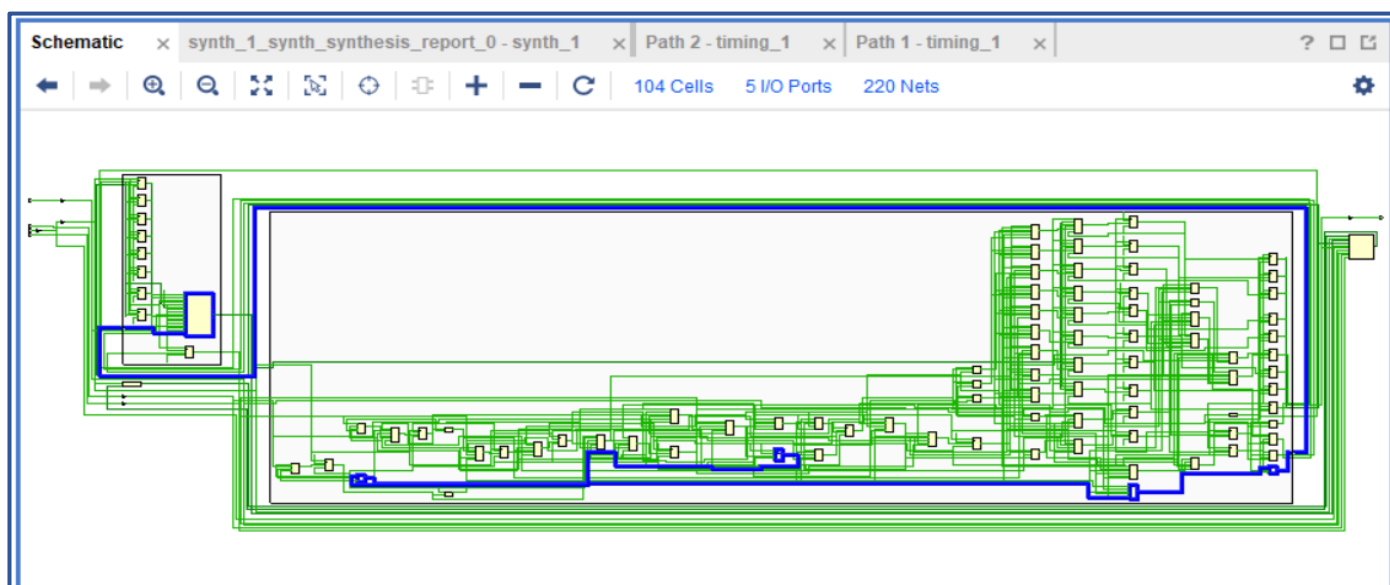
- **Synthesis:**

The screenshot shows the Vivado IDE during the Synthesis stage. The Sources window on the left lists the Netlist components: SPI_slave_top_module, Nets (87), Leaf Cells (6), dbg_hub (dbg_hub_CV), RAM (spi_sync_ram), SPI_Slave (spi_slave_if), and u_ila_0 (u_ila_0_CV). The Properties window shows the details for the selected object. The Schematic window displays a complex logic diagram with 104 Cells, 5 I/O Ports, and 220 Nets. The Messages window shows various status and warning messages, including: [Common 17-1381] The checkpoint 'D:/Digital_Design_codes/Project_2/final_project/final_project.runs/synth_1/SPI_slave_top_module.dcp' has been generated, [runtcl-4] Executing : report_utilization -file SPI_slave_top_module_utilization_synth.rpt -pb SPI_slave_top_module_utilization_synth.pb, [Common 17-206] Exiting Vivado at Fri Mar 14 00:30:36 2025..., [Synthesized Design (2 infos, 2 status messages)], [General Messages (2 infos, 2 status messages)], [Project 1-570] Preparing netlist for logic optimization, [Parsing XDC File [Constraints_basys3_SPI.xdc] (1 more like this)], [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s), and [Implemented Design (1 warning, 10 infos, 13 status messages)].



Tcl Console Messages Log Reports Design Runs Timing x Debug			
Design Timing Summary			
General Information			
Timer Settings			
Design Timing Summary			
Clock Summary (1)			
Check Timing (4)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
Timing Summary - timing_1			
Setup			
Worst Negative Slack (WNS):	5.766 ns	Worst Hold Slack (WHS):	0.157 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	88	Total Number of Endpoints:	88
All user specified timing constraints are met.			
Pulse Width			
Worst Pulse Width Slack (WPWS):	4.500 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Total Number of Endpoints:	41

Critical Path:



○ Implementation:

The screenshot displays the Vivado IDE interface during the implementation phase. The top panel shows the 'Sources' tree with the project hierarchy: SPI_slave_top_module, Nets (86), Leaf Cells (6), dbg_hub (dbg_hub), RAM (spi_sync_ram), SPI_Slave (spi_slave_if), and u_ila_0 (u_ila_0). The 'Properties' panel is empty, prompting the user to select an object.

The 'Project Summary' window shows the 'Device' tab, displaying a 4x4 grid of logic blocks labeled X0Y2, X1Y2, X0Y1, and X1Y1, with a central logic block labeled X0Y0.

The 'Messages' window displays a list of messages, including warnings and information. The 'Implementation' section shows the following messages:

- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- > [Parsing XDC File [Constraints_basys3_SPL.xdc] (1 more like this)]
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- Implementation (1 warning, 105 infos, 237 status messages)
- Design Initialization (7 infos, 7 status messages)
- > Command: link_design -top SPI_slave_top_module -part xc7a35t1cp236-1L (6 more like this)
- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

The 'Timing' window displays the 'Design Timing Summary' table:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.765 ns	Worst Hold Slack (WHS): 0.032 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4188	Total Number of Endpoints: 4172	Total Number of Endpoints: 2366

All user specified timing constraints are met.

The 'Utilization' window displays the 'Hierarchy' table:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFG (3)
SPI_slave_top_module	1365	2145	13	689	1239	126	820	1.5	5	
dbg_hub (dbg_hub)	475	727	0	235	451	24	306	0	0	
RAM (spi_sync_ram)	0	9	0	2	0	0	0	0.5	0	
SPI_Slave (spi_slave_if)	50	20	0	10	50	0	16	0	0	

The 'Hardware Manager' window shows the 'Hardware' tab, indicating that no hardware target is open. The 'Cell Properties' window is empty, prompting the user to select an object.

The 'Messages' window displays a list of messages, including warnings and information. The 'Write Bitstream' section shows the following messages:

- [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
- [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
- Write Bitstream (1 warning, 22 infos, 20 status messages)
- > Command: open_checkpoint SPI_slave_top_module_routed.dcp (19 more like this)
- [Netlist 29-17] Analyzing 138 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-479] Netlist was created with Vivado 2018.2

- Onehot Code:

- **Elaboration:**

Sources | Netlist | ? _ □ □

SPI_slave_top_module

- > Nets (25)
- > RAM (spi_sync_ram)
- > SPI_Slave (spi_slave_if)

Cell Properties | ? _ □ □ ×

Select an object to see properties

Project Summary | Schematic | ? _ □ □

130 Cells 5 I/O Ports 347 Nets

Tcl Console | Messages | Log | Reports | Design Runs | ? _ □ □

Warning (10) Info (319) Status (567) Hide All

Vivado Commands (2 warnings, 3 infos, 8 status messages)

- > General Messages (2 warnings, 3 infos, 8 status messages)
- > Elaborated Design (11 infos, 7 status messages)
- > General Messages (11 infos, 7 status messages)
- > [Synth 8-6157] synthesizing module 'SPI_slave_top_module' [Wrapper.v:1] (2 more like this)
- > [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_slave.v:19]
- > [Synth 8-6155] done synthesizing module 'spi_slave_if' (1#1) [SPI_slave.v:1] (2 more like this)
- > [Project 1-570] Preparing netlist for logic optimization
- > [Processing XDC Constraints (6 more like this)]

- **Synthesis:**

Sources | Netlist | ? _ □ □

SPI_slave_top_module

- > Nets (87)
- > Leaf Cells (6)
- > dbg_hub (dbg_hub_CV)
- > RAM (spi_sync_ram)
- > SPI_Slave (spi_slave_if)
- > u_ila_0 (u_ila_0_CV)

Properties | ? _ □ □ ×

Select an object to see properties

Schematic | ? _ □ □

110 Cells 5 I/O Ports 226 Nets

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug | ? _ □ □

Warning (6) Info (65) Status (50) Hide All

Synthesis (1 warning, 34 infos, 11 status messages)

- > Command: synth_design -top SPI_slave_top_module -part xc7a35t1cp236-1L (10 more like this)
- > [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- > [Synth 8-6157] synthesizing module 'SPI_slave_top_module' [Wrapper.v:1] (2 more like this)
- > [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_slave.v:19]
- > [Synth 8-6155] done synthesizing module 'spi_slave_if' (1#1) [SPI_slave.v:1] (2 more like this)
- > [Device 21-403] Loading part xc7a35t1cp236-1L
- > [Project 1-236] Implementation specific constraints were found while reading constraint file [D:\Digital_Design_codes\Project_2\Constraints_basys3_SPL.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil\SPI_slave_top_module_proplmpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run

Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

D:\Digital_Design_codes\Project_2\final_project\final_project.runs\synth_1\SPI_slave_top_module.vds

Read-only

```

89 INFO: [Synth 8-5544] ROM "rd_addr" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
90 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
91 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95
96 -----
97 State | New Encoding | Previous Encoding
98 -----
99 IDLE | 00001 | 000
100 CHK_CMD | 10000 | 001
101 READ_DATA | 00010 | 100
102 READ_ADD | 00100 | 011
103 WRITE | 01000 | 010
104 -----
105 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_if'

```

Tcl Console Messages Log Reports Design Runs Timing x Debug

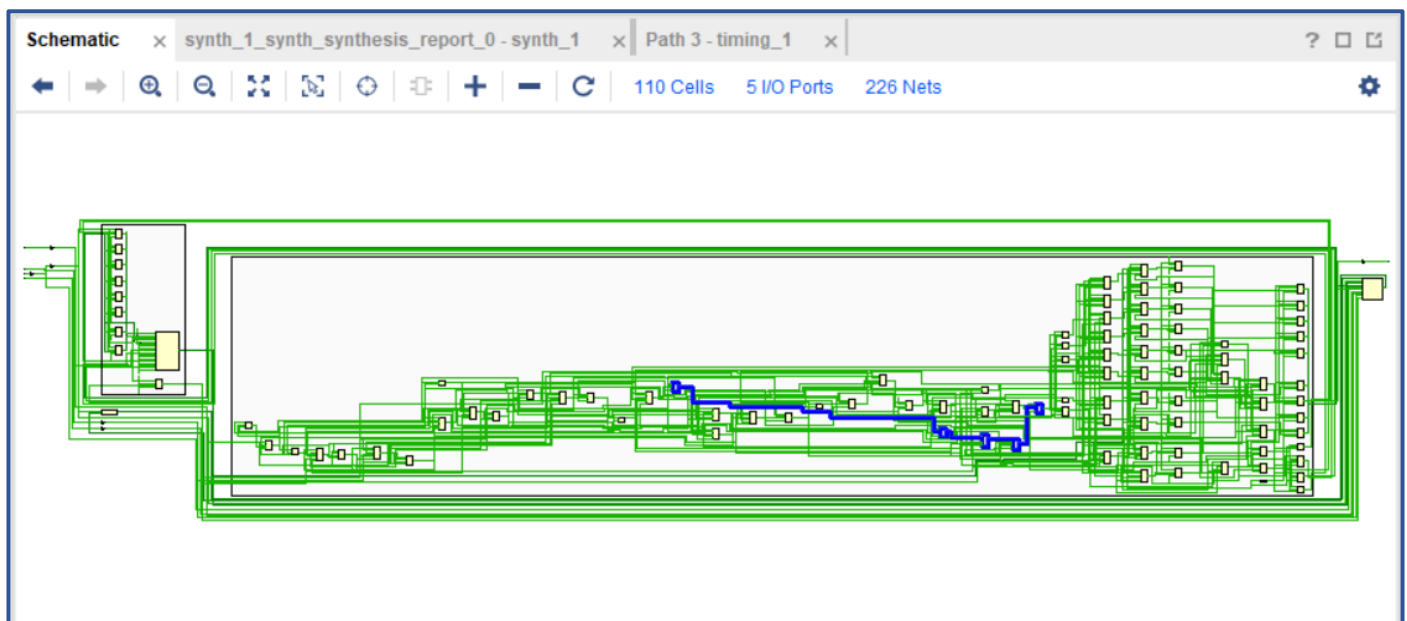
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.933 ns	Worst Hold Slack (WHS): 0.158 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 90	Total Number of Endpoints: 90	Total Number of Endpoints: 43

All user specified timing constraints are met.

Timing Summary - timing_1

Critical Path:



○ Implementation:

SourcesNetlist x ? _ □ □

SPI_slave_top_module

> Nets (86)

> Leaf Cells (6)

> dbg_hub (dbg_hub)

> RAM (spi_sync_ram)

> SPI_Slave (spi_slave_if)

> u_ila_0 (u_ila_0)

Properties? _ □ □ x

Select an object to see properties

Project Summary x Device x ? _ □ □

X0Y2

X1Y2

X0Y1

X1Y1

X0Y0

X1Y0

Tcl ConsoleMessages x Log Reports Design Runs Power DRC Methodology Timing ? _ □ □

[Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_if'

> [Synth 8-4480] The timing for the instance L0RAM/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)

[Project 1-571] Translating synthesized netlist

[Netlist 29-17] Analyzing 5 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 1 CPU seconds

> [Project 1-570] Preparing netlist for logic optimization (1 more like this)

[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

> [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)

Tcl ConsoleMessages x Log Reports Design Runs Power DRC Methodology Timing x ? _ □ □

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (2)

> Check Timing (4)

> Intra-Clock Paths

> Inter-Clock Paths

> Other Path Groups

Timing Summary - impl_1 (saved)

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.098 ns	Worst Hold Slack (WHS): 0.097 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4190	Total Number of Endpoints: 4174	Total Number of Endpoints: 2368

All user specified timing constraints are met.

Tcl ConsoleMessages x Log Reports Design Runs Power DRC Methodology Timing Utilization x ? _ □ □

Hierarchy

Summary

▼ Slice Logic

▼ Slice LUTs (7%)

▼ LUT as Memory (1%)

LUT as Shift Register

LUT as Distribute

utilization_1

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFG (3)
SPI_slave_top_module	1367	2147	13	708	1241	126	822	1.5	5	
dbg_hub (dbg_hub)	475	727	0	245	451	24	308	0	0	
RAM (spi_sync_ram)	0	9	0	2	0	0	0	0.5	0	
CDI Chain (spi_slave_if)	52	24	0	10	52	0	10	0	0	

utilization_1

Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Hardware? _ □ □ x

No content

Properties? _ □ □ x

Select an object to see properties

Tcl ConsoleMessages x Serial I/O Links Serial I/O Scans ? _ □ □

[Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_if'

> [Synth 8-4480] The timing for the instance L0RAM/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)

[Project 1-571] Translating synthesized netlist

[Netlist 29-17] Analyzing 5 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 1 CPU seconds

> [Project 1-570] Preparing netlist for logic optimization (1 more like this)

[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

- According to the time summaries of each encoding method we concluded that gray encoding method is the fastest method with the highest slack setup time.

Team Members:

Marina Bebawy Nasr

Karim Mohamed Elsayed