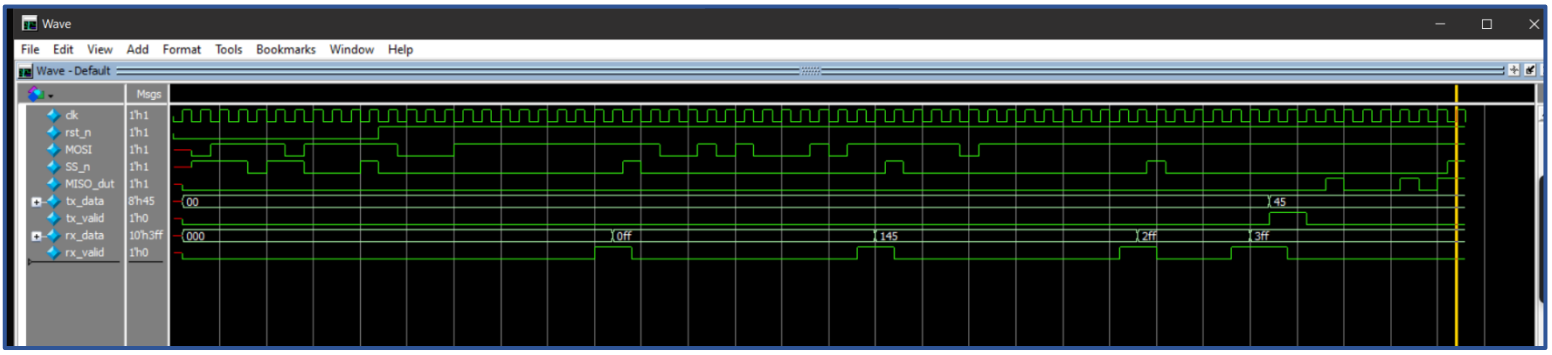
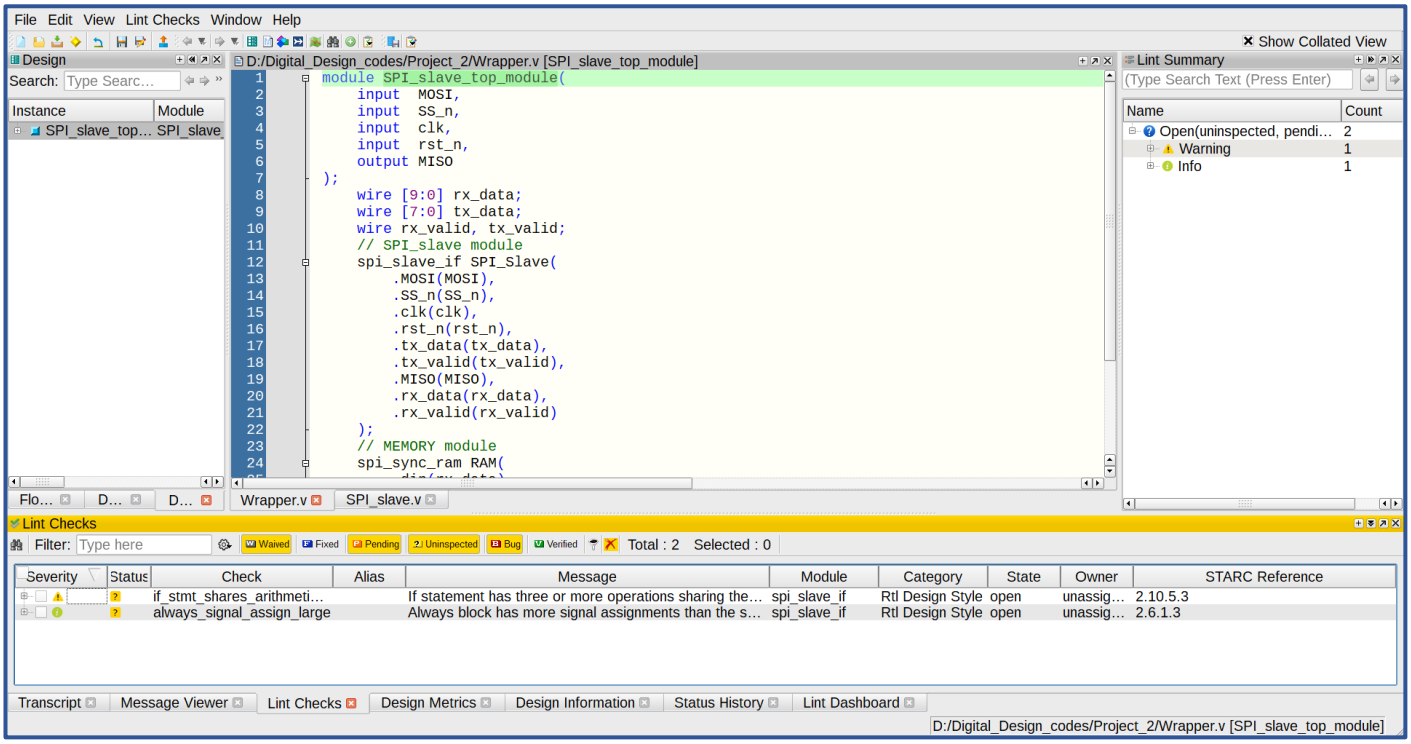
Project_2
SPI Slave with Single Port RAM

- **QuestaSim Waveform:**



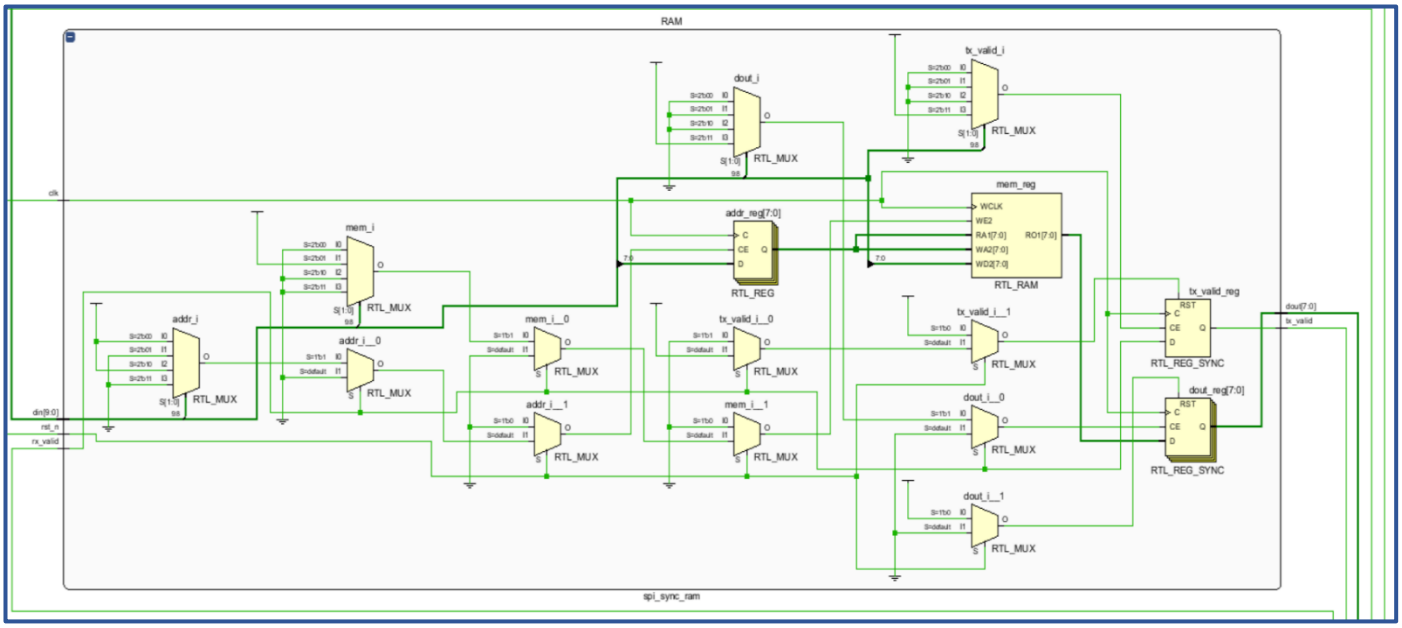
- **QuestaLint:**



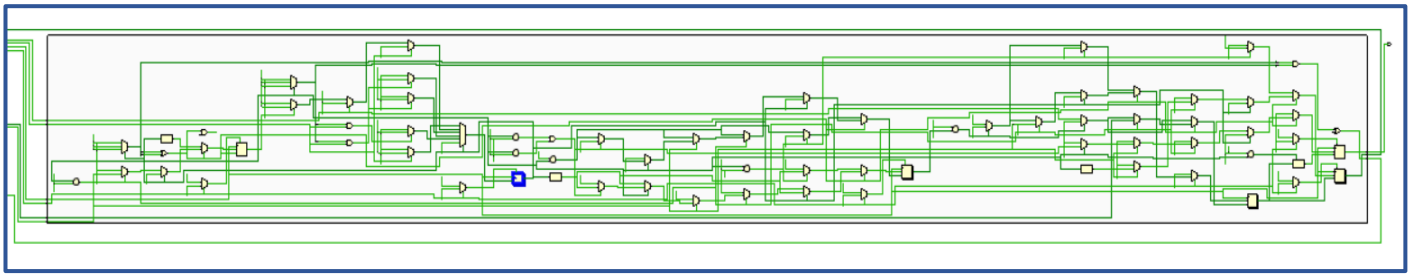
- **Gray Code:**

- **Elaboration:**

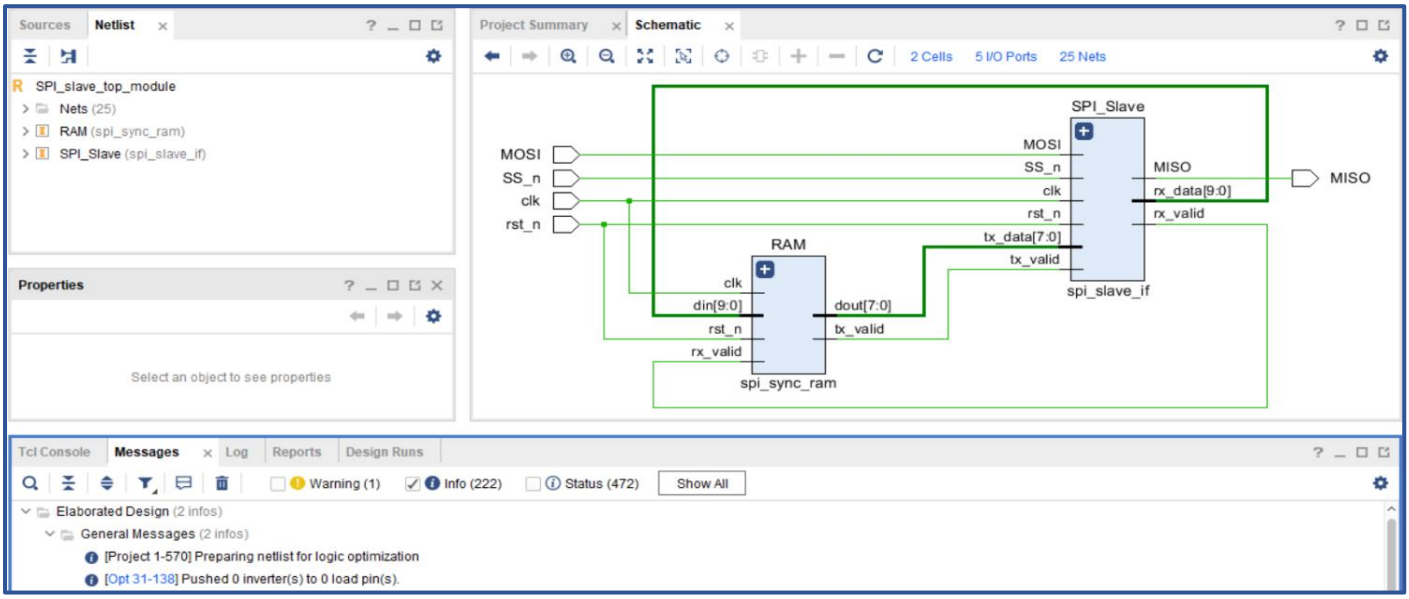
1) Ram



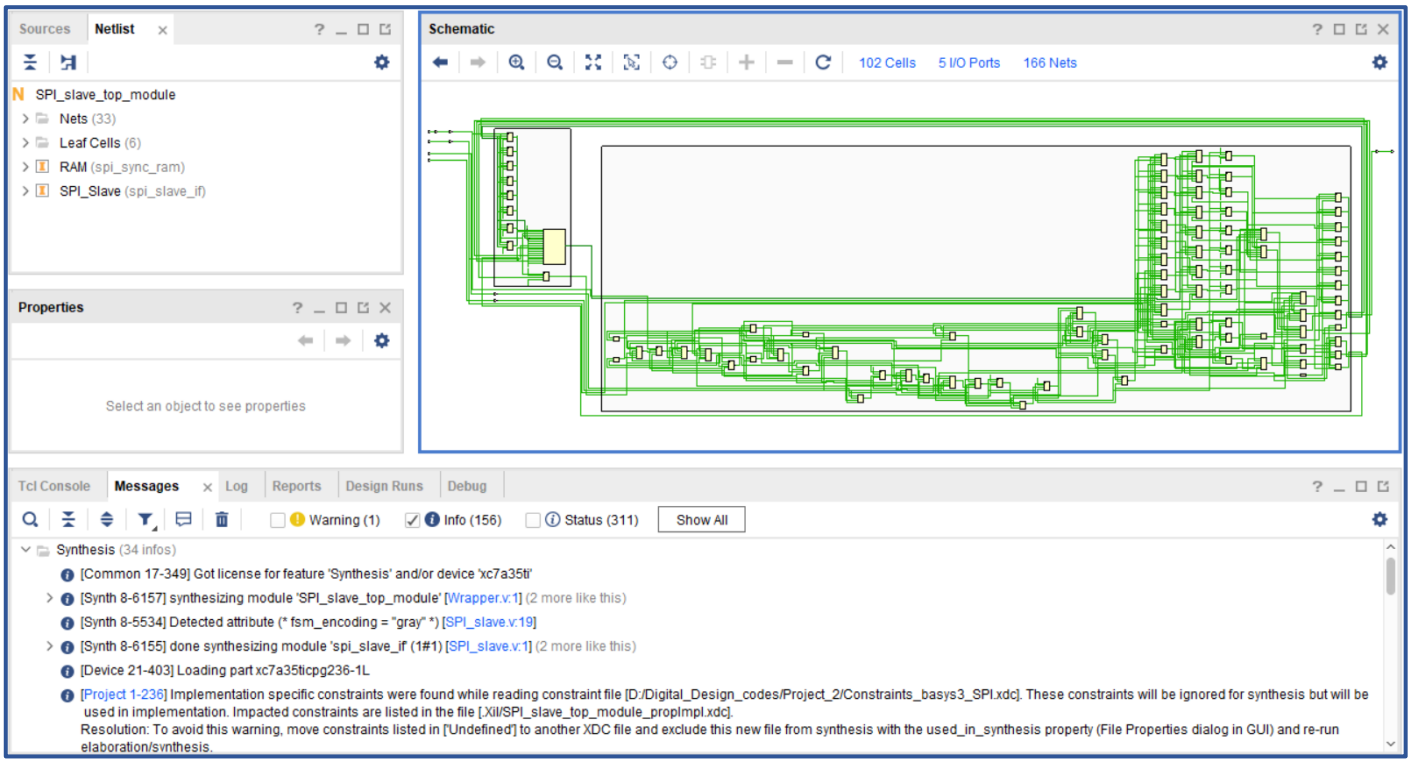
2) SPI_slave

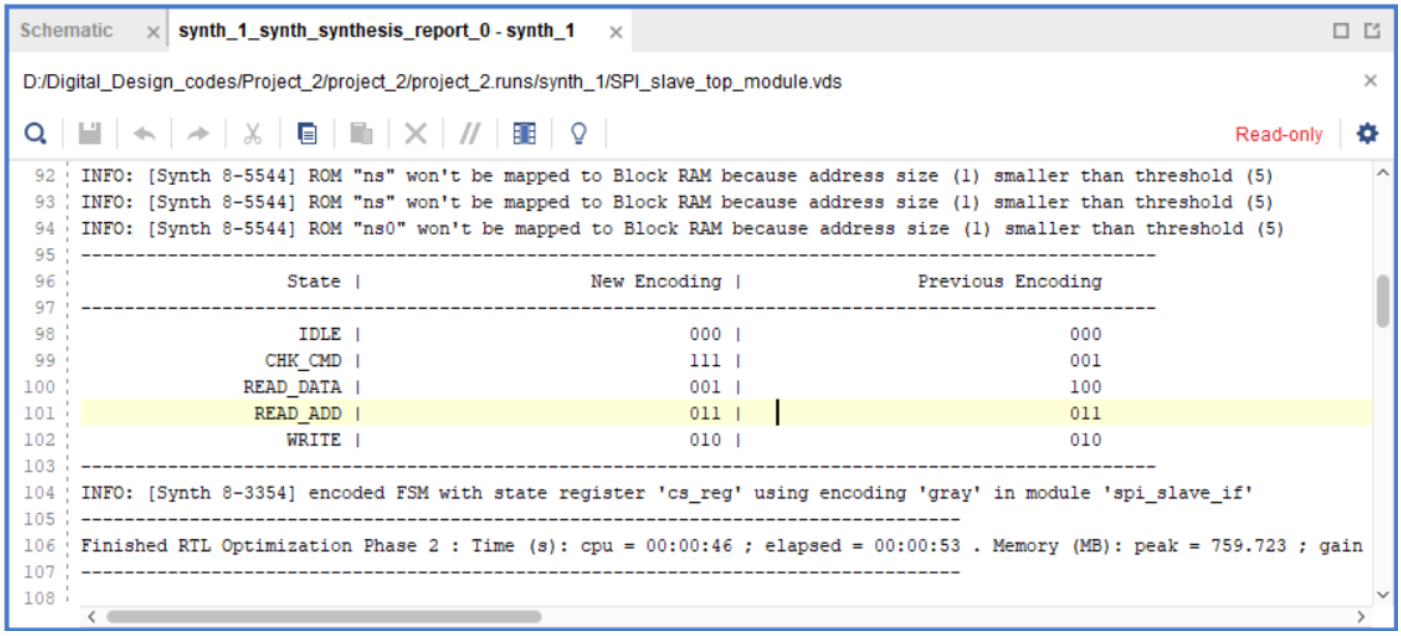


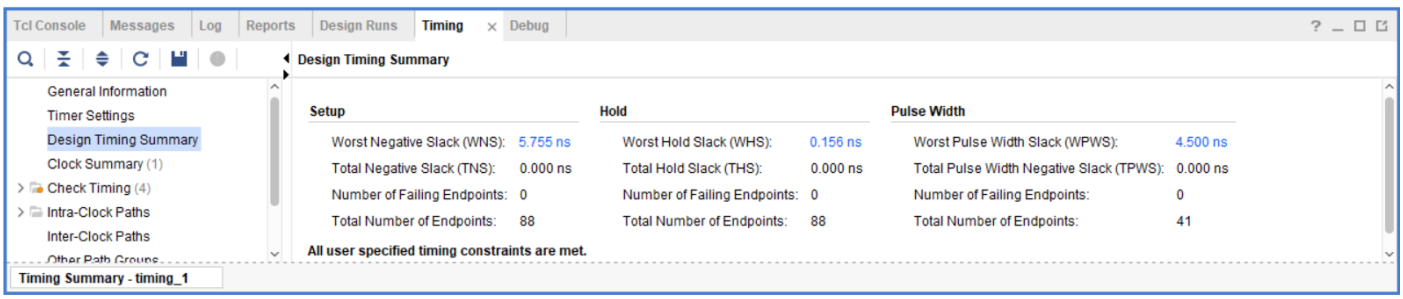
3) Wrapper



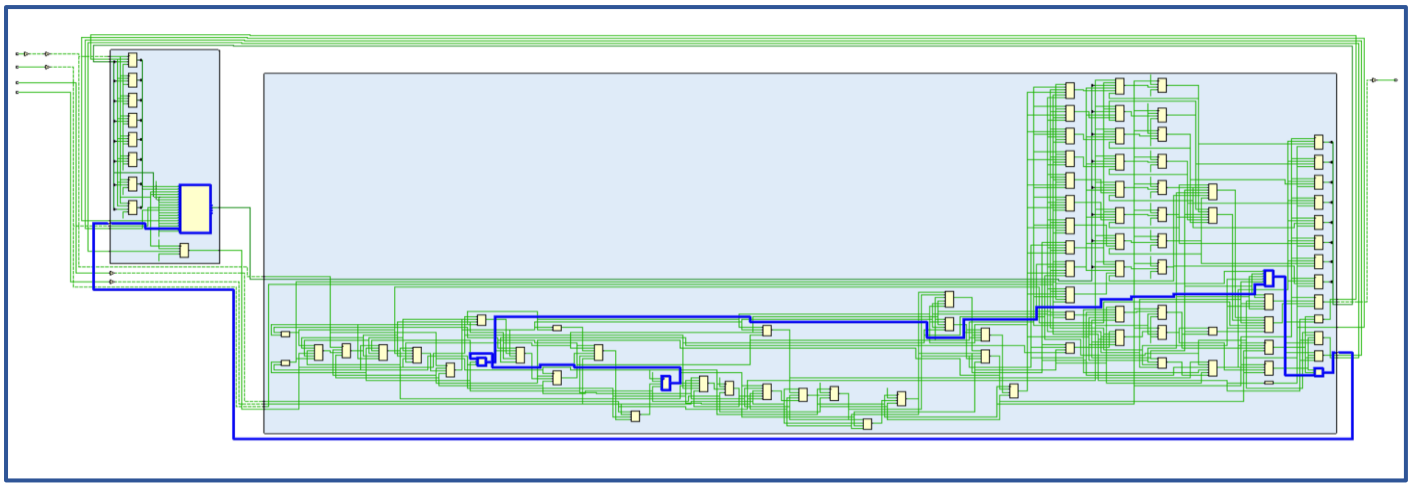
○ Synthesis:


Sources
Netlist
SPI_slave_top_module
Nets (33)
Leaf Cells (6)
RAM (spi_sync_ram)
SPI_Slave (spi_slave_if)
Properties
Select an object to see properties
Schematic
102 Cells
5 I/O Ports
166 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Warning (1)
Info (156)
Status (311)
Show All
Synthesis (34 infos)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
[Synth 8-6157] synthesizing module 'SPI_slave_top_module' [Wrapper.v:1] (2 more like this)
[Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPI_slave.v:19]
[Synth 8-6155] done synthesizing module 'spi_slave_if' (1#1) [SPI_slave.v:1] (2 more like this)
[Device 21-403] Loading part xc7a35ticpg236-1L
[Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Digital_Design_codes/Project_2/Constraints_basys3_SPI.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/SPI_slave_top_module_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

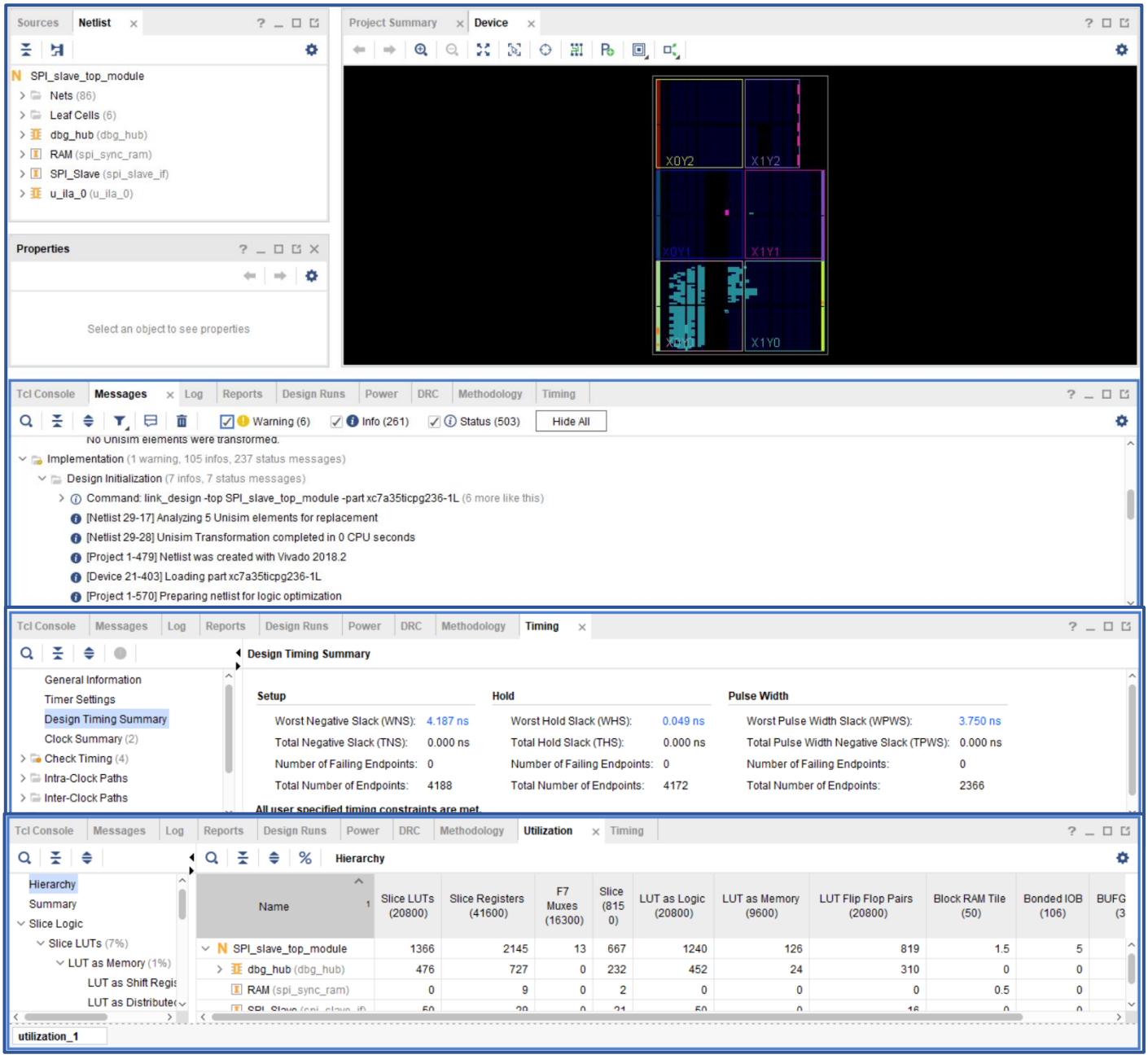

Schematic
synth_1_synth_synthesis_report_0 - synth_1
D:/Digital_Design_codes/Project_2/project_2/project_2.runs/synth_1/SPI_slave_top_module.vds
Read-only
92 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 ---
96 State | New Encoding | Previous Encoding
97 ---
98 IDLE | 000 | 000
99 CHK_CMD | 111 | 001
100 READ_DATA | 001 | 100
101 READ_ADD | 011 | 011
102 WRITE | 010 | 010
103 ---
104 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave_if'
105 ---
106 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:46 ; elapsed = 00:00:53 . Memory (MB): peak = 759.723 ; gain
107 ---
108


Tcl Console
Messages
Log
Reports
Design Runs
Timing
Debug
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (4)
Intra-Clock Paths
Inter-Clock Paths
Setup
Worst Negative Slack (WNS): 5.755 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 88
Hold
Worst Hold Slack (WHS): 0.156 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 88
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 41
All user specified timing constraints are met.
Timing Summary - timing_1

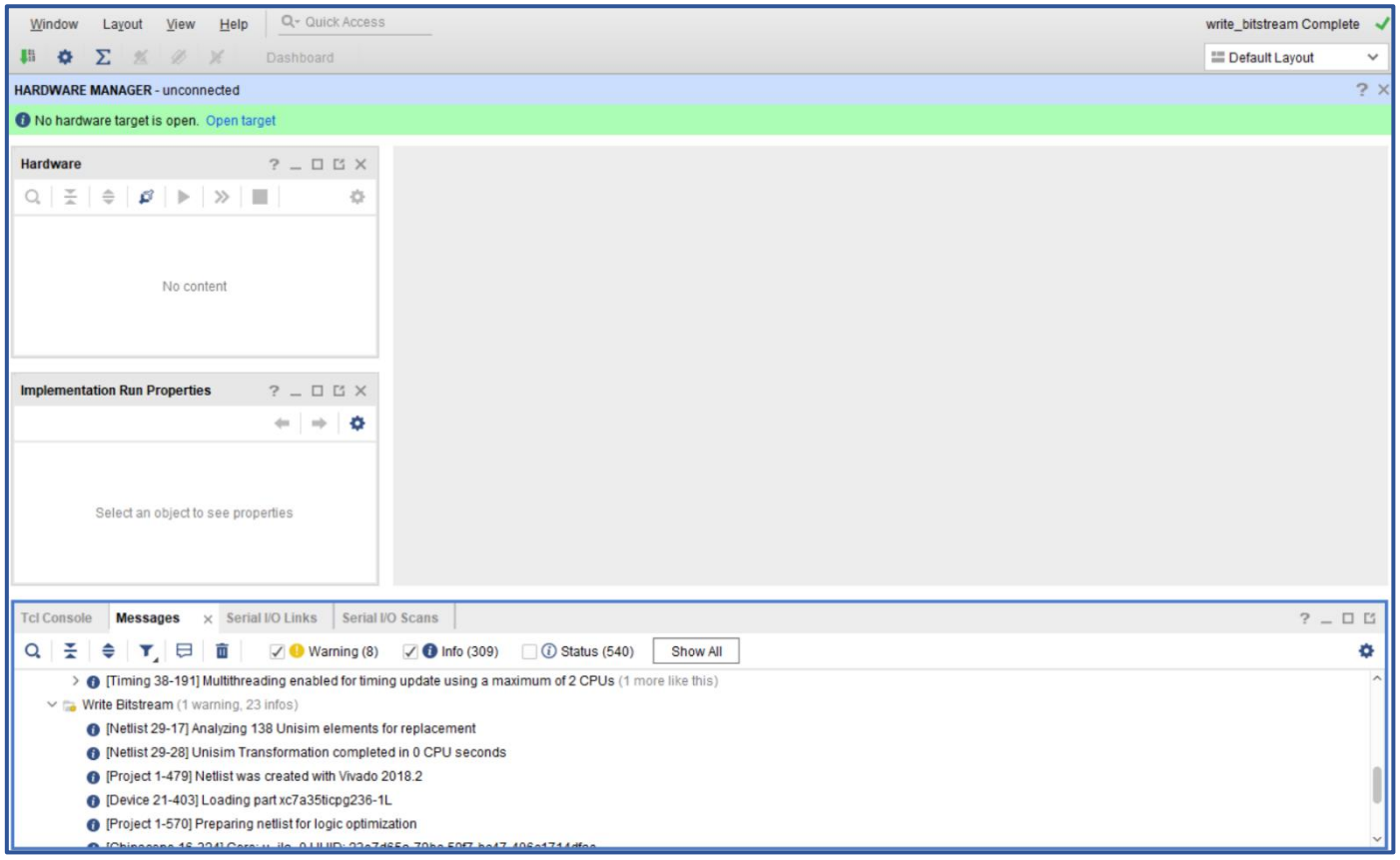
Critical Path:



○ Implementation:

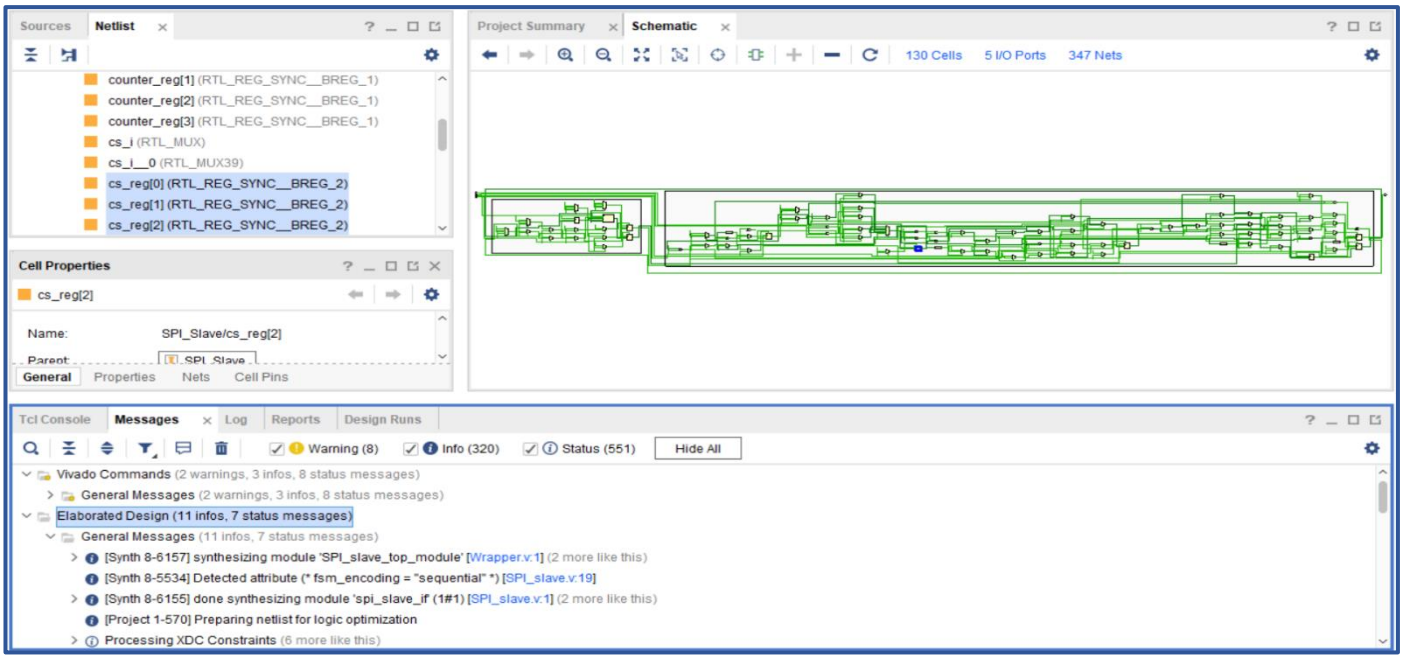


Generated Bitstream:

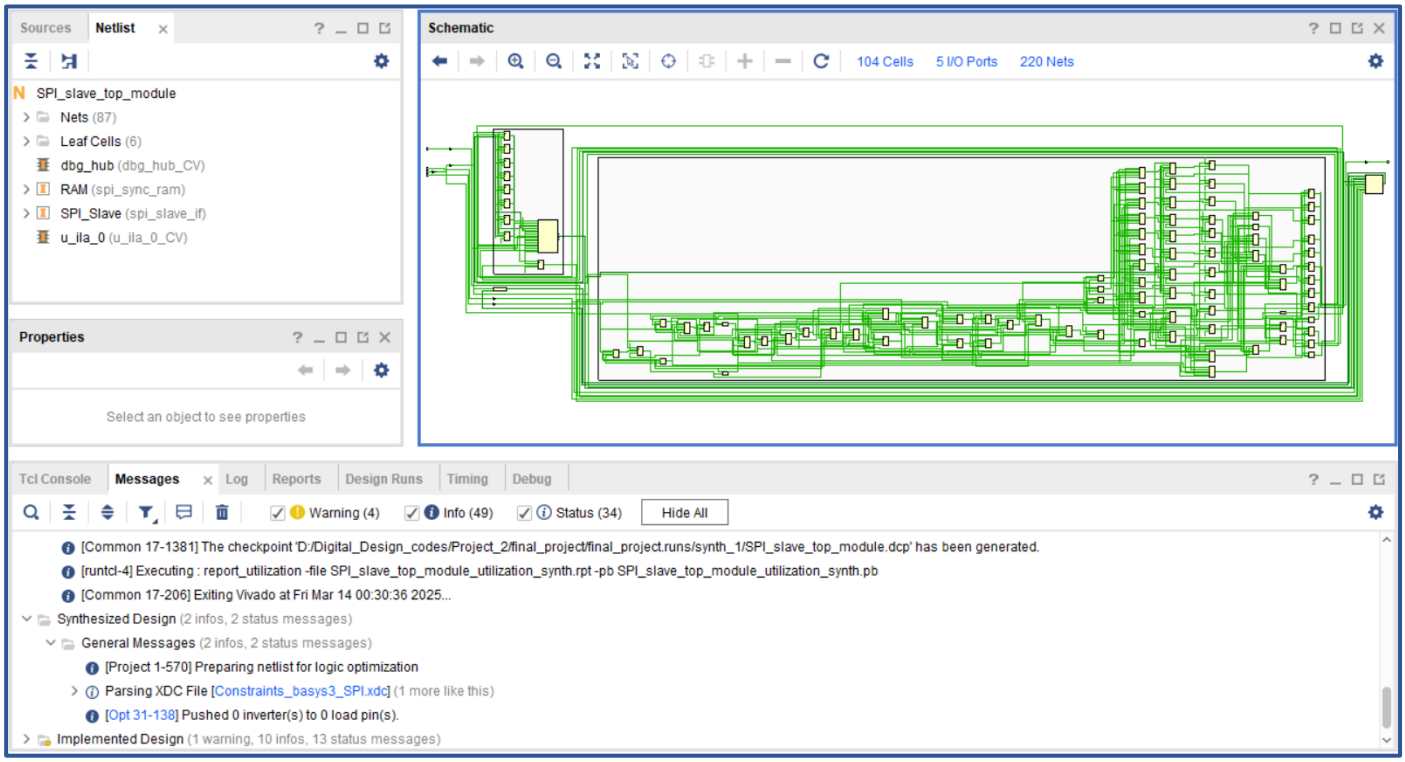


- **Binary Code:**

○ Elaboration:



○ Synthesis:



Schematic | synth_1_synth_synthesis_report_0 - synth_1

D:/Digital_Design_codes/Project_2/final_project/final_project.runs/synth_1/SPI_slave_top_module.vds

Read-only

```
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              100 |                              001
               READ_DATA |                              001 |                              100
                READ_ADD |                              010 |                              011
                   WRITE |                              011 |                              010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi_slave_if'
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 . Memory (MB): peak = 759.391 ; gain
---------------------------------------------------------------------------------
```

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug

Design Timing Summary

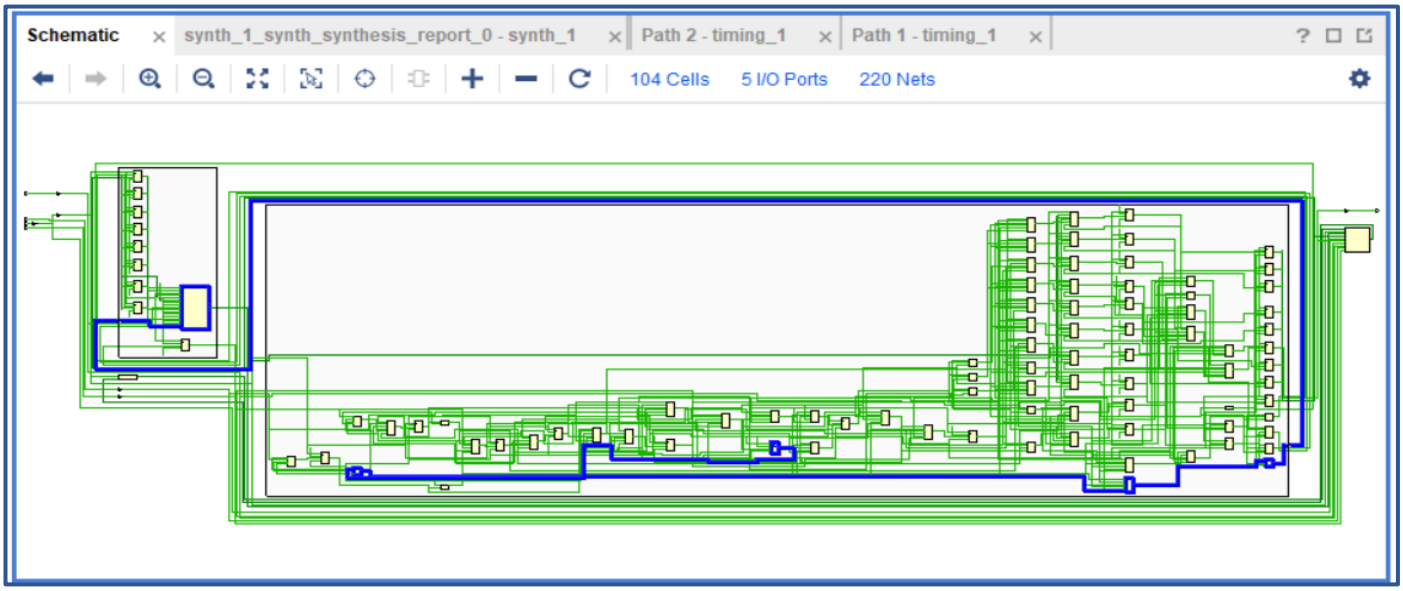
- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (4)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.766 ns	Worst Hold Slack (WHS):	0.157 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	88	Total Number of Endpoints:	88	Total Number of Endpoints:	41

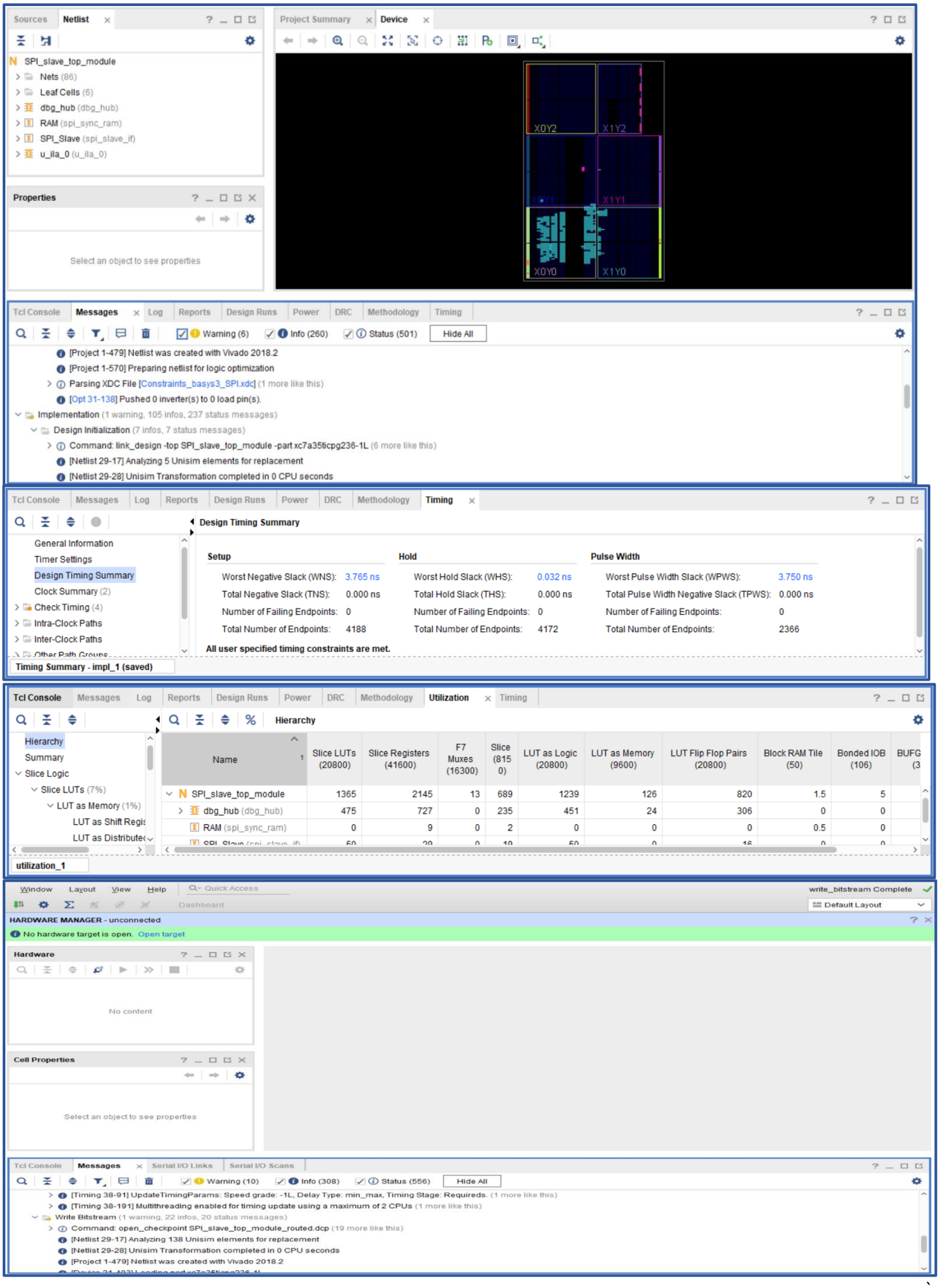
All user specified timing constraints are met.

Timing Summary - timing_1

Critical Path:

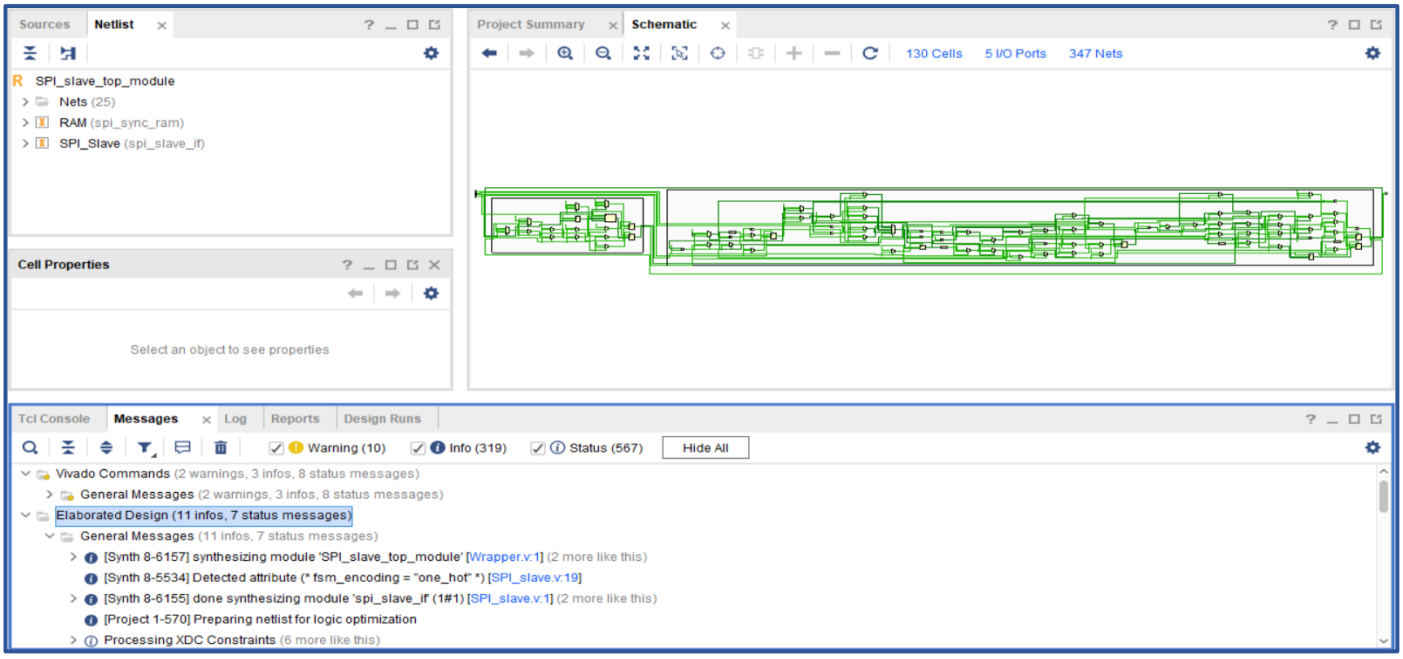


- **Implementation:**

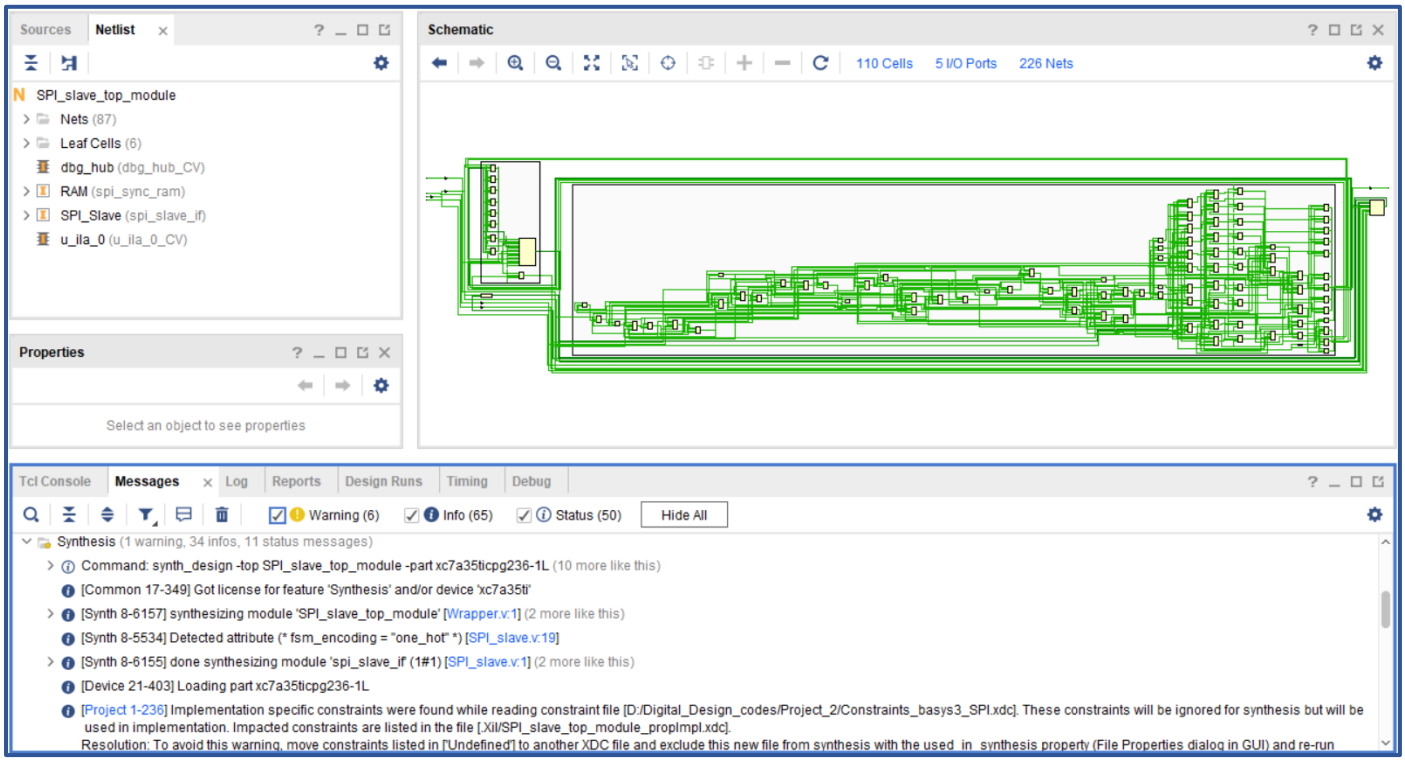


- **Onehot Code:**

○ Elaboration:



○ Synthesis:



Schematic | synth_1_synth_synthesis_report_0 - synth_1

D:/Digital_Design_codes/Project_2/final_project/final_project.runs/synth_1/SPI_slave_top_module.vds

Read-only

```
INFO: [Synth 8-5544] ROM "rd_addr" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                             000
                 CHK_CMD |                            10000 |                             001
               READ_DATA |                            00010 |                             100
                READ_ADD |                            00100 |                             011
                   WRITE |                            01000 |                             010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave_if'
---------------------------------------------------------------------------------------------------
```

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug

Design Timing Summary

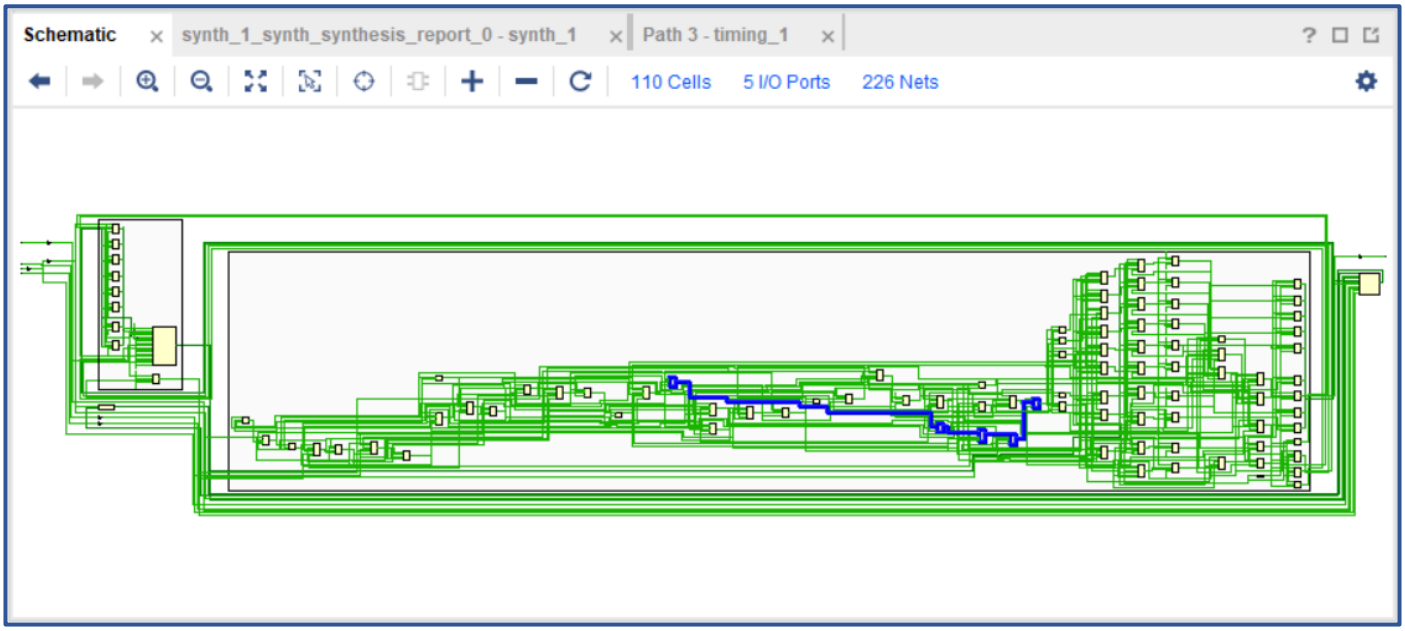
- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (4)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.933 ns	Worst Hold Slack (WHS):	0.158 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	90	Total Number of Endpoints:	90	Total Number of Endpoints:	43

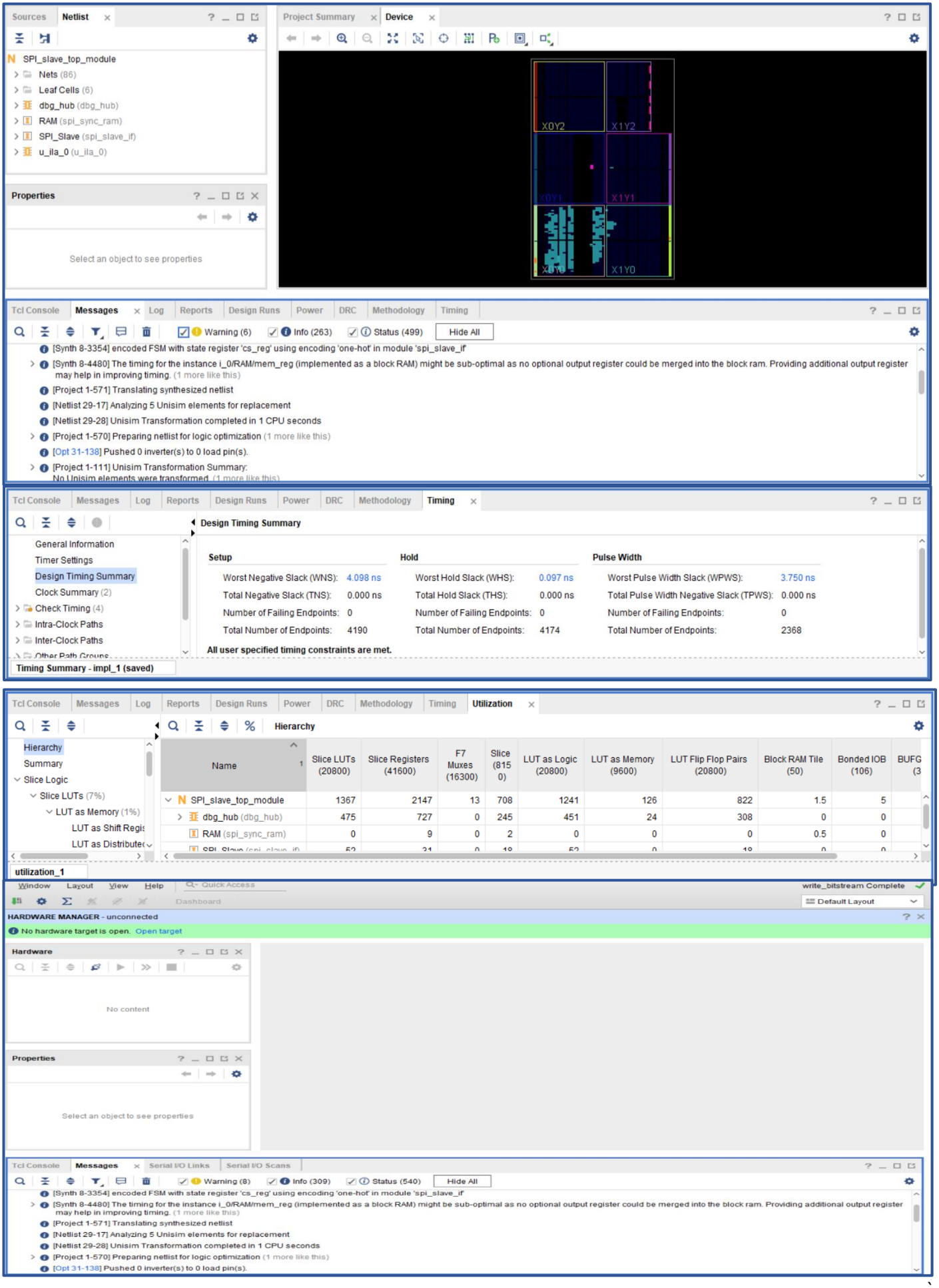
All user specified timing constraints are met.

Timing Summary - timing_1

Critical Path:



- **Implementation:**



- **According to the time summaries of each encoding method we concluded that gray encoding method is the fastest method with the highest slack setup time.**

Team Members:

Marina Bebawy Nasr
Karim Mohamed Elsayed

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