University of East London

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

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Computer Engineering and Software Systems Program - Credit Hours Engineering Programs (iCHEP)
STUDENT PORTFOLIO - Academic Year 2021/2022

UEL Module Code **CESS3005**	*UEL Module Name* **Logic Design**	
ASU Course Code **CSE111**	*ASU Course Name* **Computer Architecture**	
	Semester Fall 2021	**Date of Submission** 13/3/2022

Student Name: Karim Bassel Samir Anby
Student ID (ASU): 20P6794
Student ID (UEL): XXXXXXXXXXXXX

AIN SHAMS UNIVERSITY
I-Credit Hours Engineering Programs
(i.CHEP)

University of East London

Course Code:	CSE111	Course Name:	Logic Design	Lab Project	Date:	**13/3/2022**
Student Name:	**Karim Bassel Samir Anby**			Student ID:	20P6794	

	Mastery ≥90%				Accomplished ≥75 & <90%				Adequate ≥60 & <75%				Inadequate <60%			
	100	96	93	90	89	84	79	75	74	69	64	60	59	40	20	0
	• The project performs four different operations correctly. • Project simulation on Logisim submitted. • Wiring was color coded and correct. • Dip switches used instead of push buttons. • Minimum number of gates used. • Complete project documentation submitted.				• The project performs four different operations. • Project simulation on Logisim submitted. • Wiring was correct but not color coded. • Dip switches used instead of push buttons. • Minimum number of gates used. • Complete project documentation submitted.				• The project performs less than four different operations correctly. • Some of the project simulation on Logisim were submitted. • Wiring was not correct but not color coded. • Dip switches used instead of push buttons. • More number of gates used. • Some project documentation submitted.				• The project performs less than four different operations. • Some of the project simulation on Logisim were submitted. • Wiring was not correct but not color coded. • Push buttons used. • More number of gates used. • Some project documentation submitted.			

1st marker Total	25 marks	1st marker Signature	Hossam Abdelmunim	**ASU** Agreed Mark	24 marks
2nd Marker Total	25 marks	2nd marker Signature	Kyrelloss Nashaat	**UEL** Agreed Mark	24 marks

General Comments:

Well done!

Very good, keep going!

UEL Grading System	Agreed	ASU Grading Scale	
% equivalent at UEL	Mark Range	% at ASU	Grade
95% and higher		97% and higher	A+
82% to less than 95%	Yes Yes	93% to less than 97%	A
70% to less than 82%		89% to less than 93%	A-
66% to less than 70%		84% to less than 89%	B+
63% to less than 66%		80% to less than 84%	B
60% to less than 63%		76% to less than 80%	B-
56% to less than 60%		73% to less than 76%	C+
53% to less than 56%		70% to less than 73%	C
50% to less than 53%		67% to less than 70%	C-
45% to less than 50%		64% to less than 67%	D+
40% to less than 45%		60% to less than 64%	D
Less than 40%		Less than 60%	F

AIN SHAMS UNIVERSITY
I-Credit Hours Engineering Programs
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Report marking criteria

Course Code:	CSE111	Course Name:	Logic Design	Major Task	1	Date:	**5/1/2022**
Student Name:	**Fady Fady Fouad**			Student ID:	**20P7341**		
Student Name:	**Matthew Sherif Shalaby**			Student ID:	**20P6785**		
Student Name:	**Karim Bassel Samir**			Student ID:	**20P6794**		
Student Name:	**Shady Emad Sabry**			Student ID:	**20P7239**		

	A (89-100)				B (76-88)				C (67-75)				D (60-66)				F (0-59)			
	100	96	92	89	88	84	80	76	75	72	69	67	66	64	62	60	59	40	20	0
Literature survey (25%)	• Critical evaluation and synthesis of relevant issues and materials				• Critical evaluation of relevant issues and materials				• Accurate description of main relevant issues				• Limited evaluation and description of main issues				• Insufficient and largely irrelevant material			
Research Objectives (25%)	• Clearly defined research problem with well-structured research objectives				• Complete set of research objectives				• Limited research objectives				• Poorly defined objectives				• Research problem lacking clear objectives			
Research Methodology (25%)	• Clear and relevant research methodology with complete implementation				• Clear and relevant research methodology missing few components				• Clear research methodology missing several components				• Inappropriate research methodology				• Lack of clear research methodology			
Analysis of Results & Conclusions (25%)	• Excellent analysis of results and complete relevant conclusions				• Good analysis of results missing some minor conclusions				• Normal analysis of results missing some basic conclusions				• Incomplete analysis or results with some conclusions				• Missing proper analysis or results and no conclusions at all			

1st marker Total		1st marker Signature		**ASU** Agreed Mark	
2nd Marker Total		2nd marker Signature		**UEL** Agreed Mark	

General Comments:

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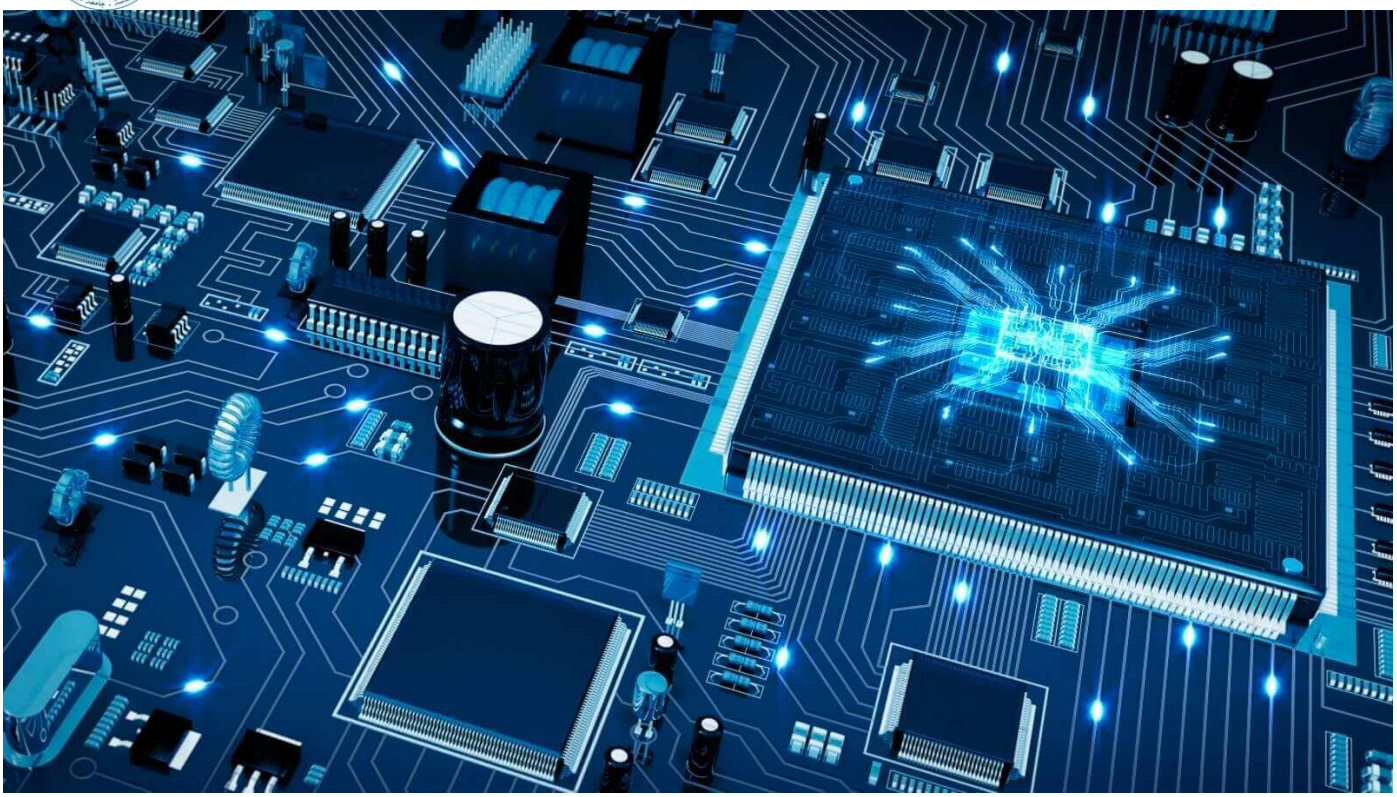
UEL Grading System	Agreed	ASU Grading Scale	
% equivalent at UEL	Mark Range	% at ASU	Grade
95% and higher		97% and higher	A+
82% to less than 95%		93% to less than 97%	A
70% to less than 82%		89% to less than 93%	A-
66% to less than 70%		84% to less than 89%	B+
63% to less than 66%		80% to less than 84%	B
60% to less than 63%		76% to less than 80%	B-
56% to less than 60%		73% to less than 76%	C+
53% to less than 56%		70% to less than 73%	C
50% to less than 53%		67% to less than 70%	C-
45% to less than 50%		64% to less than 67%	D+
40% to less than 45%		60% to less than 64%	D
Less than 40%		Less than 60%	F



Logic Design

Major Task

CSE 111

Members
Fady Fady Fouad 20P7341 **Matthew Sherif Shalaby 20P6785** **Karim Bassel Samir 20P6794** **Shady Emad Sabry 20P7239**

Phase 1:

The purpose of the circuit shown in Fig. 1 is to display the pressed key of the keypad on 7-segment. Design the combinational circuit (DM) shown in Fig. 1. Thiscircuit has input from the standard 4x4 keypad, and its output will feed the BCD- to-7 segment decoder.

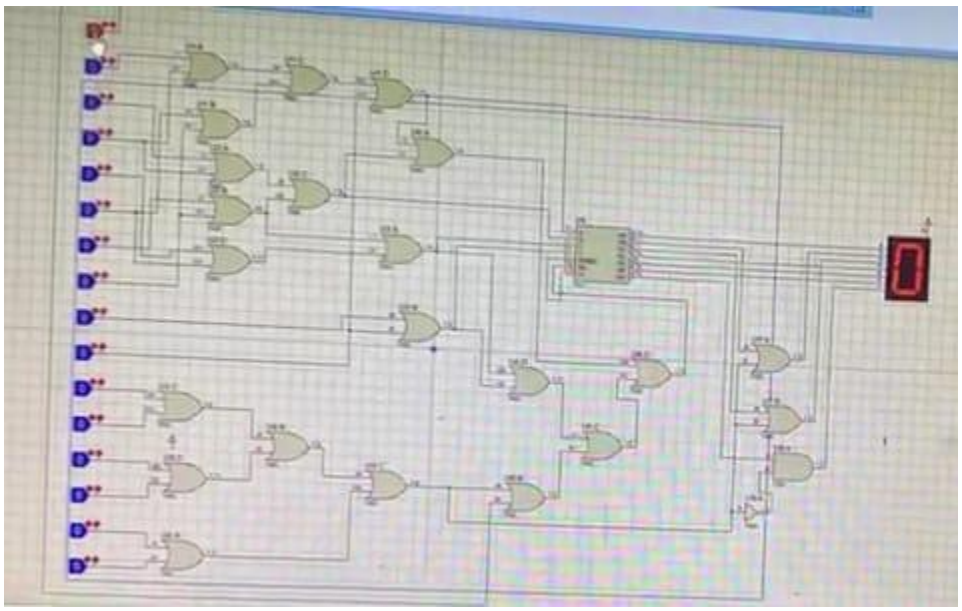
Hardware used

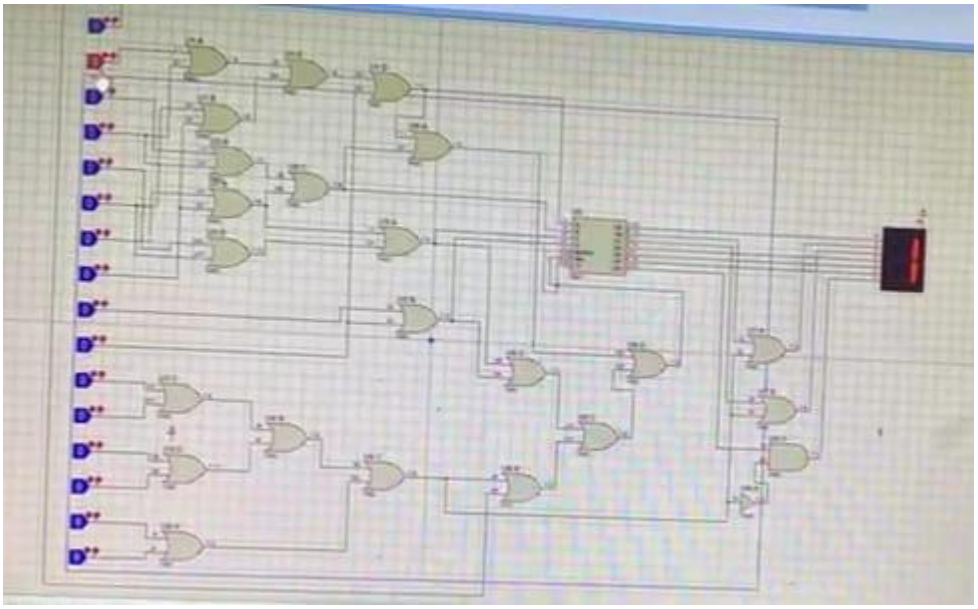
push button (16)
resistor (23)
7447 decoder
7 segment display
7432 (2-input or) (9)

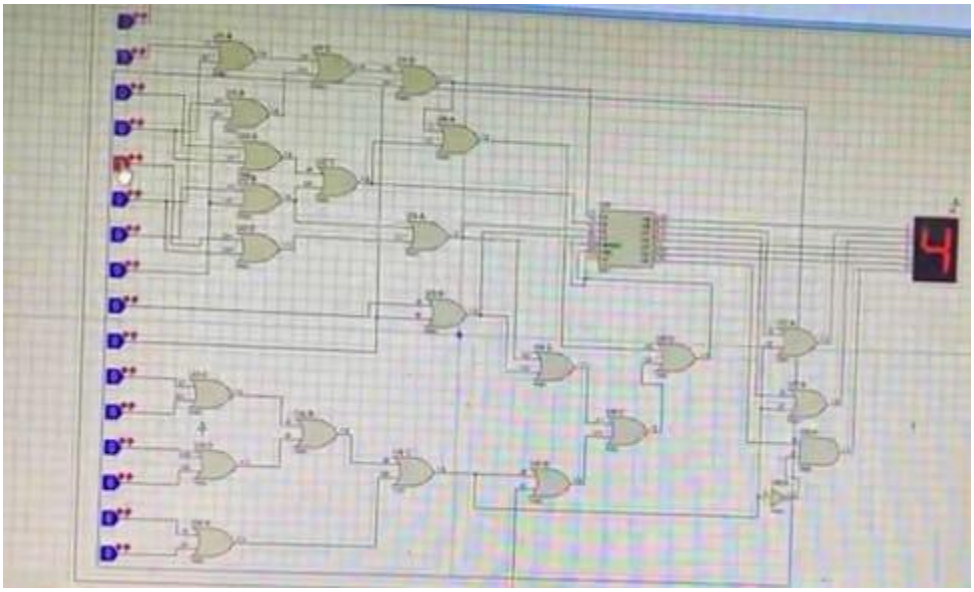
P1	P2	P3	P4	P5	P6	P7	P8	P9
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	1

For getting output E on 7 segment :

1	**0**	**0**	**0**	**0**	**0**
0	1	0	0	0	0
0	0	1	0	0	0
0	0	0	1	0	0
0	0	0	0	1	0
0	0	0	0	0	1



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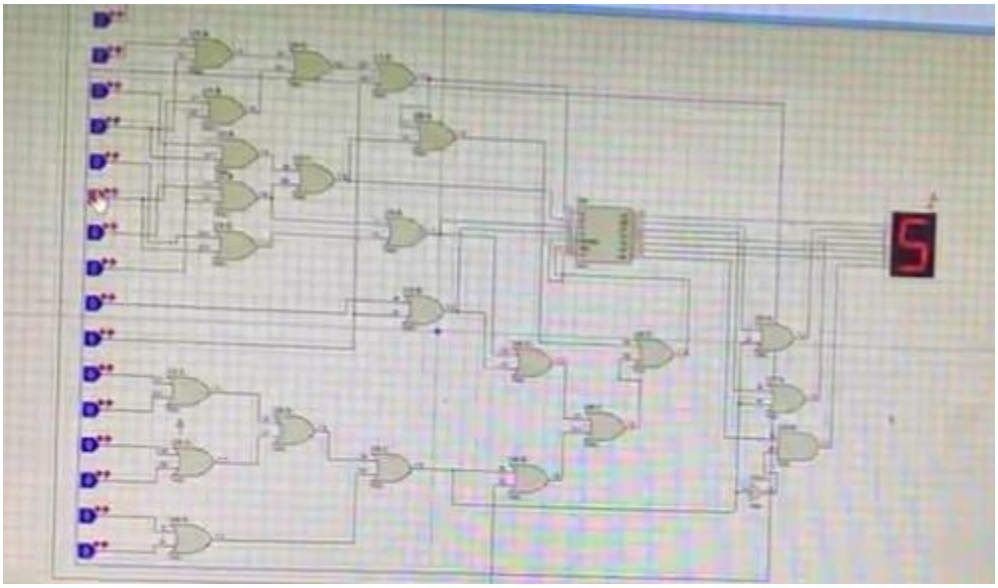
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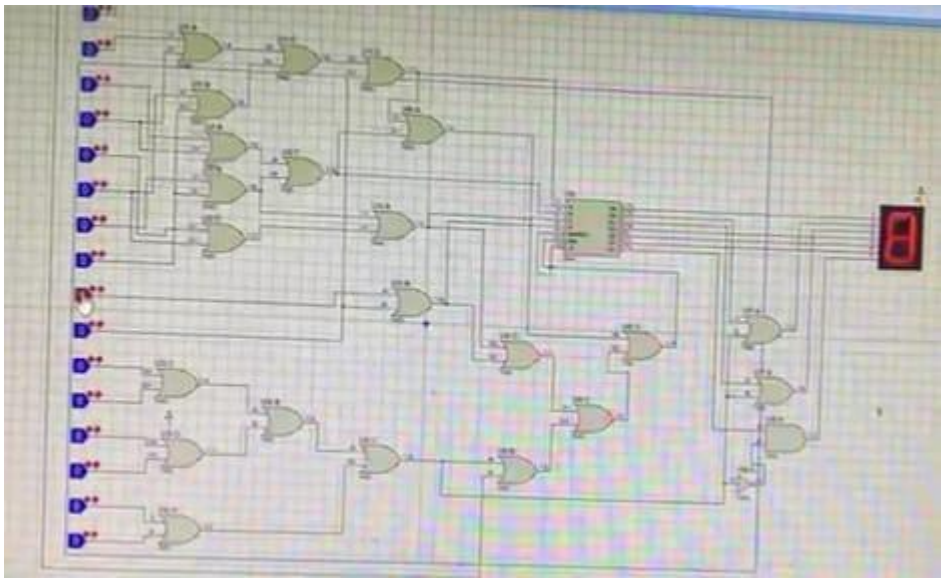
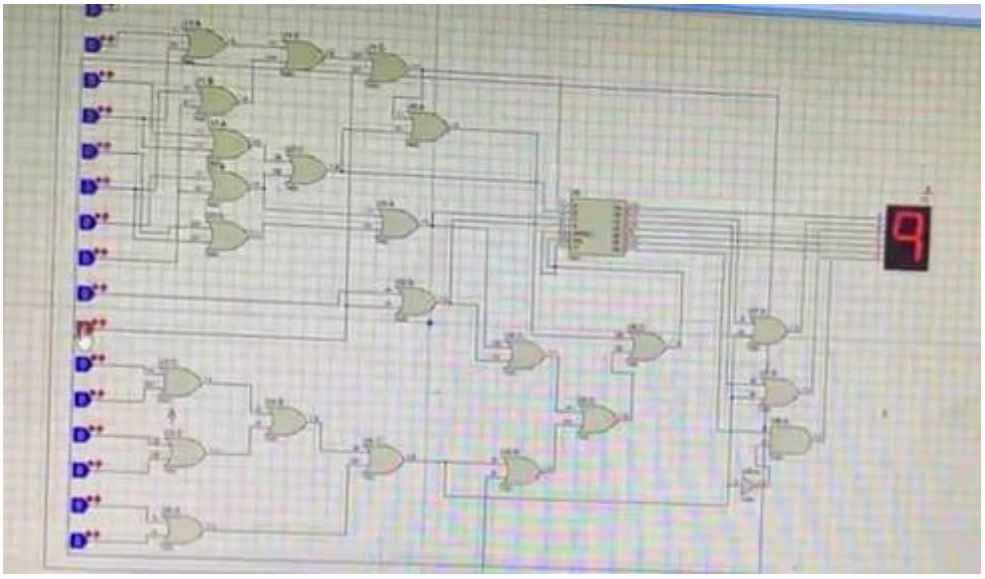
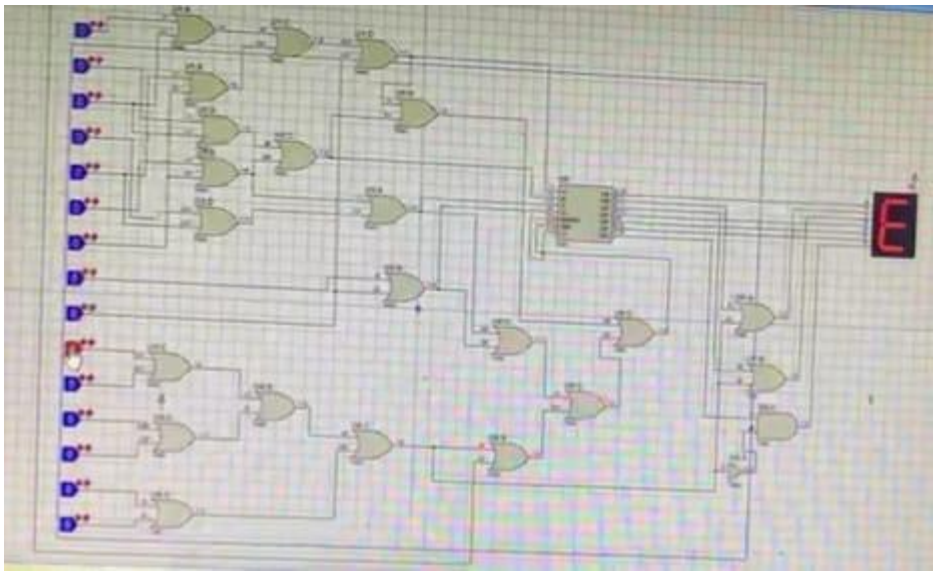
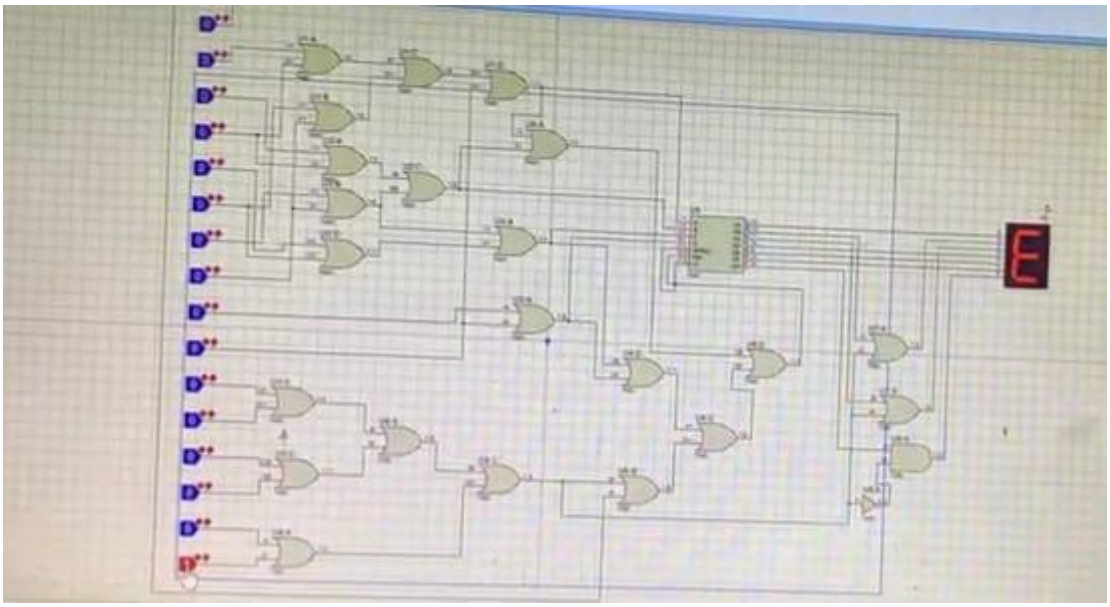








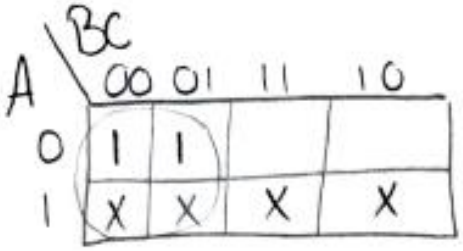
Phase 2:

Refer to Fig. 2; Design a sequential circuit with X-type flip-flops and logic gates to count the sequence: 1, 6, A1, A2, A3, A4, A5, back to 1, and repeat ; then display it on 7-segment. Where A1, A2, A3, A4, and A5 are defined, for example, as follows:

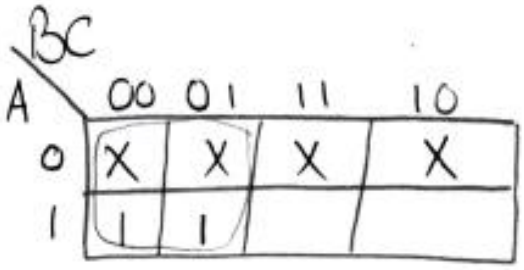
Hardware used

555 clock
Capacitor 10nF
Capacitor 10uF
Resistor 68k ohms
Resistor 8.2 k ohm
AND gate 7408
XOR gate 7486
OR gate 7432
2 jk flip flops 7476
Anodic 7 segment display
7447 decoder

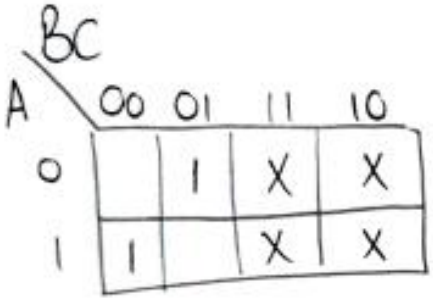
JK flip / flop Truth Table											
Present State			**Next State**			**Flip Flop Inputs**					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	1	0	0	1	x	0	x	0	x
0	0	1	1	1	0	1	x	1	x	x	1
0	1	0	0	0	1	0	x	x	1	1	x
0	1	1	0	0	1	0	x	x	1	x	0
1	0	0	0	1	1	x	1	1	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	1	0	1	x	0	x	1	x	0



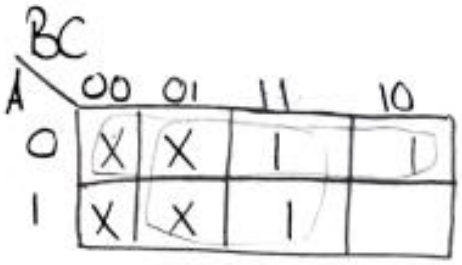
$J_A = B'$



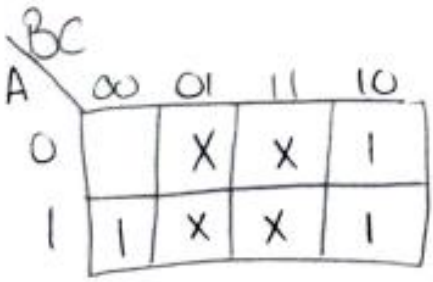
$K_A = B'$



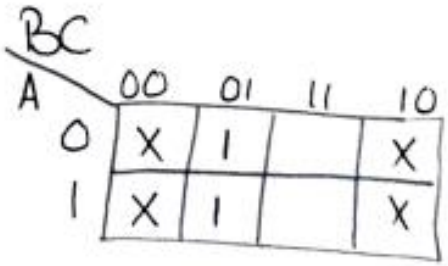
$J_B = A \oplus C$



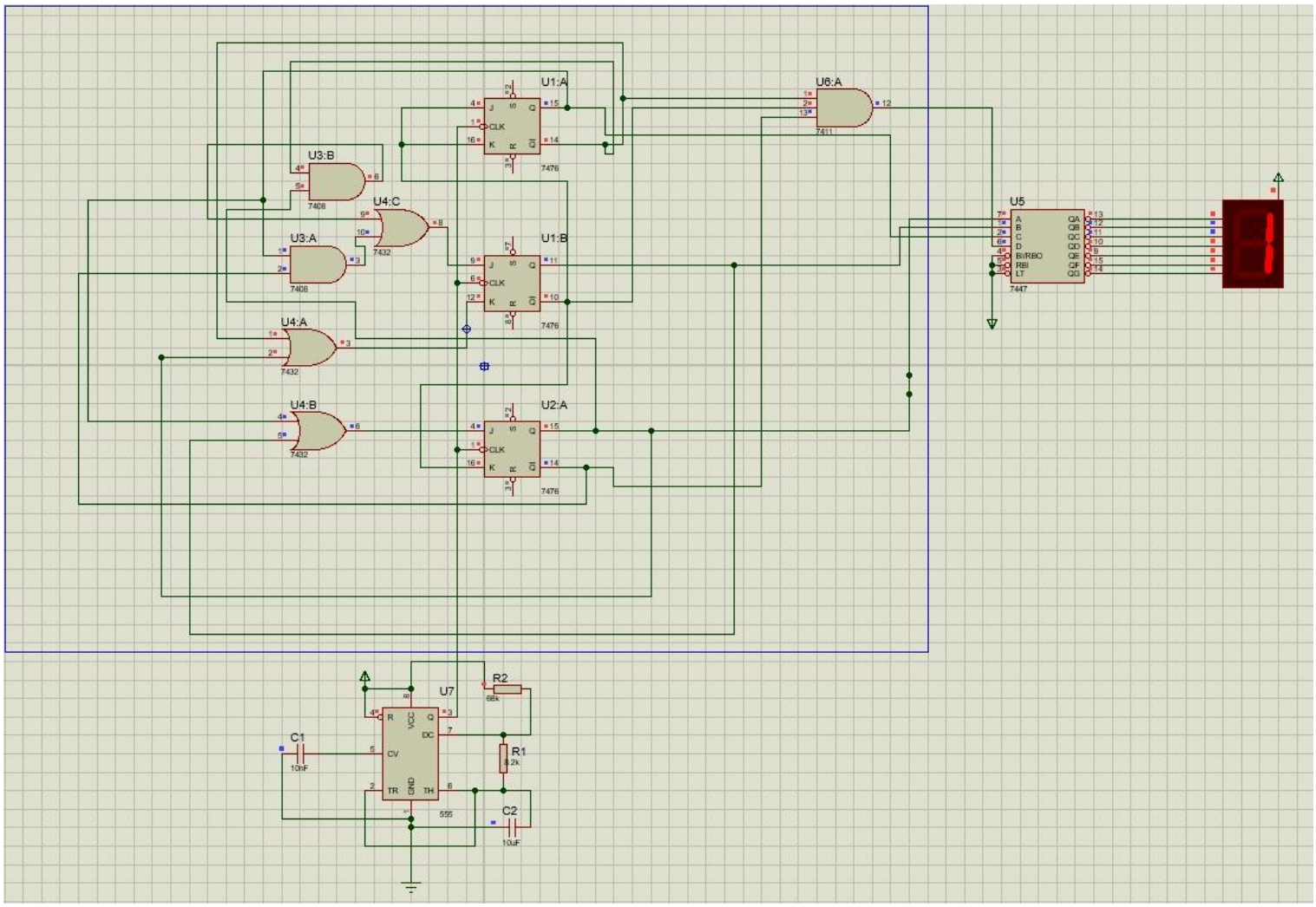
$K_B = C + A'$

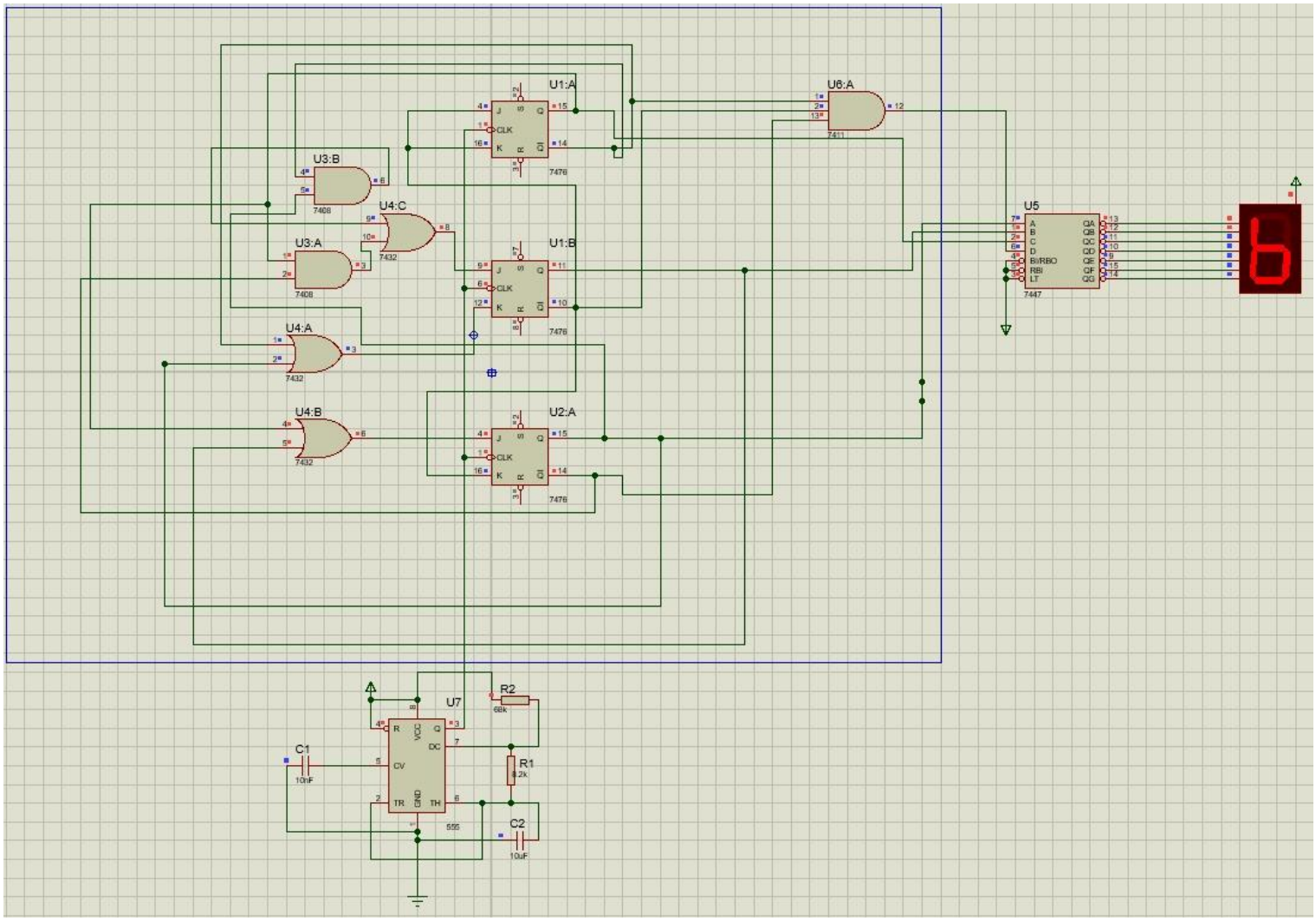


$J_C = B + A$



$K_C = B'$


U1:A
U1:B
U2:A
U3:A
U3:B
U4:A
U4:B
U4:C
U6:A
U5
U7
R1
R2
C1
C2
7476
7408
7432
7411
7447
555
10nF
10uF
68k
8.2k


U1:A
U1:B
U2:A
U3:B
U3:A
U4:C
U4:A
U4:B
U6:A
U5
U7
R2
68k
R1
6.2k
C1
10nF
C2
10uF
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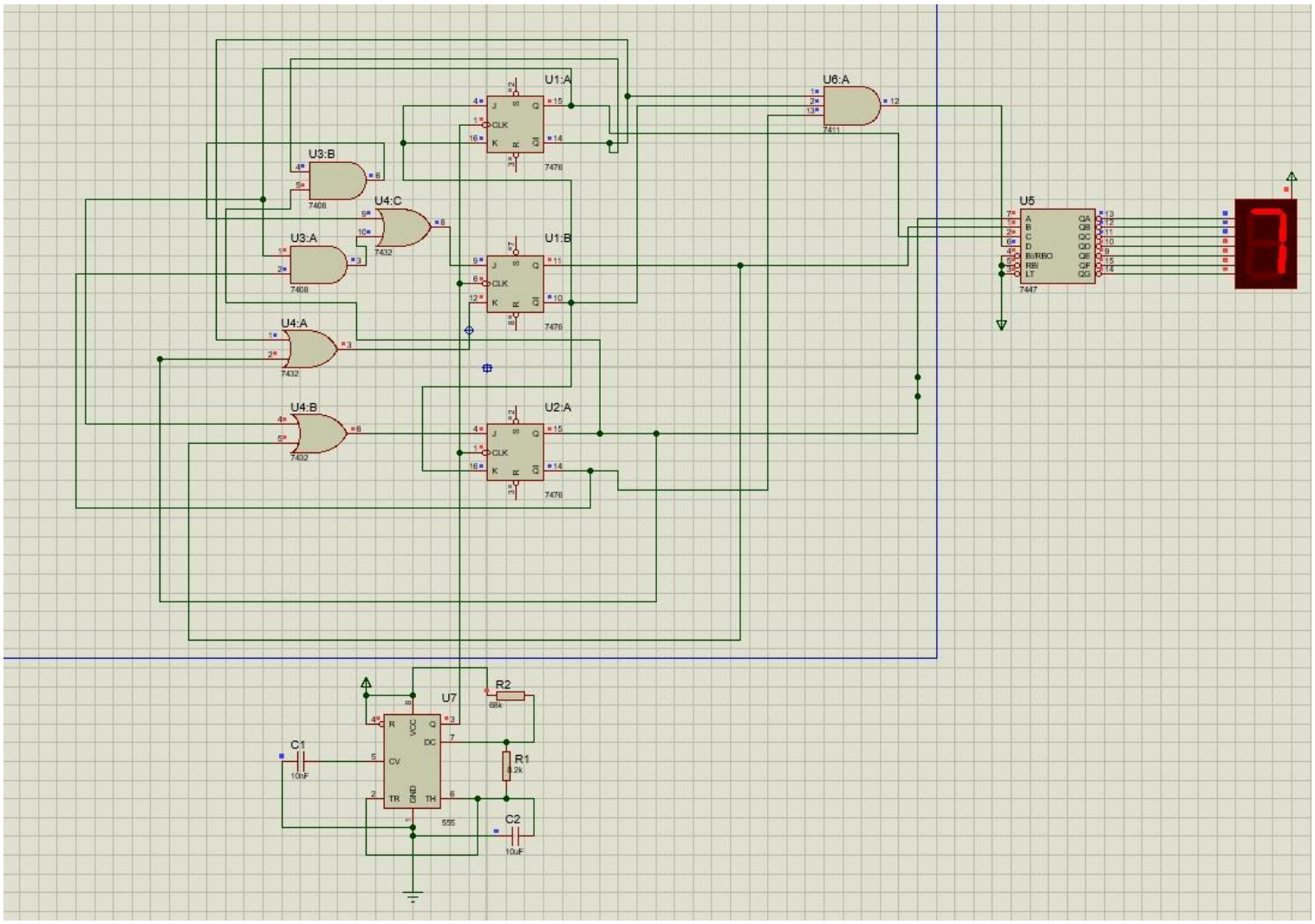
U1:A
U6:A
U3:B
U4:C
U3:A
U1:B
U5
U4:A
U4:B
U2:A
U7
R2
C1
R1
C2
7408
7432
7476
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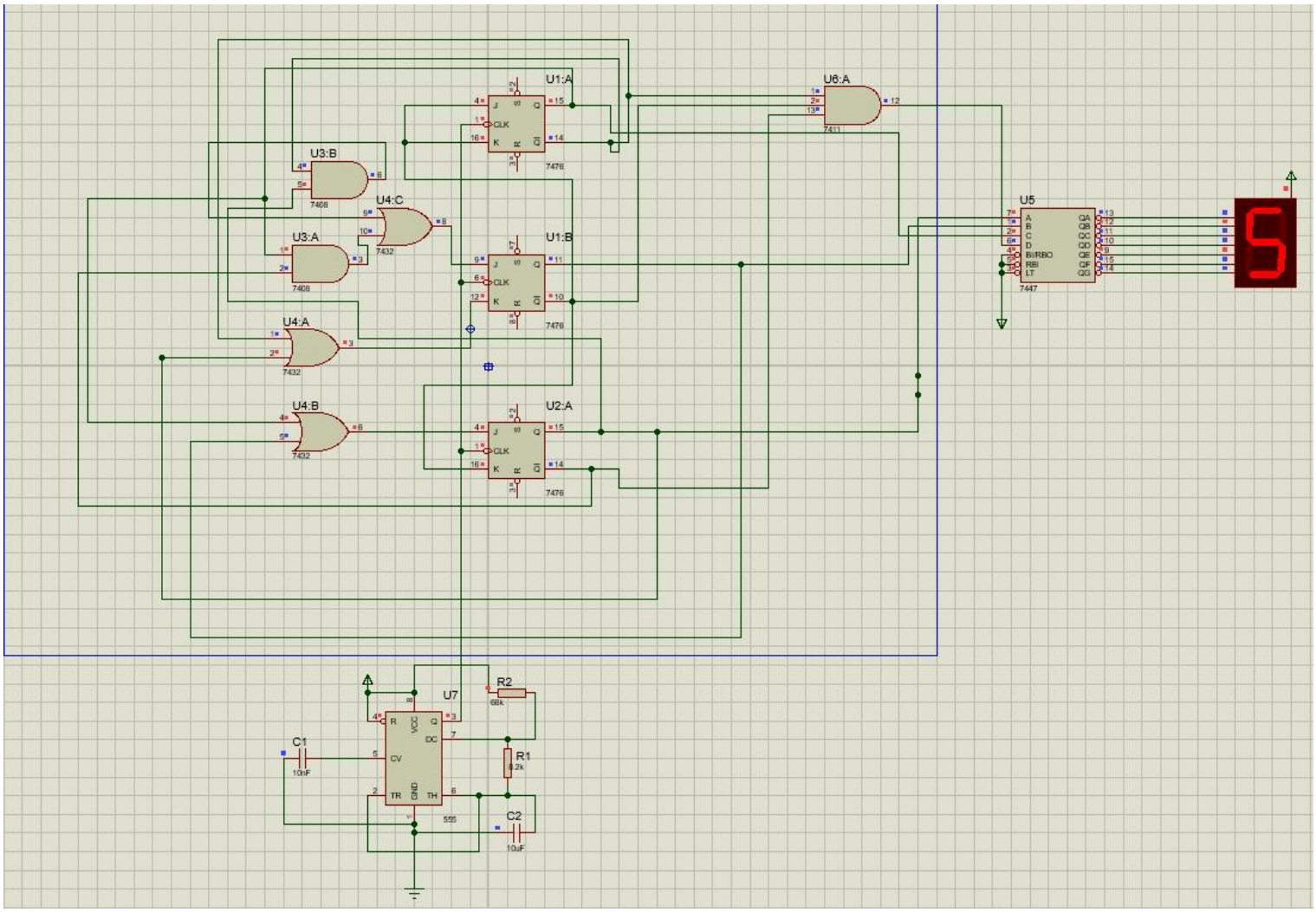
7447
555
68k
10nF
6.2k
10uF


U1:A
U1:B
U2:A
U3:A
U3:B
U4:A
U4:B
U4:C
U6:A
U5
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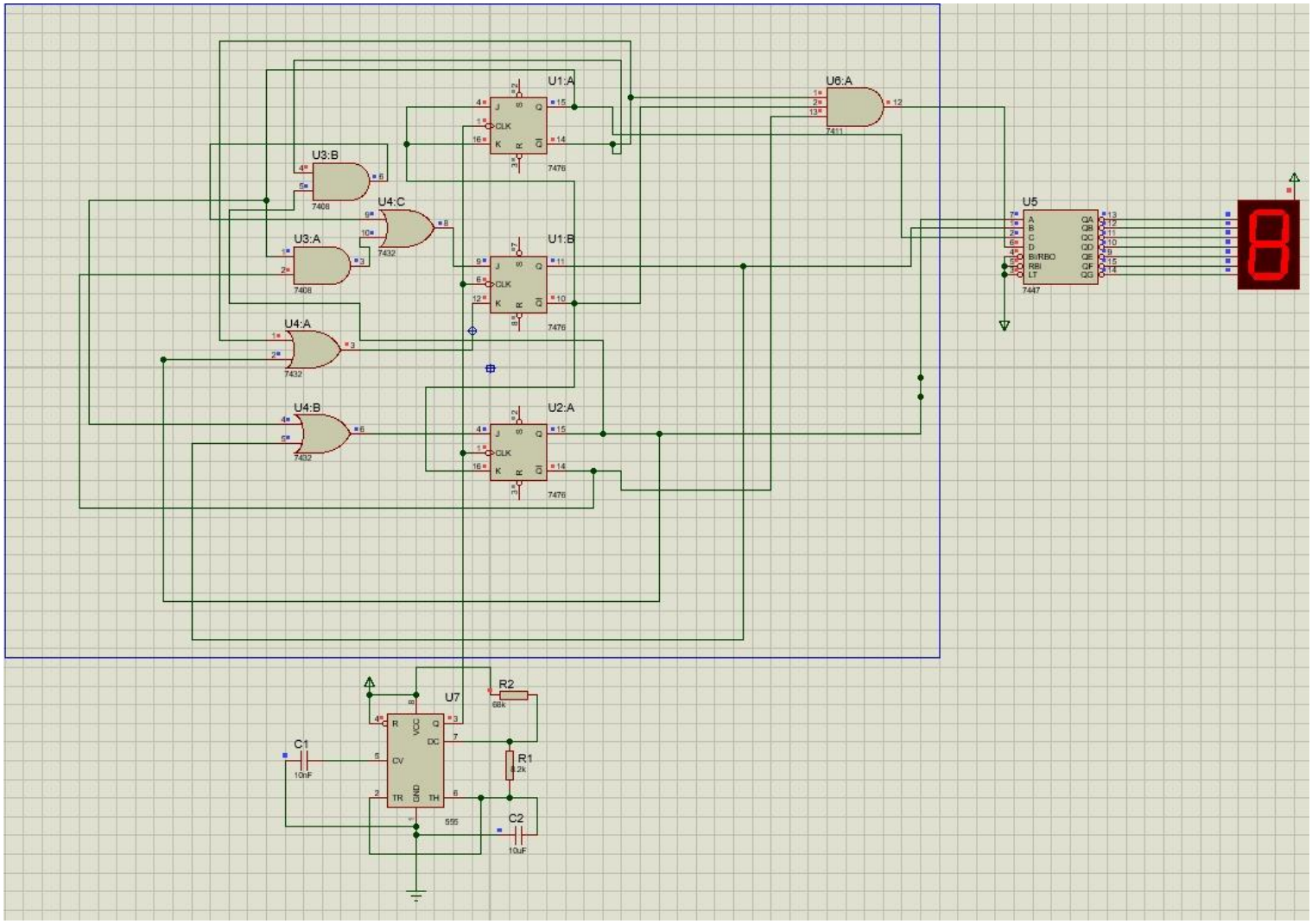
10nF
10uF
68k
4.2k


U1:A
U1:B
U2:A
U3:A
U3:B
U4:A
U4:B
U4:C
U5
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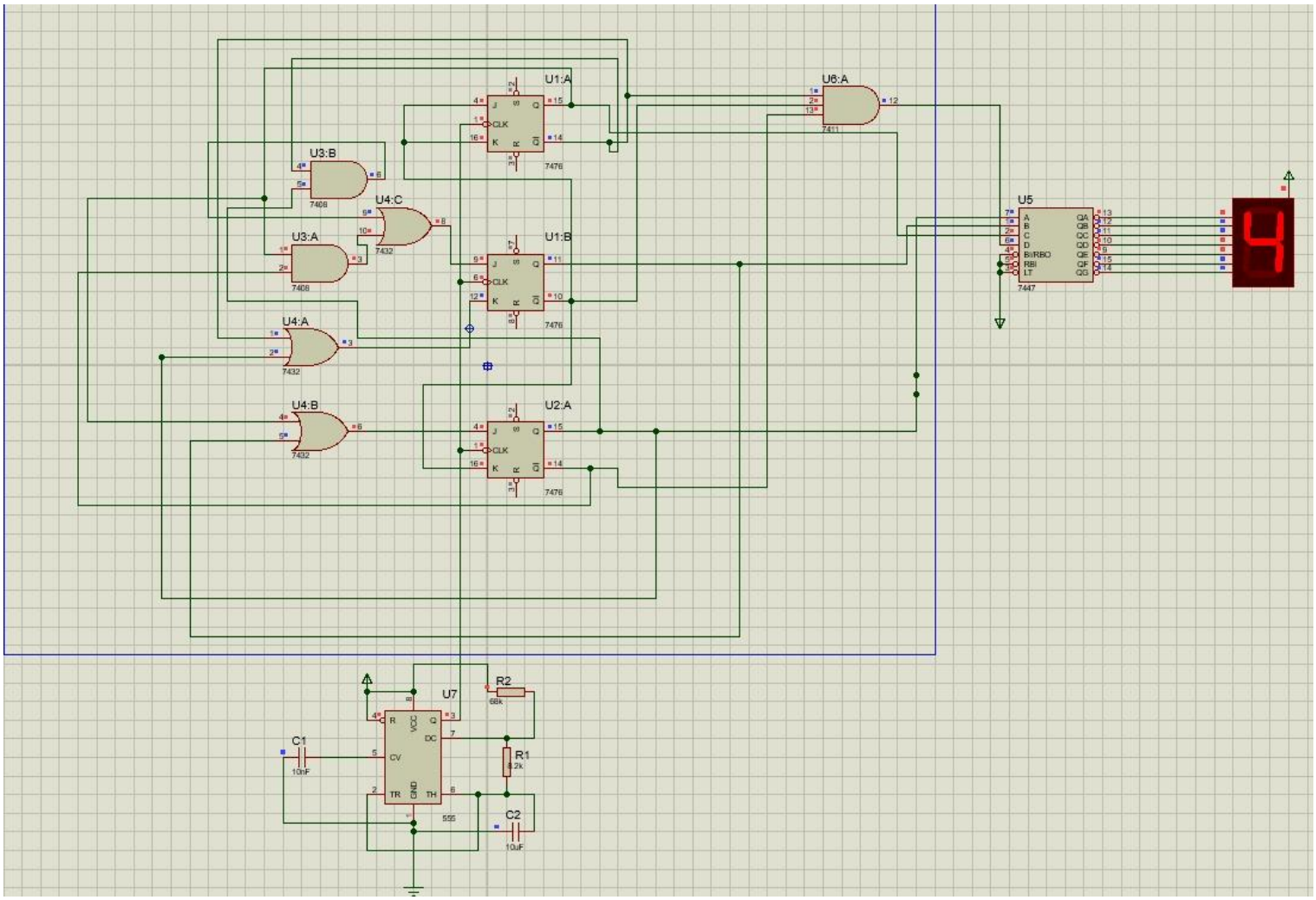
U1:A
U1:B
U2:A
U3:B
U3:A
U4:C
U4:A
U4:B
U6:A
U5
U7
R2
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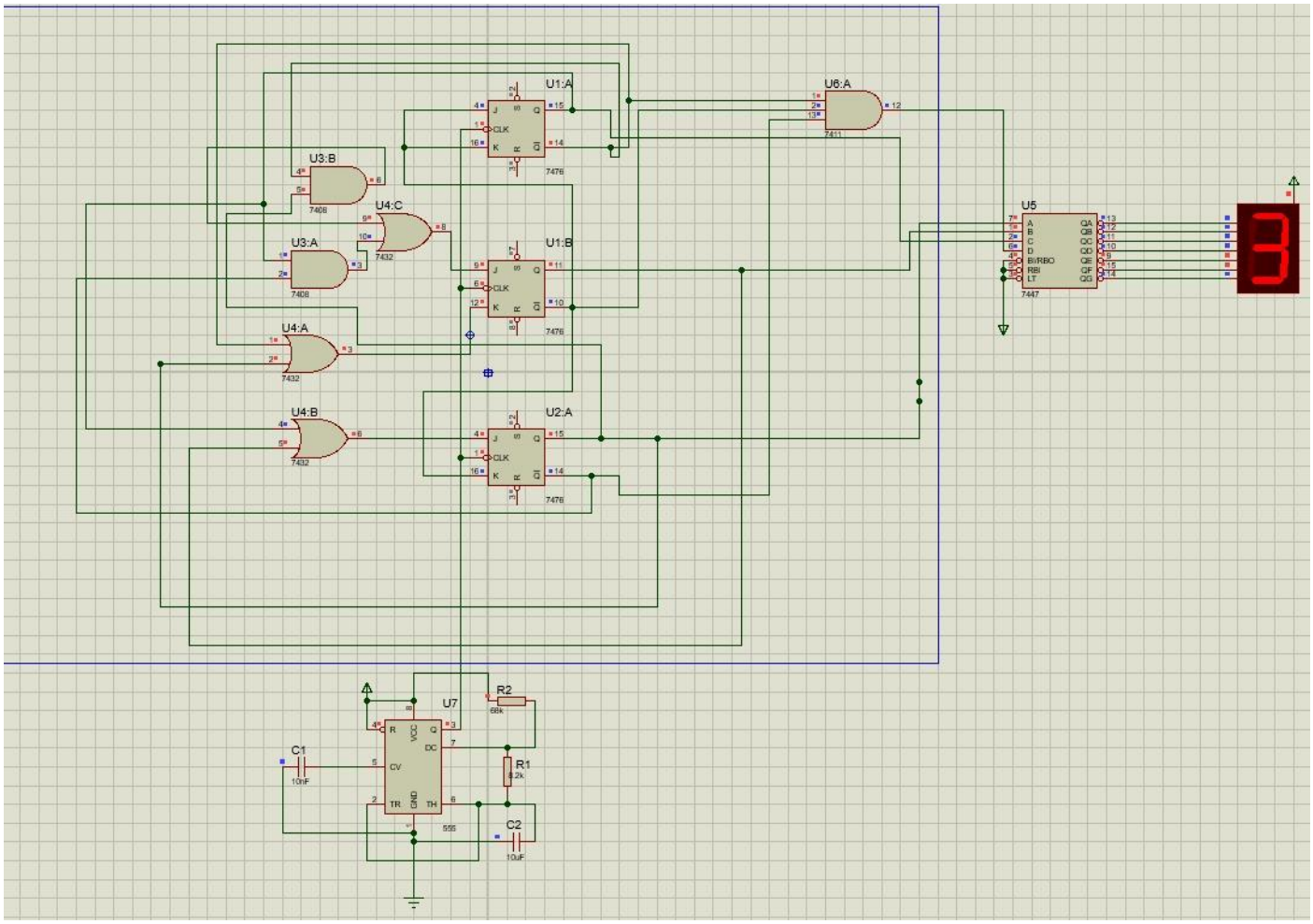
10uF


U1:A
U6:A
U3:B
U4:C
U3:A
U1:B
U4:A
U4:B
U2:A
U5
U7
R2
C1
R1
C2
7476
7411
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68k
10nF
8.2k
10uF