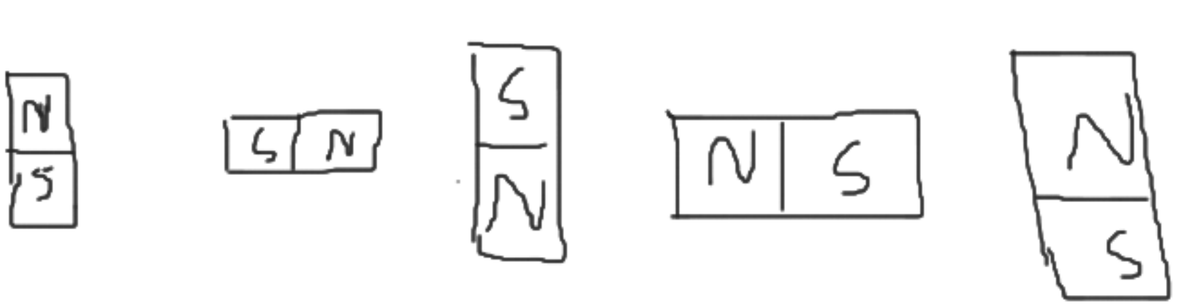
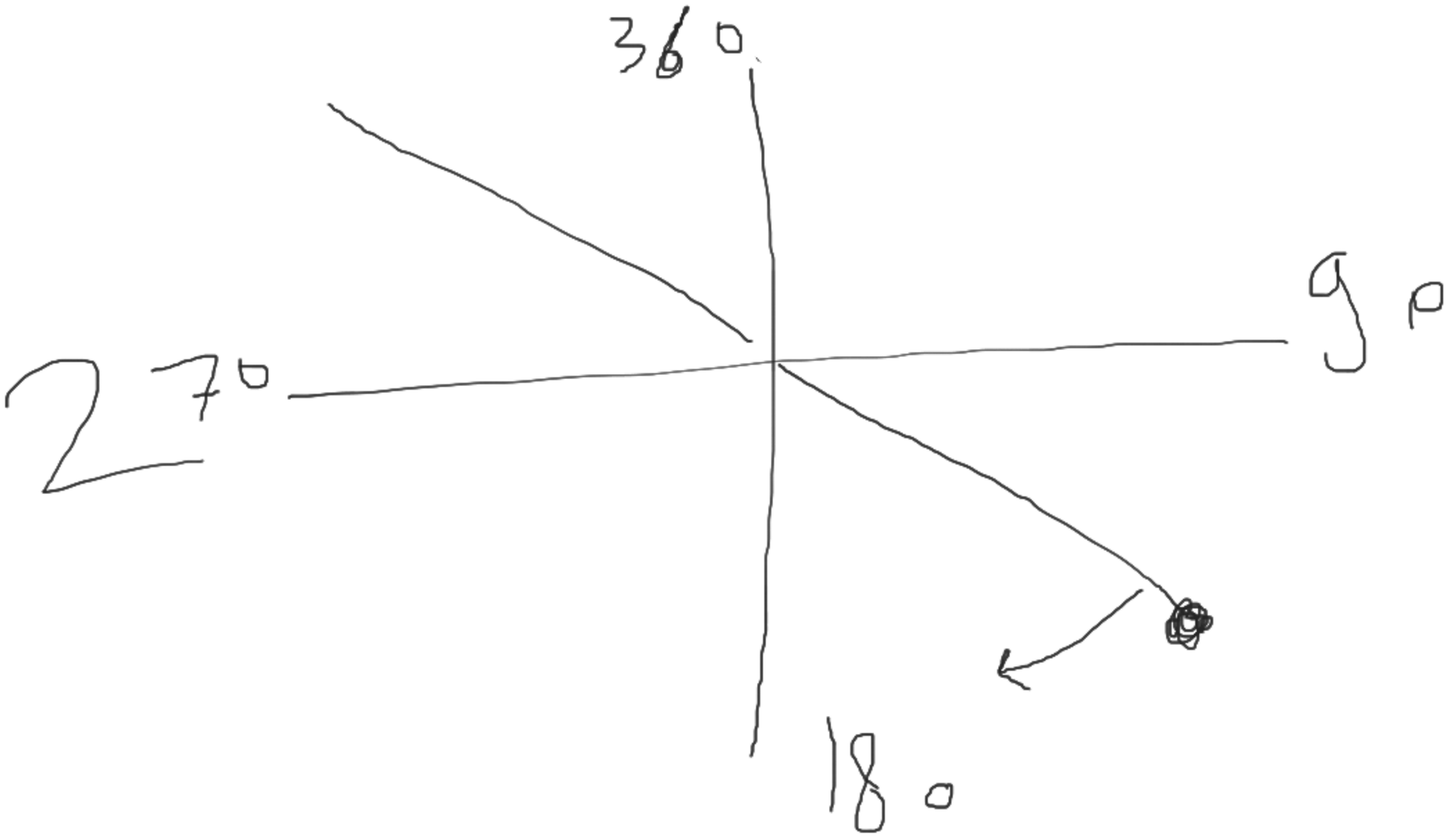
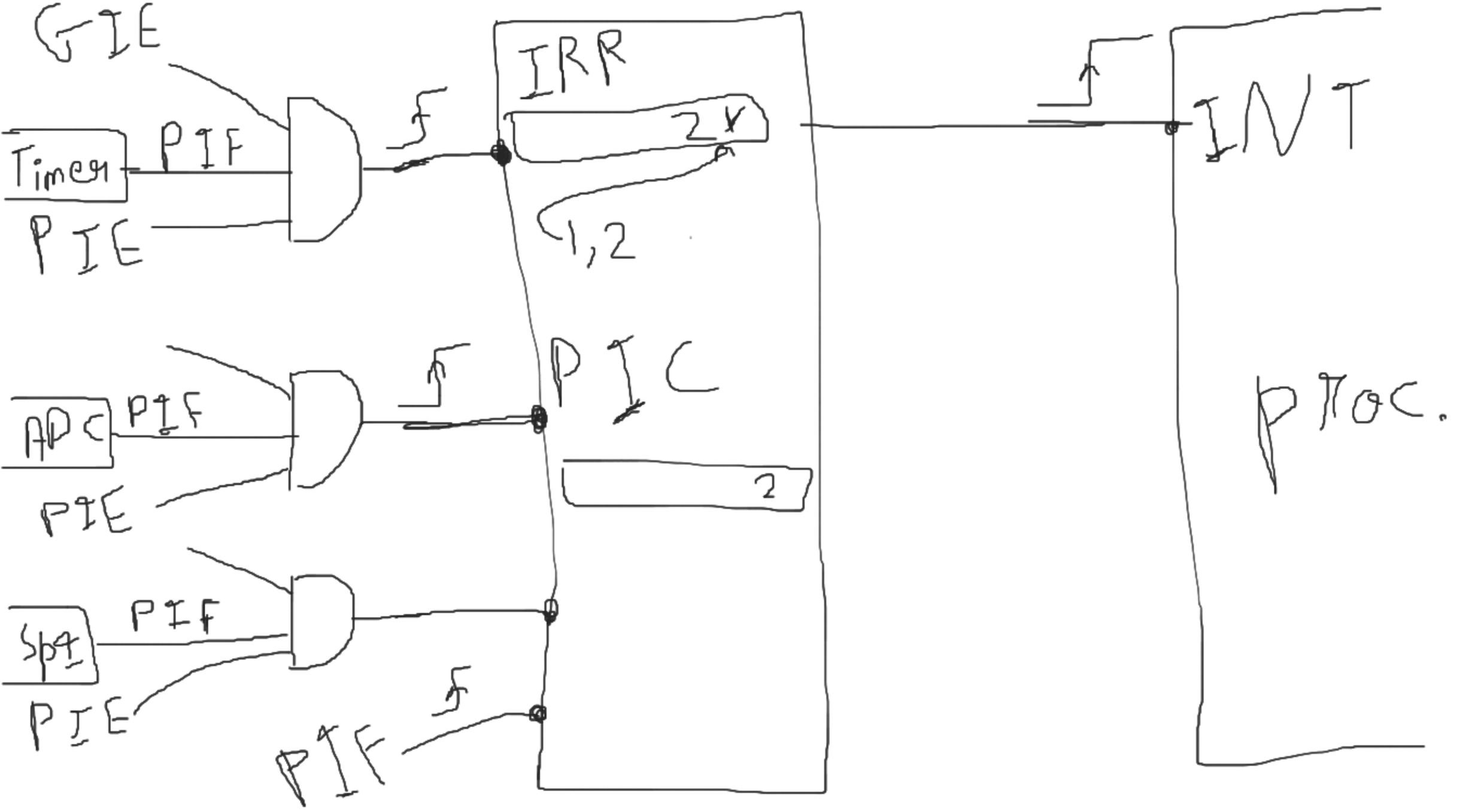
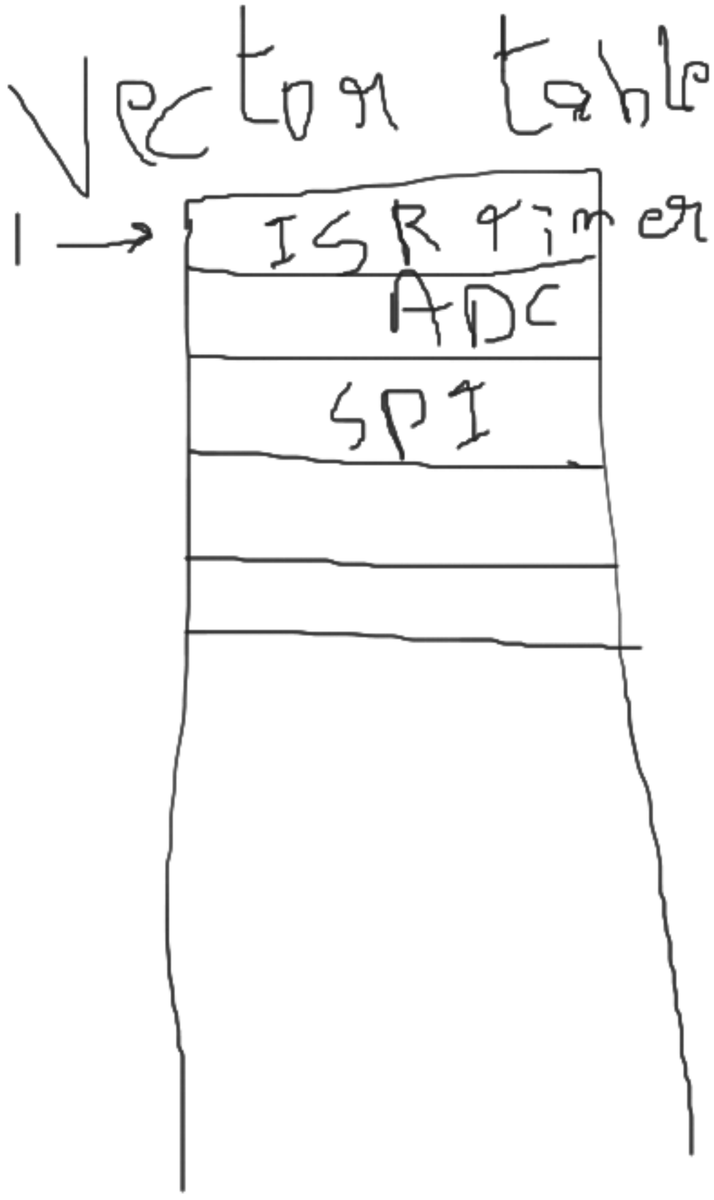


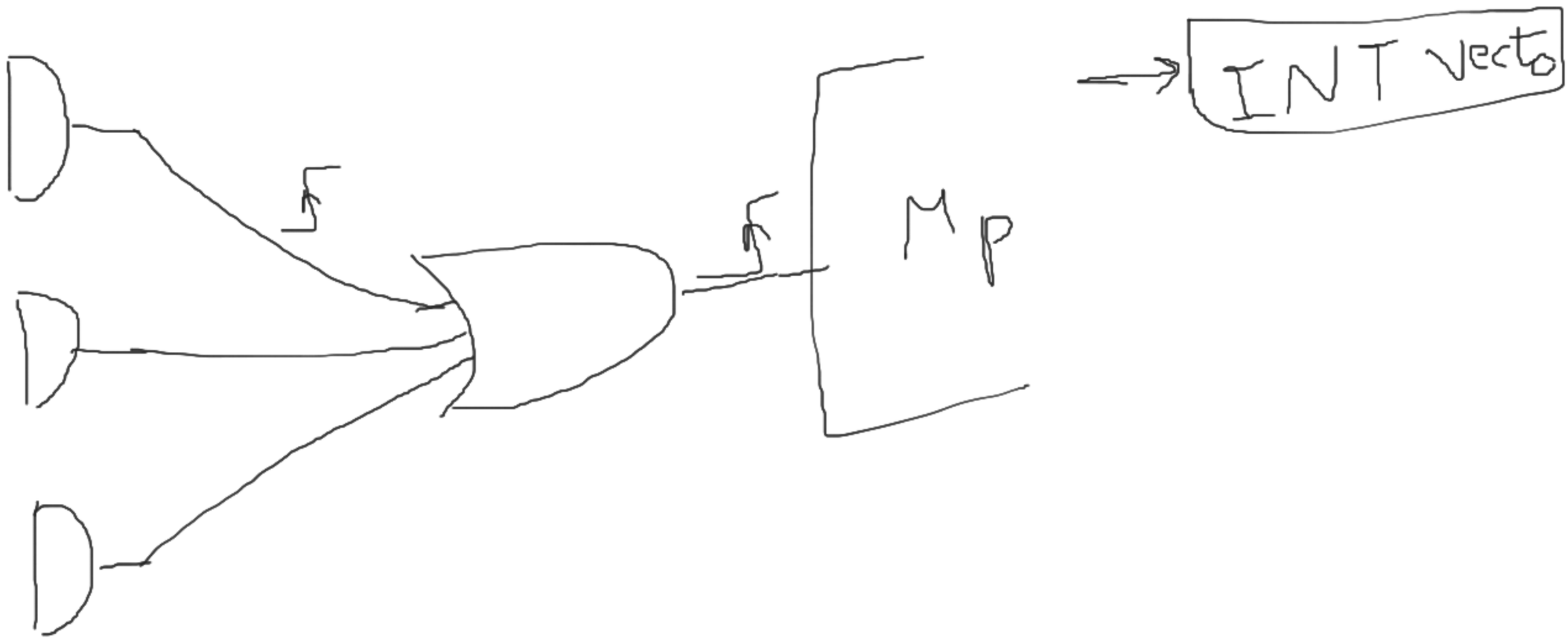
Full step

half step

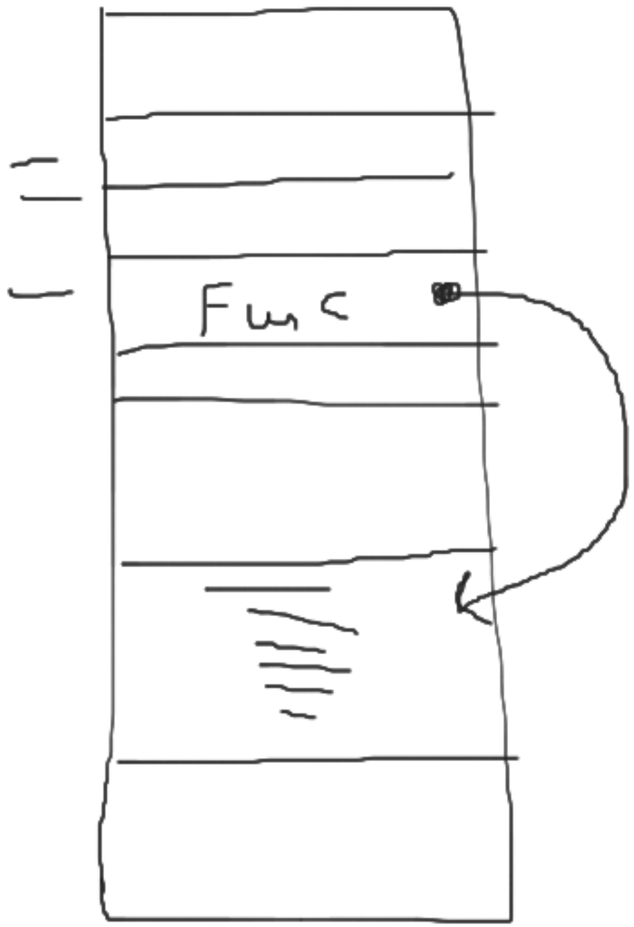

360
90
270
180

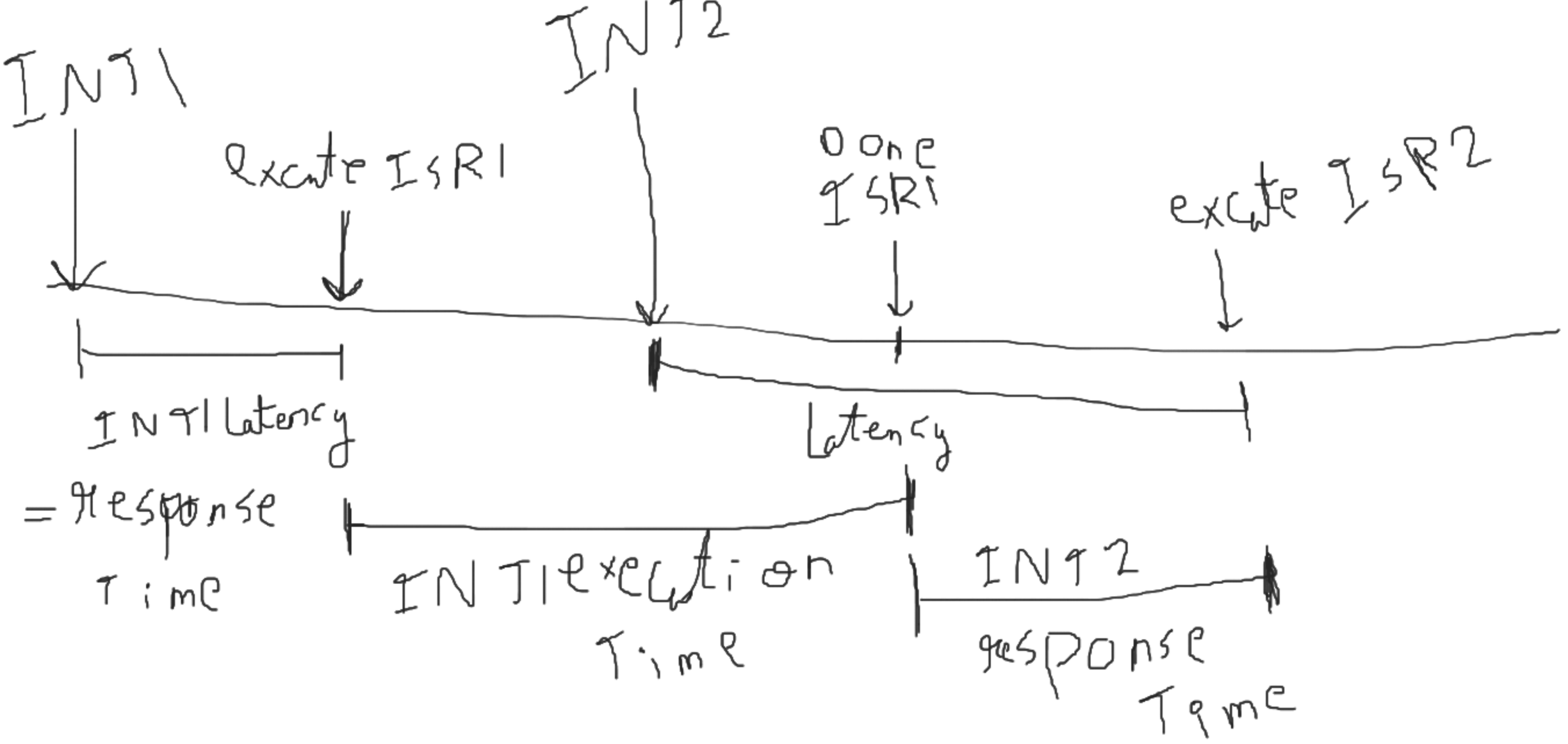

GIE
Timer
PIF
PIE
IRR
2
1,2
INT
Proc.
ADC
PIF
PIE
PIC
2
Spi
PIF
PIE
PIF

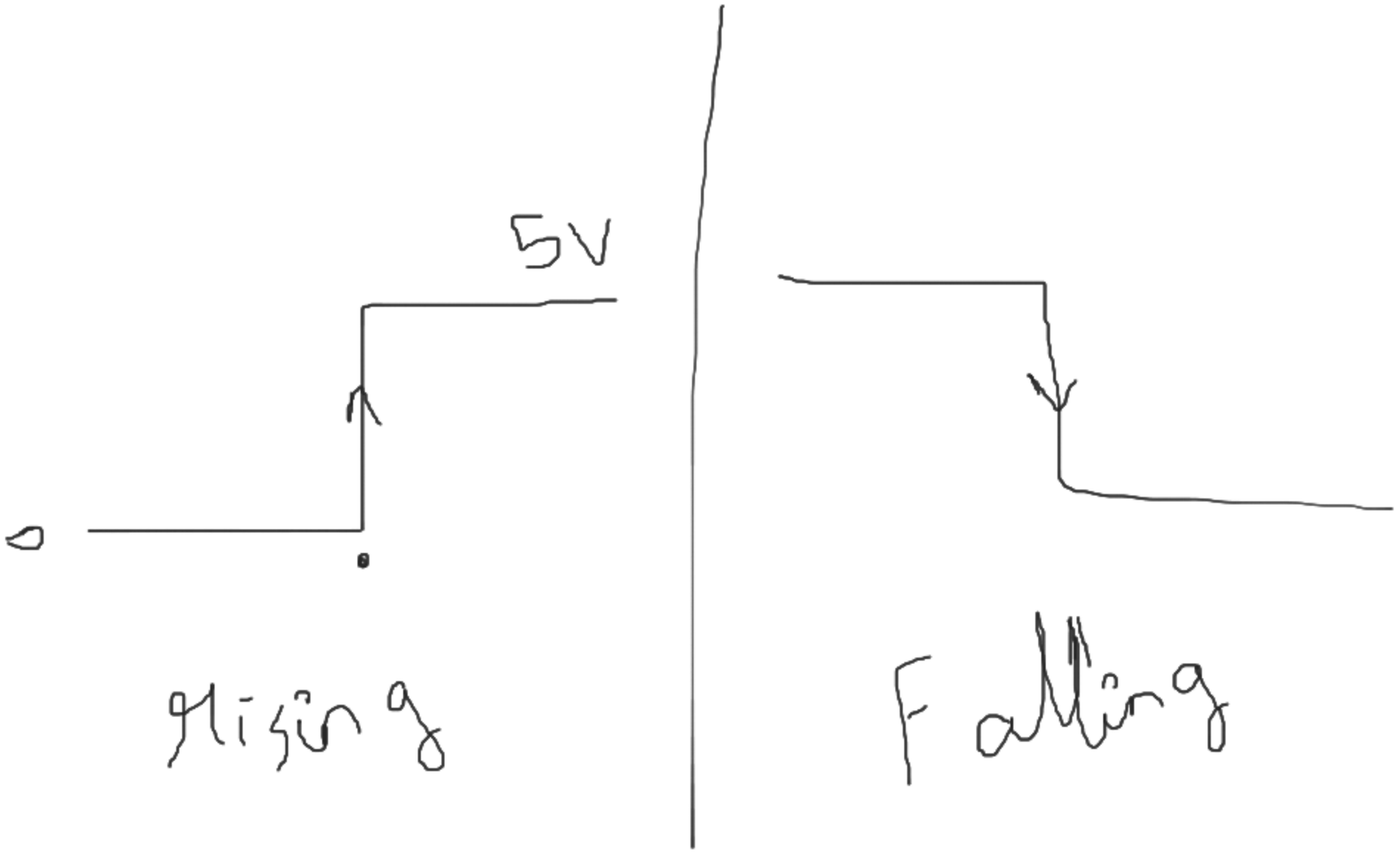

Vector table
1
ISR prior
ADC
SPI

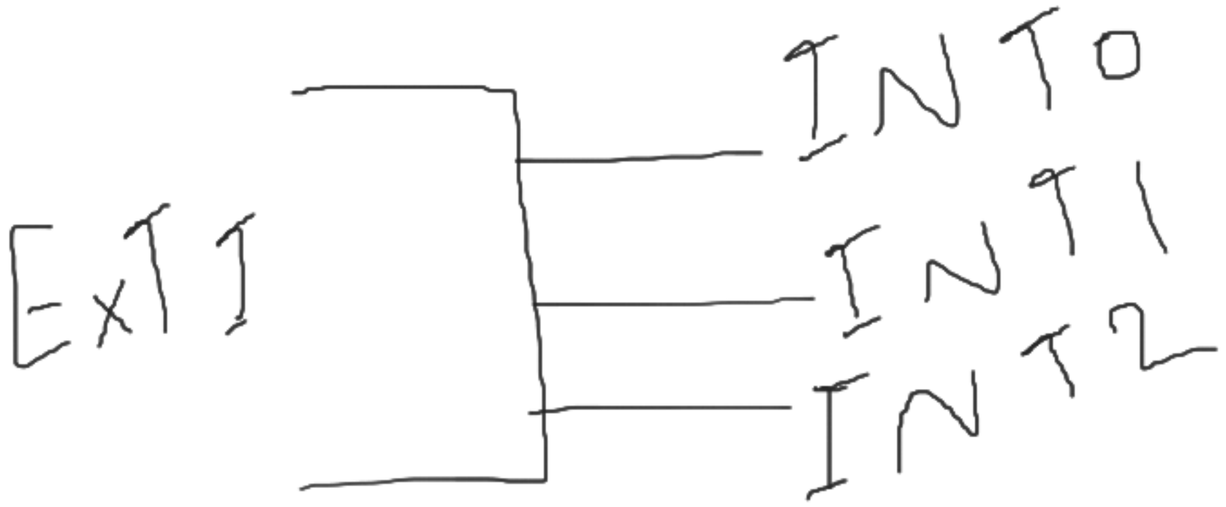

INT Vecto
Mp

Function	ISR
Callable	Not
i/p	no. i/p
return	No return
SW Context switching	HW Context


Func


INT1
Excute ISR1
INT2
Done ISR1
excute ISR2
INT1 Latency
= Response Time
Latency
INT1 execution Time
INT2 response Time


5V
0
Rising
Falling


EXTI
INT0
INT1
INT2