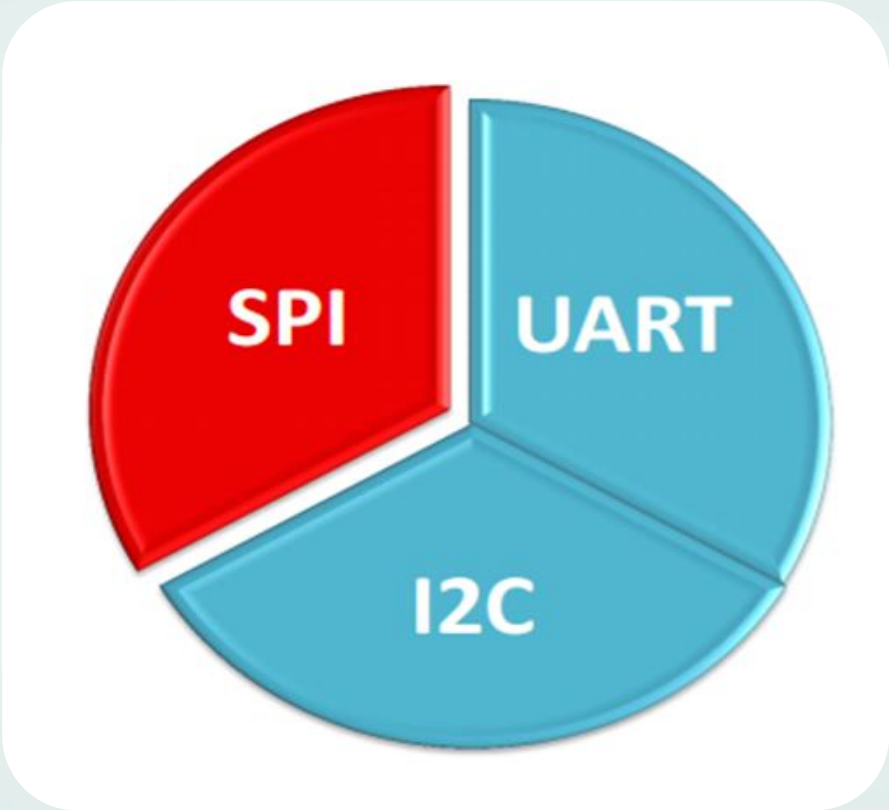
Embedded System Interfacing

Lecture 14
SPI

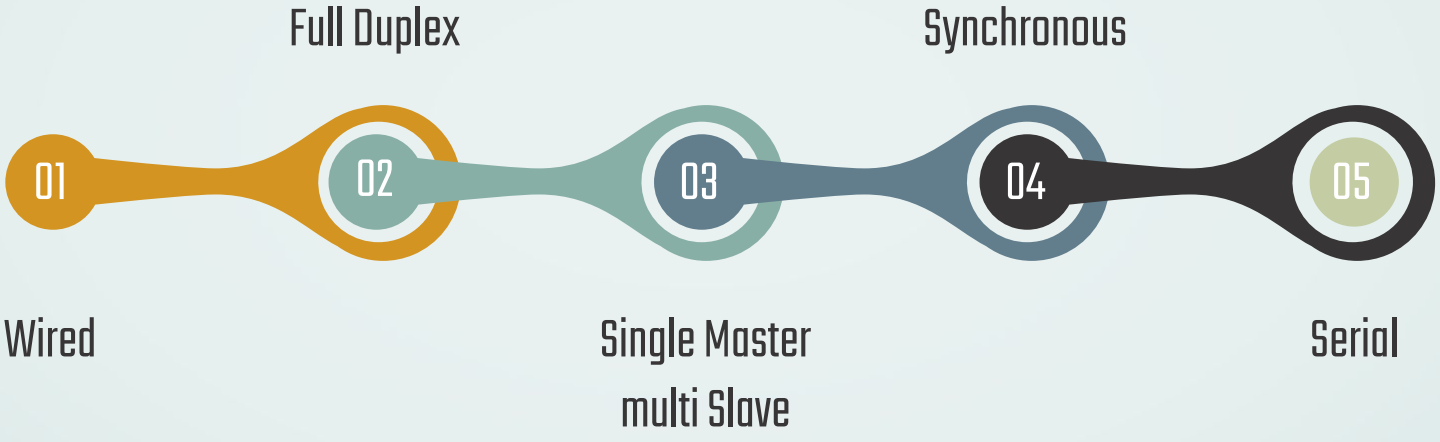
IMT SCHOOL

SPI

SPI



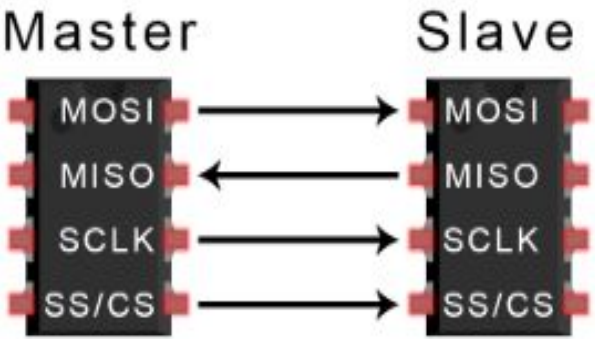
SPI Features



What is SPI ?

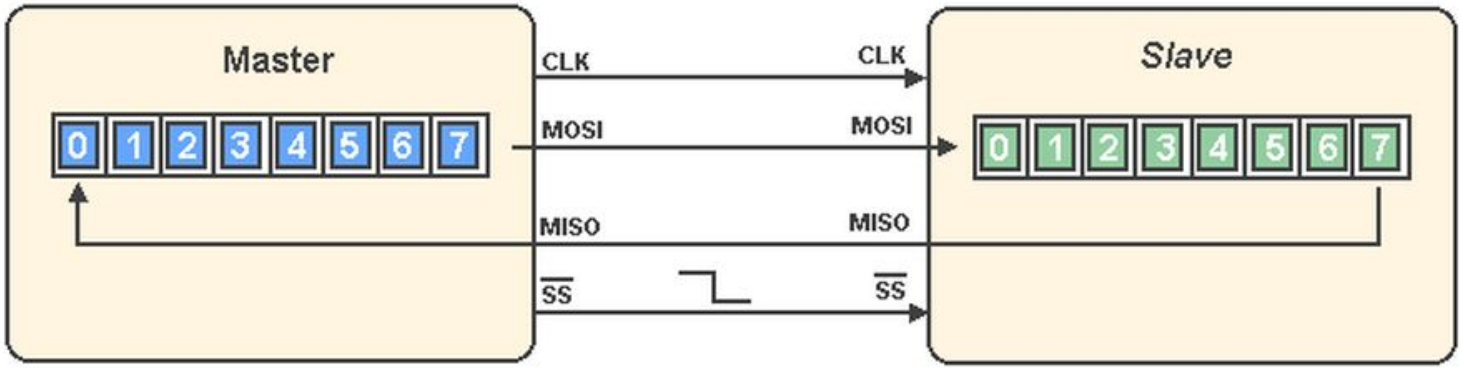
- Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication.
- The SPI bus can operate with a single master device and with one or more slave devices.

- SCLK : Serial Clock (output from master).
- MOSI : Master Output, Slave Input (output from master).
- MISO : Master Input, Slave Output (output from slave).
- SS : Slave Select (active low, output from master).



How it works ?

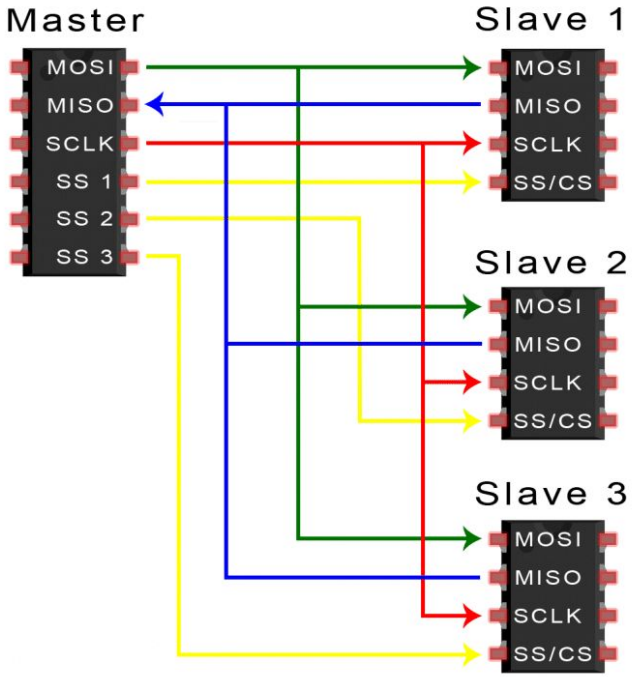
The SPI operation is a shift register operation. The master swaps a bit with the slave every
clock cycle.



SPI Network

Type 1: Independent Slaves

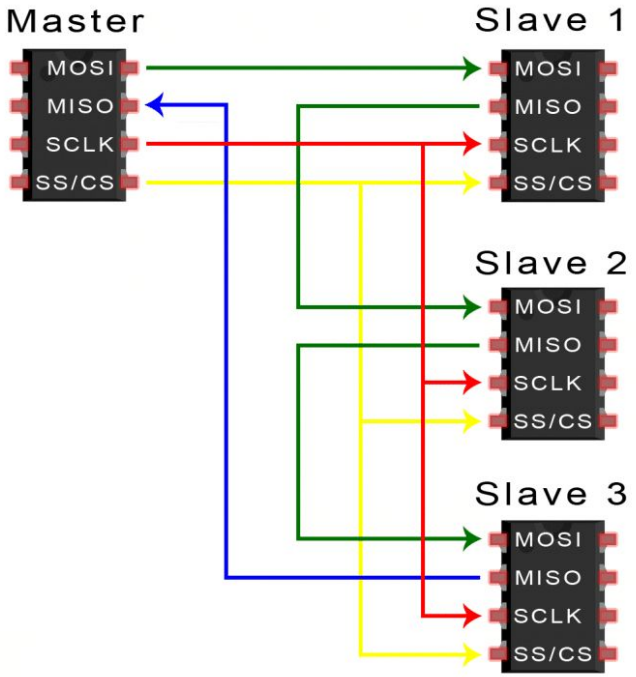
SPI can be set up to operate with a single master and a single slave, and it can be set up with multiple slaves controlled by a single master. There are two ways to connect multiple slaves to the master. If the master has multiple slave select pins, the slaves can be wired in parallel like this:



SPI Network

Type 1: Daisy Chain

If only one slave select pin is available, the slaves can be daisy-chained like this:



SPI Clock

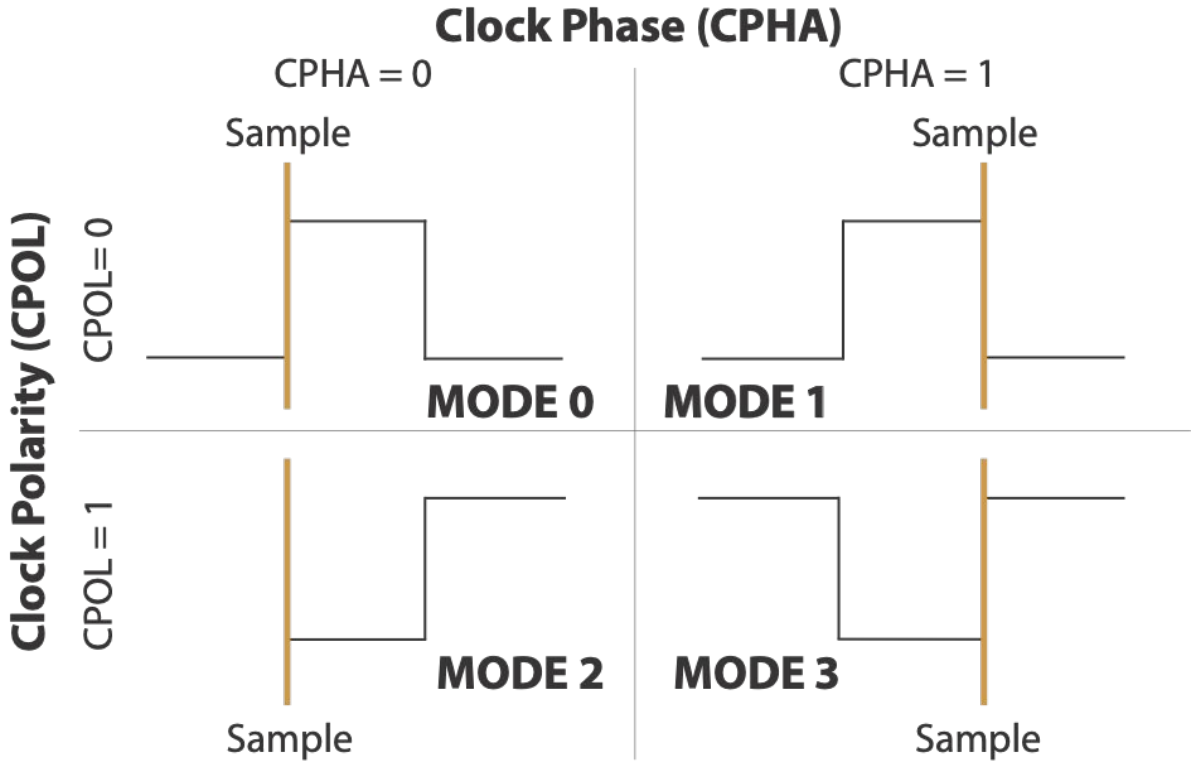
The clock signal synchronizes the output of data bits from the master to the sampling of bits by the slave. One bit of data is transferred in each clock cycle, so the speed of data transfer is determined by the frequency of the clock signal. SPI communication is always initiated by the master since the master configures and generates the clock signal.

SPI Clock Parameters:

Clock Polarity: Defines the idle state of the clock

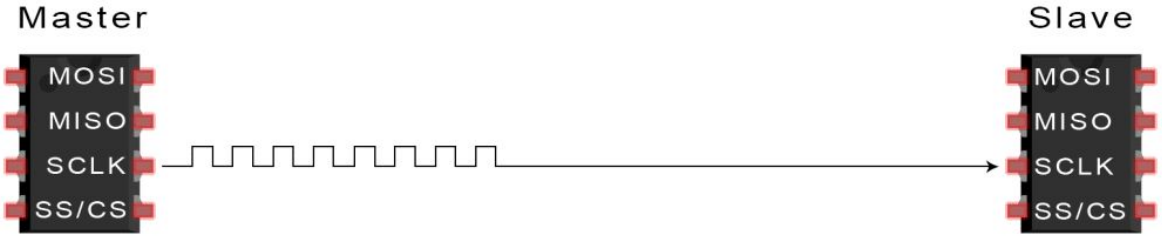
Clock Phase : Define the leading action to be taken. Because the clock has 2 edges; rising and falling edge, it is configurable to choose what to be done with the first edge (Called also Leading Edge). The master can choose to send data (Called also Toggle or Setup) with the leading edge. Or to choose to read data with leading edge (called also Sample).

SPI Clock

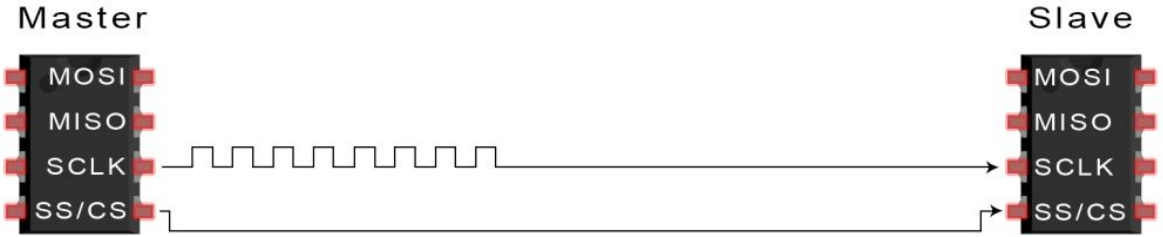

Clock Phase (CPHA)
CPHA = 0
CPHA = 1
Sample
Sample
Clock Polarity (CPOL)
CPOL= 0
CPOL = 1
MODE 0
MODE 1
MODE 2
MODE 3
Sample
Sample

Data Transmission Steps

1. The master outputs the clock signal:

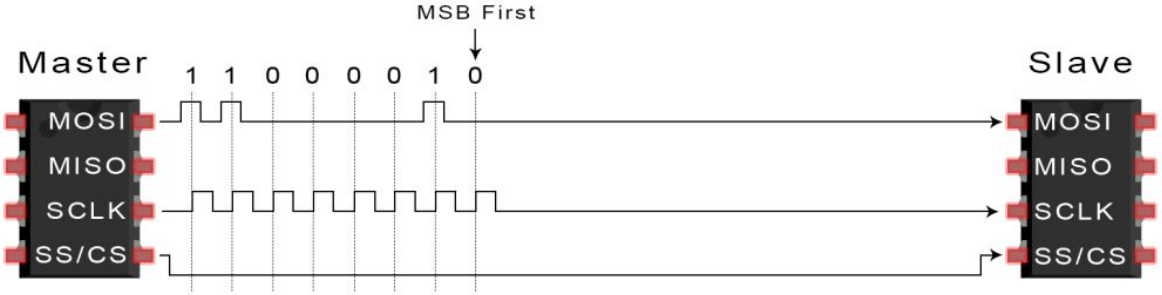


2. The master switches the SS/CS pin to a low voltage state, which activates the slave:

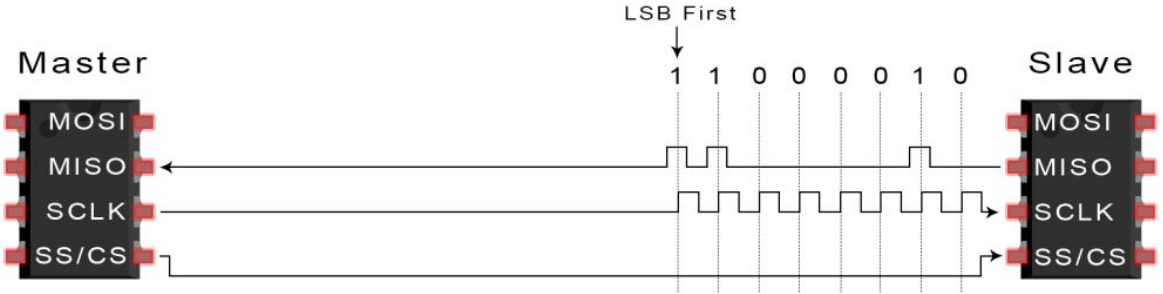


Data Transmission Steps

3. The master sends the data one bit at a time to the slave along the MOSI line. The slave reads the bits as they are received:



4. If a response is needed, the slave returns data one bit at a time to the master along the MISO line. The master reads the bits as they are received:



Advantages and Disadvantages of SPI

ADVANTAGES

- No start and stop bits, so the data can be streamed continuously without interruption
- No complicated slave addressing system like I2C
- Higher data transfer rate than I2C (almost twice as fast)
- Separate MISO and MOSI lines, so data can be sent and received at the same time

DISADVANTAGES

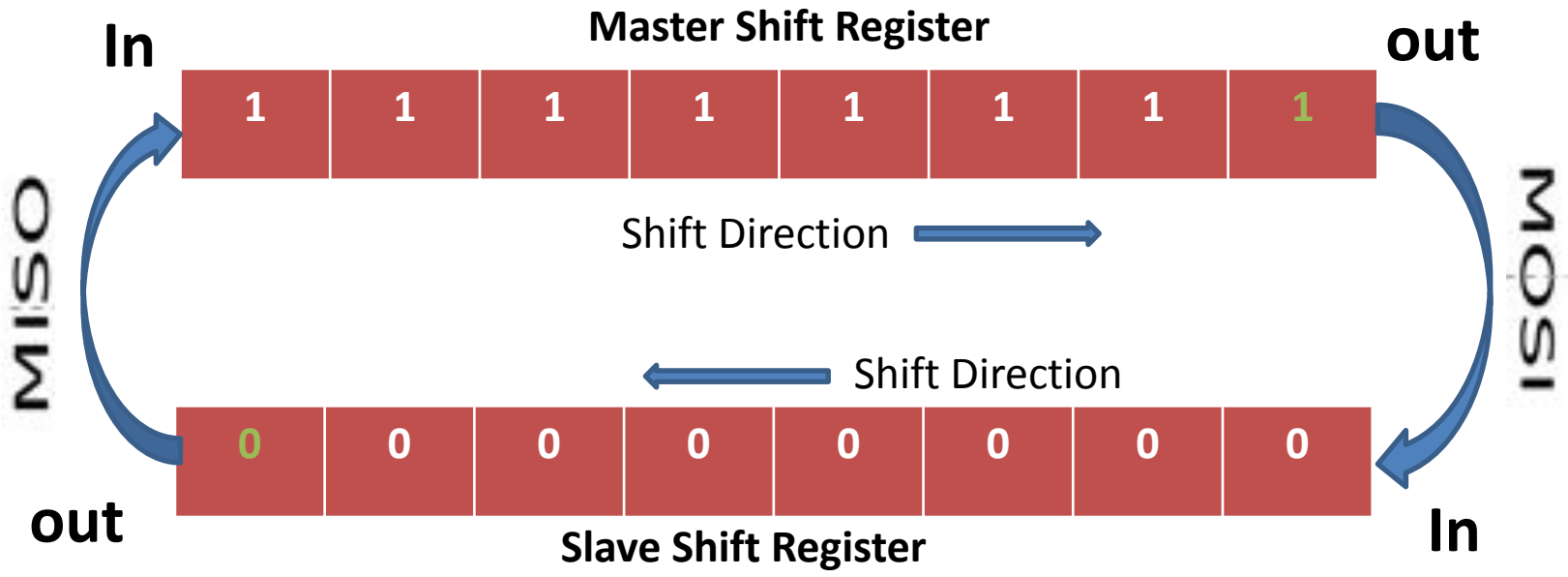
- Uses four wires (I2C and UARTs use two)
- No acknowledgement that the data has been successfully received (I2C has this)
- No form of error checking like the parity bit in UART
- Only allows for a single master

SPI Concept

THE INTERCONNECTION BETWEEN MASTER AND SLAVE

- The SPI Master initiates the communication cycle when pulling low the Slave Select SS pin of the desired Slave.
- Master and Slave prepare the data to be sent in their respective Shift Registers.

SPI Concept


In
Master Shift Register
out
1 1 1 1 1 1 1 1
MISO
Shift Direction
Shift Direction
MOSI
0 0 0 0 0 0 0 0
out
Slave Shift Register
In

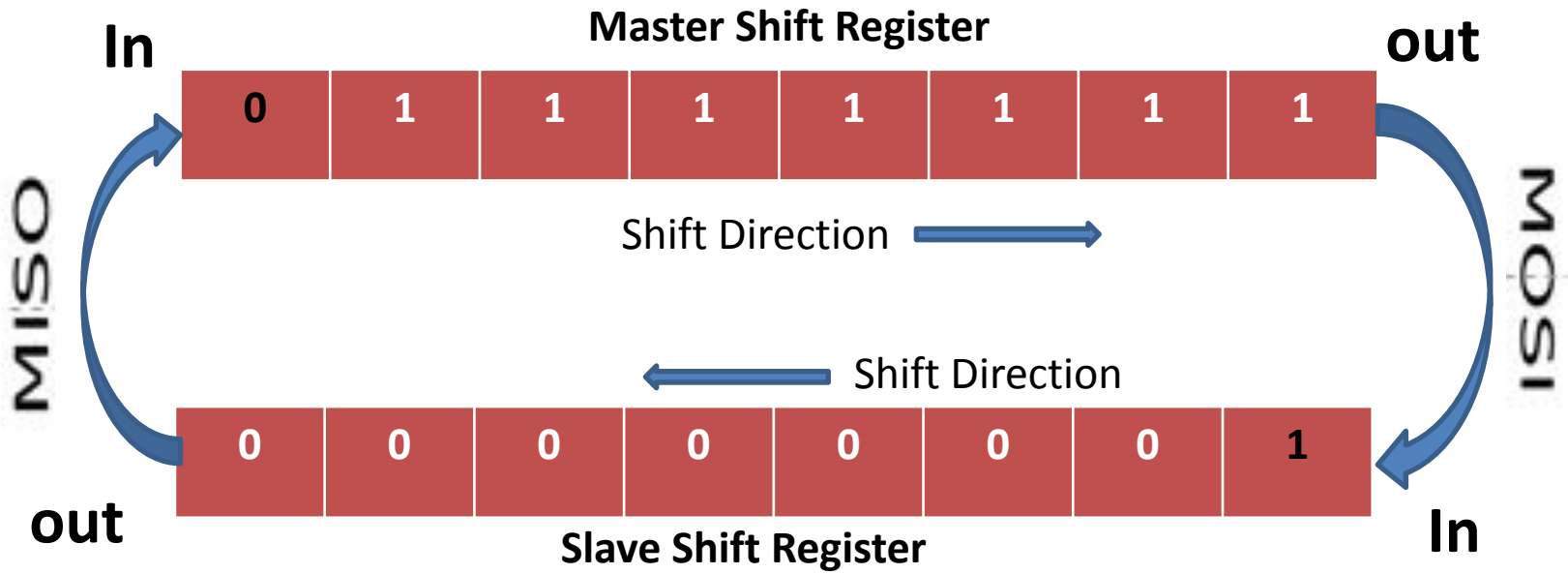
SPI Concept

SPI DATA TRANSMISSION AND RECEIVE

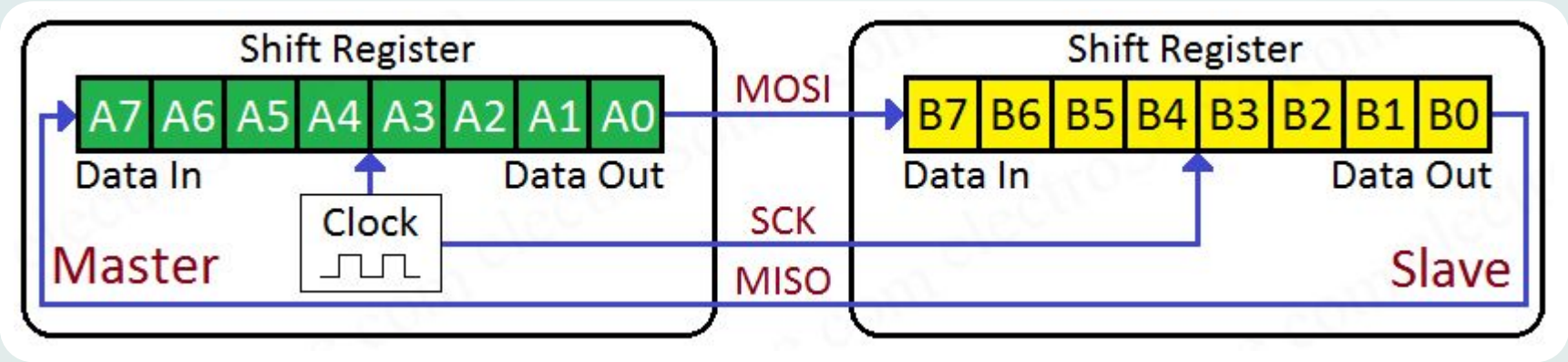
- the Master generates the required clock pulses on the SCK line to interchange data.

- Data is always shifted from Master to Slave on MOSI, line, and from Slave to Master on MISO, line.

SPI Concept


In
Master Shift Register
out
0
1
1
1
1
1
1
1
MISO
MOSI
Shift Direction
Shift Direction
0
0
0
0
0
0
0
1
out
In
Slave Shift Register

SPI Concept Summary



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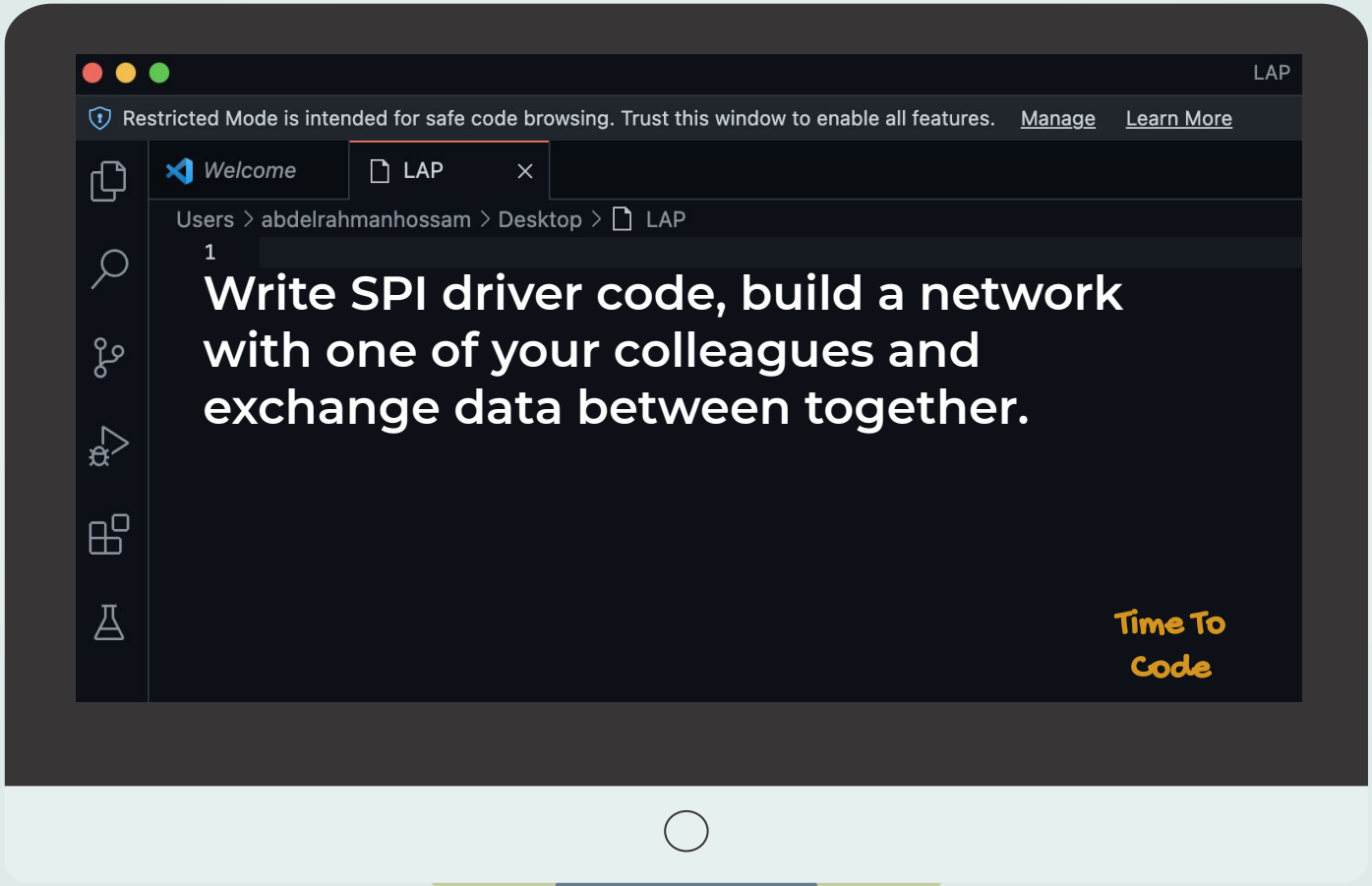

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