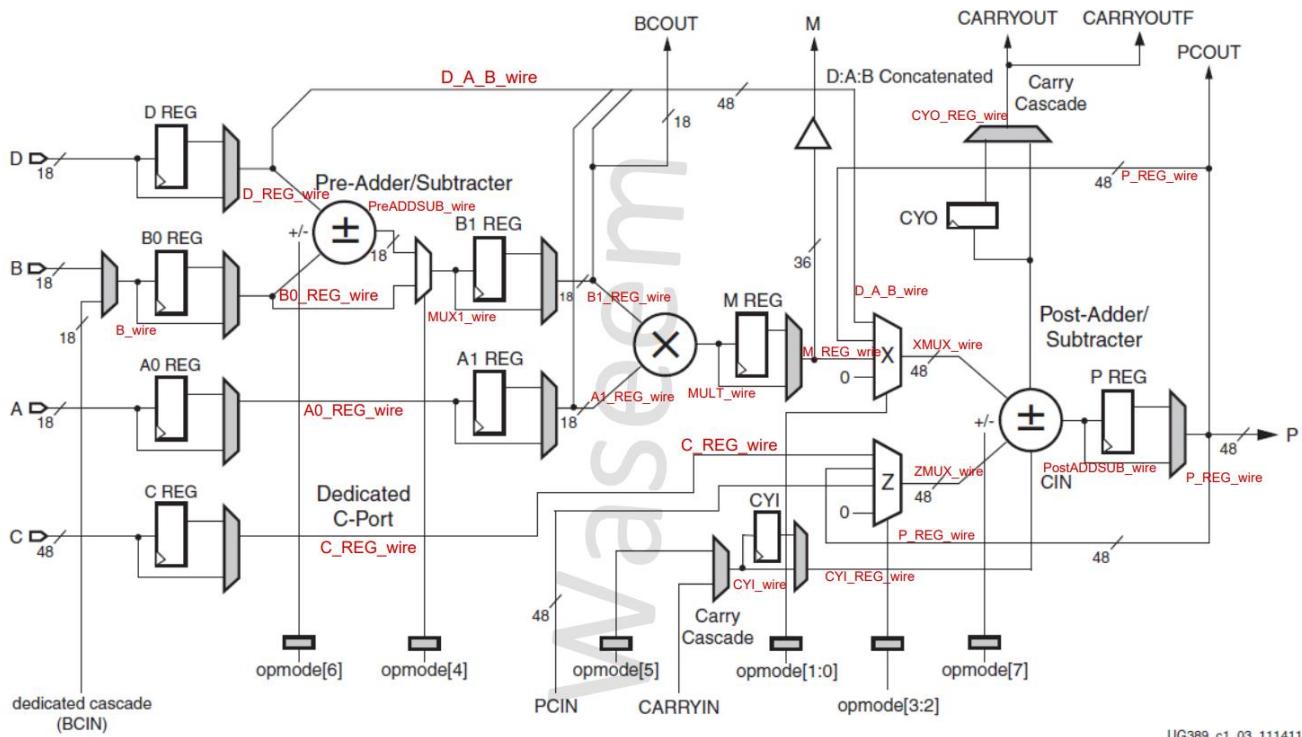


# **Project 1**

## **Spartan6\_DSB48A1**

<b>Ayman Mostafa Sayed Hassan</b>	<b>Karim Ayman Refaat</b>	<b>Youssef hesham Abdelfatah Mohamed</b>
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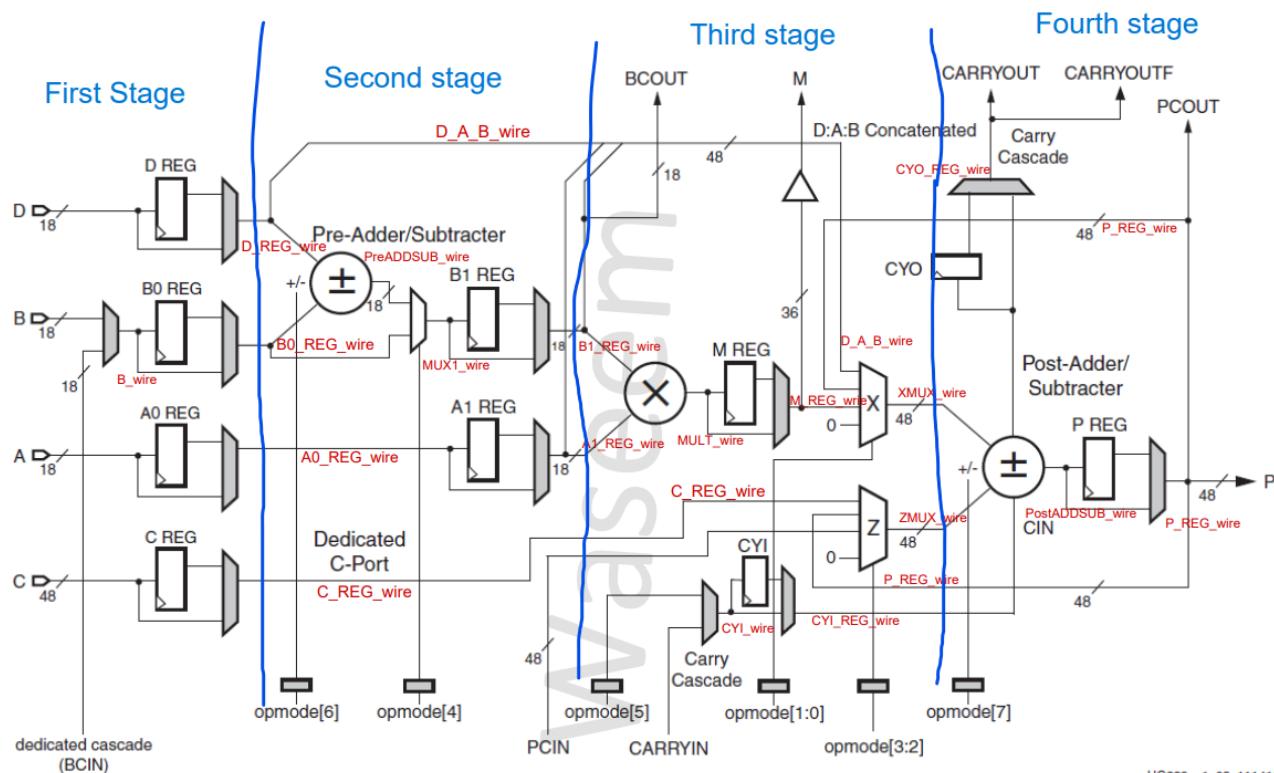
## Design and Wires Names



UG389 c1 03 111411

Note : Stages Are Commented in the Code to help in understanding the Code

^ ^ .



UG389 c1 03 111411

## Code :

D:\Digital\_Diploma\Spartan Project\Spartan\_DSB48A1\spartan.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

spartan.v tb\_spartan.v tb.memory.v

```

1  /*
2  * SPARTAN_DSB48A1 Module design Main Module
3  */
4  * Designed By : Karim Gomaa
5  */
6
7  module SPARTAN_DSB48A1(A,B,D,C,CLK,CARRYIN,opmode,BCIN,
8      RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
9      CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,
10     PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
11
12 ////////////////////////////////////////////////////////////////// Initialization //////////////////////////////////////////////////////////////////
13
14 input [17:0] A,B,D;
15 input [47:0] C;
16 input CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,
17     RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
18 input [7:0] opmode;
19 input [17:0] BCIN;
20 input [47:0] PCIN;
21
22 output reg [17:0] BCOUT;
23 output reg [47:0] PCOUT,P;
24 output reg [35:0] M;
25 output reg CARRYOUT,CARRYOUTF;
26
27 parameter A0REG=0; // Can Be 1: REG or 0 : COMB
28 parameter A1REG=1; // Can Be 1: REG or 0 : COMB
29 parameter B0REG=0; // Can Be 1: REG or 0 : COMB
30 parameter B1REG=1; // Can Be 1: REG or 0 : COMB
31 parameter CREG=1; // Can Be 1: REG or 0 : COMB
32 parameter DREG=1; // Can Be 1: REG or 0 : COMB
33 parameter MREG=1; // Can Be 1: REG or 0 : COMB
34 parameter PREG=1; // Can Be 1: REG or 0 : COMB
35 parameter CARRYINREG=1; // Can Be 1: REG or 0 : COMB
36 parameter CARRYOUTREG=1; // Can Be 1: REG or 0 : COMB
37 parameter OPMODEREGL=1; // Can Be 1: REG or 0 : COMB
38 parameter CARRYINSEL= "OPMODE5"; // Can be OPMODE5 or CARRYIN
39 parameter B_INPUT= "DIRECT"; // Can be DIRECT or CASCADE

```

Line 3, Column 2 Tab Size: 4 Verilog 3:08 AM 8/22/2023

D:\Digital\_Diploma\Spartan Project\Spartan\_DSB48A1\spartan.v - Sublime Text (UNREGISTERED)

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spartan.v tb\_spartan.v tb.memory.v

```

40 parameter RSTTYPE= "SYNC"; // Can be SYNC or ASYNC
41
42 wire [17:0] B_wire,D_REG_wire,B0_REG_wire,A0_REG_wire;
43 wire [17:0] PreADDSub_wire,MUX1_wire,B1_REG_wire,A1_REG_wire;
44 wire [35:0] MULT_wire,M_REG_wire;
45 wire [47:0] C_REG_wire,D_A_B_wire,XMUX_wire,ZMUX_wire,PostADDSub_wire,P_REG_wire;
46 wire CYI_wire,CYI_REG_wire,CYO_wire,CYO_REG_wire;
47 wire [7:0] OPMODE;
48
49 ////////////////////////////////////////////////////////////////// First Stage //////////////////////////////////////////////////////////////////
50 register #(.INPUTBITS(18),.RSTTYPE_register(RSTTYPE),.MUX_SEL(DREG)) D_Reg(.in(0),.clk(CLK),.CEREG(CED),.rst(RSTD),.register_data(D_REG_wire));
51 assign B_wire = (B_INPUT == "DIRECT")? B : BCIN;
52 register #(.INPUTBITS(18),.RSTTYPE_register(RSTTYPE),.MUX_SEL(B0REG)) B0_Reg(.in(B_wire),.clk(CLK),.CEREG(CEB),.rst(RSTB),.register_data(B0_REG_wire));
53 register #(.INPUTBITS(18),.RSTTYPE_register(RSTTYPE),.MUX_SEL(A0REG)) A0_Reg(.in(A),.clk(CLK),.CEREG(CEA),.rst(RSTA),.register_data(A0_REG_wire));
54 register #(.INPUTBITS(48),.RSTTYPE_register(RSTTYPE),.MUX_SEL(CREG)) C_Reg(.in(C),.clk(CLK),.CEREG(CEC),.rst(RSTC),.register_data(C_REG_wire));
55 register #(.INPUTBITS(8),.RSTTYPE_register(RSTTYPE),.MUX_SEL(OPMODEREG)) OPMODE_Reg(.in(opmode),.clk(CLK),.CEREG(CEOPMODE),.rst(RSTOPMODE),.register_data(OPMO
56 ////////////////////////////////////////////////////////////////// End Of First Stage //////////////////////////////////////////////////////////////////
57
58 ////////////////////////////////////////////////////////////////// Second Stage //////////////////////////////////////////////////////////////////
59 assign PreADDSub_wire = (OPMODE[6] == 1)? D_REG_wire:B0_REG_wire : D_REG_wire:B0_REG_wire;
60 assign MUX1_wire = (OPMODE[4] == 1)? PreADDSub_wire:B0_REG_wire;
61 register #(.INPUTBITS(18),.RSTTYPE_register(RSTTYPE),.MUX_SEL(B1REG)) B1_Reg(.in(MUX1_wire),.clk(CLK),.CEREG(CEB),.rst(RSTB),.register_data(B1_REG_wire));
62 register #(.INPUTBITS(18),.RSTTYPE_register(RSTTYPE),.MUX_SEL(A1REG)) A1_Reg(.in(A0_REG_wire),.clk(CLK),.CEREG(CEA),.rst(RSTA),.register_data(A1_REG_wire));
63 ////////////////////////////////////////////////////////////////// End Of Second Stage //////////////////////////////////////////////////////////////////
64
65 ////////////////////////////////////////////////////////////////// Third Stage //////////////////////////////////////////////////////////////////
66 assign MULT_wire = B1_REG_wire * A1_REG_wire;
67 register #(.INPUTBITS(36),.RSTTYPE_register(RSTTYPE),.MUX_SEL(MREG)) M_Reg(.in(MULT_wire),.clk(CLK),.CEREG(CEM),.rst(RSTM),.register_data(M_REG_wire));
68
69 assign XMUX_wire = (OPMODE[1:0] == 0'b00)? 0 :
70     (OPMODE[1:0] == 0'b01)? M_REG_wire :
71     (OPMODE[1:0] == 0'b10)? P_REG_wire : {D_REG_wire[11:0],A1_REG_wire[17:0],B1_REG_wire[17:0]};
72
73 assign ZMUX_wire = (OPMODE[3:2] == 0'b00)? 0 :
74     (OPMODE[3:2] == 0'b01)? PCIN :
75     (OPMODE[3:2] == 0'b10)? P_REG_wire : C_REG_wire ;
76
77 assign CYI_wire = (CARRYINSEL == "OPMODE5")? OPMODE[5] :

```

Line 3, Column 2 Tab Size: 4 Verilog 3:08 AM 8/22/2023

D:\Digital\_Diploma\Spartan Project\Spartan\_DSB48A1\spartan.v - Sublime Text (UNREGISTERED)

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spartan.v tb\_spartan.v tb\_memory.v

```

64 ////////////////////////////////////////////////////////////////// End Of Second Stage //////////////////////////////////////////////////////////////////
65
66 ////////////////////////////////////////////////////////////////// Third Stage //////////////////////////////////////////////////////////////////
67 assign MULT_wire = B1_REG_wire * A1_REG_wire;
68 register #(INPUTBITS(36), RSTTYPE_register(RSTTYPE), .MUX_SEL(MREG)) M_Reg(.in(MULT_wire), .clk(CLK), .CEREG(CEM), .rst(RSTM), .register_data(M_REG_wire));
69
70 assign XMUX_wire = (OPMODE[1:0] == 0'b00) ? 0 :
71           (OPMODE[1:0] == 0'b01) ? M_REG_wire :
72           (OPMODE[1:0] == 0'b10) ? P_REG_wire : {D_REG_wire[11:0], A1_REG_wire[17:0], B1_REG_wire[17:0]};
73
74 assign ZMUX_wire = (OPMODE[3:2] == 0'b00) ? 0 :
75           (OPMODE[3:2] == 0'b01) ? PCIN :
76           (OPMODE[3:2] == 0'b10) ? P_REG_wire : C_REG_wire;
77
78 assign CYI_wire = (CARRYINSEL == "OPMODE5") ? OPMODE[5] :
79           (CARRYINSEL == "CARRYIN") ? CARRYIN : 0;
80
81 register #(INPUTBITS(1), RSTTYPE_register(RSTTYPE), .MUX_SEL(CARRYINREG)) CYI_Reg(.in(CYI_wire), .clk(CLK), .CEREG(CECARRYIN), .rst(RSTCARRYIN), .register_data(CYI));
82 ////////////////////////////////////////////////////////////////// End Of Third Stage //////////////////////////////////////////////////////////////////
83
84 ////////////////////////////////////////////////////////////////// Fourth Stage //////////////////////////////////////////////////////////////////
85 assign {CYO_wire, PostADDSub_wire} = (OPMODE[7]==1) ? ZMUX_wire-(XMUX_wire+CYI_REG_wire) : ZMUX_wire+XMUX_wire+CYI_REG_wire ;
86
87 register #(INPUTBITS(1), RSTTYPE_register(RSTTYPE), .MUX_SEL(CARRYOUTREG)) CYO_Reg(.in(CYO_wire), .clk(CLK), .CEREG(CECARRYIN), .rst(RSTCARRYIN), .register_data(CYO));
88
89 register #(INPUTBITS(48), RSTTYPE_register(RSTTYPE), .MUX_SEL(PREG)) P_Reg(.in(PostADDSub_wire), .clk(CLK), .CEREG(CEP), .rst(RSTP), .register_data(P_REG_wire));
90 ////////////////////////////////////////////////////////////////// End Of Fourth Stage //////////////////////////////////////////////////////////////////
91
92
93 always @(*) begin
94   BCOUT <-B1_REG_wire;
95   PCOUT <-P_REG_wire;
96   P <-P_REG_wire;
97   M <-M_REG_wire;
98   CARRYOUT <-CYO_REG_wire;
99   CARRYOUTF <-CYO_REG_wire;
100 end
101
102 endmodule

```

Line 3, Column 2 Tab Size: 4 Verilog 3:08 AM 8/22/2023

## Register Code :

D:\Digital\_Diploma\Spartan Project\Spartan\_DSB48A1\register.v - Sublime Text (UNREGISTERED)

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spartan.v register.v tb\_spartan.v file.do

```

1 /*
2  * Register to be Instantiate in the Main Module
3  *
4  * Designed By : Karim Gomaa
5 */
6
7 module register(in,clk,CEREG,rst,register_data);
8 parameter INPUTBITS=1;
9 parameter RSTTYPE_register= "SYNC" ;
10 parameter MUX_SEL= 1; // Can Be 1: REG or 0 : COMB
11 input [INPUTBITS-1:0] in;
12 input clk,CEREG,rst;
13 output reg [INPUTBITS-1:0] register_data;
14
15 generate
16   if(RSTTYPE_register == "SYNC" && MUX_SEL == 1 ) begin
17     always @ (posedge clk) begin
18       if(rst)
19         register_data <= 0;
20       else if(CEREG)
21         register_data <= in;
22     end
23   end
24   else if (RSTTYPE_register == "ASYNC" && MUX_SEL== 1 ) begin
25     always @ (posedge clk or posedge rst) begin
26       if(rst)
27         register_data <= 0;
28       else if(CEREG)
29         register_data <= in;
30     end
31   end
32   else begin
33     always @(*)begin
34       register_data <= in;
35     end
36   end
37 endgenerate
38
39 endmodule

```

Line 1, Column 1 Tab Size: 4 Verilog 3:09 AM 8/22/2023

## TestBench Code:

D:\Digital\_Diploma\Spartan Project\1\Spartan\_DSB48A1\tb\_spartan.v - Sublime Text (UNREGISTERED)

```
File Edit Selection Find View Goto Tools Project Preferences Help
```

spartan.v register.v tb\_spartan.v file.do

```
1 module tb_spartan();
2
3 reg [17:0] A,B,D;
4 reg [47:0] C;
5 reg CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,
6 RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
7 reg [7:0] opmode;
8 reg [17:0] BCIN;
9 reg [47:0] PCIN;
10
11 wire [17:0] BCOUT;
12 wire [47:0] PCOUT,P;
13 wire [35:0] M;
14 wire CARRYOUT,CARRYOUTF;
15
16
17 SPARTAN_DSB48A1 dut(A,B,D,C,CLK,CARRYIN,opmode,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,
18 RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
19
20
21 initial begin
22     CLK=0;
23     forever
24     #2 CLK = ~CLK;
25 end
26
27 initial begin
28     D <= $urandom_range(1,10000);
29     B <= $urandom_range(1,10000);
30     A <= $urandom_range(1,10000);
31     C <= $urandom_range(1,10000);
32     RSTA<= 1;
33     RSTB<= 1;
34     RSTM<= 1;
35     RSTP<= 1;
36     RSTC<= 1;
37     RSTD<= 1;
38     RSTCARRYIN<= 1;
39     RSTOPMODE<= 1;
40     CARRYIN<= 0;
41
42
43
44
45
46
47
48
49
50
51
52
53
54
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56
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```

Line 1, Column 1 Tab Size: 4 Verilog 3:24 AM 8/22/2023

D:\Digital\_Diploma\Spartan Project\1\Spartan\_DSB48A1\tb\_spartan.v - Sublime Text (UNREGISTERED)

```
File Edit Selection Find View Goto Tools Project Preferences Help
```

spartan.v register.v tb\_spartan.v file.do

```
40 CARRYIN<= 0;
41 CEA<= 0;
42 CEB<= 0;
43 CEM<= 0;
44 CEP<= 0;
45 CEC<= 0;
46 CED<= 0;
47 CECARRYIN<= 1;
48 CEOPMODE<= 1;
49 opmode <= 7'b0000_0101;
50 BCIN <= 33;
51 PCIN<= 0;
52 #50
53
54 if(BCOUT!=0 && PCOUT!=0 && P!=0 && M!=0 && CARRYOUT!=0 && CARRYOUTF!=0) begin
55 $display("Error _- !!!!");
56 $stop;
57 end
58
59 D <= $urandom_range(1,10000);
60 B <= $urandom_range(1,10000);
61 A <= $urandom_range(1,10000);
62 C <= $urandom_range(1,10000);
63 RSTA<= 1;
64 RSTB<= 1;
65 RSTM<= 1;
66 RSTP<= 1;
67 RSTC<= 1;
68 RSTD<= 1;
69 RSTCARRYIN<= 1;
70 RSTOPMODE<= 1;
71 CARRYIN<= 1;
72 CEA<= 1;
73 CEB<= 1;
74 CEM<= 1;
75 CEP<= 1;
76 CEC<= 1;
77 CED<= 1;
78 CECARRYIN<= 1;
79 CEOPMODE<= 1;
```

Line 1, Column 1 Tab Size: 4 Verilog 3:24 AM 8/22/2023

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spartan.v register.v tb\_spartan.v file.do

```
79 CEOPMODE<= 1;
80 opmode <= 7'b0000_0101;
81 BCIN <= 33;
82 PCIN<= 0;
83 #50
84     if(BCOUT!=0 && PCOUT!=0 && P!=0 && M!=0 && CARRYOUT!=0 && CARRYOUTF!=0) begin
85         $display("Error -- !!!!");
86         $stop;
87     end
88
89 RSTA<= 1;
90 RSTB<= 0;
91 RSTM<= 1;
92 RSTP<= 1;
93 RSTC<= 1;
94 RSTD<= 1;
95 RSTCARRYIN<= 1;
96 RSTOPMODE<= 1;
97 CARRYIN<= 1;
98 CEA<= 1;
99 CEB<= 1;
100 CEM<= 1;
101 CEP<= 1;
102 CEC<= 1;
103 CED<= 1;
104 CECARRYIN<= 1;
105 CEOPMODE<= 1;
106 opmode <= 7'b0000_0101;
107 D <= $urandom_range(1,10000);
108 B <= $urandom_range(1,10000);
109 A <= $urandom_range(1,10000);
110 C <= $urandom_range(1,10000);
111 BCIN <= 33;
112 PCIN<= 0;
113 #50
114
115     if(BCOUT!=B && PCOUT!=0 && P!=0 && M!=0 && CARRYOUT!=0 && CARRYOUTF!=0) begin
116         $display("Error -- !!!!");
117         $stop;
118     end
119
120
121 RSTA<= 0;
122 RSTB<= 0;
123 RSTM<= 0;
124 RSTP<= 1;
125 RSTC<= 1;
126 RSTD<= 1;
127 RSTCARRYIN<= 1;
128 RSTOPMODE<= 1;
129 CARRYIN<= 1;
130 CEA<= 1;
131 CEB<= 1;
132 CEM<= 1;
133 CEP<= 1;
134 CEC<= 1;
135 CED<= 1;
136 CECARRYIN<= 1;
137 CEOPMODE<= 1;
138 opmode <= 7'b0000_0101;
139 D <= $urandom_range(1,10000);
140 B <= 10;
141 A <= 10;
142 C <= $urandom_range(1,10000);
143 BCIN <= 33;
144 PCIN<= 0;
145 #50
146
147     if(BCOUT!=B && PCOUT!=0 && P!=0 && M!=100 && CARRYOUT!=0 && CARRYOUTF!=0) begin
148         $display("Error -- !!!!");
149         $stop;
150     end
151
152 RSTA<= 0;
153 RSTB<= 0;
154 RSTM<= 0;
155 RSTP<= 0;
156 RSTC<= 0;
157 RSTD<= 0;
```

Line 1, Column 1 Tab Size: 4 Verilog

D:\Digital\_Diploma\Spartan Project1\Spartan\_DSB48A1\tb\_spartan.v - Sublime Text (UNREGISTERED)

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spartan.v register.v tb\_spartan.v file.do

```
118 $stop;
119 end
120
121 RSTA<= 0;
122 RSTB<= 0;
123 RSTM<= 0;
124 RSTP<= 1;
125 RSTC<= 1;
126 RSTD<= 1;
127 RSTCARRYIN<= 1;
128 RSTOPMODE<= 1;
129 CARRYIN<= 1;
130 CEA<= 1;
131 CEB<= 1;
132 CEM<= 1;
133 CEP<= 1;
134 CEC<= 1;
135 CED<= 1;
136 CECARRYIN<= 1;
137 CEOPMODE<= 1;
138 opmode <= 7'b0000_0101;
139 D <= $urandom_range(1,10000);
140 B <= 10;
141 A <= 10;
142 C <= $urandom_range(1,10000);
143 BCIN <= 33;
144 PCIN<= 0;
145 #50
146
147     if(BCOUT!=B && PCOUT!=0 && P!=0 && M!=100 && CARRYOUT!=0 && CARRYOUTF!=0) begin
148         $display("Error -- !!!!");
149         $stop;
150     end
151
152 RSTA<= 0;
153 RSTB<= 0;
154 RSTM<= 0;
155 RSTP<= 0;
156 RSTC<= 0;
157 RSTD<= 0;
```

Line 1, Column 1 Tab Size: 4 Verilog

D:\Digital\_Diploma\Spartan Project1\Spartan\_DSB48A1\tb\_spartan.v - Sublime Text (UNREGISTERED)

```

157 RSTD<= 0;
158 RSTCARRYIN<= 0;
159 RSTOPMODE<= 0;
160 CARRYIN<= 1;
161 CEA<= 1;
162 CEB<= 1;
163 CEM<= 1;
164 CEP<= 1;
165 CEC<= 1;
166 CED<= 1;
167 CECARRYIN<= 1;
168 CEOPMODE<= 1;
169 opmode <= 7'bz000_1101;
170 D <= $urandom_range(1,10000);
171 B <= 10;
172 A <= 10;
173 C <= 1;
174 BCIN <= 33;
175 PCIN<= 0;
176 #50
177 if(BCOUT!=B && PCOUT!=101 && P!=101 && M!=100 && CARRYOUT!=0 && CARRYOUTF!=0) begin
178   $display("Error -- !!!!");
179   $stop;
180 end
182
183 RSTA<= 0;
184 RSTB<= 0;
185 RSTM<= 0;
186 RSTP<= 0;
187 RSTC<= 0;
188 RSTD<= 0;
189 RSTCARRYIN<= 0;
190 RSTOPMODE<= 0;
191 CARRYIN<= 1;
192 CEA<= 1;
193 CEB<= 1;
194 CEM<= 1;
195 CEP<= 1;
196 CEC<= 1;

```

Line 1, Column 1

Tab Size: 4 Verilog

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```

183 RSTA<= 0;
184 RSTB<= 0;
185 RSTM<= 0;
186 RSTP<= 0;
187 RSTC<= 0;
188 RSTD<= 0;
189 RSTCARRYIN<= 0;
190 RSTOPMODE<= 0;
191 CARRYIN<= 1;
192 CEA<= 1;
193 CEB<= 1;
194 CEM<= 1;
195 CEP<= 1;
196 CEC<= 1;
197 CED<= 1;
198 CECARRYIN<= 1;
199 CEOPMODE<= 1;
200 opmode <= 7'bz0101_1001;
201 D <= 15;
202 B <= 10;
203 A <= 10;
204 C <= 1;
205 BCIN <= 33;
206 PCIN<= 0;
207 #50
208
209 if(BCOUT!=5 && M!=50 && CARRYOUT!=0 && CARRYOUTF!=0) begin
210   $display("Error -- !!!!");
211   $stop;
212 end
213
214 $stop;
215 end
216
217 initial begin
218   $monitor("D=%d , B=%d , A=%d , C=%d, BCOUT=%d , PCOUT=%d , P=%d , M=%d, CARRYOUT=%d, CARRYOUTF=%d",D,B,A,C,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
219 end
220
221 endmodule

```

Line 1, Column 1

Tab Size: 4 Verilog

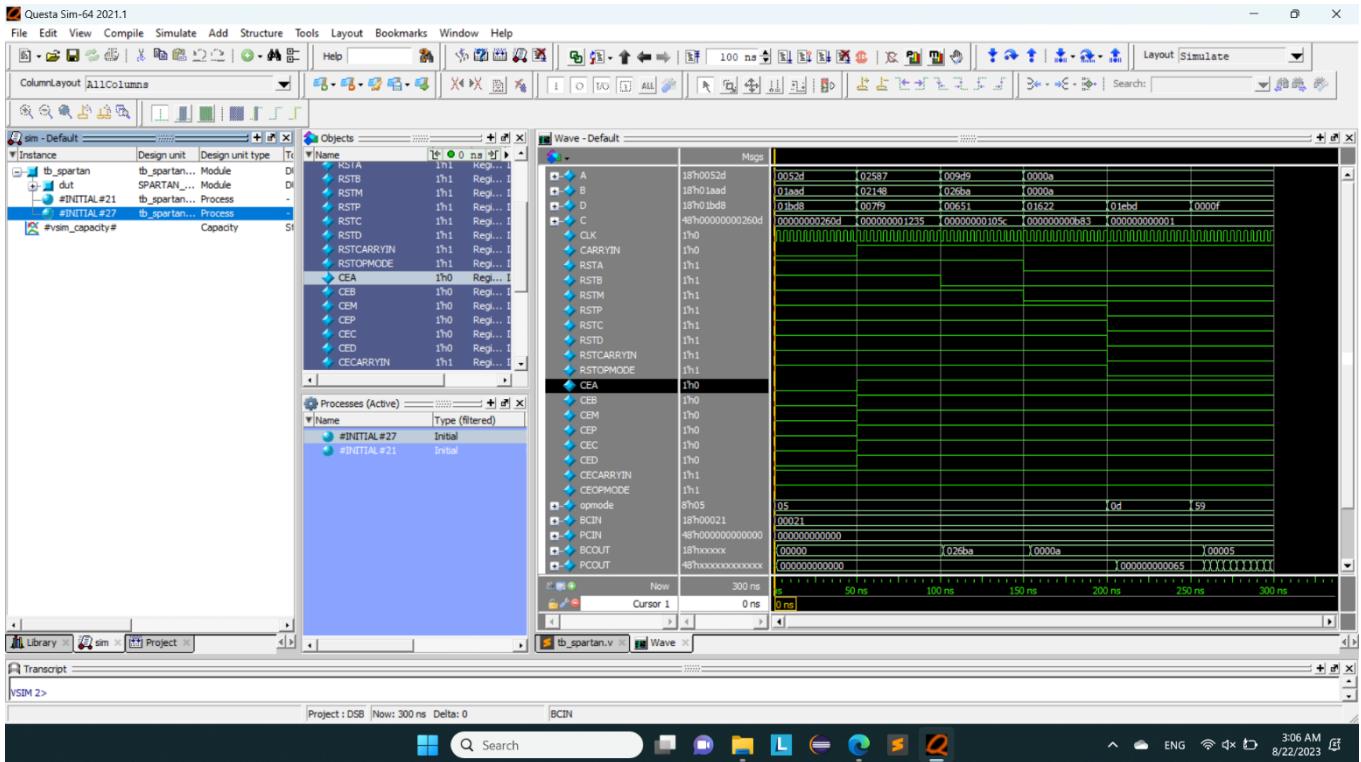
**Do file :**

```

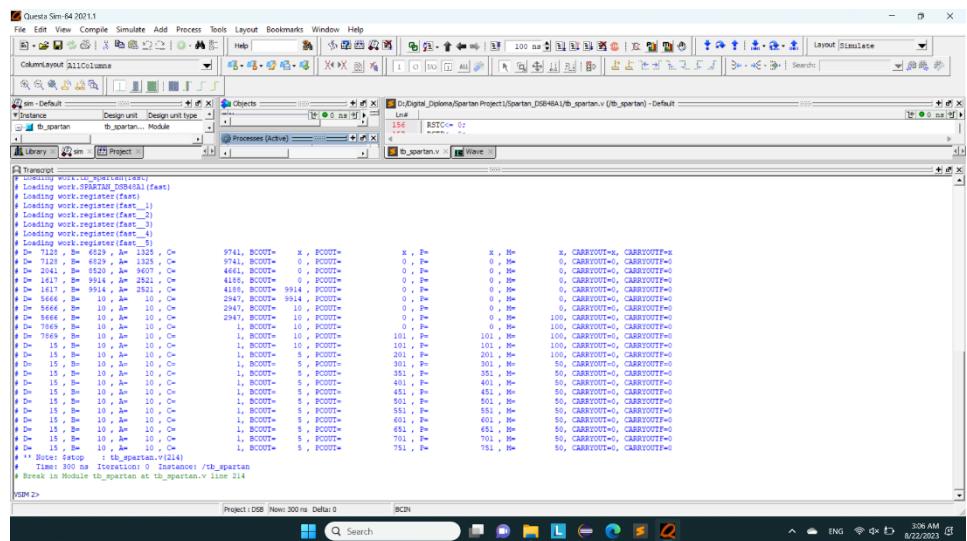
1 vlib work
2 vlog spartan.v register.v tb_spartan.v
3 vsim -voptargs+=acc work.tb_spartan
4 add wave *
5 run -all

```

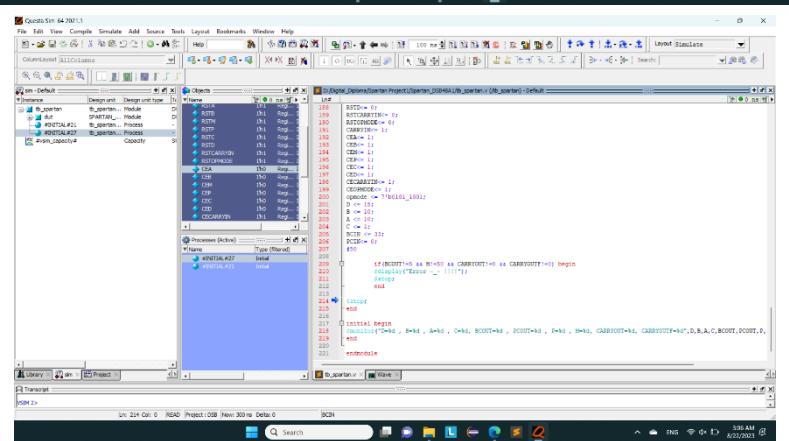
## WaveForm And Questasim Photos :



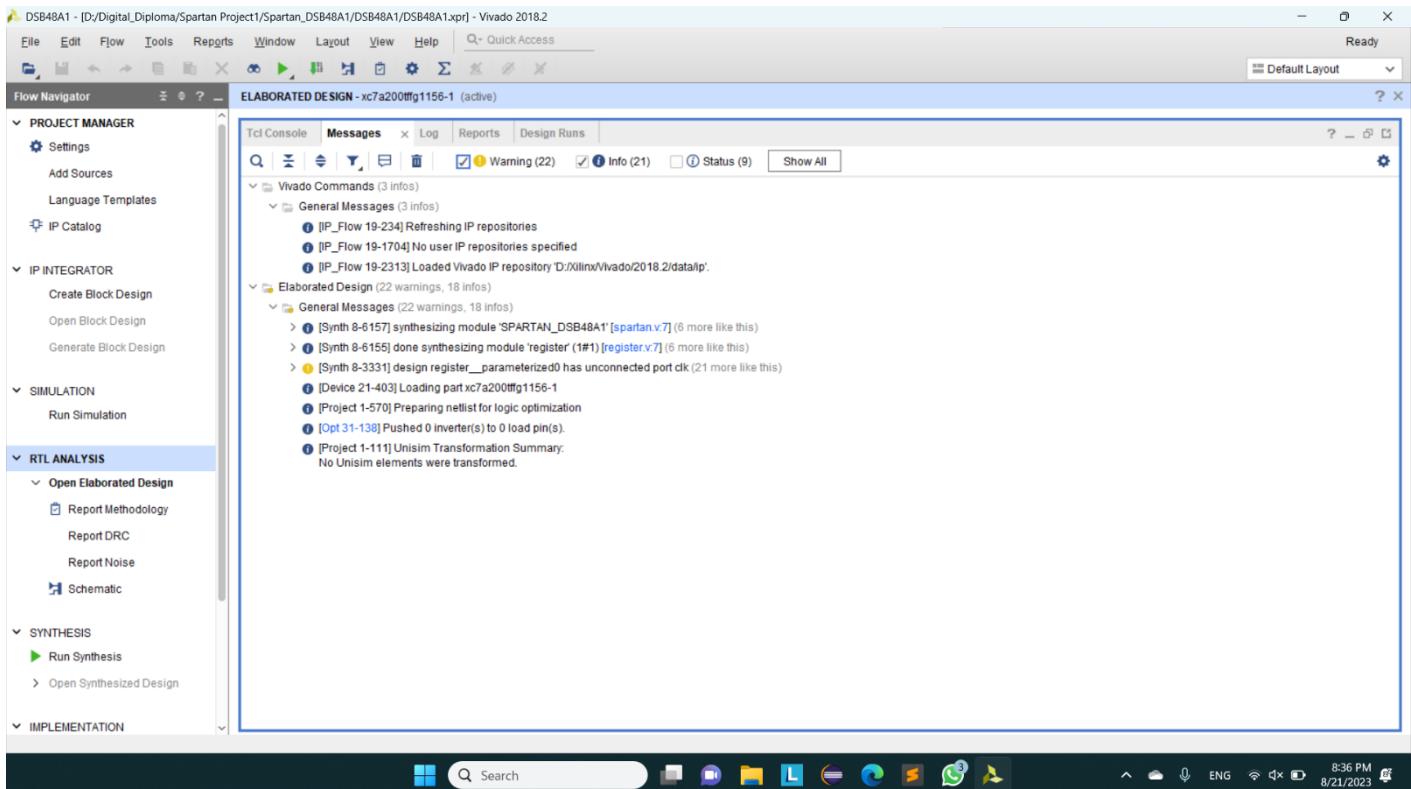
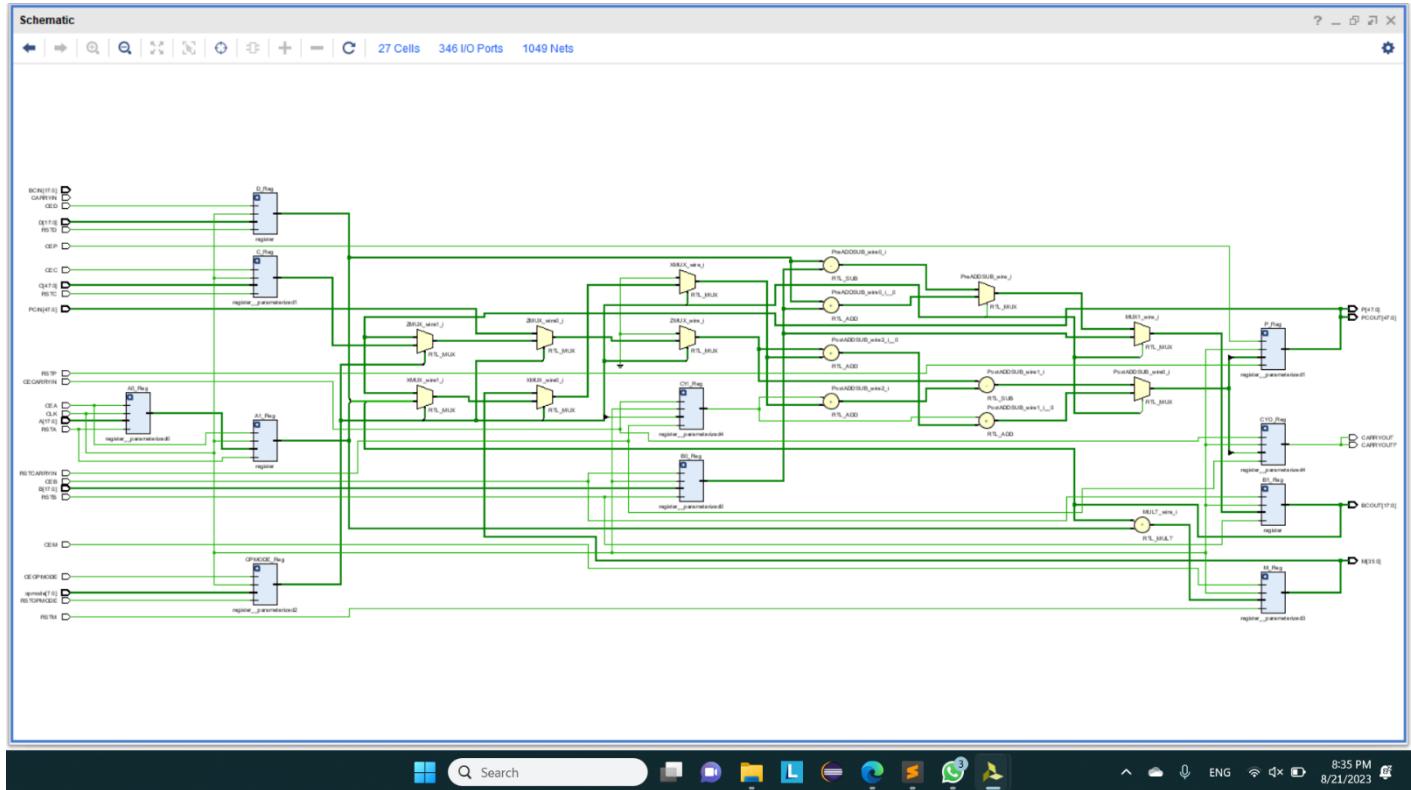
Just to Make sure  
Code is  
Working Right



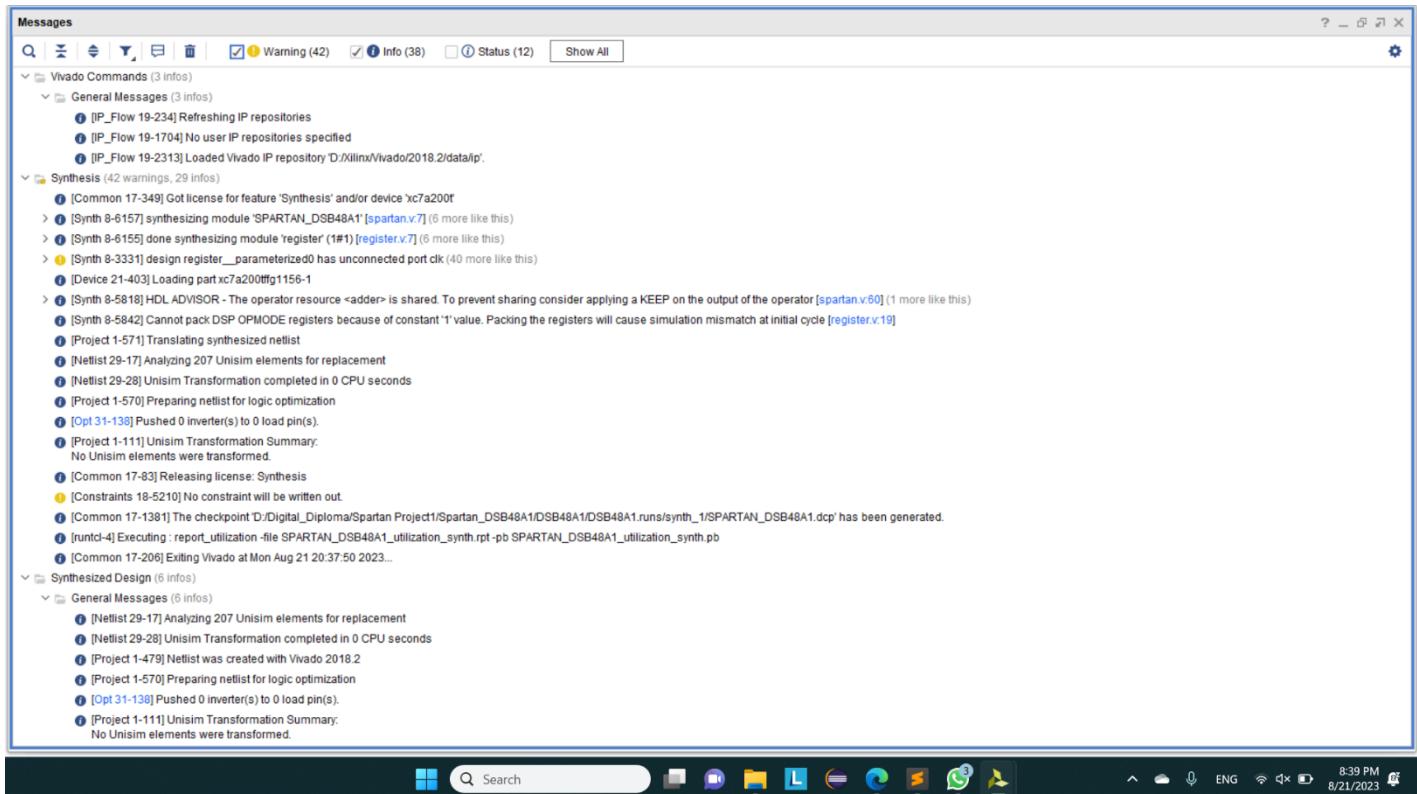
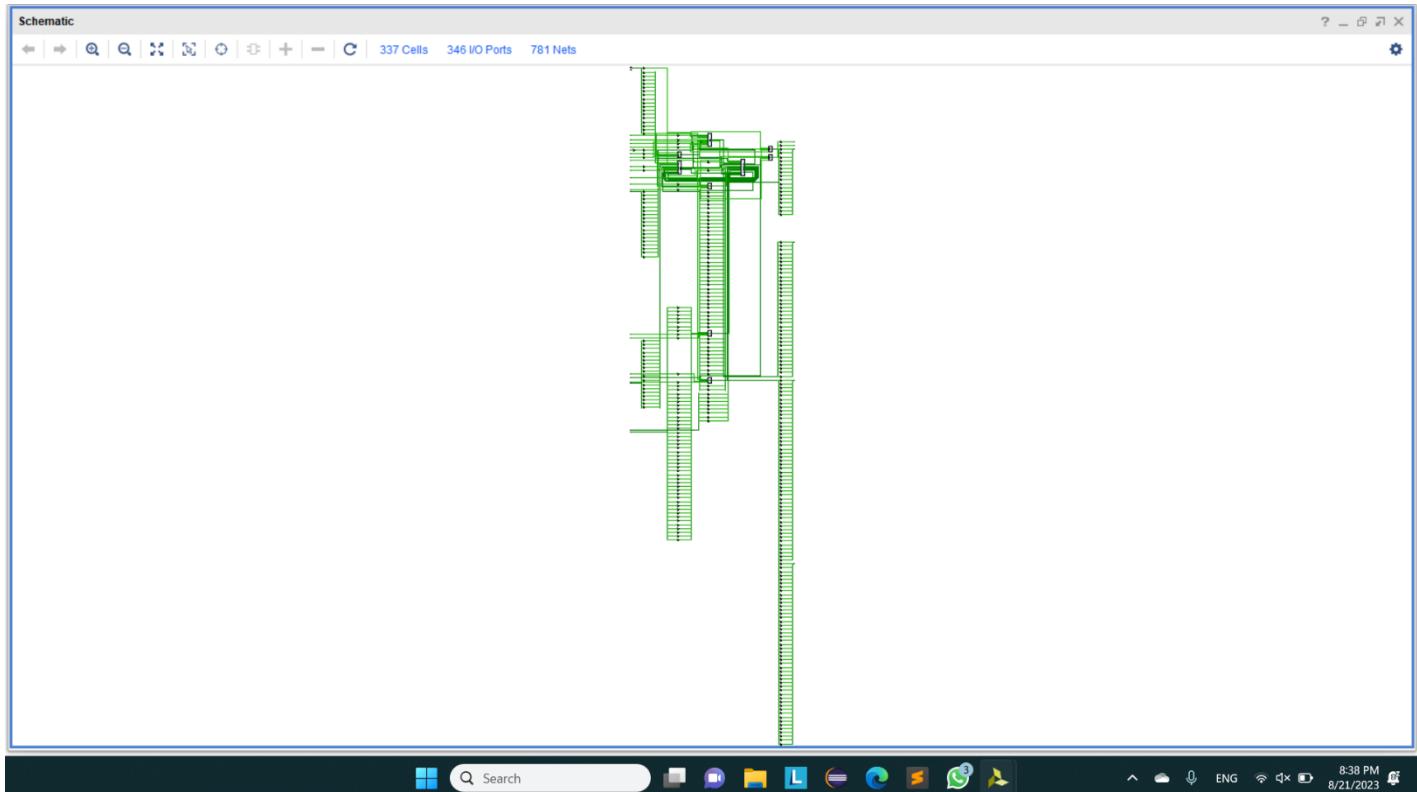
To see that code stopped in the  
Right place in testbench  
no Errors



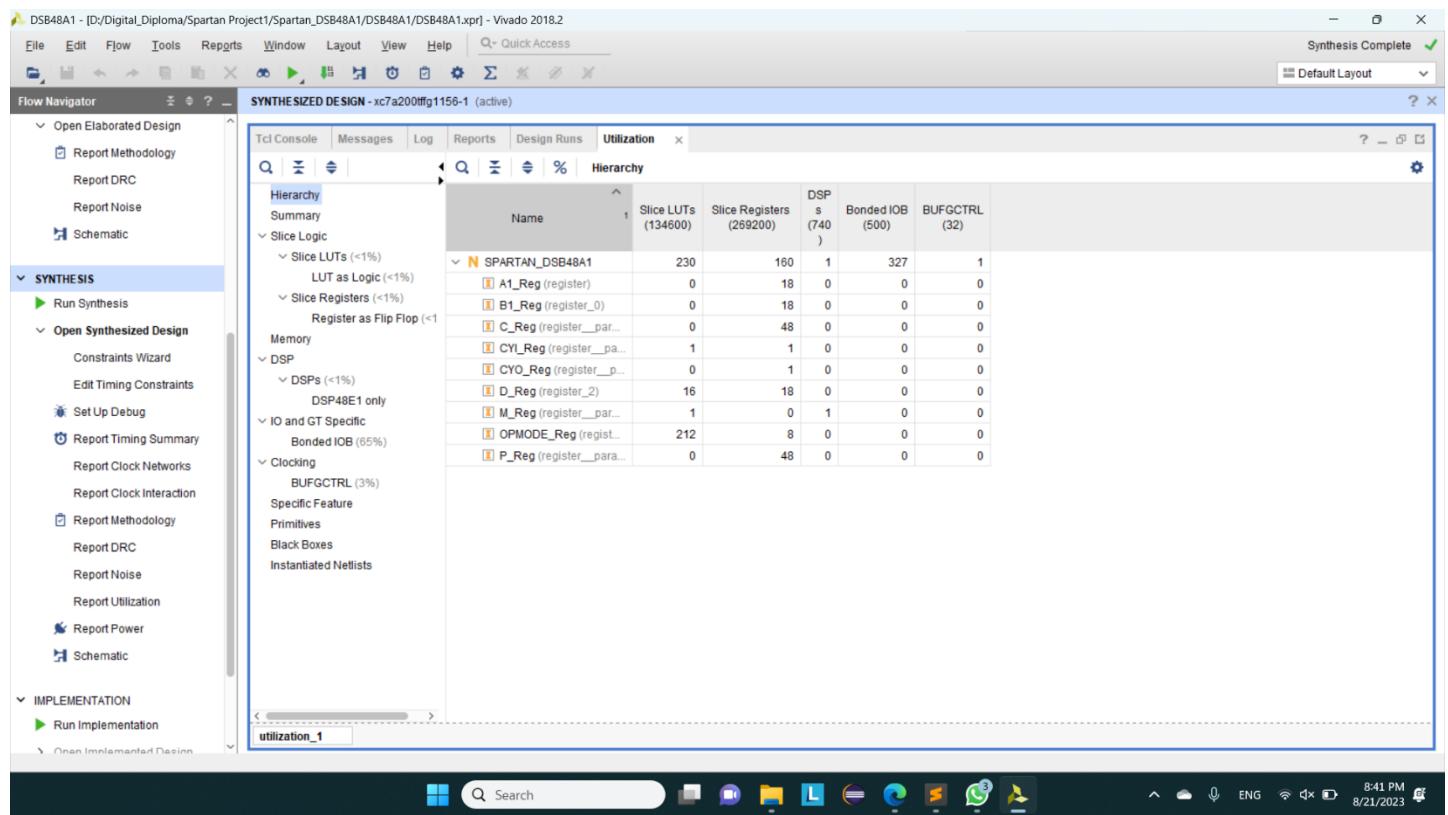
## **Elaboration: ( Schematic and Messages Snippets )**



## Synthesis: ( Schematic and Messages Snippets )



## Utilization report :



## Implementation: ( Schematic and Messages Snippets )

