ECE 497: Special Project
Weekly Report
Week 07

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What We Did

- Attempted to implement UART loopback interface in Verilog and flash to FPGA.
  - Worked correctly immediately, and on first try.
  - Means that
- Karl received a response from ChipYard maintainer, who redirected us to a Google Group.
- Both of us were preparing for exams, so we did not have as much progress.
  - Investigating using older Vivado versions for writing bitstream
  - Still working on the submodule thing.

What We Learned

- ChipYard FPGA image doesn't correctly do something with UART communication.
- ChipYard has a Google Group for getting help/support with ChipYard.
  - Need to interact with them to narrow down our possible problems.

Next Steps

- Prepare full documentation of what we have learned so far.
- Identify reasonable goals in preparation for ECE Research Day.
- Read other Verilog simulators to have a better grasp of ChipYard's.

References

Alon Amid et al. "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs." In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: 10.1109/MM.2020.2996616.