ECE 497: Special Project
Weekly Report
Week 05

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What We Did

- Spent lots of time digging through the repository trying to determine how to run a program on the SPI flash on FPGA
- Turns out, base Arty FPGA implementation does not support the SPI flash function. Was creating "SimSPI" flash that is used only for verilator (not synthesizable) Expected to use only ROM & run tethered to the simulator
- Sifive has a repository that generated an FPGA image for the Arty with SPI flash support

What We Learned

- Was able to connect to FPGA using OpenOCD debugging tool & USB debugger
- Uploaded generated bitstream to FPGA, but still couldn't utilize SPI flash
- At this point, tried to retrofit the SiFive implementation into the Chipyard Repository so I can customize using Chipyard components
- Largely Unsuccessful. SiFive requires depricated scala classes that have been removed from the Chipyard Repository.

Next Steps

- I believe the next step is to start learning Scala so that I can better understand how to create a class specifically for our needs
- A base "ArtyShell" class is provided that gives the correct pinouts for the Arty board, but it is unclear to me how SiFive utilized this when generating an FPGA image
- Almost ready to give in, have spent approx. 20 hours across the past week on tinkering with the FPGA board

References

Not Applicable this week