ECE 497: Special Project
Weekly Report
Week 02

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What We Did

- Set up Virtual machines to have similar environments.
- Clone the ChipYard repository.
- Build the toolchains required (Quite time-consuming)
- Followed documentation's example on how to generate a generic RISC-V chip.
- Used Verilator to simulate the default chip design.
  - Ran all tests (`make run-asm-tests`) (Quite time consuming)
  - Ran all benchmarks (`make run-bmark-tests`)
  - As expected, the default chip design passed all tests and benchmarks successfully.

What We Learned

- *Simulated* chip designs operate at O(1 kHz).
  - According to the documentation, these are significantly easier to debug.
- *FPGA-accelerated* chip designs operate at O(100 MHz).
  - These are also significantly more difficult to debug.
  - This speed is reached only when using FireSim (AWS).
  - We believe this implies we can write out the Verilog to Alex's FPGA and test there, albeit more slowly.
- `make run-asm-tests` runs all the instructions in the CPU design, ensuring ISA compliance.
- To get waveform outputs, run `make debug` when generating the simulated chip binary.

Next Steps

- Write the default chip out to Alex's FPGA and test.
- Use Scala/Chisel to generate a custom chip.
- Simulate the custom chip in software.
- Write the custom chip out to the FPGA.

References

Alon Amid et al. "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs." In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: 10.1109/MM.2020.2996616.