ECE 497: Special Project
Weekly Report
Week 09

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What We Did

- Successfully implemented Chipyard design with ability to output over UART
- Was solved by combination of Chipyard dev doing work on a branch & us solving an issue with the general FPGA implementation
- Error in the previous Uart "HarnessBinder" that attached the UART interface to the FPGA. Found by inspection

What We Did

- Solved erroneous UART characters & glitches. Use command from Freedom-e-sdk: `metal_tty_putc()` to output char[] to serial interface
- Made simple monitor program to receive user input. Working on parsing commands in C
- Reformatted documentation tex file to improve reading & writing abilities. Writing source files now simpler, reading output pdf simpler. Useful for final report, documentation, and ECE day presentation
- Elaborated on the setup process in our documentation with specific step-by-step instructions.

Demo

- Bitstream upload to FPGA
- Flash C Program to FPGA memory
- Monitor program in serial terminal

What We Learned

- There were several issues preventing UART communication on the FPGA. Improper implementation
- Freedom-e-sdk does not instantiate GPIO correctly $\rightarrow$ need to manually edit GPIO to make buttons/switches/leds work in our C code.
- Writing comprehensive documentation is time consuming

Next Steps

- Prepare full documentation of what we have learned so far.
  - Debugger $\rightarrow$ Setup, Upload, Tethered debug
  - Chipyard and its build process $\rightarrow$ setup, examples, supplementatal projects
  - Software used
  - Monitor Program for FPGA. Functionality to include memory examination, execute program at specific address, IO tests
- Make recorded presentation for ECE Research Day

References

Alon Amid et al. "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs." In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: 10.1109/MM.2020.2996616.