ECE 497: Special Project
Weekly Report
Week 06

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What We Did

- Alex spent lots of time going over Scala tutorials and reference material
- Successfully used Scala (and chipyard objects) to connect a switch on the FPGA with an LED
- Karl built and ran a simple FPGA image using Xilinx Vivado (catching up to Alex with FPGA)

What We Learned

- Getting an FPGA to communicate over UART is *very* difficult.
  - Reached out to Chipyard maintainers to inquire about Arty & UART communications.
- The design seems to be failing Design Rule Checking (DRC) in our version of Vivado?

Next Steps

- Work with core maintainer(s) to debug UART problems
- Karl program SPI flash with MCS image that has been causing Alex problems
- Karl continue working on Scala and getting custom project to build

References

Alon Amid et al. "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs." In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: 10.1109/MM.2020.2996616.