

ECE 497: Special Project

Weekly Report

Week 03

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What We Did

- ▶ Attempted to flash default chip to Alex's FPGA.
- ▶ Generate a non-default chip
- ▶ Run the `asm` tests on the non-default chip
- ▶ Went spelunking through the repository to find options, their definitions, and their overrides.

What We Did

- ▶ Successfully passed USB connection to FPGA through to VirtualBox VM, interfaced with FPGA in Vivado
- ▶ Conducted "Hello World" project on FPGA to ensure that bitstream was being sent to FPGA correctly.
- ▶ Used FPGA Prototyping Flow in Chipyard to generate a bitstream for the Arty FPGA board. Strangely, the default "example" project for the Arty did not pass all timing constraints. Will require investigation
- ▶ When creating bitstream in Chipyard, Vivado runs several tests on the design and produces detailed reports in a Chipyard folder.


```

1 Copyright 1980-2020 Xilinx, Inc. All Rights Reserved.
2 -----
3 | Tool Version : Vivado v.2020.2 (l1664) built 3062766 Wed Nov 18 09:12:47 MST 2020
4 | Date       : Wed Feb 18 23:41:46 2021
5 | Host      : alex-virtualbox.coding-oct-bit Ubuntu 20.04.2 LTS
6 | Command   : report_utilization -file /home/alex/Desktop/ecad97/weekly_report/week_03/utilization_report.txt -name utilization_1
7 | Design    : script001testharness
8 | Device    : xc7stcpg24-ll
9 | Design State : Synthesized
10 -----
11
12 Utilization Design Information
13
14 Table of Contents
15 -----
16 1. Slice Logic
17 1.1 Summary of Registers by Type
18 2. Memory
19 3. DSP
20 4. IO and IO Specific
21 5. Clocking
22 6. Specific Feature
23 7. Primitives
24 8. Block Nodes
25 9. Instantiated Modules
26
27 1. Slice Logic
28 -----
29
30 -----
31 | Site Type      | Used | Placed | Available | Utilize |
32 -----
33 | Slice LUTs*    | 9505 | 0 | 20000 | 40.65 |
34 | LUT as Logic   | 7931 | 0 | 20000 | 30.13 |
35 | LUT as Memory  | 174 | 0 | 9000 | 1.98 |
36 | LUT as distributed RAM | 172 | 0 |  |  |
37 | LUT as Shift Register | 2 | 0 |  |  |
38 | Slice Registers | 4179 | 0 | 41000 | 10.65 |
39 | Register as Flip-Flop | 4178 | 0 | 41000 | 10.64 |
40 | Register as Latch | 1 | 0 | 41000 | <0.01 |
41 | F8 Blocks      | 256 | 0 | 16000 | 1.57 |
42 | F8 Blocks      | 60 | 0 | 8150 | 0.74 |
43 -----
44
45 * Warning: The final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

```

Figure: Utilization Report Overview

What We Learned

- ▶ The repository is incredibly complicated
- ▶ **VERY** deep directory nesting (Partly due to Scala/Java project directory conventions).
- ▶ Putting the generated chip on an FPGA seems to be much more difficult than originally thought.
- ▶ Generating a non-default chip can be very easy or very hard.
 - ▶ Some of the options that must be overridden to ensure a different chip is built and simulated/benchmarked are not easy to understand or find.

Next Steps

- ▶ Continue trying to write the default chip out to Alex's FPGA and test.
- ▶ Practice generating other non-default chips to understand all the options used when generating a new chip.
- ▶ Hopefully, start defining a new, custom, chip using what we know, and building a very small proof-of-concept.



Alon Amid et al. “Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs.” In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: [10.1109/MM.2020.2996616](https://doi.org/10.1109/MM.2020.2996616).