ECE 497: Special Project
Weekly Report
Week 06

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What We Did

- Alex spent lots of time going over Scala tutorials and reference material
- Successfully used Scala (and chipyard objects) to connect a switch on the FPGA with an LED on the FPGA
- Karl built and ran a simple FPGA image using Xilinx Vivado (catching up to Alex with FPGA)

What We Learned

- Getting an FPGA to communicate over UART is *very* difficult. Will reach out to Chipyard maintainers to inquire about Arty & UART communications.
- The design seems to be failing Design Rule Checking (DRC) in our version of Vivado?

Next Steps

- one
- two

References

Not Applicable this week