ECE 497: Special Project
Weekly Report
Week 01

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ChipYard Amid et al. 2020

- This is the intended behavior.
- A platform for designing, simulating, and implementing RISC-V hardware systems using open-source libraries
- Supports three main RISC-V core designs: Rocket Core, BOOM (Berkeley Out-of-Order Machine), and CVA6 Core
- It seems that the Rocket Core is the most uniformly supported (sifive-blocks library provides several system components intended to be used with the Rocket Core)
- It is important to note that FPGA prototyping is supported, and the specific FPGA board I already own is explicitly supported (Xilinx Arty 35T)

Toolchain

Simulation

- Supports several simulation platforms, one of which is Verilator. Verilator is an Open-Source platform for simulating RTL logic, maintained by Veripool
- For advanced simulation, FireSim can be used to simulate fast FPGA boards to ensure pre-silicon verification and performance testing. FireSim is intended to be used on AWS cloud instances, so funding would be required if we intend to use this simulator. Provides comprehensive I/O simulation, including timing-accurate DRAM, Ethernet, etc. simulations. I anticipate that the Xilinx Vivado suite should provide sufficient FPGA simulation for our needs.

Simulation

- Provides instructions for complete simulation using Verilator, including waveform generation. ECE Department Saturn Server provides tools that can be used to analyze waveforms (CosmoScope)

RTL Generators

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Documentation

Our Focus

- Develop a working RISC-V chip prototype.
- Something else too.

References

Alon Amid et al. "Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs." In: *IEEE Micro* 40.4 (2020), pp. 10–21. ISSN: 1937-4143. DOI: 10.1109/MM.2020.2996616.