Preliminary
Subject to change without notice

V_{DS}	1200 V
$I_{D\ @\ 25^{\circ}C}$	140 A
$R_{DS(on)}$	13 mΩ

CPM3-1200-0013A

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- C3M SiC MOSFET technology
- High blocking voltage with low on-resistance
- Resistant to Latch-up
- Fast intrinsic diode with low reverse recovery (Qrr)
- Easy to parallel and simple to drive
- Optimized gate resistance for modules

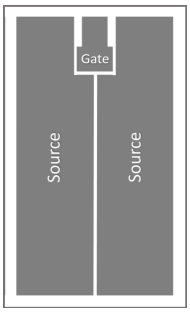
Benefits

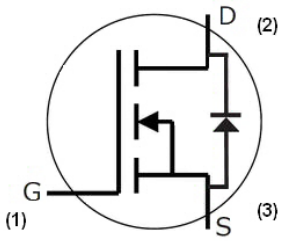
- Higher system efficiency
- Reduced cooling requirements
- Low conduction losses over temperature
- Increased system switching frequency

Applications

- EV motor drive
- Solar inverters
- High voltage DC/DC converters
- Load switch

Chip Outline





Part Number	Die Size (mm)
CPM3-1200-0013A	4.36 x 7.26

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC (f >1 Hz)	Note 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note 2
I_D	Continuous Drain Current	140	A	V_{GS} =15 V, T_C = 25˚C	Note 3
		90		V_{GS} =15 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	200	A	Pulse width t_P limited by T_{jmax}	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	˚C		
T_{Proc}	Maximum Processing Temperature	325	˚C	10 min. maximum	

Note (1): When using MOSFET body diode V_{GSmax} =-4V/+19V
Note (2): MOSFET can also safely operate at 0V/+15V
Note (3): Assumes a $R_{\theta JC}$ < 0.27 K/W

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	1.7	2.4	3.5	V	V_{DS} = V_{GS}, I_D = 20 mA	Fig. 11
			1.7		V	V_{DS} = V_{GS}, I_D = 20 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		13	16	mΩ	V_{GS} = 15 V, I_D = 70 A	Fig. 4, 5, 6
			21			V_{GS} = 15 V, I_D = 70 A, T_J = 175ºC	
g_{fs}	Transconductance		63		S	V_{DS}= 20 V, I_{DS}= 70 A	Fig. 7
			70			V_{DS}= 20 V, I_{DS}= 70 A, T_J = 175ºC	
C_{iss}	Input Capacitance		7670		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		275				
C_{rss}	Reverse Transfer Capacitance		12				
E_{oss}	C_{oss} Stored Energy		110		µJ		Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		2.1		mJ	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 75 A, $R_{G(ext)}$ = 2.5Ω, L= 57 µH,	
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)		1.5				
$t_{d(on)}$	Turn-On Delay Time		TBD		ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V I_D = 75 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	
t_r	Rise Time		TBD				
$t_{d(off)}$	Turn-Off Delay Time		TBD				
t_f	Fall Time		TBD				
$R_{G(int)}$	Internal Gate Resistance		5.9		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		67		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 75 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		56				
Q_g	Total Gate Charge		235				

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.4		V	V_{GS} = -4 V, I_{SD} = 75 A T_J = 25 °C	Fig. 8, 9 and 10
		3.8		V	V_{GS} = -4 V, I_{SD} = 75 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		97	A	V_{GS} = -4 V	Note 1
$I_{S, pulse}$	Diode pulse Current		200	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	Note 1
t_{rr}	Reverse Recover time	TBD		ns	V_{GS} = -4 V, I_{SD} = 30 A, V_R = 600 V dif/dt = 4500 A/µs, T_J = 175 °C	Note 2
Q_{rr}	Reverse Recovery Charge	TBD		nC		
I_{rrm}	Peak Reverse Recovery Current	TBD		A		

Typical Performance

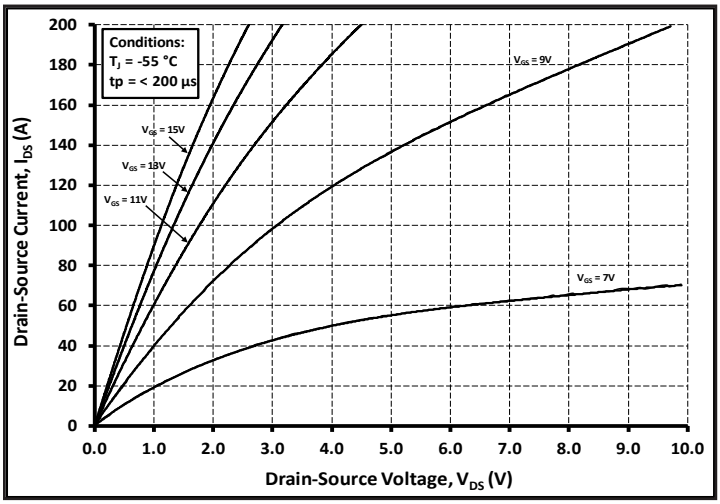


Figure 1. Output Characteristics T_J = -55 ºC

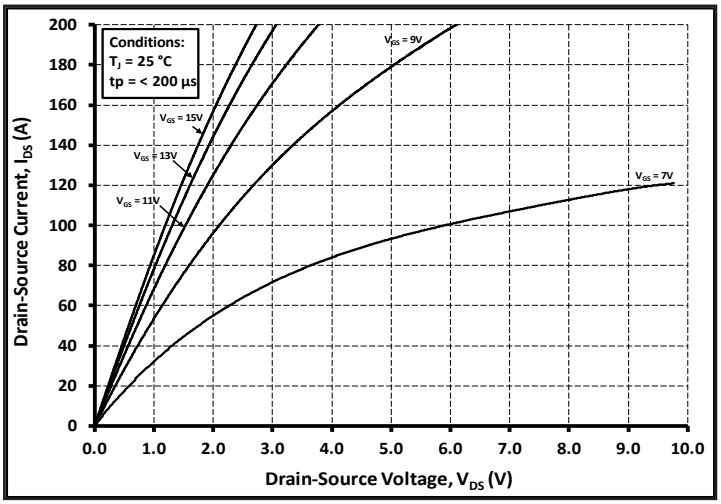


Figure 2. Output Characteristics T_J = 25 ºC

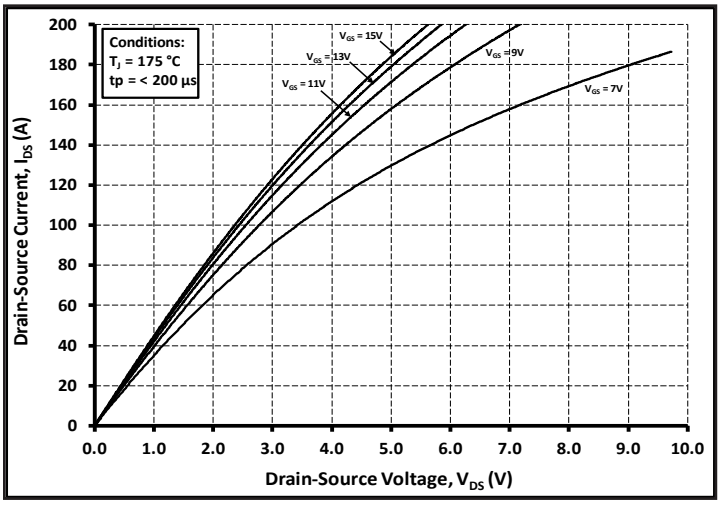


Figure 3. Output Characteristics T_J = 175 ºC

Figure 4. Normalized On-Resistance vs. Temperature

Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

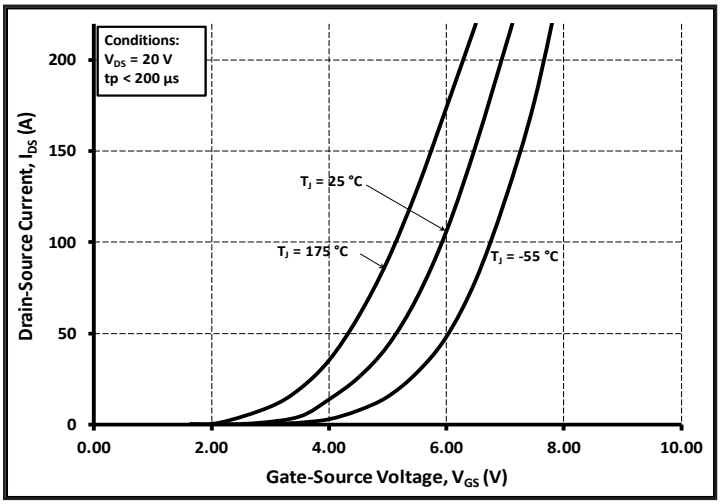


Figure 7. Transfer Characteristic for Various Junction Temperatures

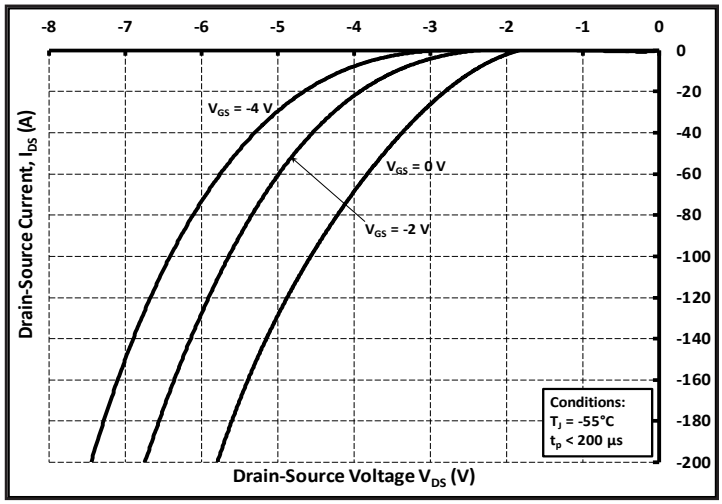


Figure 8. Body Diode Characteristic at -55 ºC

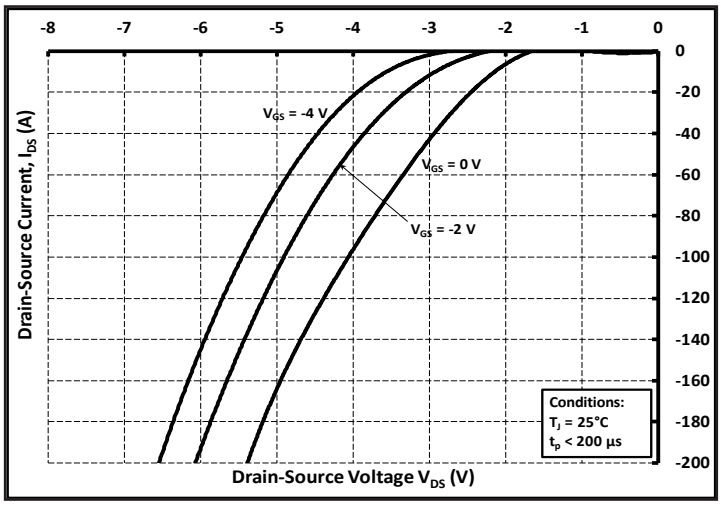


Figure 9. Body Diode Characteristic at 25 ºC

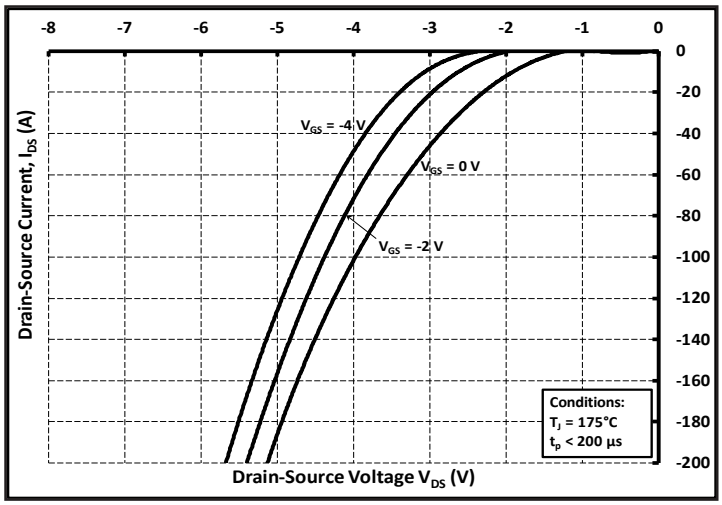


Figure 10. Body Diode Characteristic at 175 ºC

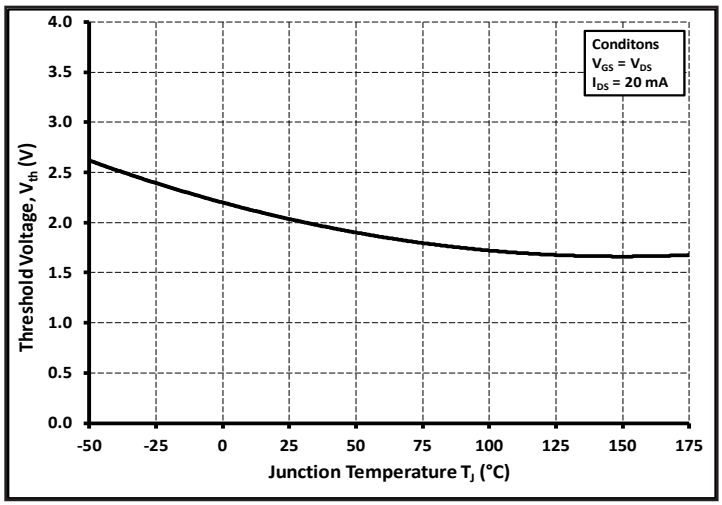


Figure 11. Threshold Voltage vs. Temperature

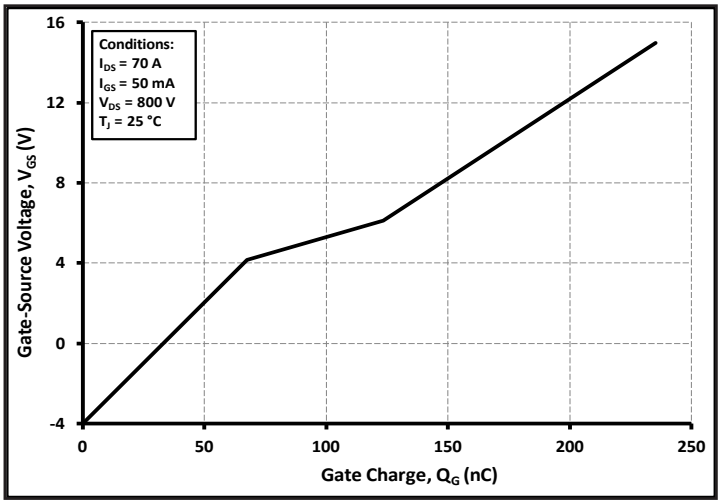


Figure 12. Gate Charge Characteristics

Typical Performance

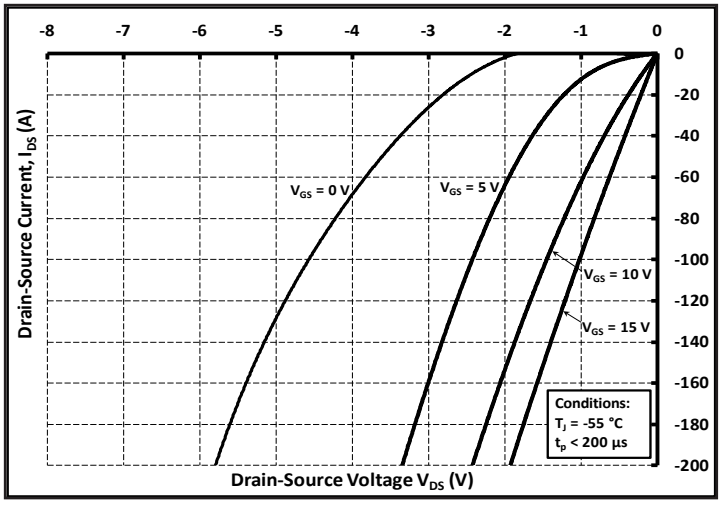


Figure 13. 3rd Quadrant Characteristic at -55 ºC

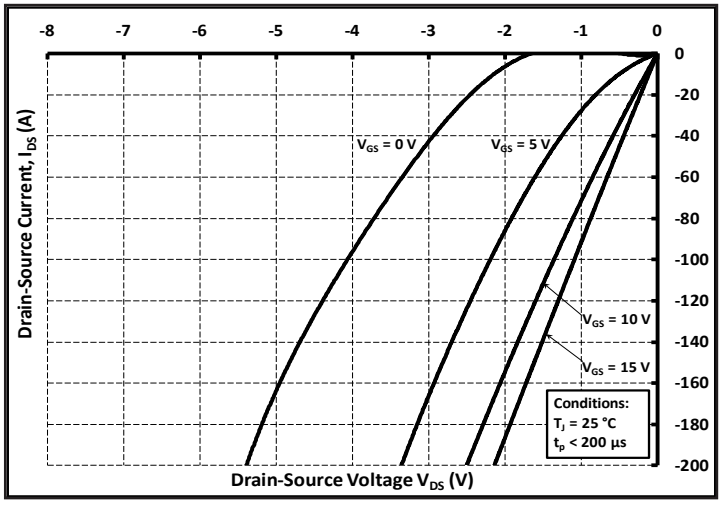


Figure 14. 3rd Quadrant Characteristic at 25 ºC

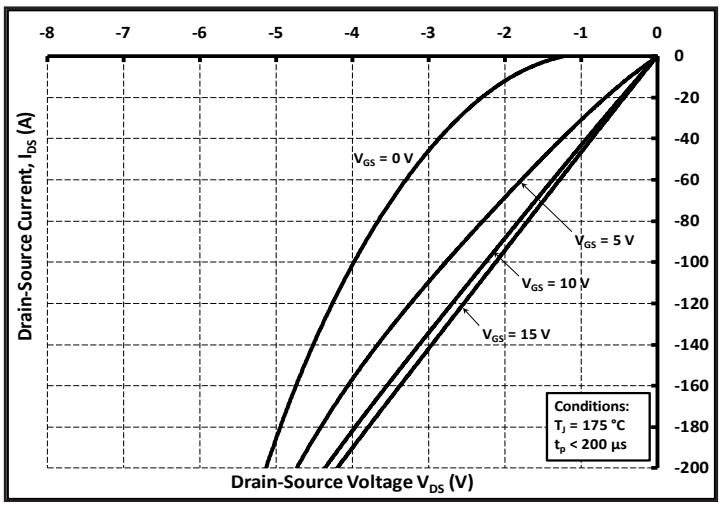


Figure 15. 3rd Quadrant Characteristic at 175 ºC

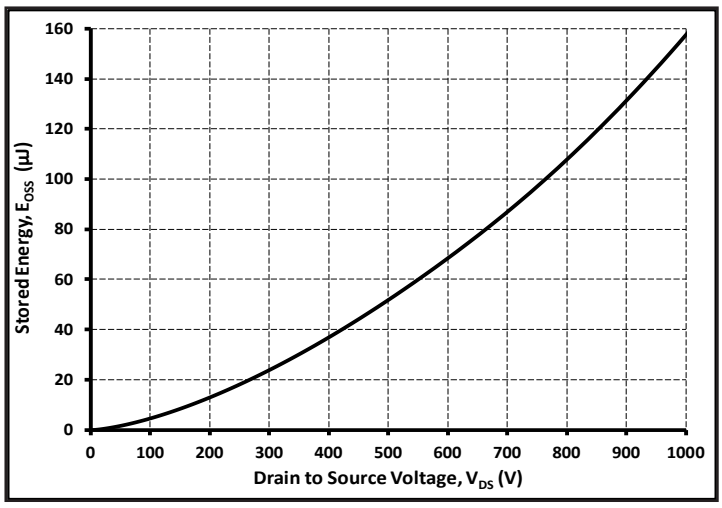


Figure 16. Output Capacitor Stored Energy

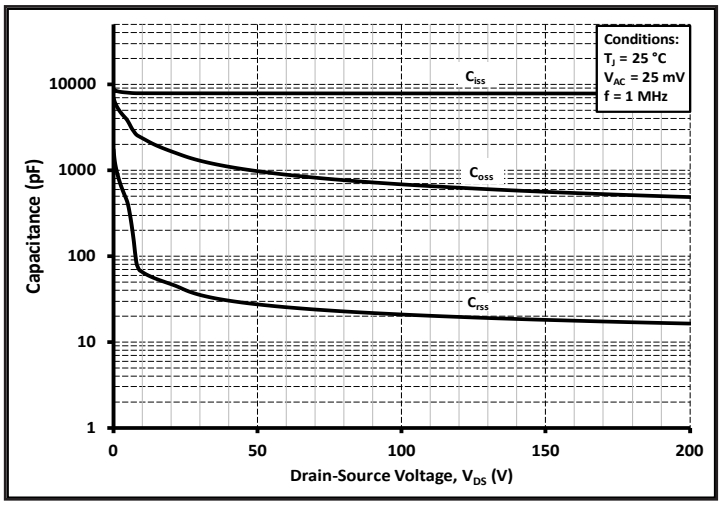


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

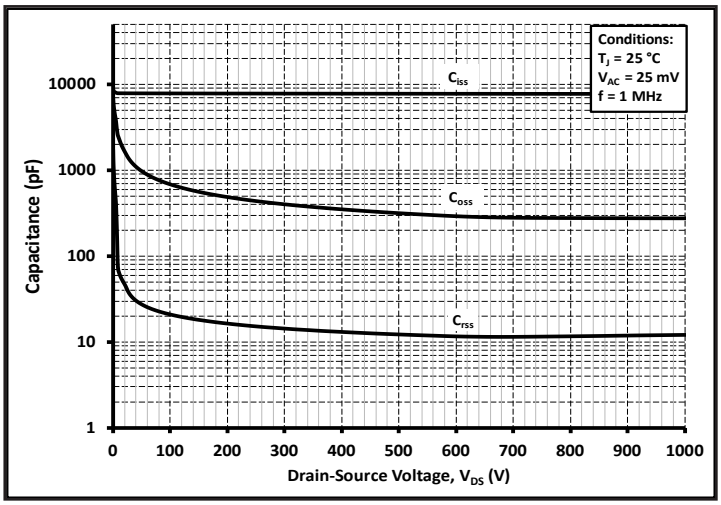
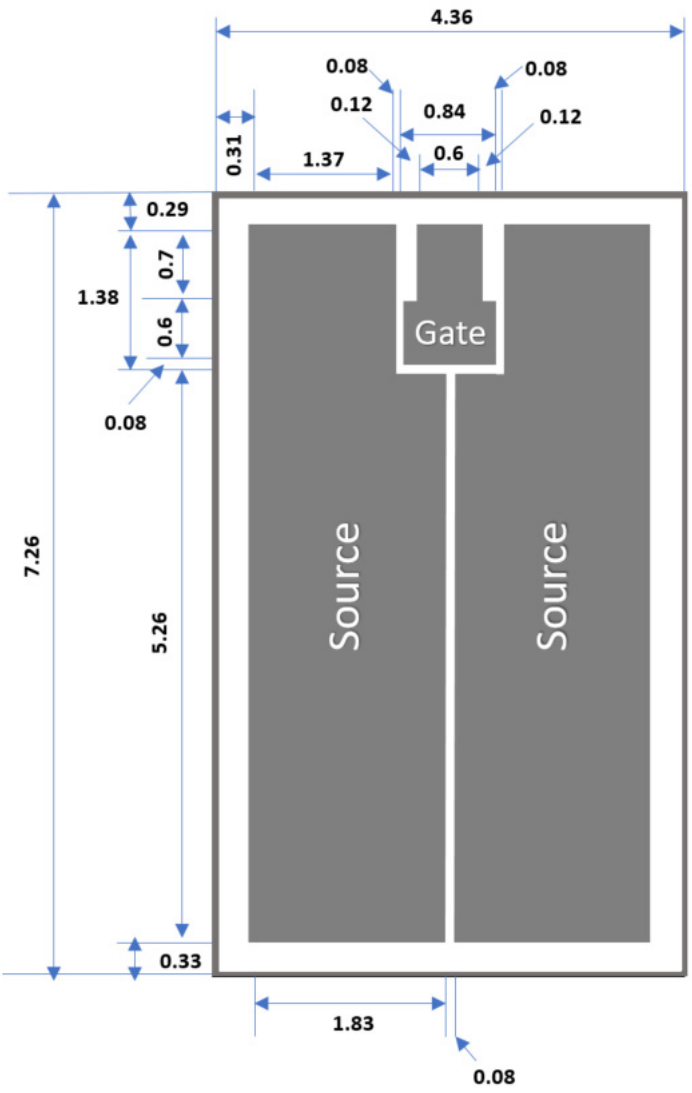


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Mechanical Parameters

Parameter	Typ	Unit
Die Dimensions (L x W)	4.36 x 7.26	mm
Exposed Source Pad Metal Dimensions	1.83 x 5.26 (X2)	mm
Exposed Source Pad Metal Dimensions	1.37 x 1.38 (X2)	mm
Gate Pad Dimensions	0.6 x 0.7 (X2)	mm
Gate Pad Dimensions	0.84 x 0.6 (X2)	mm
Chip Thickness	180 ± 10%	µm
Frontside (Source) metallization (Al)	4	µm
Frontside (Gate) metallization (Al)	4	µm
Backside (Drain) metallization (Ni/Au)	0.8 / 0.1	µm

Chip Dimensions



Not drawn to scale

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **SiC MOSFET Isolated Gate Driver reference design: www.wolfspeed.com/power/Tools-and-Support**
- **Application Considerations for Silicon-Carbide MOSFETs: www.wolfspeed.com/power/Tools-and-Support**

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.wolfspeed.com/power