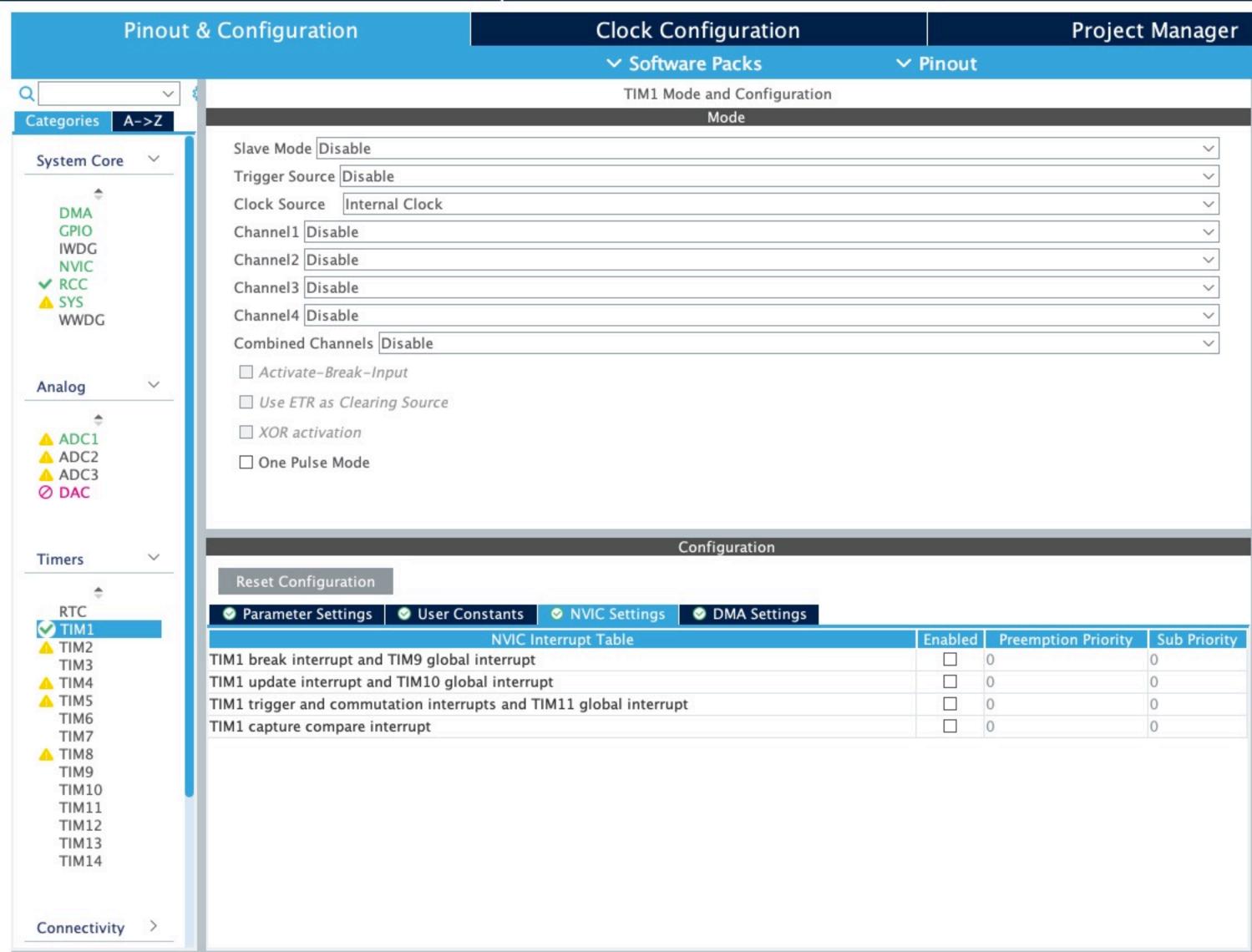
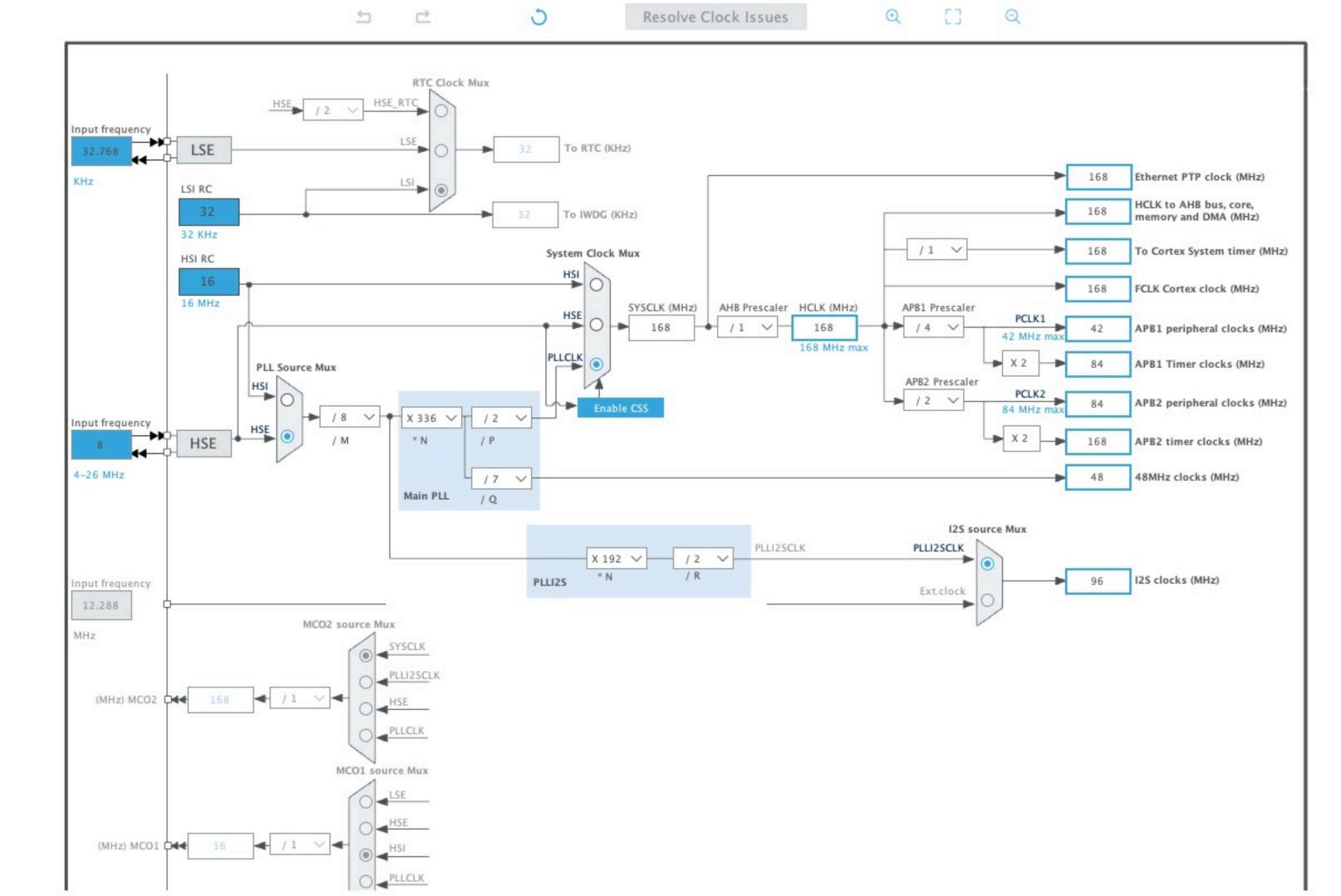


Mode High Speed Clock (HSE) Crystal/Ceramic Resonator Low Speed Clock (LSE) Crystal/Ceramic Resonator ☐ Master Clock Output 1 ☐ Master Clock Output 2 ☐ Audio Clock Input (I2S_CKIN) Configuration Reset Configuration Parameter Settings User Constants NVIC Settings Search Signals ☐ Show only Modified Pins Search (Ctrl+F) Maximum outp... GPIO output level GPIO Pull-up/P... Pin Name 🌲 Signal on Pin GPIO mode User Label Modified PC14-OSC32_IN RCC_OSC32_IN n/a n/a n/a n/a PC14-OSC32_IN **~** PC15-OSC32_O... RCC_OSC32_OUT n/a n/a PC15-OSC32_O... **~** n/a n/a PH0-OSC_IN PH0-OSC_IN RCC_OSC_IN **✓** n/a n/a n/a n/a PH1-OSC_OUT RCC_OSC_OUT PH1-OSC_OUT 4 n/a n/a n/a n/a

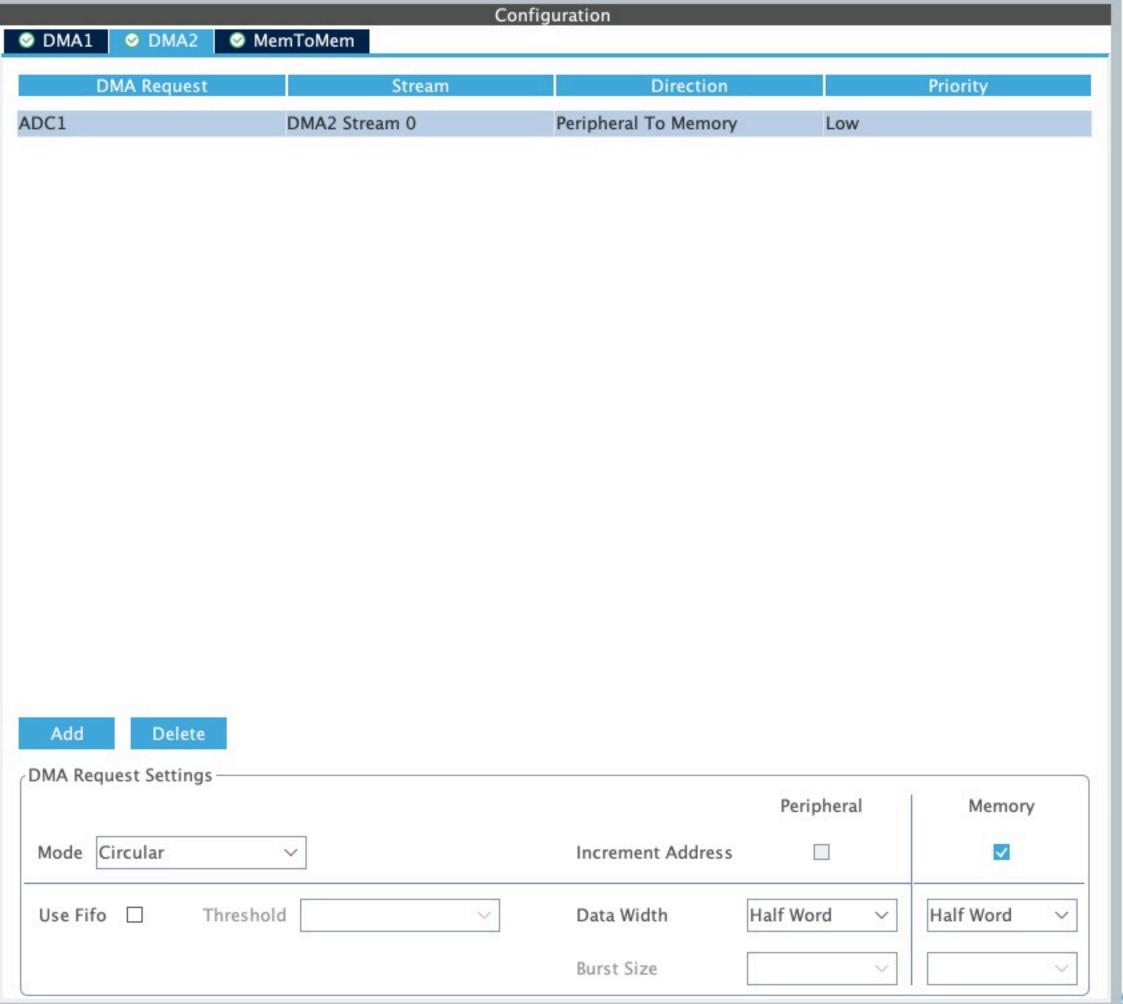
ADC1 Mode and Configuration	1			
Mode				
■ INO				
☑ IN1				
□ IN2				
□ IN3				
■ IN4				
■ IN5				
■ IN6				
■ IN7				
□ IN8				-
□ IN9				
■ IN10				
□ IN11				
□ IN12				
Configuration				- 1
Reset Configuration				
		ttings		
NVIC Interrupt Table	Enabled	T	Preemption Priority	Sub Priority
ADC1, ADC2 and ADC3 global interrupts		0		0
DMA2 stream0 global interrupt	~	0		0

ategories A->Z	Configuration	_	_	
System Core Y				
•	Priority Group 0 bits for pre-emption priority 4 bits for V Sort by Premption Priority a	and Sub Pric	ority	☐ Sort by interrupts names
DMA GPIO	Search (Ctrl+F)			▼ Force DMA channels Interrupts
IWDG NVIC	NVIC Interrupt Table	Enabled	P	reemption Priority Sub Priority
✓ RCC	Non maskable interrupt	~	0	0
SYS WWDG	Hard fault interrupt	~	0	0
	Memory management fault	~	0	0
	Pre-fetch fault, memory access fault	~	0	0
alog ~	Undefined instruction or illegal state	~	0	0
	System service call via SWI instruction	~	0	0
	Debug monitor	~	0	0
ADC1 ADC2	Pendable request for system service	~	0	0
ADC3	Time base: System tick timer	~	0	0
DAC	PVD interrupt through EXTI line 16		0	0
	Flash global interrupt		0	0
	RCC global interrupt		0	0
ers v	ADC1, ADC2 and ADC3 global interrupts		0	0
	TIM1 break interrupt and TIM9 global interrupt		0	0
TC =	TIM1 update interrupt and TIM10 global interrupt		0	0
IM1	TIM1 trigger and commutation interrupts and TIM11 global interrupt		0	0
IM2	TIM1 capture compare interrupt		0	0
M3	I2C1 event interrupt		0	0
M4 M5	I2C1 error interrupt		0	0
M6	SPI1 global interrupt		0	0
М7	SPI3 global interrupt		0	0
M8	DMA2 stream0 global interrupt	~	0	0
M9 M10	USB On The Go FS global interrupt	~	0	0
IM11	FPU global interrupt		0	0
TIM12 TIM13 TIM14				
onnectivity >	☐ Enabled Preemption Priority	∨ Sub Pri	ority	~

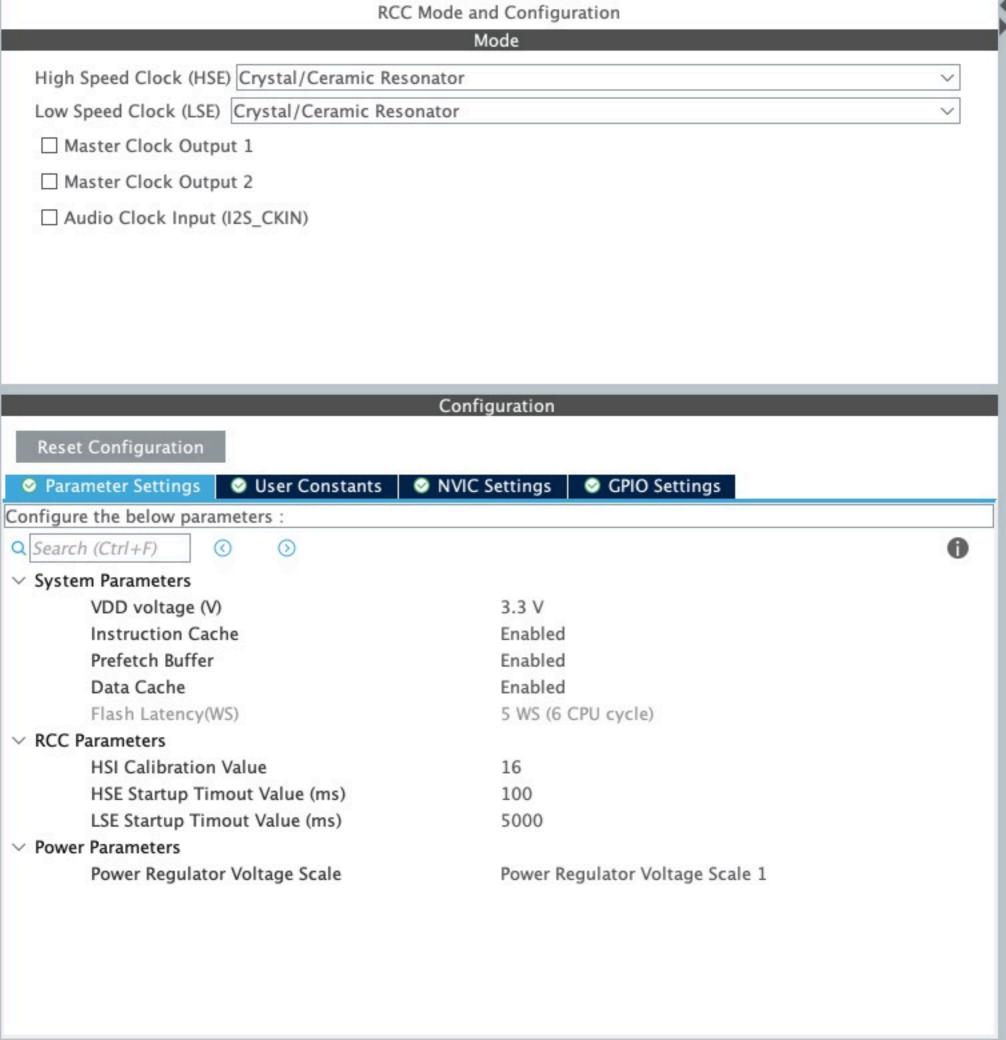




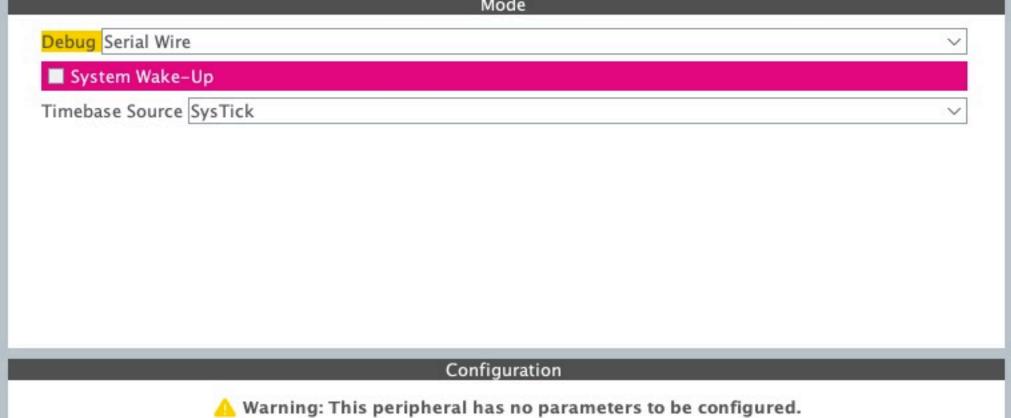
ADC1 Mode and Configuration					
	Mode				
■ INO					
✓ IN1					
□ IN2					
□ IN3					
C	Configuration				
	201111garacion				
Reset Configuration					
	NVIC Settings				
Configure the below parameters :					
Q Search (Ctrl+F) ① ①		0			
∨ ADCs_Common_Settings					
Mode	Independent mode				
∨ ADC_Settings					
Clock Prescaler	PCLK2 divided by 8				
Resolution	12 bits (15 ADC Clock cycles)				
Data Alignment	Right alignment				
Scan Conversion Mode	Disabled				
Continuous Conversion Mode	Enabled				
Discontinuous Conversion Mode	Disabled				
DMA Continuous Requests	Enabled				
End Of Conversion Selection	EOC flag at the end of single channel conversion				
∨ ADC_Regular_ConversionMode					
Number Of Conversion	1				
External Trigger Conversion Source	Regular Conversion launched by software				
External Trigger Conversion Edge	None				
> Rank	1				
∨ ADC_Injected_ConversionMode					
Number Of Conversions	0				
∨ WatchDog					
Enable Analog WatchDog Mode					



STEACH PLANE STANKE AND STANKE WITH THE STANKE STAN	NVIC Mode and Con			∨ Pinout			
Enabled interrupt table	(9)						
Enabled interrupt table	Configuratio						
Enabled interrupt table		Configuration					
STEACH PLANE STANKE AND STANKE WITH THE STANKE STAN			(2)				
	Select for init sequence or	Generate Enable in	✓ Generate I	. Call HAL han			
Non maskable interrupt			~				
Hard fault interrupt			✓				
Memory management fault			✓				
Pre-fetch fault, memory access			✓				
Undefined instruction or illegal			✓				
System service call via SWI instr			✓				
Debug monitor			~				
Pendable request for system se			~				
			~	~			
		✓	✓	~			
		V	V	V			
			T. E. T. V.				
	<u> </u>		init code)				
Rank		Interrupt name					
		Ĵ					
	Undefined instruction or illegal System service call via SWI instr Debug monitor Pendable request for system se Time base: System tick timer DMA2 stream0 global interrupt USB On The Go FS global interru	Undefined instruction or illegal System service call via SWI instr Debug monitor Pendable request for system se Time base: System tick timer DMA2 stream0 global interrupt USB On The Go FS global interru	Undefined instruction or illegal System service call via SWI instr Debug monitor Pendable request for system se Time base: System tick timer DMA2 stream0 global interrupt USB On The Go FS global interru	Undefined instruction or illegal System service call via SWI instr Debug monitor Pendable request for system se Time base: System tick timer DMA2 stream0 global interrupt USB On The Go FS global interru Interrupt unmasking ordering table (interrupt init code is moved after all the peripheral init code)	Undefined instruction or illegal System service call via SWI instr Debug monitor Pendable request for system se Time base: System tick timer DMA2 stream0 global interrupt USB On The Go FS global interru Interrupt unmasking ordering table (interrupt init code is moved after all the peripheral init code)		



RCC Mo	de and Confi	gurati	ion	
	Mode			4 9
High Speed Clock (HSE) Crystal/Ceramic Resona	tor			~
Low Speed Clock (LSE) Crystal/Ceramic Resonat	or			~
☐ Master Clock Output 1				
☐ Master Clock Output 2				
☐ Audio Clock Input (I2S_CKIN)				
	Configuration			
Reset Configuration				
	NVIC Settings	0	GPIO Settings	
NVIC Interrupt Table	Enabled		Preemption Priority	Sub Priority
RCC global interrupt		0		0



ADC1 Mo	ode and Configuration	
	Mode	
■ INO		
✓ IN1		
□ IN2		
	Configuration	
Reset Configuration		
	NVIC Settings	
Configure the below parameters :		
Q Search (Ctrl+F) ③ ①		0
✓ ADCs_Common_Settings		
Mode	Independent mode	
✓ ADC_Settings		
Clock Prescaler	PCLK2 divided by 8	
Resolution	12 bits (15 ADC Clock cycles)	
Data Alignment	Right alignment	
Scan Conversion Mode	Disabled	
Continuous Conversion Mode	Enabled	
Discontinuous Conversion Mode	Disabled	
DMA Continuous Requests	Enabled	
End Of Conversion Selection	EOC flag at the end of single channel conversion	
∨ ADC_Regular_ConversionMode		
Number Of Conversion	1	
External Trigger Conversion Source	Regular Conversion launched by software	
External Trigger Conversion Edge	None	
∨ Rank	1	
Channel	Channel 1	
Sampling Time	3 Cycles	
∨ ADC_Injected_ConversionMode		
Number Of Conversions	0	
∨ WatchDog		
Enable Analog WatchDog Mode		

Pinout & Configuration

Clock Configu

. C.-france Barden

