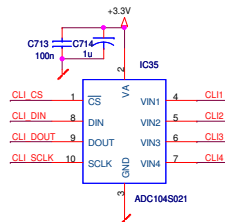


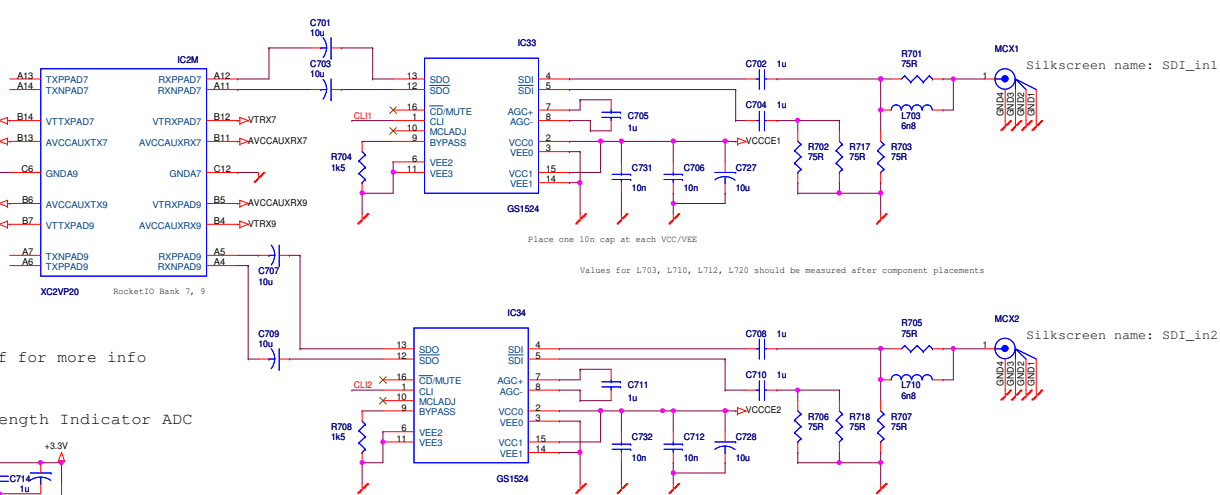
See page 251 in XAPP514.pdf for more info

Cable Length Indicator ADC



CLI signals to FPGA

CLI_CS
CLI_DIN
CLI_DOUT
CLI_SCLK



Place one 10n cap at each VCC/VEE

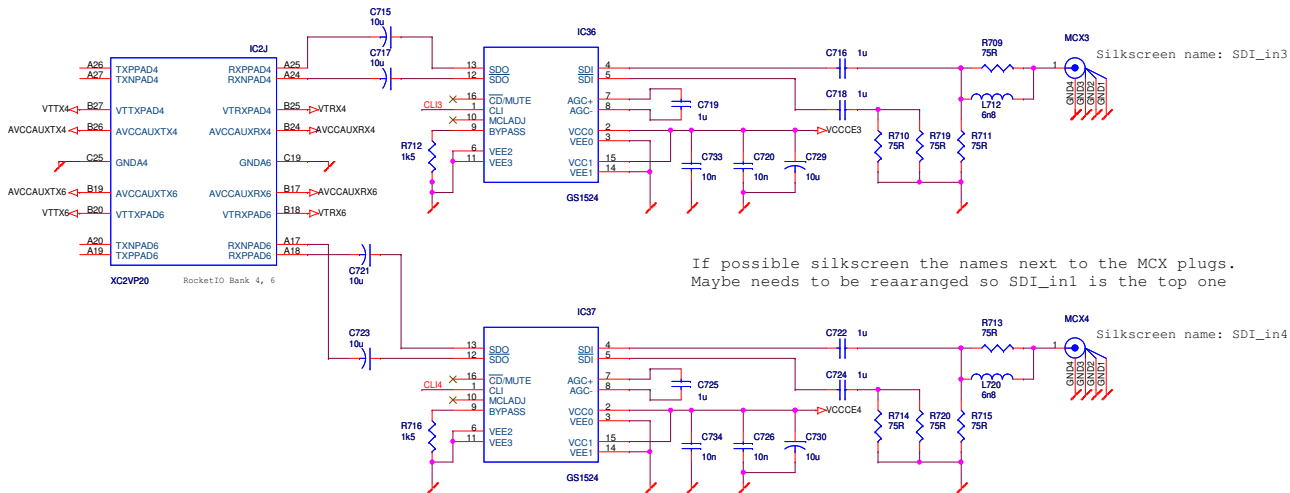
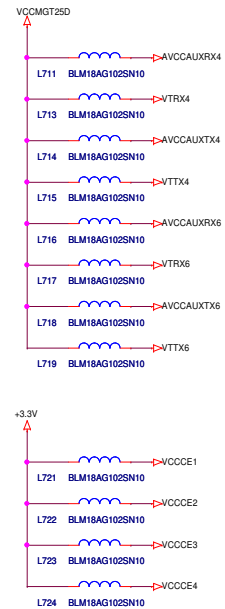
Values for L703, L710, L712, L720 should be measured after component placements

Place MCX plugs on upper side of PCB

Caps on input side of cable equalizer should be 1206 ceramic, but use case, a matched tantalum footprint, where plus is towards MCX connector

Place 10u Input caps VERY close to RIO. if not, traces should be ZDIFF100 between RIO and input caps.

Layout should be done as similar as to GS1524A datasheet - see page 14 - Also CAD file for suggested component placement will be given by DK-T.



If possible silkscreen the names next to the MCX plugs. Maybe needs to be rearranged so SDI_in1 is the top one

Title		
SDI input to RocketIO		
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